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ADM1029

Dual PWM Fan Controller and Temperature Monitor for High Availability Systems

The ADM1029 is a versatile fan controller and monitor for use in personal computers, servers, telecommunications equipment, or any high-availability system where reliable control and monitoring of multiple cooling fans is required. Each ADM1029 can control the speed of one or two fans and can measure the speed of fans that have a tachometer output. The ADM1029 can also measure the temperature of one or two external sensing diodes or an internal temperature sensor, allowing fan speed to be adjusted to keep system temperature within acceptable limits. The ADM1029 has FAULT inputs for use with fans that can signal failure conditions, and inputs to detect whether or not fans are connected.

The ADM1029 communicates with the host processor over an System Management (SMBus) serial bus. It supports eight different serial bus addresses, so that up to eight devices can be connected to a common bus, controlling up to sixteen fans. This makes software support and hardware design scalable.

The ADM1029 has an interrupt output ($\overline{INT}$) that allows it to signal fault conditions to the host processor. It also has a separate, cascadable fault output ($\overline{CFAULT}$) that allows the ADM1029 to signal a fault condition to other ADM1029s.

The ADM1029 has a number of useful features including an automatic fan speed control option implemented in hardware with no software requirement, automatic use of backup fans in the event of fan failure, and supports hot-swapping of failed fans.

Features

- Software Programmable and Automatic Fan Speed Control
- Automatic Fan Speed Control Allows Control
- Independent of CPU Intervention after Initial Setup
- Control Loop Minimizes Acoustic Noise and Power Consumption
- Remote and Local Temperature Monitoring
- Dual Fan Speed Measurement
- Supports Backup and Redundant Fans
- Supports Hot Swapping of Fans
- Cascadable Fault Output Allows Fault Signaling between Multiple ADM1029s
- Address Pin Allows Up to Eight ADM1029s in A System
- Small 24-lead QSOP Package
- This is a Pb-Free Device*

Applications

- Network Servers and Personal Computers
- Microprocessor-based Office Equipment
- High Availability Telecommunications Equipment

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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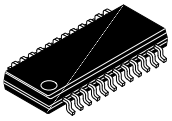
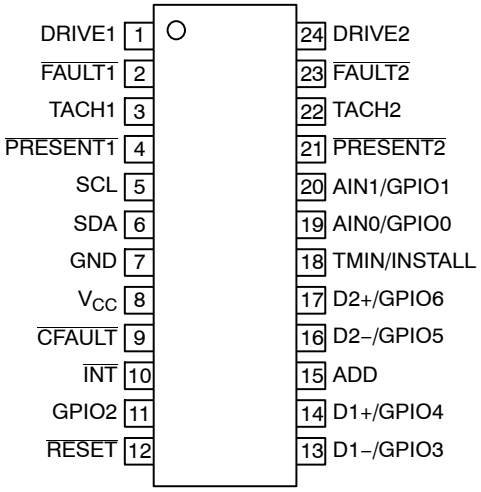


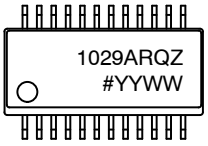
QSOP 24
CASE 492B

PIN ASSIGNMENT



ADM1029
Top View
(Not To Scale)

MARKING DIAGRAM



1029ARQZ	= Special Device Code
#	= Pb-Free Package
YYWW	= Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 49 of this data sheet.

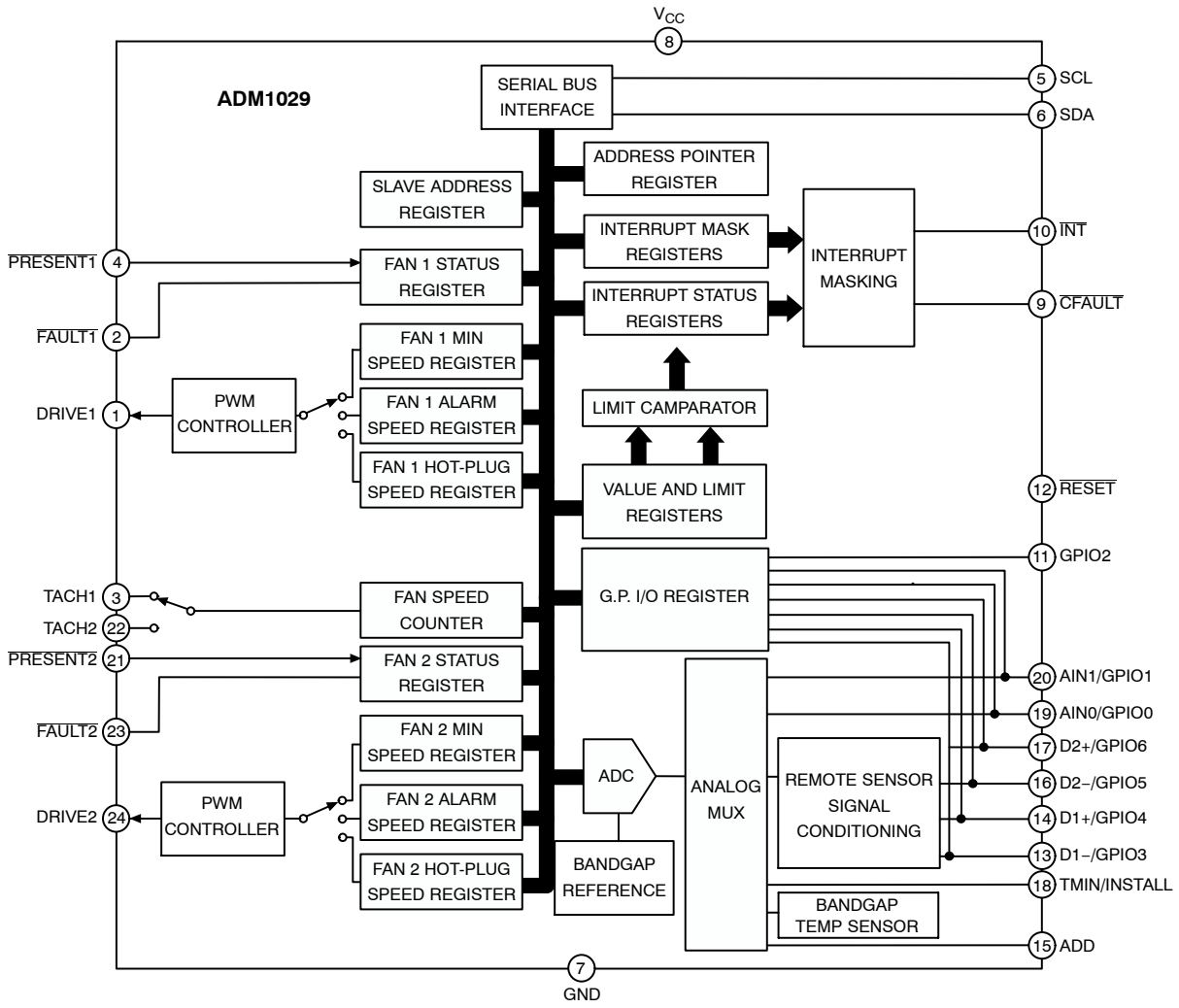


Figure 1. Functional Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Rating	Value	Unit
Positive Supply Voltage (V_{CC})	6.5	V
Voltage on Pins 13–18	−0.3 to (V_{CC} + 0.3)	V
Voltage on Any Other Input or Output Pin	−0.3 to +6.5	V
Input Current at Any Pin	±5	mA
Package Input Current	±20	mA
Maximum Junction Temperature (T_J max)	150	°C
Storage Temperature Range	−65 to + 150	°C
Lead Temperature Vapor Phase (60 sec) Infrared (15 sec)	 215 200	°C
ESD Rating All Pins	2,000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 2. THERMAL CHARACTERISTICS

Package Type	θ_{JA}	θ_{JC}	Unit
24-lead QSOP	105	39	°C/W

Table 3. PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	DRIVE1	Open Drain Digital Output. Pulsewidth Modulated (PWM) output to control the speed of Fan 1. Requires 10 kΩ typical pull-up resistor.
2	$\overline{\text{FAULT1}}$	Open Drain Digital I/O. When used with a fan having a fault output, a Logic 0 input to this pin signals a fault on Fan 1. Also used as a fault output.
3	TACH1	Open Drain Digital Input. Digital fan tachometer input for Fan 1. Will accept logic signals up to 5 V even when VCC is lower than 5 V.
4	$\overline{\text{PRESENT1}}$	Open Drain Digital Input. A shorting link in the fan connector holds this pin low when Fan 1 is connected.
5	SCL	Open Drain Digital Input. Serial Bus Clock. Requires 2.2 kΩ pull-up typical.
6	SDA	Digital I/O. Serial Bus bidirectional data. Open-drain output requires 2.2 kΩ pull-up.
7	GND	System Ground
8	V_{CC}	Power (3.0 V to 5.5 V). Typically powered from 3.3 V power rail. Bypass with the parallel combination of 10 μF (electrolytic or tantalum) and 0.1 μF (ceramic) bypass capacitors.
9	$\overline{\text{CFAULT}}$	Open Drain Digital I/O. Cascade fault input/output used for fault signaling between multiple ADM1029s.
10	$\overline{\text{INT}}$	Digital Output. Interrupt Request (Open Drain). The output is enabled when Bit 1 of the Configuration Register is set to 0. The default state is enabled.
11	GPIO2	Open Drain Digital I/O. General-purpose logic I/O pin.
12	$\overline{\text{RESET}}$	Open Drain Digital Input. Active low reset input.
13	D1−/GPIO3	Analog Input/Open Drain Digital I/O. Connected to cathode of external temperature-sensing diode, or may be reconfigured as a general-purpose logic input/output.
14	D1+/GPIO4	Analog Input/Open Drain Digital I/O. Connected to anode of external temperature-sensing diode, or may be reconfigured as a general-purpose logic input/output.
15	ADD	Eight-level Analog Input. Used to set the three LSBs of the serial bus address.
16	D2−/GPIO5	Analog Input/Open Drain Digital I/O. Connected to cathode of external temperature-sensing diode, or may be reconfigured as a general-purpose logic input/output.
17	D2+/GPIO6	Analog Input/Open Drain Digital I/O. Connected to anode of external temperature-sensing diode, or may be reconfigured as a general-purpose logic input/output.
18	TMIN/INSTALL	Eight-level Analog Input. The voltage on this pin defines whether automatic fan speed control is enabled, the minimum temperature at which the fan(s) will turn on in automatic speed control mode, and the number of fans that should be installed.
19	AIN0/GPIO0	Analog Input/Open Drain Digital I/O. May be configured as a 0 V to 2.5 V analog input or as a general-purpose digital I/O pin.
20	AIN1/GPIO1	Analog Input/Open Drain Digital I/O. May be configured as a 0 V to 2.5 V analog input or as a general-purpose digital I/O pin.
21	$\overline{\text{PRESENT2}}$	Open Drain Digital Input. A shorting link in the fan connector holds this pin low when Fan 2 is connected.
22	TACH2	Open Drain Digital Input. Digital fan tachometer input for Fan 2. Will accept logic signals up to 5 V even when V_{CC} is lower than 5 V.
23	$\overline{\text{FAULT2}}$	Open Drain Digital I/O. When used with a fan having a fault output, a Logic 0 input to this pin signals a fault on Fan 2. Also used as a fault output.
24	DRIVE2	Open Drain Digital Output. Pulsewidth Modulated (PWM) output to control the speed of Fan 2. Requires 10 kΩ typical pull-up resistor.

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted. (Note 1 and 2))

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Supply Voltage, V_{CC}		3.0	3.3	5.5	V
Supply Current, I_{CC}	Interface Inactive, ADC Active ADC Inactive, DAC Active Shutdown Mode	– – –	1.7 1.5 10	3.0 – 60	mA mA μA
TEMPERATURE-TO-DIGITAL CONVERTER					
Internal Sensor Accuracy		–	±1.0	±3.0	°C
Resolution		–	1.0	–	°C
External Diode Sensor Accuracy	0°C < T_D < 100°C	–	±3.0	±5.0	°C
Resolution		–	1.0	–	°C
Remote Sensor Source Current	High Level Low Level	– –	90 5.5	– –	μA
ANALOG-TO-DIGITAL CONVERTER					
Total Unadjusted Error, TUE (Note 3)		–	–	±1.0	%
Differential Non-linearity, DNL		–	–	±1.0	LSB
Power Supply Sensitivity		–	±1.0	–	%/V
Conversion Time Analog Input or Internal Temperature External Temperature		 – –	 11.6 185.6	 – –	ms
FAN RPM-TO-DIGITAL CONVERTER					
Accuracy	60°C ≤ T_A ≤ 100°C: V_{CC} = 3.3 V	–	–	±6	%
Full-scale Count		–	–	255	
Fan 1 to Fan 2 Nominal Input RPM (Note 4)	Divisor = 1, Fan Count = 153 Divisor = 2, Fan Count = 153 Divisor = 4, Fan Count = 153 Divisor = 8, Fan Count = 153	– – – –	8800 4400 2200 1100	– – – –	RPM
Internal Clock Frequency		56.4	60.0	63.6	kHz
OPEN-DRAIN DIGITAL OUTPUTS ($\overline{INT}$, $\overline{CFAULT}$)					
Output Low Voltage, V_{OL}	I_{OUT} = −6.0 mA, V_{CC} = 3 V	–	–	0.4	V
High Level Output Current, I_{OH}	$V_{OUT} = V_{CC}$	–	0.1	1.0	μA
OPEN-DRAIN SERIAL DATA BUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}	I_{OUT} = −6.0 mA, V_{CC} = 3 V	–	–	0.4	V
High Level Output Leakage Current, I_{OH}	$V_{OUT} = V_{CC}$	–	0.1	1.0	μA
SERIAL BUS DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V_{IH}		2.1	–	–	V
Input Low Voltage, V_{IL}		–	–	0.8	V
Hysteresis		–	500	–	mV
DIGITAL INPUT LOGIC LEVELS ($\overline{RESET}$, GPIO1−6, $\overline{FAULT1/2}$, TACH1/2, $\overline{PRESENT1/2}$)					
Input High Voltage, V_{IH}		2.1	–	–	V
Input Low Voltage, V_{IL}		–	–	0.8	V
DIGITAL INPUT CURRENT					
Input High Current, I_{IH}	$V_{IN} = V_{CC}$	−1.0	–	–	μA
Input Low Current, I_{IL}	V_{IN} = 0	–	–	1.0	μA
Input Capacitance, C_{IN}		–	20	–	pF
SERIAL BUS TIMING (Note 5)					
Clock Frequency, f_{SCLK}	See Figure 2 for All Parameters.	10	–	100	kHz
Glitch Immunity, t_{SW}		–	50	–	ns

Table 4. ELECTRICAL CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}, V_{CC} = V_{MIN} to V_{MAX}, unless otherwise noted. (Note 1 and 2))

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SERIAL BUS TIMING (Note 5)					
Bus Free Time, t_{BUF}		4.7	–	–	μs
Start Setup Time, $t_{SU; STA}$		4.7	–	–	μs
Start Hold Time, $t_{HD; STA}$		4.0	–	–	μs
Stop Condition Setup Time, $t_{SU; STO}$		4.0	–	–	μs
SCL Low Time, t_{LOW}		1.3	–	–	μs
SCL High Time, t_{HIGH}		4.0	–	50	μs
SCL, SDA Rise Time, t_R		–	–	1,000	ns
SCL, SDA Fall Time, t_F		–	–	300	ns
Data Setup Time, $t_{SU; DAT}$		250	–	–	ns
Data Hold Time, $t_{HD; DAT}$		300	–	–	ns

1. All voltages are measured with respect to GND, unless otherwise specified.
2. Typicals are at T_A = 25°C and represent the most likely parametric norm. Shutdown current typ is measured with V_{CC} = 3.3 V.
3. Total unadjusted error (TUE) includes offset, gain, and linearity errors of the ADC, multiplexer.
4. The total fan count is based on two pulses per revolution of the fan tachometer output.
5. Timing specifications are tested at logic levels of V_{IL} = 0.8 V for a falling edge and V_{IH} = 2.1 V for a rising edge.

NOTE: Specifications subject to change without notice.

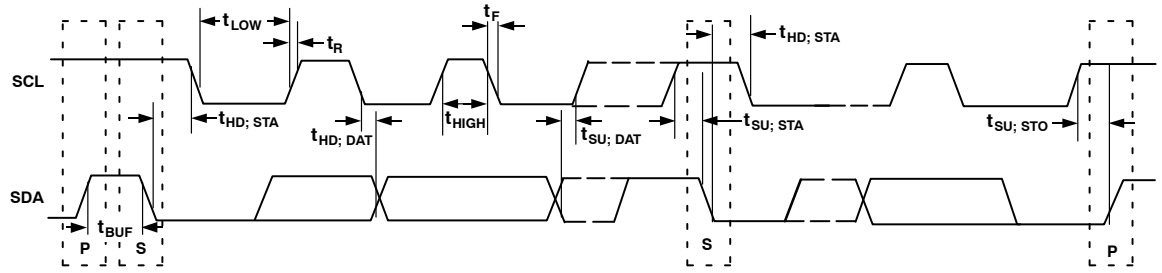


Figure 2. Serial Bus Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

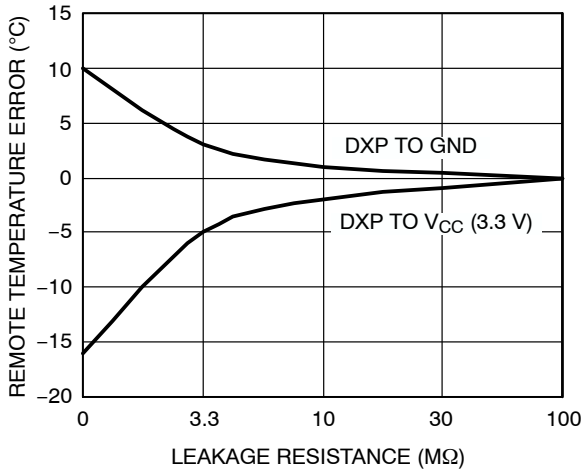


Figure 3. Remote Temperature Error vs. PC Board Track Resistance

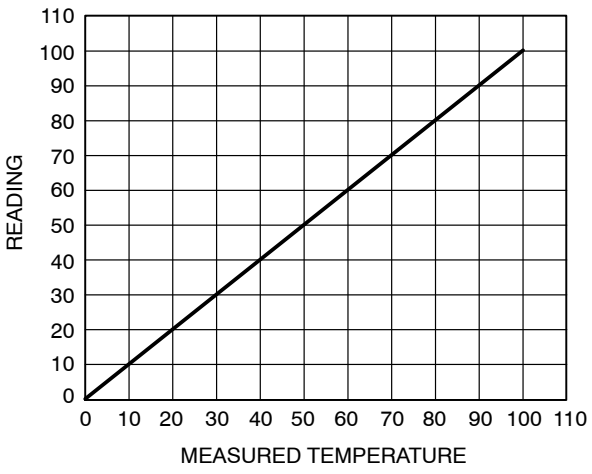


Figure 4. Pentium® III Temperature Measurement vs. ADM1029 Reading

TYPICAL PERFORMANCE CHARACTERISTICS

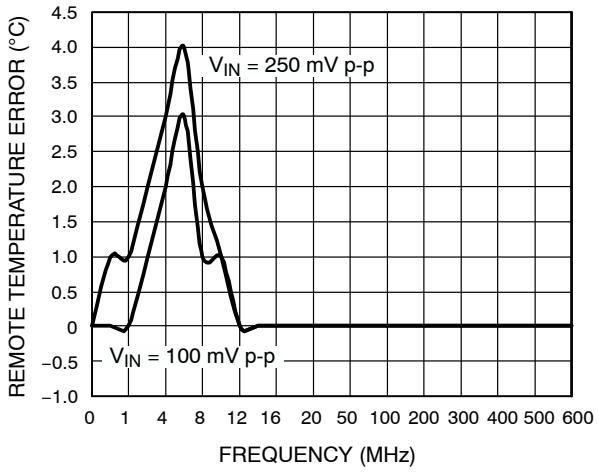


Figure 5. Remote Temperature Error vs. Power Supply Noise Frequency

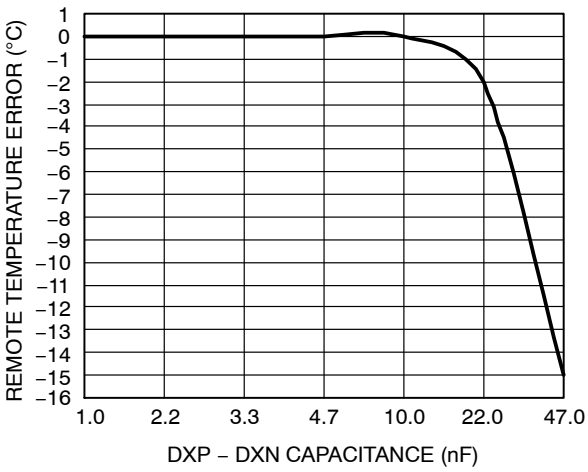


Figure 6. Remote Temperature Error vs. Capacitance between D+ and D−

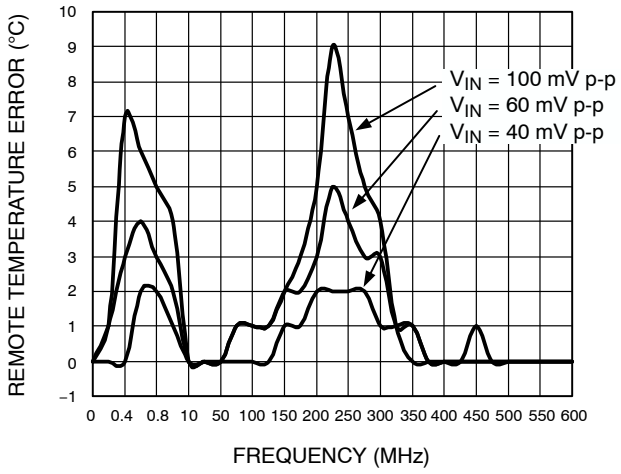


Figure 7. Remote Temperature Error vs. Common-mode Noise Frequency

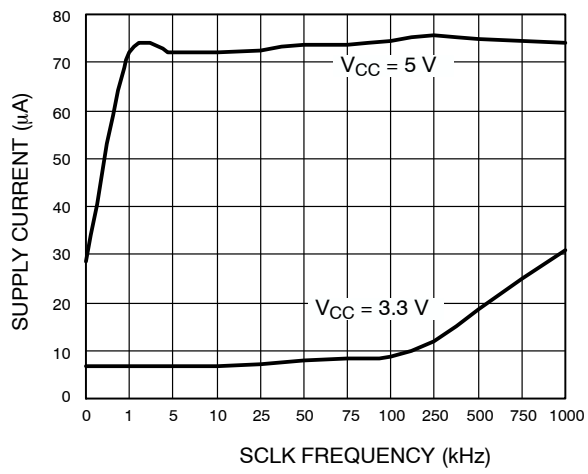


Figure 8. Standby Current vs. Clock Frequency

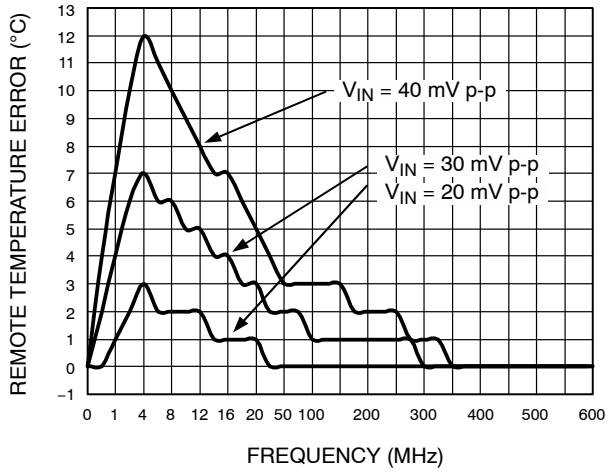


Figure 9. Remote Temperature Error vs. Differential-mode Noise Frequency

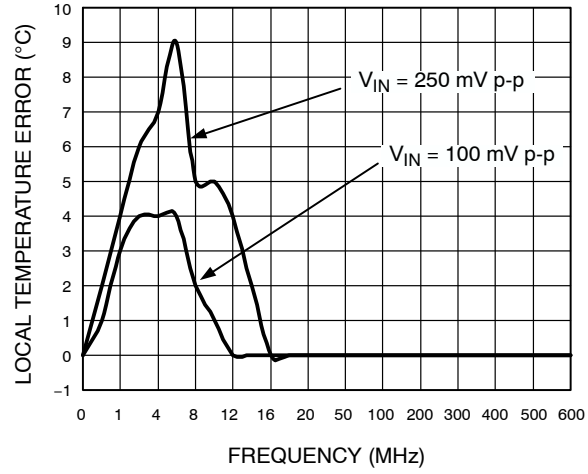


Figure 10. Local Sensor Temperature Error vs. Power Supply Noise Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

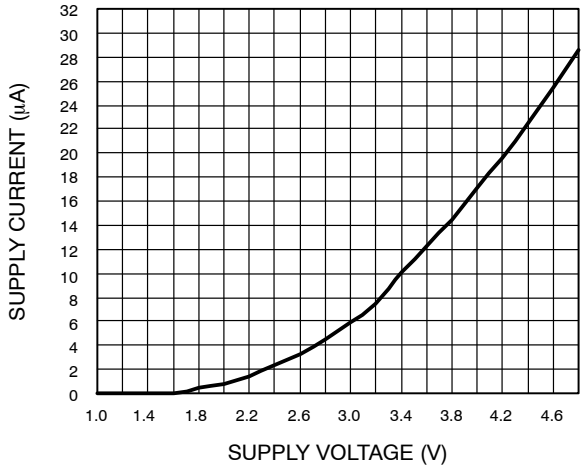


Figure 11. Standby Supply Current vs. Supply Voltage

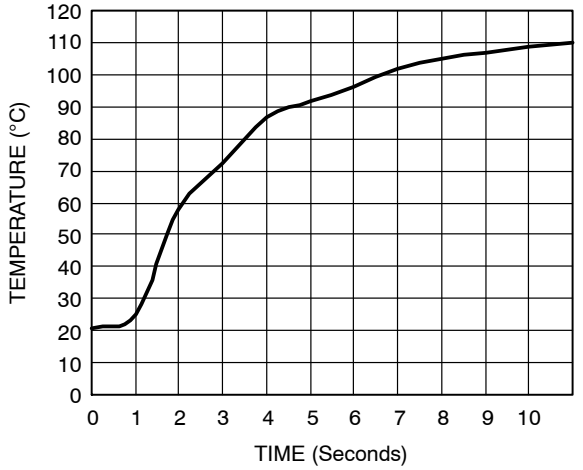


Figure 12. ADM1029 Response to Thermal Shock

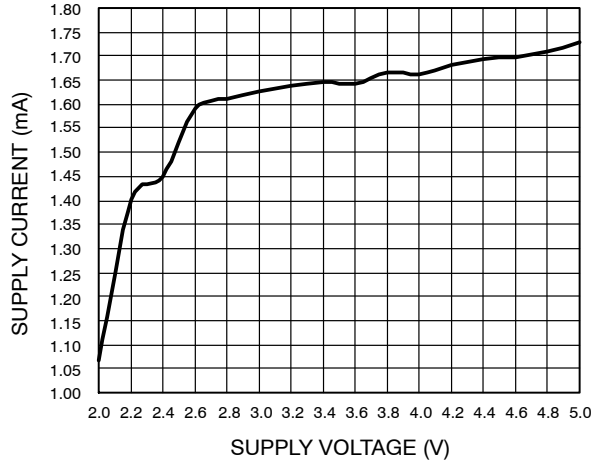


Figure 13. Supply Current vs. Supply Voltage

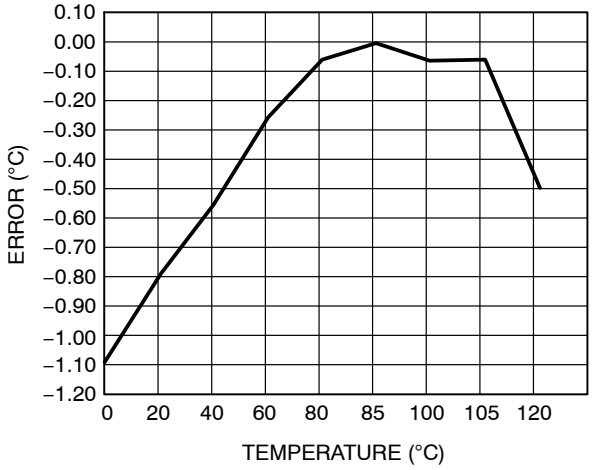


Figure 14. Remote Temperature Error

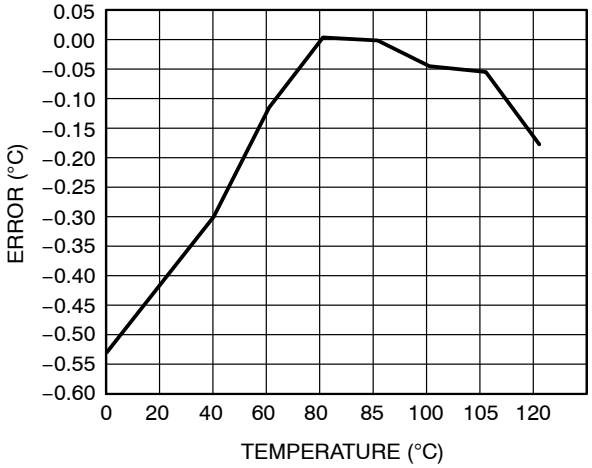


Figure 15. Local Temperature Error

Functional Description

Serial Bus Interface

Control of the ADM1029 is carried out via the serial bus. The ADM1029 is connected to this bus as a slave device, under the control of a master device.

The ADM1029 has a 7-bit serial bus address. The four MSBs of the address are set to 0101. The three LSBs can be set by the user to give a total of eight different addresses, allowing up to eight ADM1029s to be connected to a single serial bus segment.

To minimize device pin count and size, the three LSBs are set using a single pin (ADD, Pin 15). This is an 8-level input whose input voltage is set by a potential divider. The voltage on ADD is sampled immediately after power-up and digitized by the on-chip ADC to determine the value of the 3 LSBs. Since ADD is sampled only at power-up, any changes made while power is on will have no effect.

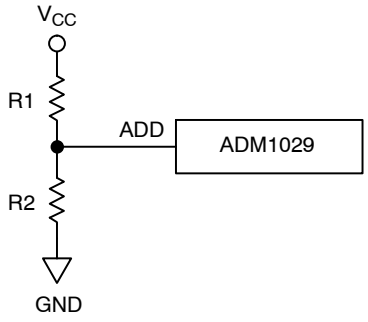


Figure 16. Setting the Serial Address

Table 5 shows resistor values for setting the 3 LSBs of the serial bus address. The same principle is used to set the voltage on Pin 18 (TMIN/INSTALL), which controls the automatic fan speed control function, and also tells the ADM1029 how many fans should be installed, as described later.

If several ADM1029s are used in a system, their ADD inputs can tap off a single potential divider, as shown in Figure 17.

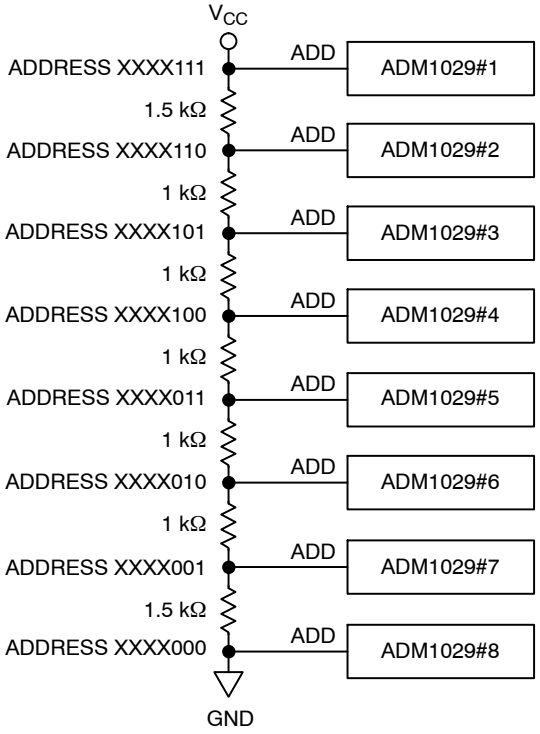


Figure 17. Setting Address of up to Eight ADM1029s

Table 5. RESISTOR RATIOS FOR SETTING SERIAL BUS ADDRESS

3 MSBs of ADC	Ideal Ratio R2/(R1 + R2)	R1 (kΩ)	R2 (kΩ)	Actual R2/(R1 + R2)	Error (%)	Address
111	N/A	0	∞	1	0	0101111
110	0.8125	18	82	0.82	+0.75	0101110
101	0.6875	22	47	0.6812	−0.63	0101101
100	0.5625	12	15	0.5556	−0.69	0101100
011	0.4375	15	12	0.4444	+0.69	0101011
010	0.3125	47	22	0.3188	+0.63	0101010
001	0.1875	82	18	0.18	−0.75	0101001
000	N/A	∞	0	0	0	0101000

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high-to-low transition on the serial data line SDA, while the serial clock line SCL remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/$\overline{W}$ bit, which determines the direction of the data transfer, i.e., whether data will be written to or read from the slave device.
The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0, the master will

write to the slave device. If the R/$\overline{W}$ bit is a 1 the master will read from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low-to-high transition when the clock is high may be interpreted as a STOP signal. The number of data bytes that can be transmitted over the serial bus in a single READ or WRITE operation is limited only by what the master and slave devices can handle.
3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the tenth clock pulse to assert a STOP condition. In READ mode, the master device will override the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the tenth clock pulse, high during the tenth clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation, because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

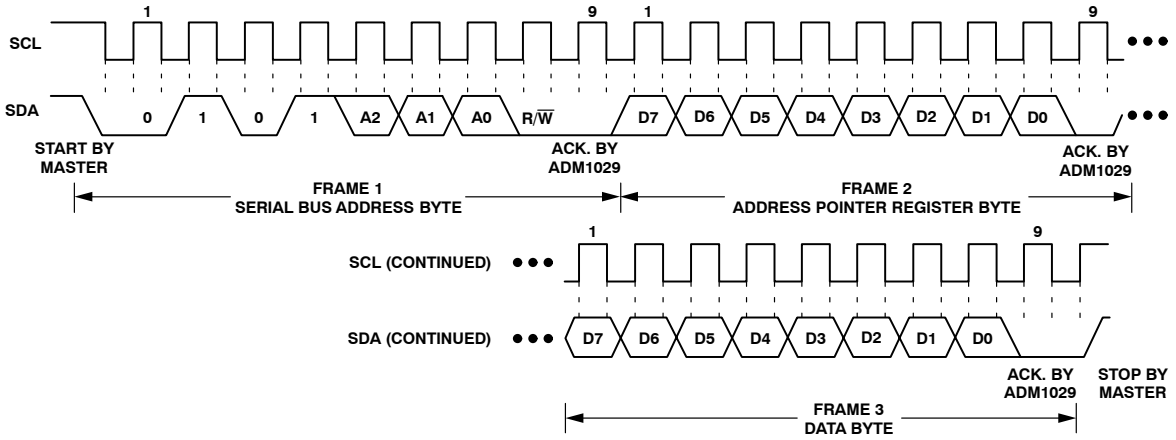


Figure 18. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

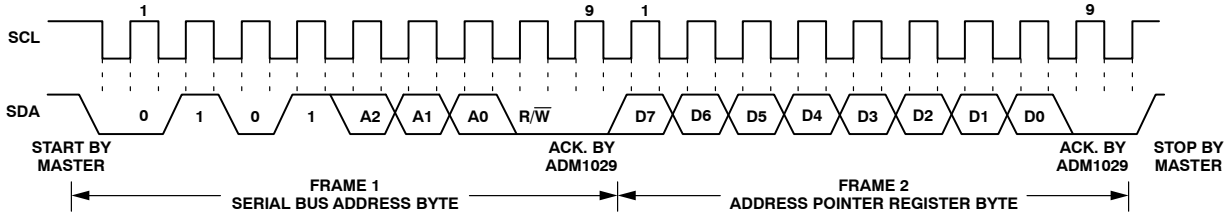


Figure 19. Writing to the Address Pointer Register Only

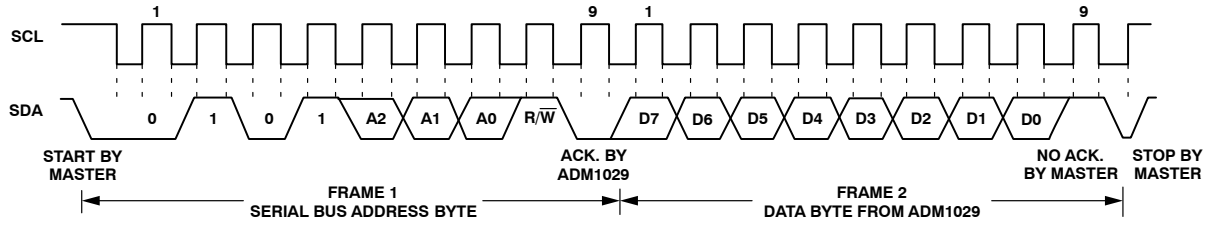


Figure 20. Reading Data from a Previously Selected Register

In the case of the ADM1029, write operations contain either one or two bytes, and read operations contain one byte, and perform the following functions:

To write data to one of the device data registers or read data from it, the Address Pointer Register must be set so that the correct data register is addressed, data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the Address Pointer Register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register.

This is illustrated in Figure 18. The device address is sent over the bus followed by R/$\overline{W}$ set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the Address Pointer Register. The second data byte is the data to be written to the internal data register.

When reading data from a register there are two possibilities:

1. If the ADM1029's Address Pointer Register value is unknown or not the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by performing a write to the ADM1029 as before, but only the data byte containing the register address is sent, as data is not to be written to the register. This is shown in Figure 19.
   A read operation is then performed consisting of the serial bus address, R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register. This is shown in Figure 20.
2. If the Address Pointer Register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the Address Pointer Register, so Figure 19 can be omitted.

NOTE: although it is possible to read a data byte from a data register without first writing to the Address Pointer Register, if the Address Pointer Register is already at the correct value, it is not possible to write data to a register without writing to the Address Pointer Register, because the first data byte of a write is always written to the Address Pointer Register.

Alert Response Address

The ADM1029 has an interrupt ($\overline{INT}$) output that is asserted low when a fault condition occurs. Several $\overline{INT}$ outputs can be wire OR'd to a common interrupt line. When the host processor receives an interrupt request, it would normally need to read the interrupt status register of each device to identify which device had made the interrupt request. However, the ADM1029 supports the optional Alert Response Address function of the SMBus protocol. When the host processor receives an interrupt request it can send a general call address (0001100) over the bus. The device asserting $\overline{INT}$ will then send its own slave address back to the host processor, so the device asserting $\overline{INT}$ can be identified immediately.

If more than one device is asserting $\overline{INT}$, all devices will try to respond with their slave address, but an arbitration process ensures that only the lowest address will be received by the host.

After sending its slave address, the first device will then clear its $\overline{INT}$ output. The host can then check if the $\overline{INT}$ is still low and send the general call again if necessary until all devices asserting $\overline{INT}$ have responded.

The ARA function can be disabled by setting Bit 2 of the Configuration Register (address 01h).

Temperature Measurement System

Local Temperature Measurement

The ADM1029 contains an on-chip bandgap temperature sensor, whose output is digitized by the on-chip ADC. The temperature data is stored in the Local Temp Value Register (address A0h). As both positive and negative temperatures can be measured, the temperature data is stored in two's complement format, as shown in Table 6. Theoretically, the temperature sensor and ADC can measure temperatures from –128°C to +127°C with a resolution of 1°C, but temperatures outside the operating temperature range of the device cannot be measured by the internal sensor.

Remote Temperature Measurement

The ADM1029 can measure the temperature of one or two remote diode-connected transistors, connected to Pins 13 and 14 and/or 16 and 17. The data from the temperature measurements is stored in the Remote 1 and Remote 2 Temp Value Registers (addresses A1h and A2h).

If two remote temperature measurements are not required, Pins 16 and 17 can be reconfigured as general-purpose logic I/O pins, as explained later.

The forward voltage of a diode or diode-connected transistor, operated at a constant current, exhibits a negative temperature coefficient of about –2 mV/°C. The absolute value of V_{BE} varies from device to device and individual calibration is required to null this out so, unfortunately, the technique is unsuitable for mass production.

The technique used in the ADM1029 is to measure the change in V_{BE} when the device is operated at two different currents.

This is given by:

$$\Delta V_{BE} = KT/q \times \ln(N) \quad \text{(eq. 1)}$$

where:
K is Boltzmann's constant
q is charge on the carrier
T is absolute temperature in Kelvins
N is ratio of the two currents

Figure 21 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor,

provided for temperature monitoring on some microprocessors, but it could equally well be a discrete transistor.

If a discrete transistor is used, the collector will not be grounded, and should be linked to the base. If a PNP transistor is used, the base is connected to the D– input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D– input and the base to the D+ input.

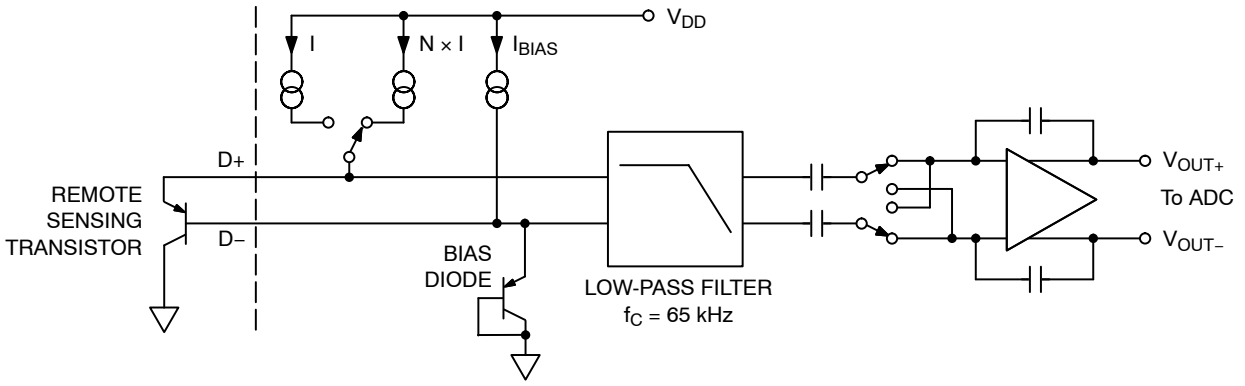


Figure 21. Signal Conditioning for Remote Diode Temperature Sensors

To prevent ground noise interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but biased above ground by an internal diode at the D– input. If the sensor is used in a noisy environment, a capacitor of value up to 1000 pF may be placed between the D+/D– pins.

To measure ΔV_{BE}, the sensor is switched between operating currents of I and N × I. The resulting waveform is passed through a 65 kHz low-pass filter to remove noise, and to a chopper-stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{BE}. This voltage is measured by the ADC to give a temperature output in 8-bit two's complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles. An external temperature measurement takes nominally 9.6 ms.

The results of external temperature measurements are stored in 8-bit, two's complement format, as illustrated in Table 6.

Offset Registers

Digital noise and other error sources can cause offset errors in the temperature measurement, particularly on the remote sensors. The ADM1029 offers a way to minimize these effects. The offsets on the three temperature channels can be measured during system characterization and stored as two's complement values in three offset registers at addresses 30h to 32h. The offset values are automatically added to, or subtracted from, the temperature values, depending on whether the two's complement number corresponds to a positive or negative offset. Offset values from –15°C to +15°C are allowed.

The default value in the offset registers is zero, so if no offsets are programmed, the temperature measurements are unaltered.

Temperature Limits

The contents of the Local and Remote Temperature Value Registers (addresses A0h to A2h) are compared to the contents of the High and Low Limit Registers at addresses 90h to 92h and 98h to 9Ah. How the ADM1029 responds to overtemperature/undertemperature conditions depends on the status of the Temperature Fault Action Registers (addresses 40h to 42h). The response of $\overline{\text{CFAULT}}$, $\overline{\text{INT}}$, and fan-speed-to-temperature events depends on the setting of these registers, as explained later.

Table 6. TEMPERATURE DATA FORMAT

Temperature	Digital Output
–128°C	1000 0000
–125°C	1000 0011
–100°C	1001 1100
–75°C	1011 0101
–50°C	1100 1110
–25°C	1110 0111
0°C	0000 0000
+10°C	0000 1010
+25°C	0001 1001
+50°C	0011 0010
+75°C	0100 1011
+100°C	0110 0100
+125°C	0111 1101
+127°C	0111 1111

Layout Considerations

Digital boards can be electrically noisy environments, and care must be taken to protect the analog inputs from noise, particularly when measuring the very small voltages from a remote diode sensor. The following precautions should be taken:

1. Place the ADM1029 as close as possible to the remote sensing diode. Provided that the worst noise sources such as clock generators, data/address buses, and CRTs are avoided, this distance can be 4 to 8 inches.
2. Route the D+ and D– tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks if possible.
3. Use wide tracks to minimize inductance and reduce noise pickup. Ten mil track minimum width and spacing is recommended.

Figure 22. Arrangement of Signal Tracks

4. Try to minimize the number of copper/solder joints, which can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D– path and at the same temperature.
   Thermocouple effects should not be a major problem as 1°C corresponds to about 240 μV, and thermocouple voltages are about 3 μV/°C of temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200 μV.
5. Place 0.1 μF bypass and 1000 pF input filter capacitors close to the ADM1029.
6. If the distance to the remote sensor is more than 8 inches, the use of twisted pair cable is recommended. This will work up to about 6 to 12 feet.
7. For really long distances (up to 100 feet), use shielded twisted pair such as Belden #8451 microphone cable. Connect the twisted pair to D+ and D– and the shield to GND close to the ADM1029. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect the measurement. When using long cables, the filter capacitor may be reduced or removed.

Cable resistance can also introduce errors. 1 Ω series resistance introduces about 0.5°C error.

Temperature-related Registers

Table 7 is a list of registers on the ADM1029 that are specific to temperature measurement and control.

Table 7. TEMPERATURE-SPECIFIC REGISTERS

Address	Description
0x06	Temp Devices Installed
0x30	Local Temp Offset
0x31	Remote 1 Temp Offset
0x32	Remote 2 Temp Offset
0x40	Local Temp Fault Action
0x41	Remote 1 Temp Fault Action
0x42	Remote 2 Temp Fault Action
0x48	Local Temp Cooling Action
0x49	Remote 1 Temp Cooling Action
0x4A	Remote 2 Temp Cooling Action
0x80	Local Temp TMIN
0x81	Remote 1 Temp TMIN
0x82	Remote 2 Temp TMIN
0x88	Local Temp TRANGE/THYST
0x89	Remote 1 Temp TRANGE/THYST
0x8A	Remote 2 Temp TRANGE/THYST
0x90	Local Temp High Limit
0x91	Remote 1 Temp High Limit
0x92	Remote 2 Temp High Limit
0x98	Local Temp Low Limit
0x99	Remote 1 Temp Low Limit
0x9A	Remote 2 Temp Low Limit
0xA0	Local Temp Value
0xA1	Remote 1 Temp Value
0xA2	Remote 2 Temp Value

The flowchart in Figure 23 shows how to configure the ADM1029 to measure temperature. It also shows how to configure the ADM1029's behavior for out-of-limit temperature measurements.

Fan Interfacing

The ADM1029 can be interfaced to many types of fan. It can be used to control the speed of a simple two-wire fan. It can measure the speed of a fan with a tach output, and it can accept a logic input from fans with a FAULT output. By means of a shorting link in the fan connector it can also determine if a fan is present or not and if fans have been hot-swapped.

The ADM1029 can control or monitor one or two fans. Bits 0 and 1 of the Fans Supported In System Register (03h) tell the ADM1029 how many fans it should be controlling/monitoring.

In the following descriptions "installed" means that the corresponding bit of register 03h is set and the ADM1029

expects to see a fan interfaced to it. It does not necessarily mean that the fan is actually, physically, connected.

If a fan is installed, events such as a fault output and hot-swapping of the fan can cause $\overline{INT}$ and $\overline{CFAULT}$ to be asserted, unless they are masked for that particular event. If a fan is not installed, but is still physically connected to the ADM1029, these events will be ignored with respect to asserting $\overline{INT}$ or $\overline{CFAULT}$, but will still be reflected in the corresponding Fan Status Register.

Setting Bit 0 indicates that Fan 1 is installed and is set to 1 at power-up by default. Setting Bit 1 indicates that Fan 2 is installed and depends on the state of Pin 18 (TMIN/INSTALL) at power-up.

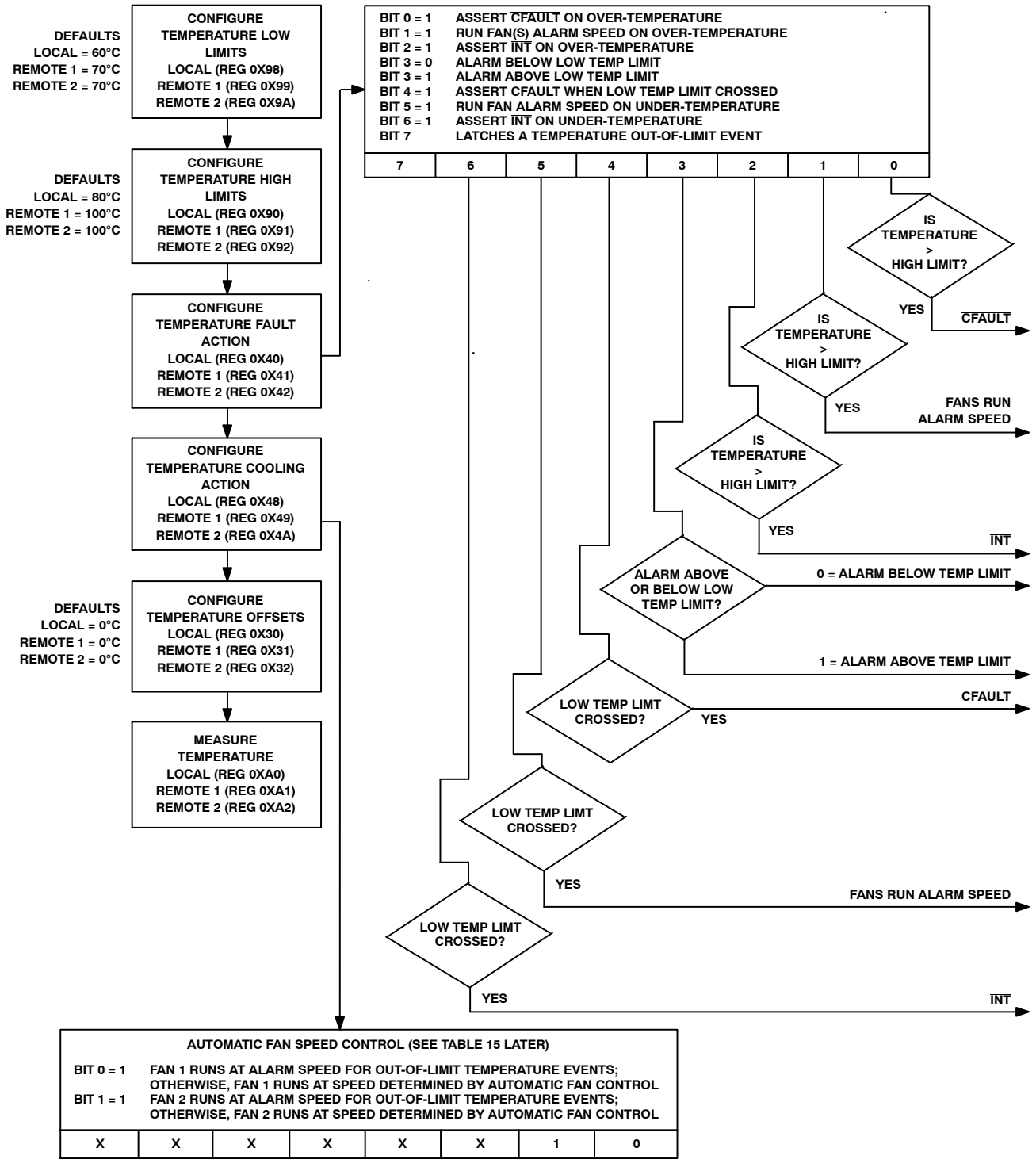


Figure 23. Temperature Sensing Flowchart

If two fans are installed, Bit 0 would be 1 by default and Pin 18 would be tied high* to set Bit 1. If only one fan is installed, it would normally be Fan 1 and Pin 18 would be tied low* to clear Bit 1. However, both of these bits can be modified by writing to the register, so it is possible to have Fan 2 installed and not Fan 1, or even have no fans installed.

* Note that Pin 18 also sets TMIN for automatic fan speed control. If this function is used, Pin 18 would be set to some other level according to Table 13.

$\overline{\text{FAULT}}$ Inputs/Outputs

The ADM1029 can be used with fans that have a fault output which indicates if the fan has stalled or failed. If one or both of the $\overline{\text{FAULT}}$ inputs (Pin 2 or Pin 23) goes low, both $\overline{\text{INT}}$ and $\overline{\text{CFAULT}}$ will be asserted.

Events on the fault inputs are also reflected in Bits 2 and 3 of the corresponding Fan Status Registers at addresses 10h and 11h. Bit 2 reflects the inverse state of the $\overline{\text{FAULT}}$ pin (0 if $\overline{\text{FAULT}}$ is high, 1 if $\overline{\text{FAULT}}$ is low), while Bit 3 is latched high if a $\overline{\text{FAULT}}$ input goes low. It must be cleared by writing a zero to it.

If the fan(s) being used do not have a $\overline{\text{FAULT}}$ output, the $\overline{\text{FAULT}}$ input(s) on the ADM1029 should be pulled high to V_{CC}.

The $\overline{\text{FAULT}}$ pins can also be configured as open-drain outputs by setting Bit 5 of the corresponding Fan Fault Action Register (18h or 19h). If a $\overline{\text{FAULT}}$ pin is configured as an output, it will still function as an input. This means that when a fault input occurs it will be latched low by the fault output, even if the fault input is removed. The fault output can be used to drive a fan failure indicator such as an LED.

If the $\overline{\text{FAULT}}$ pin is used as an output, any input to the $\overline{\text{FAULT}}$ pin should also be open-drain. This will avoid the fault input trying to source a high current into the $\overline{\text{FAULT}}$ pin if the fault input goes high while the fault output is low.

Fan Present Inputs

The fan $\overline{\text{PRESENT}}$ signal is implemented by a shorting link to ground in the fan connector. When the fan is plugged in, the corresponding $\overline{\text{PRESENT}}$ input (Pin 4 or Pin 21) on the ADM1029 is pulled low. If the fan is unplugged, the $\overline{\text{PRESENT}}$ input will be pulled high. $\overline{\text{INT}}$ and $\overline{\text{CFAULT}}$ will be asserted (unless masked) and the event will be reflected in Bits 0 and Bit 1 of the corresponding Fan Status Register.

Appearance or disappearance of a $\overline{\text{PRESENT}}$ input signal during normal operation signals to the ADM1029 that a fan has been hot-plugged or unplugged. $\overline{\text{INT}}$ and $\overline{\text{CFAULT}}$ will be asserted (unless masked). When a fan is hot-plugged, Bit 7 of the corresponding Fan Status Register will be set and a Fan Free Wheel Test commences automatically.

Fan Speed Measurement

The fan counter does not count the fan tach output pulses directly, because at low fan speeds it would take several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an onchip oscillator into the input of an 8-bit counter.

The fan speed measuring circuit is initialized on the first rising edge of a fan tach pulse after monitoring is enabled by setting Bit 4 of the Configuration Register. It then starts counting on the rising edge of the second tach pulse and counts for four fan tach periods, until the rising edge of the sixth tach pulse, or until the counter overranges if the fan tach period is too long.

After the speed of the first fan has been measured, the speed of the second fan (if installed) will be measured in the same way. The measurement cycle will repeat until monitoring is disabled. The fan speed measurements are stored in the Fan Tach Value registers at addresses 70h and 71h.

If both fans are installed, Fan 1 will be measured first. If only one fan is installed, the ADM1029 will still try to measure both fans, starting with Fan 1, but the measurement on the noninstalled fan will time out when the Fan Tach Value count overranges.

The fan speed count is given by:

$$\text{Count} = f \times 4 \times 60/R/N \quad \text{(eq. 2)}$$

where:
f is oscillator frequency in Hz
factor 4 is because 4 tach periods are counted
factor 60 is to convert minutes to seconds
R = fan speed in RPM
N is number of tach pulses per revolution

The frequency of the oscillator can be adjusted to suit the expected frequency range of the fan tach pulses, which depends on the fan speed and the number of tach pulses produced for each revolution of the fan, which is either 1, 2, or 4. The oscillator frequency is set by Bits 7 and 6 of the Fan Configuration Registers (68h for Fan 1 and 69h for Fan 2).

Table 8. OSCILLATOR FREQUENCIES

Bit 7	Bit 6	Oscillator Frequency (Hz)
0	0	Measurement Disabled
0	1	470
1	0	940
1	1	1880

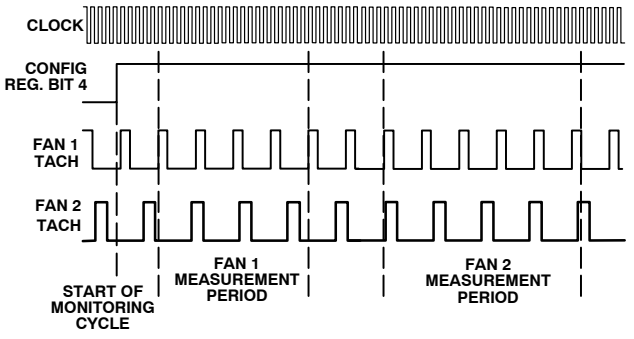


Figure 24. Fan Speed Measurement

Fan Speed Limits

Fans generally do not overspeed if run from the correct voltage, so the failure condition of interest is under-speed due to electrical or mechanical failure. For this reason only low-speed limits are programmed into the Tach Limit Registers for the fans. These registers are at address 78h for Fan 1 and 79h for Fan 2. It should be noted that, since fan period rather than speed is being measured, the fan speed count will be larger the slower the fan speed. Therefore a fan failure fault will occur when the measurement *exceeds* the limit value.

For the most accurate fan failure indication, the oscillator frequency should be chosen to give as large a limit value as possible without the counter overranging. A count close to ¾ full-scale or 191 is the optimum value.

For example, if a fan produces two tach pulses per revolution and the fan failure speed is to be 600 rpm, the oscillator frequency should be set to 940 Hz. This will give a count at the fail speed of:

$$940 \times 4 \times 60/600/2 = 188 \quad \text{(eq. 3)}$$

If the oscillator frequency were only 470 Hz, the count would be 94, while an oscillator frequency of 1880 Hz cannot be used because the count would be 376 and the counter would overrange.

Fan Monitoring Cycle Time

Five complete tach periods are required to carry out a fan speed measurement Therefore, if the start of a fan measurement just misses a rising edge, the measurement can take almost six tach periods for each fan.

The worst-case monitoring cycle time is when both fans are under speed and the fan speed counter counts up to its maximum value. The actual count takes 256 oscillator pulses over four tach periods, plus a further two tach periods or 128 oscillator pulses before the count starts. The total monitoring cycle time is therefore:

$$t_{MEAS} = 384/f_{OSC(FAN\ 1)} + 384/f_{OSC(FAN\ 2)} \quad \text{(eq. 4)}$$

In order to read a valid result from the Fan Tach Value Registers, the total monitoring time allowed after starting the monitoring cycle should be greater than this.

Tach Signal Conditioning

Signal conditioning in the ADM1029 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 V to 5 V, even if V_{CC} is less than 5 V. In the event that these inputs are supplied from fan outputs that exceed 0 V to 5 V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range.

Figures 25 a to 28 show circuits for most common fan tach outputs.

If the fan tach output has a resistive pull-up to V_{CC}, it can be connected directly to the fan input, as shown in Figure 25.

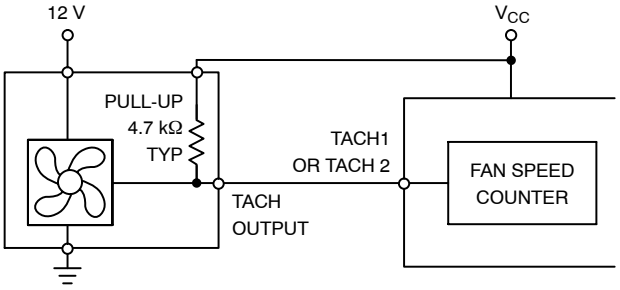
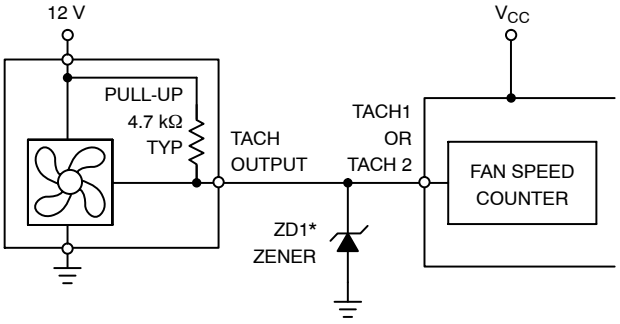


Figure 25. Fan with Tach Pull-up to $+V_{CC}$

If the fan output has a resistive pull-up to 12 V (or other voltage greater than 6.5 V), the fan output can be clamped with a Zener diode, as shown in Figure 26. The Zener voltage should be chosen so that it is greater than V_{IH} but less than 6.5 V, allowing for the voltage tolerance of the Zener. A value of between 3 V and 5 V is suitable.



* Choose ZD1 Voltage Approx. 0.8 × V_{CC}

Figure 26. Fan with Tach. Pull-up to Voltage > 6.5 V (e.g., 12 V) Clamped with Zener Diode

If the fan has a strong pull-up (less than 1 kΩ) to 12 V, or a totem-pole output, a series resistor can be added to limit the Zener current, as shown in Figure 27. Alternatively, a resistive attenuator may be used, as shown in Figure 28.

R1 and R2 should be chosen such that:

$$2\ V < V_{PULLUP} \times R2/(R_{PULLUP} + R1 + R2) < 5\ V \quad \text{(eq. 5)}$$

The fan inputs have an input resistance of nominally 160 kΩ to ground, so this should be taken into account when calculating resistor values.

With a pull-up voltage of 12 V and pull-up resistor less than 1 kΩ, suitable values for R1 and R2 would be 100 kΩ and 47 kΩ. This will give a high input voltage of 3.83 V.

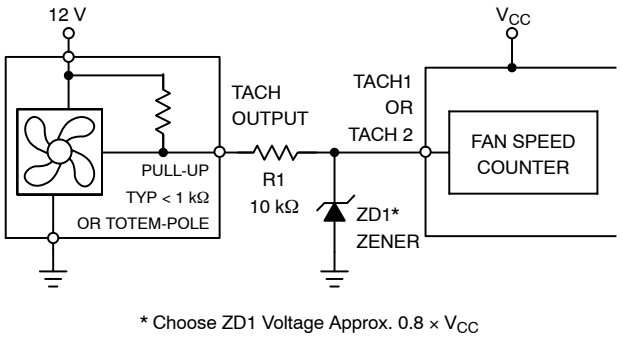


Figure 27. Fan with Strong Tach. Pull-up to > V_{CC} or Totem-pole Output, Clamped with Zener and Resistor

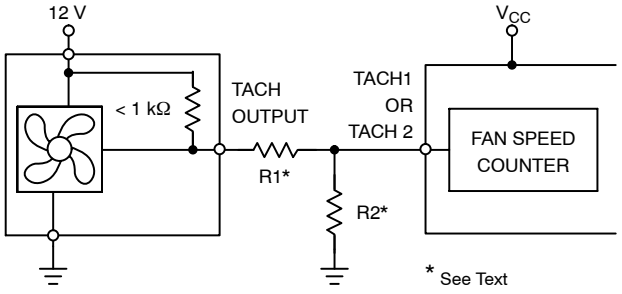


Figure 28. Fan with Strong Tach. Pull-up to > V_{CC} or Totem-pole Output, Attenuated with R1/R2

Fan Speed Control

Fan speed is controlled using pulsewidth modulation (PWM). The PWM outputs (Pins 1 and 24) give a pulse output with a programmable frequency (default 250 Hz) and a duty-cycle defined by the contents of the relevant fan speed register, or by the automatic fan speed control when this mode is enabled. The speed at which a fan runs is determined by fault conditions and the settings of various control and mask registers.

A fan can only be driven if it is defined as being supported by the controller in register 02h. The ADM1029 supports up to two fans, so Bits 0 and 1 of this register are permanently set. This register is read-only.

A fan will only be driven if it is defined as being supported by the system in register 03h. If Bit 0 of this register is set, it indicates that Fan 1 is installed. This is the power-on default. If Bit 1 is set, it indicates that Fan 2 is installed. This bit is set by the state of Pin 18 at power-up. This register is read/write and the default/power-on setting can be overwritten. If a fan is not supported in register 03h it will not be driven, even if it is physically installed.

The PWM outputs are open-drain outputs. They require pull-up resistors and must be amplified and buffered to drive the fans.

Minimum Speed

The normal operating fan speed is set by the four LSBs of the Fan 1 and Fan 2 Minimum/Alarm Speed Registers (addresses 60h, 61h). These bits also set the minimum speed at which a fan will run in automatic control mode. These bits should be set to 05h. This corresponds to 33% PWM duty-cycle, which is the lowest speed at which most fans will run reliably.

Fan(s) will run at minimum speed if there is no fault condition, automatic fan speed is disabled, and there are no other overriding conditions.

Alarm Speed

Alarm speed is set by the four MSBs of the Fan 1 and Fan 2 Minimum/Alarm Speed Registers (addresses 60h, 61h). Fan(s) will run at alarm speed if any of the following conditions occurs, assuming the condition has not been masked out using the Fan Event Mask Registers:

- Setting Bit 0 of register 07h forces Fan 1 to run at alarm speed (Set Fan x Alarm Speed Register).
- Setting Bit 1 of register 07h forces Fan 2 to run at alarm speed (Set Fan x Alarm Speed Register).
  If monitoring is disabled by clearing Bit 4 of the Configuration Register, all fans controlled by the ADM1029 will run at alarm speed.
- When a GPIO pin is configured as an input by setting Bit 0 of the corresponding GPIO Behavior Register, and Bit 4 of the GPIO Behavior Register is also set, all fans controlled by the ADM1029 will go to alarm speed when the logic input is asserted (high or low, depending on the polarity bit, Bit 1 of the corresponding GPIO Behavior Register).
- If Bit 7 of a Fan Fault Action Register is set (18h – Fan 1, 19h – Fan 2) the corresponding fan will go to alarm speed when $\overline{\text{CFAULT}}$ is pulled low by an external source.
- If a tach measurement exceeds the set limit, all fans controlled by the ADM1029 will run at alarm speed.
- If a fan fault input pin is asserted (low), all fans controlled by the ADM1029 will run at alarm speed.
- If Bit 1 of a Temp. Fault Action Register is set (40h – Local Sensor, 41h – Remote 1, 42h – Remote 2), all fans controlled by the ADM1029 will go to alarm speed if the corresponding temperature high limit is exceeded.
- If Bit 5 of a Temp. Fault Action Register is set, all fans controlled by the ADM1029 will go to alarm speed if a temperature input crosses the corresponding temperature low limit, the direction depending on the setting of Bit 3 of the Temp. Control register. (0 = alarm when input goes below low limit, 1 = alarm when input goes above low limit).
- If Bit 1 of an AIN Behavior Register is set (50h – AIN0, 51h – AIN1), all fans controlled by the ADM1029 will go to alarm speed if the corresponding AIN high limit is exceeded.
- If Bit 5 of an AIN Behavior Register is set, all fans controlled by the ADM1029 will go to alarm speed if

an analog input crosses the corresponding AIN low limit, the direction depending on the setting of Bit 3 of the AIN control register. (0 = alarm when input goes below low limit, 1 = alarm when input goes above low limit).

- If a thermal override occurs while the ADM1029 is in sleep mode, all fans controlled by the ADM1029 will run at alarm speed.

Hot-plug Speed

Hot-plug speed is set by the four LSBs of the Fan 1 and Fan 2 Configuration Registers (addresses 68h and 69h). The PWM frequency is set by Bits 4 and 5 of these registers, while Bits 6 and 7 set the number of pulses per revolution for fan speed measurement.

Fan(s) will run at hot-plug speed if any of the following conditions occur, assuming the condition has not been masked using the Fan Event Mask Registers:

- If a fan is unplugged, the other fan (if any) controlled by the ADM1029 will run at hot-plug speed.
- Setting Bit 0 of register 08h forces Fan 1 to run at hot-plug speed (Set Fan x Hot-plug Speed).
- Setting Bit 1 of register 08h forces Fan 2 to run at hot-plug speed (Set Fan x Hot-plug Speed).
- When a GPIO pin is configured as an input by setting Bit 0 of the corresponding GPIO Behavior Register, and Bit 5 of the GPIO Behavior Register is also set, all fans controlled by the ADM1029 will go to hot-plug speed when the logic input is asserted (high or low, depending on the polarity bit, Bit 1 of the corresponding GPIO Behavior Register).
- If Bit 6 of a Fan Fault Action Register is set (18h for Fan 1, 19h for Fan 2) the corresponding fan will go to hot-plug speed when $\overline{\text{CFAULT}}$ is pulled low by an external source.

NOTE: if operating conditions and register settings are such that both alarm speed and hot-plug speed would be triggered, which one takes priority is determined by Bit 5 of the Fan 1 and Fan 2 Status Registers (addresses 10h and 11h). If this bit is set, hot-plug speed takes priority. If it is cleared, alarm speed takes priority.

Full Speed

Fans will run at full speed if the corresponding bits in the Set Fan x Full Speed Register (address 09h) are set: Bit 0 for Fan 1 and Bit 1 for Fan 2.

Fan Mask Registers

The effect of various conditions on fan speed can be enabled or disabled by mask registers. In all these registers, setting Bit 0 of the register enables Fan 1 to go to alarm speed or hot-plug speed if the corresponding event occurs, while setting Bit 1 enables Fan 2. Clearing these bits masks the effect of the corresponding event on fan speed.

Registers 20h and 21h are Fan Event Mask Registers. Bits 0 and 1 of register 20h enable (bit set) or mask (bit clear) the effect of a Fan 1 fault (underspeed or fault input) on Fan 1 and Fan 2 speed. Similarly, Bits 0 and 1 of register 21h enable (bit set) or mask (bit clear) the effect of a Fan 2 Fault on Fan 1 and Fan 2 speed.

Registers 38h to 3Eh are GPIO X Event Mask Registers. Bits 0 and 1 of these registers enable or mask the effect of a GPIO assertion on Fan 1 and Fan 2 speed.

NOTE: Registers 48h to 4Ah are Temp. Cooling Action Registers. Bits 0 and 1 of these registers enable or mask the effect of Local, Remote 1, and Remote 2 temperature faults on Fan 1 and Fan 2 speed. These registers also determine which temperature channel controls each fan in automatic fan speed control mode, as described later.

Registers 58h and 59h are AIN Event Mask Registers. Bits 0 and 1 of these registers enable or mask the effect of an AIN out-of-limit event on Fan 1 and Fan 2 speed.

Modes of Operation

The ADM1029 has three different modes of operation. These modes determine the behavior of the system.

1. PWM Duty Cycle Select Mode (directly sets fan speed under software control)
2. Thermal Trip Mode
3. Automatic Fan Speed Control Mode

PWM Duty Cycle Select Mode

The ADM1029 may be operated under software control by clearing bits <1:0> of the three Temp Cooling Action Registers (Reg 0x48, 0x49, 0x4A). Once under Software Control, each fan speed may be controlled by programming values of PWM Duty Cycle in to the device. Values of PWM Duty Cycle between 0% to 100% may be written to the four LSBs of the Fan 1 and Fan 2 Minimum/Alarm Speed Registers (addresses 60h, 61h). to control the speed of each fan. Table 9 shows the relationship between hex values written to the Minimum/Alarm Speed Registers and PWM duty cycle obtained.

Table 9. PWM DUTY CYCLE SELECT MODE

Hex Value	PWM Duty Cycle
00	0%
01	7%
02	14%
03	20%
04	27%
05	33% Recommended
06	40%
07	47%
08	53%
09	60%
0A	67%
0B	73%
0C	80%
0D	87%
0E	93%
0F	100% (Default)

It is recommended that the minimum PWM duty cycle be set to 33% (0x05). This has been determined to be the lowest PWM duty cycle that most fans will run reliably at. Note that the PWM duty cycle values programmed in to these registers also define the PWM duty cycle that the fans will turn on at, in Automatic Fan Speed Control Mode. It is recommended that after power-up, the PWM duty cycle is set to 33% before enabling Automatic Fan Speed Control.

Thermal Trip Mode

The ADM1029 can thermally trip the fan(s) for simple on/off fan control, or 2-speed fan control. For example, a fan can be programmed to run at 33% duty cycle. If the temperature exceeds the high temperature limit set for that temperature channel, the fan can automatically trip and run at Alarm Speed. The fan will continue to run at Alarm Speed even if the temperature error condition subsides, until the Latch Temp Fault bit (Bit 7 of the Temp x Fault Action Reg) is cleared in software by writing a 0 to it. To configure Fan 1 normally, run at 33% but to thermally trip to Alarm Speed for a Remote 2 measured temperature of 70°C, set up the following registers:

1. Configure the normal PWM duty cycle for Fan 1 to 33%.

   Fan 1 Minimum/Alarm Speed Reg (0x60) = 0xF5

2. Set the Remote 2 High Temperature Limit = 70°C.

   Remote 2 Temp High Limit Reg (0x92) = 0x46

3. Configure Alarm Speed on Overtemperature function for Remote 2 Temperature channel.

   Set Bit 1 of Temp 2 Fault Action Reg (0x42)

4. Enable Fan 1 to be controlled by Remote 2 Temperature.

   Set Bit 0 of Temp 2 Cooling Action Reg (0x4A)

Once the fan thermally trips to Alarm Speed, it will continue to run at Alarm Speed until the temperature drops below the High Temperature Limit and the Latch Temp Fault bit (Bit 7 of the Temp 2 Fault Action Reg) is cleared to 0.

Event Latch Bits

Certain events that occur will cause latch bits to be set in various registers on the ADM1029. Once a latch bit is set, it will need to be cleared by software for the system to return to normal operation. To detect if a latch bit has been set, the $\overline{\text{INT}}$ pin can be used to signal a latch event to the system supervisor. Alternatively, the Status Registers can be polled periodically, and any latch bits that are set can be cleared. The events that cause latch bits to be set are:

1. Thermal Events. If the fan is run at Alarm Speed on Overtemperature or Undertemperature, this will set the Latch Temp Fault bit (Bit 7 of the Temp x Fault Action Registers 0x40–0x42).
2. Missing Fan. If a fan is missing, i.e., has been unplugged, the Missing Latch bit (Bit 1 of Fan x Status Registers) is set.
3. Hotplugged Fan. If a new fan is inserted into the system, Bit 7 (Hotplug Latch bit) of the Fan x Status Register is set.
4. FAULT Asserted. If the fan becomes stuck and its FAULT output asserts low, Bit 2 (Fault Latch bit) of the Fan x Status register is set.
5. TACH Failure. If the fan runs underspeed or becomes stuck, then Bit 6 (Tach Fault Latch Bit) of the Fan x Status Register is set.

Automatic Fan Speed Control

The ADM1029 has a local temperature channel and two remote temperature channels, which may be connected to an on-chip diode-connected transistor on a CPU or a general-purpose discrete transistor. These three temperature channels may be used as the basis for an automatic fan speed control loop to drive fans using Pulsewidth Modulation (PWM).

How Does The Control Loop Work?

The Automatic Fan Speed Control Loop is shown in Figure 29.

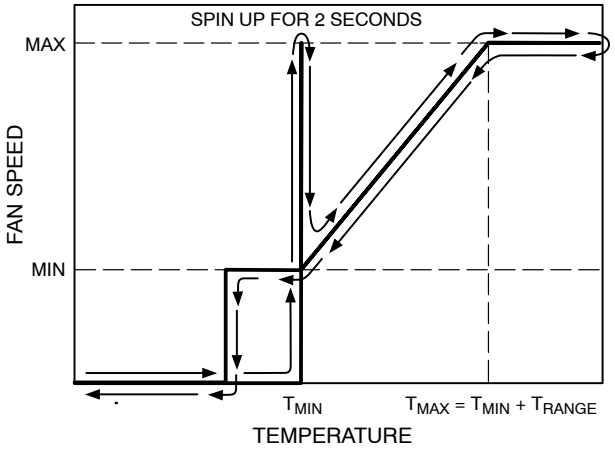


Figure 29. Automatic Fan Speed Control

In order for the fan speed control loop to work, certain loop parameters need to be programmed in to the device:

1. **T_{MIN}**. This is the temperature at which a fan should switch on and run at minimum speed. The fan will only turn on once the temperature being measured rises above the T_{MIN} value programmed. The fan will spin up for a predetermined time (default = 2 secs). See Fan Spin-up section for more details.
2. **T_{RANGE}**. This will be the temperature range over which the ADM1029 will automatically adjust fan speed. As the temperature increases beyond T_{MIN}, the PWM duty cycle will be increased accordingly.

The T_{RANGE} parameter actually defines the fan speed versus temperature slope of the control loop.

3. **T_{MAX}**. This is defined as the temperature at which a fan will be at its maximum speed. At this temperature, the PWM duty cycle driving the fan will be 100%. T_{MAX} is given by T_{MIN} + T_{RANGE}. Since this parameter is the sum of the T_{MIN} and T_{RANGE} parameters, it does *not* need to be programmed into a register on-chip.
4. Programmable hysteresis is included in the control loop to prevent the fans continuously switching on and off if the temperature is close to T_{MIN}. The fans will continue to run until such time as the temperature drops below T_{MIN}–T_{HYST}. The four MSBs of the T_{RANGE}/T_{HYST} registers (Registers 0x88, 0x89, 0x8A) contain a temperature hysteresis value that can be programmed from 0001 to 1111. This allows a temperature hysteresis range from 1°C to 15°C for each temperature measurement channel.

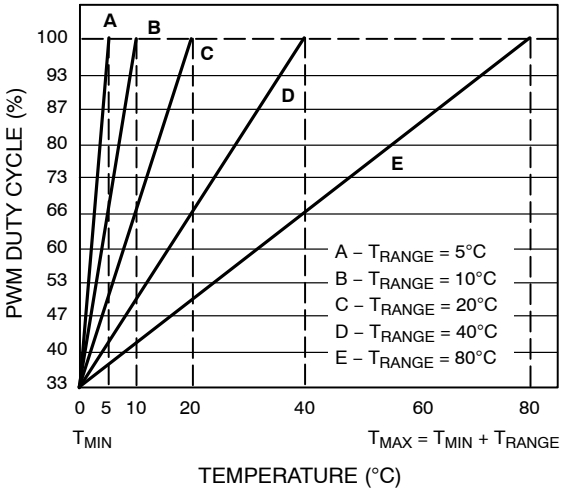


Figure 30. PWM Duty Cycle vs. Temperature Slopes (T_{RANGE})

Figure 30 shows the different control slopes determined by the T_{RANGE} value chosen, and programmed in to the ADM1029. T_{MIN} was set to 0°C to start all slopes from the same point. It can be seen how changing the T_{RANGE} value affects the PWM Duty Cycle vs. Temperature Slope.

Figure 31 shows how for a given T_{RANGE}, changing the T_{MIN} value affects the loop. Increasing the T_{MIN} value will increase the T_{MAX} (temperature at which the fan runs full speed) value, since T_{MAX} = T_{MIN} + T_{RANGE}. Note, however, that the PWM Duty Cycle versus Temperature slope remains exactly the same. Changing the T_{MIN} value merely shifts the control slope.

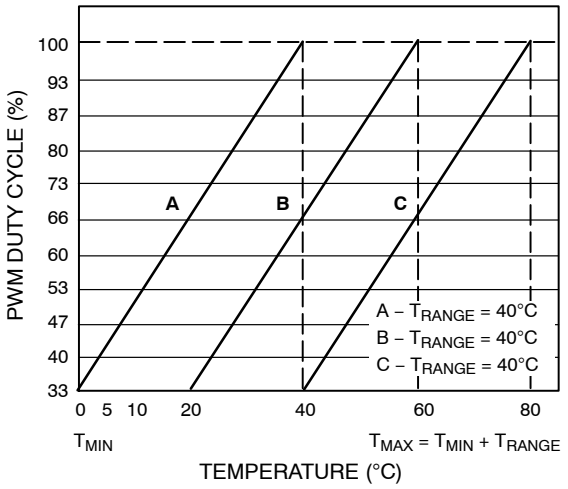


Figure 31. Effect of Increasing T_{MIN} Value on Control Loop

Fan Spin-up

As previously mentioned, once the temperature being measured exceeds the T_{MIN} value programmed, the fan will turn on at minimum speed (default = 33% duty cycle). However, the problem with fans being driven by PWM is that 33% duty cycle is not enough to reliably start the fan spinning. The solution is to spin the fan up for a predetermined time, and once the fan has spun up, its running speed may be reduced in line with the temperature being measured.

The ADM1029 allows fan spin-up times between 1/64 second and 16 seconds. The Fan Spin-up Register (Register 0x0C) allows the spin-up time for the fans to be programmed. Bit 3 of this register, when set, disables fan spin-up for both fans.

Table 10. FAN SPIN-UP TIMES

Bits 2:0	Spin-up Times (Fan Spin-up Register)
000	16 Seconds
001	8 Seconds
010	4 Seconds
011	2 Seconds (Default)
100	1 Second
101	1/4 Second
110	1/16 Second
111	1/64 Second

Once the Automatic Fan Speed Control Loop parameters have been chosen, the ADM1029 device may be programmed. The ADM1029 is placed into Automatic Fan

Speed Control Mode by writing to the three Temperature Cooling Action Registers (Registers 0x48, 0x49, 0x4A). The device powers up in Automatic Fan Speed Control Mode by default, as long as the T_{MIN}/Install pin (Pin 18) does not have the disable option selected (T_{MIN}/Install pin tied low or high). The default setting is that both fans will run at the fastest speed calculated by all three temperature channels. The control mode offers flexibility in that the user can decide which temperature channel/channels control each fan (five options).

Table 11. AUTOMATIC MODE FAN BEHAVIOR

Option	Temperature Cooling Action
1	Bit 0 Register 0x49 and/or Bit 1 Reg 0x4A = Remote Temp 1 Controls Fan 1, Remote Temp 2 Controls Fan 2
2	Bit 0 Register 0x48 and Bit 1 Register 0x48 = 1 Local Temp Controls Fan 1 and/or Fan 2
3	Bit 0 Register 0x49 and Bit 1 Register 0x49 = Remote Temp 1 Controls Fan 1 and/or Fan 2
4	Bit 0 Register 0x4A and Bit 1 Register 0x4A = Remote Temp 2 Controls Fan 1 and/or Fan 2
5	Bits 0, 1 Reg 0x48, 0x49, 0x4A = 1 Max Speed Calculated by Local and Remote Temperature Channels Controls Fans 1 and/or 2

When Option 5 is chosen, this offers increased flexibility. The Local and Remote temperature channels can have independently programmed control loops with different control parameters. Whichever control loop calculates the fastest fan speed based on the temperature being measured, drives both fans.

Figures 32 and 33 show how the fan's PWM duty cycle is determined by two independent control loops. This is the type of Automode Fan Behavior seen when Bits 0 and 1 of all three Temperature Cooling Action Registers = 11. Figure 32 shows the control loop for the Local Temperature channel. Its T_{MIN} value has been programmed to 20°C, and its T_{RANGE} value is 40°C.

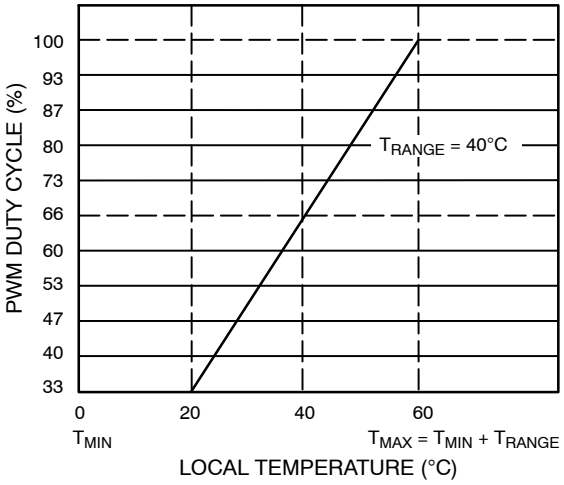


Figure 32. Max Speed Calculated by Local Temperature Control Loop Drive Fan

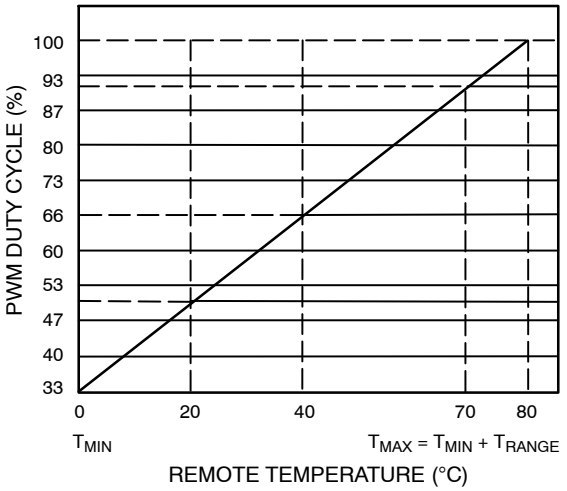


Figure 33. Max Speed Calculated by Remote Temperature Control Loop Drive Fan

The local temperature's T_{MAX} will thus be 60°C. Figure 33 shows the control loop for the Remote 1 Temperature channel. Its T_{MIN} value has been set to 0°C, while its T_{RANGE} = 80°C. Therefore, the Remote 1 Temperature's T_{MAX} value will be 80°C.

If both temperature channels measure 40°C, both control loops will calculate a PWM duty cycle of 66%. Therefore, the fans will be driven at 66% duty cycle.

If both temperature channels measure 20°C, the local channel will calculate 33% PWM duty cycle, while the Remote 1 channel will calculate 50% PWM duty cycle. Thus, the fans will be driven at 50% PWM duty cycle. Consider the local temperature measuring 60°C, while the Remote 1 temperature is measuring 70°C. The PWM duty cycle calculated by the local temperature control loop will be 100% (since the temperature = T_{MAX}). The PWM duty cycle calculated by the Remote 1 temperature control loop at 70°C will be approximately 90%. So the fans will run full speed (100% duty cycle). Remember that the fan speed will be based on the fastest speed calculated, and is not necessarily based on the highest temperature measured. Depending on the control loop parameters programmed, a lower temperature on one channel may actually calculate a faster speed than a higher temperature on another channel.

Programming the Automatic Fan Speed Control Loop

1. Program a value for T_{MIN}
2. Program a value for the slope T_{RANGE}
3. $T_{MAX} = T_{MIN} + T_{RANGE}$
4. Program a value for Fan Spin-up Time
5. Program the desired Automatic Fan Speed Control Mode Behavior, i.e., which temperature channel controls each fan

Other Control Loop Parameters?

Having programmed all the above loop parameters, are there any other parameters to worry about?

T_{MIN} was defined as being the temperature at which a fan switched on and ran at minimum speed. This minimum speed should be set to 33%. If the minimum PWM duty cycle is programmed to 33%, the fan control loops will operate as previously described.

It should be noted, however, that changing the minimum PWM duty cycle affects the control loop behavior.

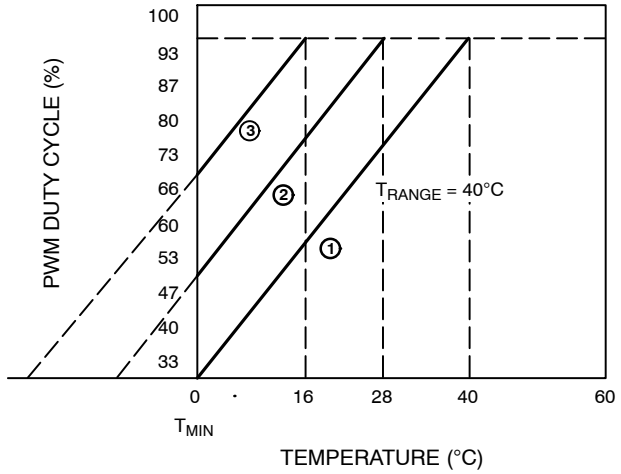


Figure 34. Effect of Changing Minimum Duty Cycle on Control Loop with T_{MIN} and T_{RANGE} Values

Table 12. PWM DUTY CYCLE SELECT MODE

Decimal Value	PWM Duty Cycle
00	0%
01	7%
02	14%
03	20%
04	27%
05	33% Recommended
06	40%
07	47%
08	53%
09	60%
10 (0x0A)	67%
11 (0x0B)	73%
12 (0x0C)	80%
13 (0x0D)	87%
14 (0x0E)	93%
15 (0x0F)	100% (Default)

* Bits <3:0> set the Minimum PWM duty cycle for Automatic Mode. Bits <7:4> set the Alarm Speed PWM duty cycle.

Slope 1 of Figure 34 shows T_{MIN} set to 0°C and the T_{RANGE} chosen is 40°C. In this case, the fan's PWM duty cycle will vary over the range 33% to 100%. The fan will run full speed at 40°C. If the minimum PWM duty cycle at which the fan runs at T_{MIN} is changed, its effect can be seen on Slopes 2 and 3. Take Case 2, where the minimum PWM duty cycle is reprogrammed from 33% (default) to 53%. The fan will actually reach full speed at a much lower temperature, 28°C. Case 3 shows that when the minimum PWM duty cycle was increased to 73%, the temperature at which the fan ran full speed was 16°C. So the effect of increasing the minimum PWM duty cycle, with a fixed T_{MIN} and fixed T_{RANGE}, is that the fan will actually reach full speed (T_{MAX}) at a lower temperature than T_{MIN} + T_{RANGE}. How can T_{MAX} be calculated?

In Automatic Fan Speed Control Mode, the registers holding the minimum PWM duty cycle at T_{MIN}, are the Minimum/Alarm Speed Registers (addresses 60h, 61h). Table 12 shows the relationship between the decimal values written to the Minimum/Alarm Speed Registers and PWM duty cycle obtained.

The temperature at which each fan will run full speed (100% duty cycle) is given by:

$$T_{MAX} = T_{MIN} + ((\text{Max DC} - \text{Min DC}) \times T_{RANGE}/10) \quad \text{(eq. 6)}$$

where:

T_{MAX} = Temperature at which fan runs full speed
T_{MIN} = Temperature at which fan will turn on
Max DC = Maximum Duty Cycle (100%) = 15 decimal
Min DC = Duty Cycle at TMIN, programmed into Fan Speed Config Register (default = 33% = 5 decimal)
T_{RANGE} = PWM Duty Cycle versus Temperature Slope

Example 1

T_{MIN} = 0°C, T_{RANGE} = 40°C
Min DC = 53% = 8 decimal (Table 12)

Calculate T_{MAX}

$$T_{MAX} = T_{MIN} + ((\text{Max DC} - \text{Min DC}) \times T_{RANGE}/10)$$

$$T_{MAX} = 0 + ((100\%\ \text{DC} - 53\%\ \text{DC}) \times 40/10) \quad \text{(eq. 7)}$$

$$T_{MAX} = 0 + ((15 - 8) \times 4) = 28$$

T_{MAX} =28 °C. (As seen on Slope 2 of Figure 34)

Example 2

T_{MIN} = 0°C, T_{RANGE} = 40°C
Min DC = 73% = 11 decimal (Table 12)

Calculate T_{MAX}

$$T_{MAX} = T_{MIN} + ((\text{Max DC} - \text{Min DC}) \times T_{RANGE}/10)$$

$$T_{MAX} = 0 + ((100\%\ \text{DC} - 73\%\ \text{DC}) \times 40/10) \quad \text{(eq. 8)}$$

$$T_{MAX} = 0 + ((15 - 11) \times 4) = 16$$

T_{MAX} =16 °C. (As seen on Slope 3 of Figure 34)

Example 3

T_{MIN} = 0°C, T_{RANGE} = 40°C
Min DC = 33% = 5 decimal (Table 12)

Calculate T_{MAX}

$$T_{MAX} = T_{MIN} + ((\text{Max DC} - \text{Min DC}) \times T_{RANGE}/10)$$

$$T_{MAX} = 0 + ((100\%\ \text{DC} - 33\%\ \text{DC}) \times 40/10) \quad \text{(eq. 9)}$$

$$T_{MAX} = 0 + ((15 - 5) \times 4) = 40$$

T_{MAX} =40 °C. (As seen on Slope 1 of Figure 34)

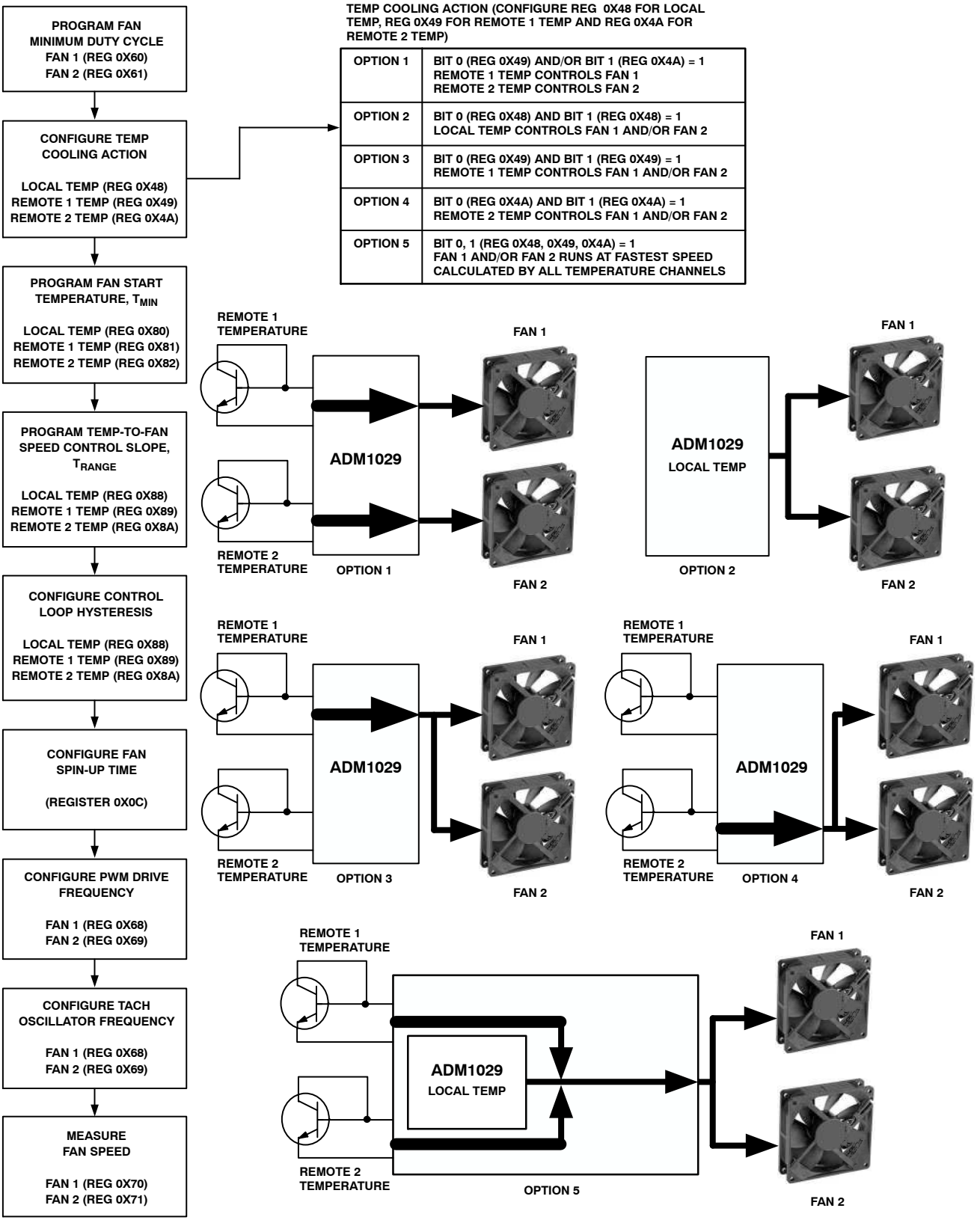


Figure 35. Configuring Automatic Fan Speed Control

Table 13. RESISTOR RATIOS FOR SETTING T_{MIN} AND NUMBER OF FANS INSTALLED USING TMIN/INSTALL PIN (PIN 18)

3 MSBs of ADC	Ideal Ratio R2/(R1 + R2)	R1 (kΩ)	R2 (kΩ)	Actual R2/(R1 + R2)	Error (%)	T_{MIN}	Fans Installed
111	N/A	0	∞	1	0	Disabled	2
110	0.8125	18	82	0.82	0.75	48°C	2
101	0.6875	22	47	0.6812	−0.63	40°C	2
100	0.5625	12	15	0.5556	−0.69	32°C	2
011	0.4375	15	12	0.4444	0.69	32°C	1
010	0.3125	47	22	0.3188	0.63	40°C	1
001	0.1875	82	18	0.18	−0.75	48°C	1
000	N/A	∞	0	0	0	Disabled	1

In this case, since the Minimum Duty Cycle is the default 33%, the equation for T_{MAX} reduces to:

$$T_{MAX} = T_{MIN} + ((\text{Max DC} - \text{Min DC}) \times T_{RANGE}/10)$$
$$T_{MAX} = T_{MIN} + ((15 - 5) \times T_{RANGE}/10)$$
$$T_{MAX} = T_{MIN} + (10 \times T_{RANGE}/10) \quad \text{(eq. 10)}$$
$$\mathbf{T_{MAX} = T_{MIN} + T_{RANGE}}$$

Enabling Automatic Fan Speed Control Using TMIN/INSTALL Pin (Pin 18)

Automatic fan control can also be enabled in hardware by Pin 18 (TMIN/INSTALL). This is an 8-level input with multiple functions, which is sampled only at power-up.

If only one fan is installed, the voltage on Pin 18 should be kept at less than $V_{CC}/2$, which clears Bit 1 of register 03h. Within this voltage range, four voltage levels define the minimum temperature at which the fan will operate in automatic speed control mode.

If two fans are installed, the voltage on Pin 18 should be between $V_{CC}/2$ and V_{CC}, which sets Bit 1 of register 03h. Within this voltage range, four voltage levels define the minimum temperature at which the fans will operate in automatic speed control mode.

Resistor values for setting the voltage on Pin 18 are given in Table 13. If automatic fan speed control is not used, Pin 18 can simply be strapped to ground (one fan) or V_{CC} (two fans), depending on how many fans are installed. Under this condition, the fans will run full speed until the device is written to by software to change fan speed.

When automatic fan speed control is enabled at power-up by the TMIN/INSTALL pin, Bit 4 of the Configuration register is set to enable monitoring, and Bits 0 and 1 of all Temp. Cooling Action Registers are set, so any temperature channel will automatically control all fans that are installed.

NOTE: if automatic fan speed control is enabled and an event occurs that would cause a fan to go to alarm or hot-plug speed (e.g., temperature fault), that event will override the automatic fan speed control. If the event affects only one fan, the other fan will remain under automatic control.

Fan-related Registers

Table 14 is a list of registers on the ADM1029 that are specific to fan speed measurement and control:

Table 14. TEMPERATURE-SPECIFIC REGISTERS

Address	Description
0x02	Fans Supported By Controller
0x03	Fans Supported In System
0x07	Set Fan x Alarm Speed
0x08	Set Fan x Hot-Plug Speed
0x09	Set Fan x Full Speed
0x10	Fan 1 Status
0x11	Fan 2 Status
0x18	Fan 1 Fault Action
0x19	Fan 2 Fault Action
0x20	Fan 1 Event Mask
0x21	Fan 2 Event Mask
0x48	Local Temp Cooling Action
0x49	Remote 1 Cooling Action
0x4A	Remote 2 Cooling Action
0x60	Fan 1 Minimum/Alarm Speed
0x61	Fan 2 Minimum/Alarm Speed
0x68	Fan 1 Configuration
0x69	Fan 2 Configuration
0x70	Fan 1 Tach Value
0x71	Fan 2 Tach Value
0x78	Fan 1 Tach High Limit
0x79	Fan 2 Tach High Limit

Fan Configuration Registers

Registers 0x68 and 0x69 are the Fan 1 and Fan 2 Configuration Registers. These allow the PWM output frequencies to be selected for each fan. The default PWM drive frequency is 250 Hz. Bits <7:6> adjust the fan tach oscillator frequency for fan tach measurements. Bits <3:0> allow the Hot Plug PWM duty cycle value for each fan to be programmed.

Figures 36 and 37 show how to configure the fans to handle thermal or fault events.

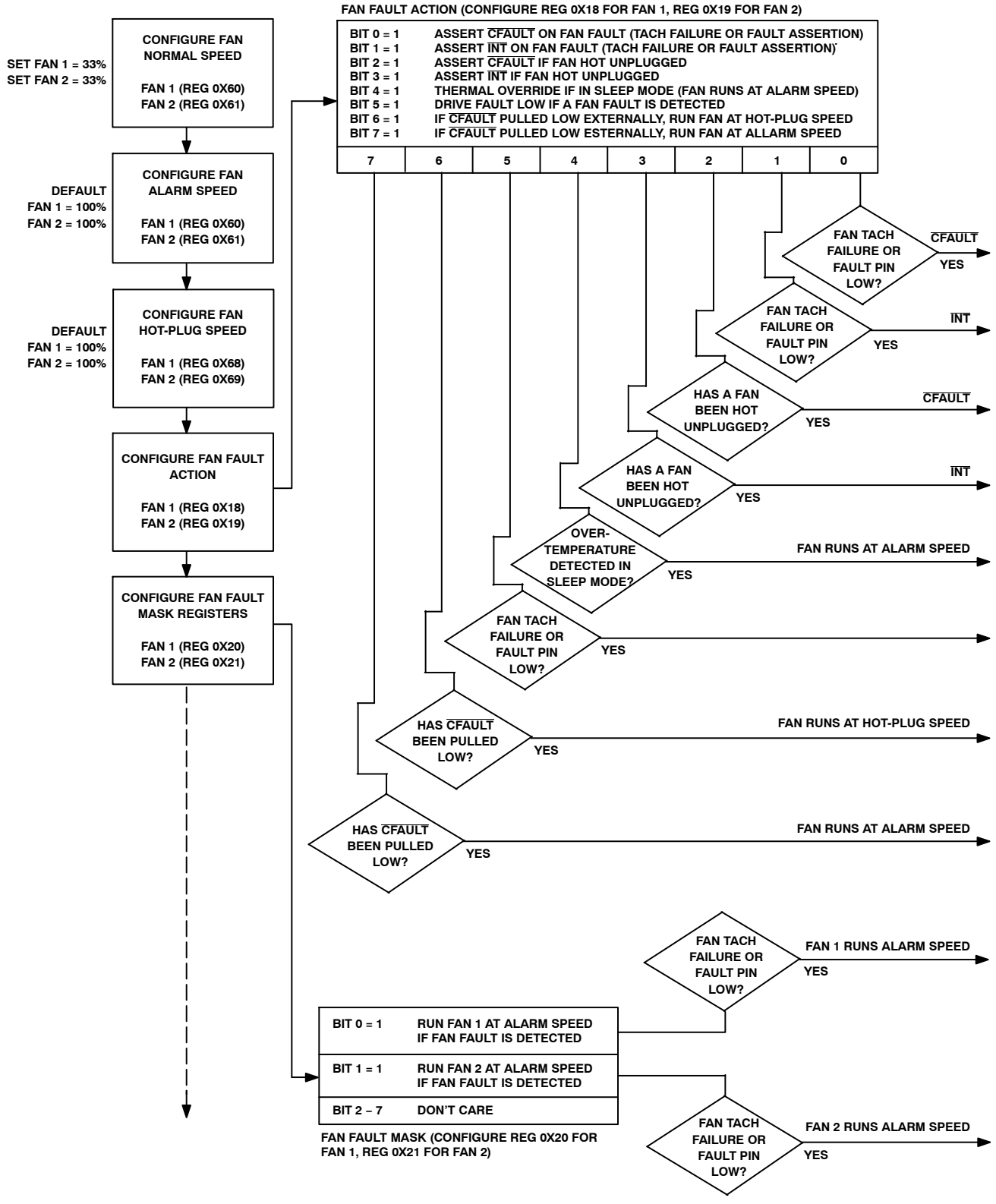


Figure 36. Fan Configuration Flowchart

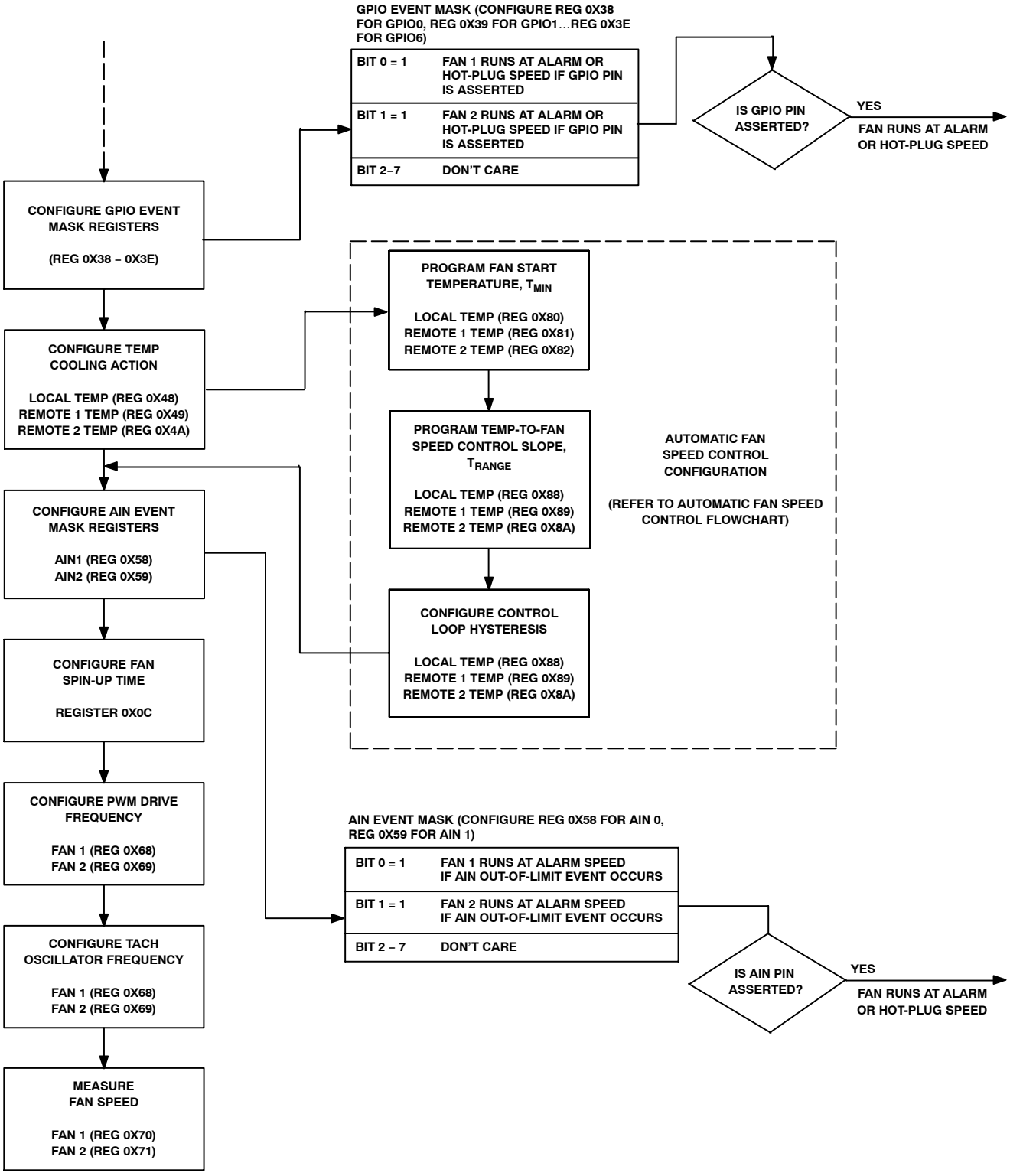


Figure 37. Fan Configuration Flowchart (Continued)