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Secondary-Side Controller with Current Share and Housekeeping

ADM1041

PRODUCT FEATURES

Digital calibration via internal EEPROM
Supports SSI specification
Comprehensive fault detection
Reduced component count on secondary side
Standalone or microcontroller control

SECONDARY-SIDE FEATURES

Generates error signal for primary-side PWM
Output voltage adjustment and margining
Current sharing
Current limit adjustment
OrFET control
Programmable soft-start slew rate
Standalone or microcontroller operation
Differential load voltage sense
AC mains undervoltage detection (ac sense)
Overvoltage protection

INTERFACE AND INTERNAL FEATURES

SMBus interface (I^2C compatible)
Low-drift precision 2.5 V reference
Voltage error amplifier
Differential current sense
Sense resistor or current transformer option
Overvoltage protection
Undervoltage protection
Overcurrent protection
Overtemperature protection
Start-up undervoltage blanking
Programmable digital debounce and delays
352-byte EEPROM available for field data
160-byte EEPROM for calibration
Ground continuity monitoring

APPLICATIONS

Network servers
Web servers
Power supply control

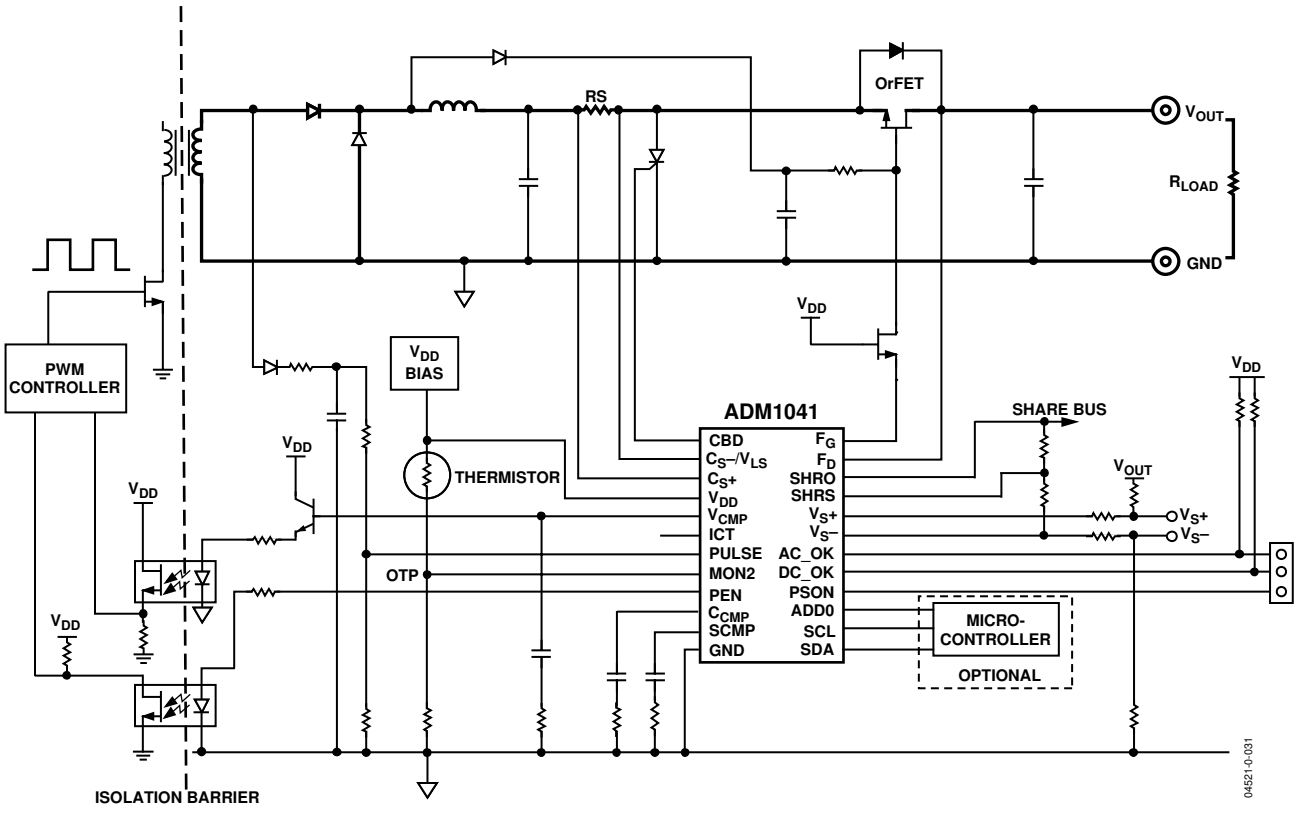

Figure 1. Typical Application Circuit

Rev. A

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REVISION HISTORY

3/04-Revision Sp0: Initial Version

5/04-Changed from Rev. Sp0 to Rev. A

GENERAL DESCRIPTION

The ADM1041 is a secondary-side and management IC specifically designed to minimize external component counts and to eliminate the need for manual calibration or adjustment on the secondary-side controller. The principle application of this IC is to provide voltage control, current share, and housekeeping functions for single output in N+1 server power supplies.

The ADM1041 is manufactured with a 5 V CMOS process and combines digital and analog circuitry. An internal EEPROM provides added flexibility in the trimming of timing and voltage and selection of various functions. Programming is done via an SMBus serial port that also allows communication capability with a microprocessor or microcontroller.

The usual configuration using this IC is on a one per output basis. Outputs from the IC can be wire-ORed together or bused in parallel and read by a microprocessor. A key feature on this IC is support for an OrFET circuit when higher efficiency or power density is required.

SAMPLE APPLICATION CIRCUIT DESCRIPTION

Figure 1 shows a sample application circuit using the ADM1041. The primary side is not detailed and the focus is on the secondary side of the power supply.

The ADM1041 controls the output voltage from the power supply to the designed programmed value. This programmed value is determined during power supply design and is digitally adjusted via the serial interface. Digital adjustment of the current sense and current limit is also calibrated via the serial interface, as are all of the internal timing specifications.

The control loop consists of a number of elements, notably the inputs to the loop and the output of the loop. The ADM1041 takes the loop inputs and determines what, if any, adjustments are needed to maintain a stable output. To maintain a stable loop, the ADM1041 uses three main inputs:

- Remote voltage sense
- Load current sense
- Current sharing information

In this example, a resistor divider senses the output current as a voltage drop across a sense resistor (RS) and feeds a portion into the ADM1041. Remote local voltage sense is monitored via V_S+ and V_S- pins. Finally, current sharing information is fed back via the share bus. These three elements are summed together to generate a control signal (V_{CMP}), which closes the loop via an optocoupler to the primary side PWM controller.

Another key feature of the ADM1041 is its control of an OrFET. The OrFET causes lower power dissipation across the ORing diode. The main function of the OrFET is to disconnect the power supply from the load in the event of a fault occurring during steady state operation, for example, if a filter capacitor or rectifier fails and causes a short. This eliminates the risk of bringing down the load voltage that is supplied by the redundant configuration of other power supplies. In the case of a short, a reverse voltage is generated across the OrFET. This reverse voltage is detected by the ADM1041 and the OrFET is shut down via the F_G pin. This intervention prevents any interruption on the power supply bus. The ADM1041 can then be interrogated via the serial interface to determine why the power supply has shut down.

This application circuit also demonstrates how temperature can be monitored within a power supply. A thermistor is connected between the V_{DD} and MON2 pins. The thermistor's voltage varies with temperature. The MON2 input can be programmed to trip a flag at a voltage corresponding to an overheating power supply. The resulting action may be to turn on an additional cooling fan to help regulate the temperature within the power supply.

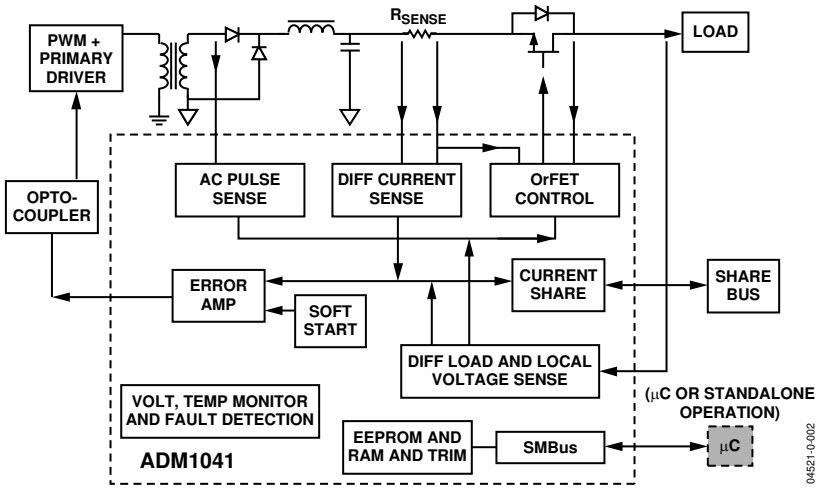

Figure 2. Application Block Diagram

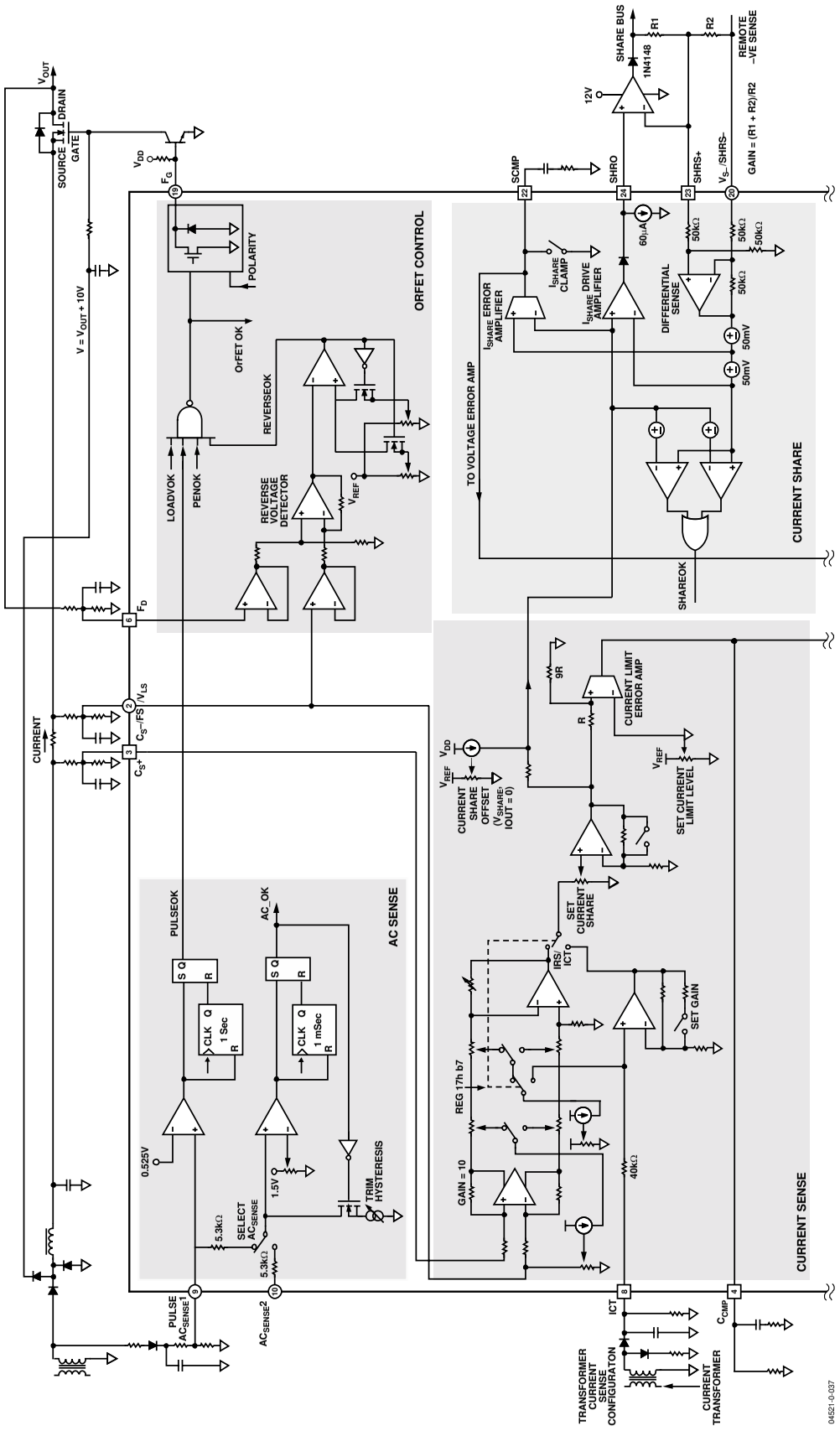

Figure 3. Chip Diagram, Part 1

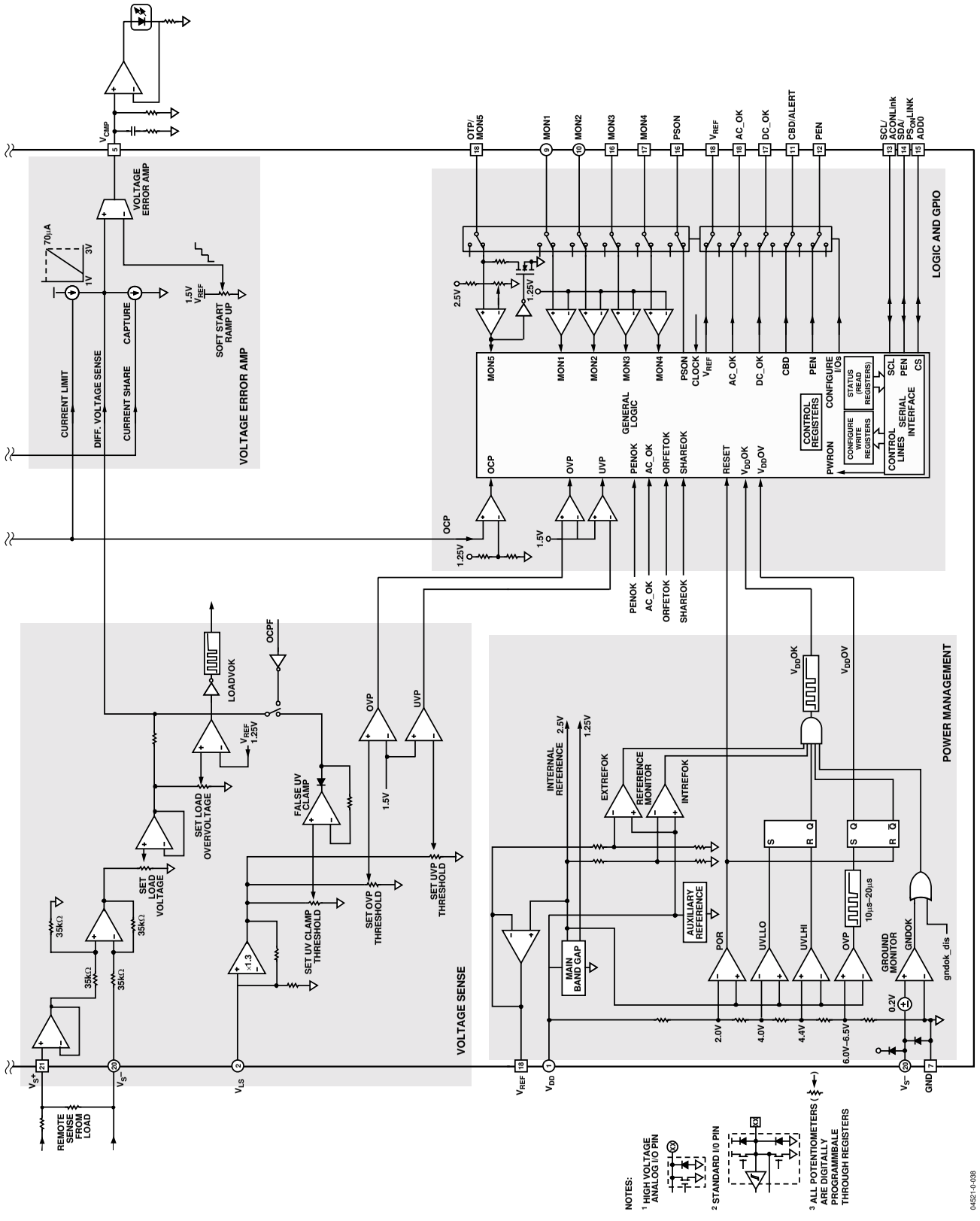

Figure 4. Chip Diagram, Part 2

SPECIFICATIONS

T_A = −40 to +85°C, V_{DD} = 5 V ± 10%, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLIES					
V_{DD}	4.5	5.0	5.5	V	
I_{DD}, Current Consumption		6	10	mA	
Peak I_{DD}, during EEPROM Erase Cycle[1, 2]			40	mA	
UNDERVOLTAGE LOCKOUT, V_{DD}					See Figure 9.
Start-Up Threshold	4	4.3	4.5	V	
Stop Threshold	3.7	4	4.2	V	
Hysteresis		0.3		V	
V_{REF}, 2.5 V_{REFOUT}					Reg 0Fh[4:2] = 111. See Table 24.
Output Voltage	2.49	2.50	2.51	V	I_{REF} = 1 mA, T_A = 25°C
Line Regulation	−5	0	+5	mV	4.5 V ≤ V_{DD} ≤ 5.5 V
Load Regulation	−5	0	+5	mV	0 mA ≤ I_{REF} ≤ 2 mA
Temperature Stability[2]		±100		ppm/°C	I_{REF} = 1 mA
Long-Term Stability[2]		±5		mV	Over 1,000 hr, T_J = 125°C
Current Limit		10	20	mA	V_{REF} = 2.4 V
Output Resistance[2]		0.5		Ω	
Load Capacitance		1		nF	Recommended for stability
Ripple Due to Autozero[2]		±5		mV p-p	V_{REF} refreshed at 30 kHz
POWER BLOCK PROTECTION					
V_{DD} Overvoltage	5.8	6.2	6.5	V	
V_{DD} Overvoltage Debounce	10		20	µs	Latching
V_{REF} Overvoltage		2.9		V	Internal
V_{REFOUT} Undervoltage		2.1		V	External
Open Ground	0.1	0.2	0.35	V	V_{GND} positive with respect to V_S−
Debounce	100		200	µs	V_{DD}OK
POWER-ON RESET					
DC Level	1.5	2.2	2.75	V	V_{DD} rising
DIFFERENTIAL LOAD VOLTAGE SENSE INPUT, (V_S−, V_S+)					See Figure 6. V_{NOM} = (V_S+ − V_S−) V_{NOM} is typically 2 V
V_S− Input Voltage			0.5	V	Voltage on Pin 20
V_S+ Input Voltage			V_{DD} − 2	V	Voltage on Pin 21
V_S− Input Resistance		35		kΩ	
V_S+ Input Resistance	500			kΩ	
V_{NOM} Adjustment Range		1.7 to 2.3		V	
Set Load Voltage Trim Step		0.10 to 0.14		%	1.7 V ≤ V_{NOM} ≤ 2.3 V typ
		1.74 –> 3.18		mV	8 bits, 255 steps
					Reg 19h[7:0]. See Table 34
Set Load Overvoltage Trim Range		105 to 120		%	1.7 V ≤ V_{NOM} ≤ 2.3 V min
Set Load Overvoltage Trim Step		0.09		%	8 bits, 255 step/s
		1.6		mV	Reg 08h[7:0]. See Table 17.
					V_S+ = 2.24 V
Recover from Load OV False to F_G True		100		µs	Reg 03h[1:0] = 00. See Table 12.
		200		µs	Reg 03h[1:0] = 01. See Table 12.
		300		µs	Reg 03h[1:0] = 10. See Table 12.
		400		µs	Reg 03h[1:0] = 11. See Table 12.
Operate Time from Load OV to F_G False		2		µs	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOCAL VOLTAGE SENSE, V_{LS}, AND FALSE UV CLAMP					See Figure 9.
Input Voltage Range[3]		2.3	V_{DD}–2	V	Set by external resistor divider.
Stage Gain		1.3			At V_{LS} = 1.8 V
False UV Clamp, V_{LS}, Input Voltage Nominal, and Trim Range	1.3	1.85	2.1	V	
Clamp Trim Step		0.2		%	V_{RANGE}
Clamp Trim Step		3.1		mV	8 bits, 255 steps, Reg 18h[7:0]. See Table 33.
Local Overvoltage	1.9	2.4	2.85	V	
Nominal and Trim Range					
OV Trim Step		0.15		%	V_{RANGE}
OV Trim Step		3.7		mV	8 bits, 255 steps Reg 0Ah[7:0]. See Table 33.
Noise Filter, for OVP Function Only	5		25	µs	
Local Undervoltage	1.3	1.7	2.1	V	
Nominal and Trim Range					
UV Trim Step		0.18		%	V_{RANGE}
UV Trim Step		3.1		mV	8 bits, 255 steps, Reg 09h[7:0]. See Table 18.
Noise Filter, for UVP Function Only	300		600	µs	
VOLTAGE ERROR AMPLIFIER, V_{CMP}					See Figure 14.
Reference Voltage $V_{REF\_SOFT\_START}$	1.49		1.51	V	T_A = 25°C
Temperature Stability[2]		±100		µV/°C	−40°C ≤ T_A ≤ 85°C
Long-Term Voltage Stability[2]		±0.2		%	Over 1,000 hr, T_J = 125°C
Soft-start Period Range	0		40	ms	Ramp is 7 bit, 127 steps
Set Soft-start Period		300		µs	Reg 10h[3:2] = 00. See Table 25.
		10		ms	Reg 10h[3:2] = 01. See Table 25.
		20		ms	Reg 10h[3:2] = 10. See Table 25.
		40		ms	Reg 10h[3:2] = 11. See Table 25.
Unity Gain Bandwidth, GBW		1		MHz	See Figure 11.
Transconductance	1.9	2.7	3.5	mA/V	At I_{VCMP} = ±180 µA
Source Current	250			µA	At V_{VCMP} > 1 V
Sink Current	250			µA	At V_{VCMP} < V_{DD} − 1 V
DIFFERENTIAL CURRENT SENSE INPUT, C_S−, C_S+					Reg 17h[7] = 0. See Table 18. I_{SENSE} mode. See Figure 13.
Common-Mode Range	0		V_{DD}–2	V	Set by external divider
External Divider Tolerance Trim Range (with respect to input)		−5		mV	Reg 16h[5:3] = 000. See Table 31.
		−10		mV	Reg 16h[5:3] = 001. See Table 31.
		−20		mV	Reg 16h[5:3] = 010. See Table 31.
		5		mV	Reg 16h[5:3] = 100. See Table 31.
		10		mV	Reg 16h[5:3] = 101. See Table 31.
		20		mV	Reg 16h[5:3] = 110. See Table 31.
External Divider Tolerance Trim Step Size (with respect to input)		20		µV	V_{CM} = 2.0 V
		39		µV	8 bits, 255 steps
		78		µV	Reg 14h[7:0]. See Table 29.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC Offset Trim Range (with respect to input)		−8		mV	Reg 17h[2:0] = 000. See Table 32 .
		−15		mV	Reg 17h[2:0] = 001. See Table 32.
		−30		mV	Reg 17h[2:0] = 010. See Table 32.
		8		mV	Reg 17h[2:0] = 100. See Table 32.
		15		mV	Reg 17h[2:0] = 101. See Table 32.
		30		mV	Reg 17h[2:0] = 110. See Table 32.
DC Offset Trim Step Size		30		µV	V_{CM} = 2.0 V, V_{DIFF} = 0 V
(with respect to input)		50		µV	8 bits, 255 steps
		120		µV	Reg 15h[7:0]. See Table 30.
CURRENT SENSE CALIBRATION					
Total Current Sense Error[2] (Gain and Offset)					V_{CSCM} = 2.0V, 0°C ≤ T_A ≤ 85 °C SHRS = SHRO = 2 V. Gain = 230x
		±3		%	Chopper ON
		±6		%	Chopper OFF
Gain Range (I_{SENSE})					Input voltage range at C_S+, C_S−
Gain Setting 1 (Reg 16h[2:0] = 000)		65		V/V	34.0 mV – 44.5 mV. Gain = 65×
Gain Setting 2 (Reg 16h[2:0] = 001)		85		V/V	26.0 mV – 34.0 mV. Gain = 85×
Gain Setting 3 (Reg 16h[2:0] = 010)		110		V/V	20.0 mV – 26.0 mV. Gain = 110×
Gain Setting 4 (Reg 16h[2:0] = 100)		135		V/V	16.0 mV – 20.0 mV. Gain = 135×
Gain Setting 5 (Reg 16h[2:0] = 101)		175		V/V	12.0 mV – 16.0 mV. Gain = 175×
Gain Setting 6 (Reg 16h[2:0] = 110)		230		V/V	9.5 mV – 12.0 mV. Gain = 230×
Full Scale (No Offset)		2.0		V	V_{ZO} = 0
Attenuation Range		65 to 99		%	Reg 06h[7:1]. See Table 15.
Current Share Trim Step (at SHRO)		0.4		%	SHRS = SHRO = 1 V
		8		mV	7 bits, 127 steps I_{SHARE} slope
Gain Accuracy[2, 4], 40 mV at C_S+, C_S−	−5		+5	%	0 V ≤ V_{CSCM} ≤ 0.3 V. Gain = 65× V_{CSCM} = Input Common Mode
Gain Accuracy[2, 4], 20 mV at C_S+, C_S−	−5	±1	+5	%	V_{CSCM} = 2.0V, 0°C ≤ T_A ≤ 85°C Gain = 135×
Gain Accuracy[2, 4], 40 mV at C_S+, C_S−	−2.5	±0.5	+2.5	%	V_{CSCM} = 2.0 V, 0°C ≤ T_A ≤ 85°C Gain = 65×
SHARE BUS OFFSET					See Figure 13.
Current Share Offset Range	1.25			V	Reg 17h[7] = 1. See Table 32. Reg 17h[5] = 1. See Table 32.
Zero Current Offset Trim Step					0 ≤ V_{TRIM} ≤ 1.25 V
		0.4		%	8 bits, 255 steps, V_{CT} = 1.0 V
		5.5		mV	Reg 05h[7:0]. See Table 14.
CURRENT TRANSFORMER SENSE INPUT, I_{CT}					Reg 17h[7] = 1. See Table 32. Reg 06h = FEh. See Table 15.
Gain Setting 0		4.5		V/V	Reg 17h[5] = 0, V_{SHARE} = 2 V. Table 31
Gain Setting 1		2.57		V/V	Reg 17h[5] = 1. See Table 32.
					Reg 15h = 05h, approx 1 µA. See Table 30. V_{SHARE} = 2 V.
CT Input Sensitivity	0.45	0.5	0.68	V	Gain setting = 4.5
CT Input Sensitivity	0.79	1.0	1.20	V	Gain setting = 2.57
Input Impedance[2]	20	50		kΩ	
Source Current		2.0		µA	See Current Transformer Input Section.
Source Current Step Size		170		nA	15 steps Reg 15h[3:0]. See Table 30.
Reverse Current for Extended SMBus Addressing (Source Current)[5]	3.5	5	7	mA	See Figure 38. See Absolute Maximum Ratings.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT LIMIT ERROR AMPLIFIER					See Figure 13
Current Limit Trim Range[2]	105		130	%	After I_{SHARE} calibration
Current Limit Trim Step		1.1		%	
Current Limit Trim Step		26.5		mV	$2.0 \le V_{SHARE} \le 2.8$ V typ. 5 bits, 31 steps. Reg 04h[7:3]. See Table 13.
Transconductance	100	200	300	µA/V	I_{CCMP} = ±20 µA. See Figure 12.
Output Source Current		40		µA	V_{CCMP} = > 1 V
Output Sink Current		40		µA	V_{CCMP} = < V_{DD} − 1 V
CURRENT SHARE DRIVER					See Figure 14.
Output Voltage[6]	V_{DD} − 0.4			V	R_L = 1 kΩ, $V_{SHRS} \le V_{DD}$ − 2 V
Short Circuit Source Current			55	mA	
Source Current			15	mA	Current at which V_{OUT} does not drop by more than 5%
Sink Current		60	100	µA	V_{SHARE} = 2.0 V
CURRENT SHARE DIFFERENTIAL SENSE AMPLIFIER					See Figure 14.
V_S− Input Voltage			0.5	V	Voltage on Pin 20
V_{SHRS} Input Voltage			V_{DD} − 2	V	Voltage on Pin 23
Input Impedance[2]	65	100		kΩ	V_{SHRS} = 0.5 V, V_S− = 0.5 V
Gain		1.0		V/V	
CURRENT SHARE ERROR AMPLIFIER					
Transconductance, SHRS to SCMP	100	200	300	µA/V	I_{SCMP} = ±20 µA
Output Source Current		40		µA	V_{SCMP} > 1 V
Output Sink Current		40		µA	V_{SCMP} < V_{DD} − 1 V
Input Offset Voltage	40	50	60	mV	Master/slave arbitration
Share OK Window Comparator Threshold					SHRS = 2 V ± SHR_{THRESH}
(Share Drive Error)		±100		mV	Reg 04h[1:0] = 00. See Table 13.
		±200		mV	Reg 04h[1:0] = 01. See Table 13.
		±300		mV	Reg 04h[1:0] = 10. See Table 13.
		±400		mV	Reg 04h[1:0] = 11. See Table 13.
CURRENT LIMIT					Figure 10.
Current Limit Control Lower Threshold	1.3			V	V_{CCMP} = 0.7 V, V_S+ = 1.5 V
Current Limit Control Upper Threshold			3.5	V	V_S+ = 0 V, V_{SCMP} = 0 V
CURRENT SHARE CAPTURE					V_{SCMP} = 3.5 V.
Current Share Capture Range	0.7	1	1.3	%	Reg 10h[5:4] = 00. See Table 25.
	1.4	2	2.6	%	Reg 10h[5:4] = 01. See Table 25.
	2.1	3	3.9	%	Reg 10h[5:4] = 10. See Table 25.
	2.8	4	5.2	%	Reg 10h[5:4] = 11. See Table 25.
Capture Threshold	0.6	1.0	1.4	V	
FET OR GATE DRIVE					Open-drain N-channel FET
Output Low Level (On)			0.4	V	I_{IO} = 5 mA
			0.8	V	I_{IO} = 10 mA
Output Leakage Current	−5		+5	µA	
REVERSE VOLTAGE COMPARATOR, FS, FD					V_{CS-} = FS
Common-Mode Range	0.25	2.0	V_{DD} − 2	V	Voltage set by C_S resistor divider Voltage on C_S− pin. T_A = 25°C.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Reverse Voltage Detector Turn-Off Threshold					V_{CS-} = 2 V for threshold specs
		100		mV	Reg 03h[7:6] = 00. See Table 12.
		150		mV	Reg 03h[7:6] = 01. See Table 12.
		200		mV	Reg 03h[7:6] = 10. See Table 12.
		250		mV	Reg 03h[7:6] = 11. See Table 12.
Reverse Voltage Detector Turn-On Threshold					V_{CS-} = 2 V for threshold specs
		20		mV	Reg 03h[5:4] = 00. See Table 12.
		30		mV	Reg 03h[5:4] = 01. See Table 12.
		40		mV	Reg 03h[5:4] = 10. See Table 12.
		50		mV	Reg 03h[5:4] = 11. See Table 12.
FD Input Impedance	500			kΩ	
FS Input Impedance		20		kΩ	
$AC_{SENSE}1/AC_{SENSE}2$ COMPARATOR					Reg 12h[2] = 0
					Reg 0Dh[3:2] = 00. See Table 22 .
(AC or Bulk Sense)					Reg 12h[2] = 1
					Reg 0Eh[7:6] = 00. See Table 23.
Threshold Voltage		1.25		V	
Threshold Adjust Range	1.10		1.40	V	Min: DAC = 0
					Max: DAC = Full Scale
Threshold Trim Step		0.8		%	1.10 ≤ V_{TRIM} ≤ 1.4 V
		10		mV	5 bits, 31 steps
					Reg 0Ch[7:3]. See Table 21.
Hysteresis Adjust Range		200−550		mV	$V_{ACSENSE}$ > 1 V, $R_{THEVENIN}$ = 909R
Hysteresis Trim Step		50		mV	200 ≤ V_{TRIM} ≤ 550 mV. 7 steps
					Reg 0Ch[2:0]. See Table 21.
Noise Filter	0.6	1	1.2	ms	
PULSE-IN					
Threshold Voltage		0.525		V	
PULSE_OK On Delay		1		µs	
PULSE_OK Off Delay	0.8	1	1.2	s	
OSCILLATOR	−5		+5	%	Unless otherwise specified
OCP					
OCP Threshold Voltage[2]	0.3	0.5	0.7	V	Force C_{CMP} for drop in V_{CMP}
					Reg 11h[2] = 0. See Table 26.
OCP Shutdown Delay Time (Continuous Period in Current Limit)		1		s	Reg 12h[4:3] = 00. See Table 27.
		2		s	Reg 12h[4:3] = 01. See Table 27.
		3		s	Reg 12h[4:3] = 10. See Table 27.
		4		s	Reg 12h[4:3] = 11. See Table 27.
OCP Fast Shutdown Delay Time	0		100	ms	Reg 11h[2] = 1. See Table 26.
					VC_{CMP} = 1.5 V
MON1, MON2, MON3, MON4					
Sense Voltage	1.21	1.25	1.29	V	
Hysteresis		0.1		V	
OVP Noise Filter	5		25	µs	
UVP Noise Filter	300		600	µs	
OTP (MON5)					Reg 0Fh[4:2] = 01x or 10x. Table 24.
Sense Voltage Range	2.2		2.45	V	
OTP Trim Step		24		mV	2.1 ≤ V_{TRIM} ≤ 2.45 V
					4 bits, 15 steps, Reg 0Bh[7:4].
					See Table 20.
Hysteresis	100	130	160	µA	V_{OTP} = 2 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OVP Noise Filter	5		25	µs	Reg 0Fh[4:2] = 010 or 100. See Table 24.
UVP Noise Filter	300		600	µs	Reg 0Fh[4:2] = 011 or 101. See Table 24.
PSON[7]					Reg 0Eh[4:2] = 00x. See Table 23.
Input Low Level[8]			0.8	V	
Input High Level[8]	2.0			V	
Debounce		80		ms	Reg 0Fh[1:0] = 00. See Table 24.
		0		ms	Reg 0Fh[1:0] = 01. See Table 24.
		40		ms	Reg 0Fh[1:0] = 10. See Table 24.
		160		ms	Reg 0Fh[1:0] = 11. See Table 24.
PEN[7], DC_OK[7], CBD, AC_OK					
Open-Drain N-Channel Option					
Output Low Level = On[8]			0.4	V	I_{SINK} = 4 mA
Open-Drain P-Channel					V_{OH_PEN}
Output High Level = On[8]	2.4			V	I_{SOURCE} = 4 mA
Leakage Current	−5		+5	µA	
DC_OK[7]					Reg 0Fh[7:5] = 00x. See Table 24.
DC_OK, On Delay (Power-On and OK Delay)		400		ms	Reg 0Eh[1:0] = 00. See Table 23.
		200		ms	Reg 0Eh[1:0] = 01.See Table 23.
		800		ms	Reg 0Eh[1:0] = 10. See Table 23.
		1600		ms	Reg 0Eh[1:0] = 11. See Table 23.
DC_OK, Off Delay (Power-Off Early Warning)		2		ms	Reg 10h[7:6] = 00. See Table 25.
		0		ms	Reg 10h[7:6] = 01. See Table 25.
		1		ms	Reg 10h[7:6] = 10. See Table 25.
		4		ms	Reg 10h[7:6] = 11. See Table 25.
SMBus, SDL/SCL					
Input Voltage Low[8]			0.8	V	
Input Voltage High[8]	2.2			V	
Output Voltage Low[8]			0.4	V	V_{DD} = 5 V, I_{SINK} = 4 mA
Pull-Up Current	100		350	µA	
Leakage Current	−5		+5	µA	
ADD0, HARDWIRED ADDRESS BIT					
ADD0 Low Level[8]			0.4	V	
ADD0 Floating		V_{DD}/2		V	Floating
ADD0 High[8]	V_{DD} − 0.5			V	
SERIAL BUS TIMING					See Figure 5.
Clock Frequency			400	kHz	
Glitch Immunity, t_{SW}			50	ns	
Bus Free Time, t_{BUF}	4.7			µs	
Start Setup Time, $t_{SU;STA}$	4.7			µs	
Start Hold Time, $t_{HD;STA}$	4			µs	
SCL Low Time, t_{LOW}	4.7			µs	
SCL High Time, t_{HIGH}	4			µs	
SCL, SDA Rise Time, t_R			1000	ns	
SCL, SDA Fall Time, t_F			300	ns	
Data Setup Time, $t_{SU;DAT}$	250			ns	
Data Hold Time, $t_{HD;DAT}$	300			ns	
EEPROM RELIABILITY					
Endurance[9]	100	250		k cycles	
Data Retention[10]	100			Years	

[1] This specification is a measure of I_{DD} during an EEPROM page erase cycle. The current is a dynamic. Refer to Figure 29 for a typical I_{DD} plot during an EEPROM page erase.
[2] Specification is not production tested, but is supported by characterization data at initial product release.
[3] Four external divider resistors are the same ration, which is selected to produce 2.0 V nominal at Pin 21 while at zero load current. Recommended values are

	3.3 V	5.0 V	12 V
R_{TOP}	680R	1K.5	5K1
R_{BOTTOM}	1K	1K	1K

[4] Chopper off.
[5] The maximum specification here is the maximum source current of Pin 8 as specified by the Absolute Maximum Ratings.
[6] All internal amplifiers accept inputs with common range from GND to V_{DD} − 2 V. The output is rail to rail but the input is limited to GND to V_{DD} − 2 V. See Figure 6.
[7] These pins can be configured as open-drain N-channel or P-channel, (except PSON) and as normal or inverted logic polarity. Refer to Table 45.
[8] A logic true or false is defined strictly according to the signal name. Low and high refer to the pin or signal voltages.
[9] Endurance is qualified to 100,000 cycles as per JEDEC std. 22 method A117, and measured at −40°C, +25°C, and +85°C. Typical endurance at 25°C is 250,000 cycles.
[10] Retention lifetime equivalent at junction temperature (T_J) = 55°C as per JEDEC std. 22 method A117. Retention lifetime based on an activation energy of 0.6 V. Derates with junction temperature.

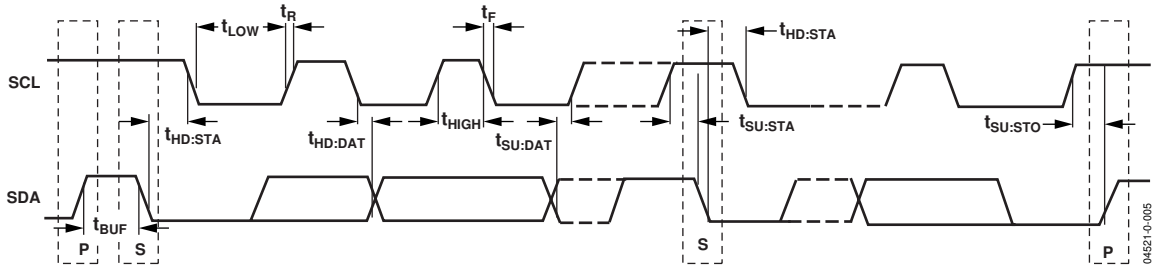

Figure 5. Serial Bus Timing Diagram

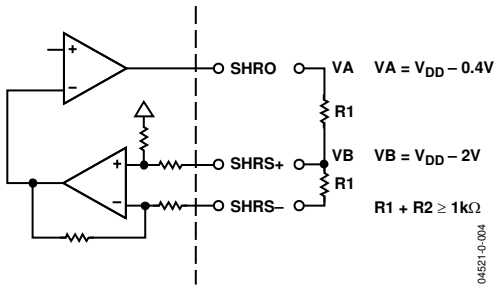

Figure 6. Amplifier Inputs and Outputs

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (Continuous), V_{DD}	6.5 V
Data Pins SDA, SCL, V_{DATA}	V_{DD} + 0.5 V, GND − 0.3 V
Continuous Power at 25°C, $P_{D\text{-}QSOP24}$	450 mW
Operating Temperature, T_{AMB}	−40°C to +85°C
Junction Temperature, T_J	150°C
Storage Temperature, T_{STG}	−60°C to +150°C
Lead Temperature (Soldering, 10 Seconds), T_L	300°C
ESD Protection on All Pins, V_{ESD}	2 kV
Thermal Resistance, Junction to Air, θ_{JA}	150°C/W
I_{CT} Source Current[1]	7 mA

[1] This is the maximum current that can be sourced out from Pin 8 (I_{CT} pin).

Thermal Characteristics

24-Lead QSOP Package:
θ_{JA} = 150°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

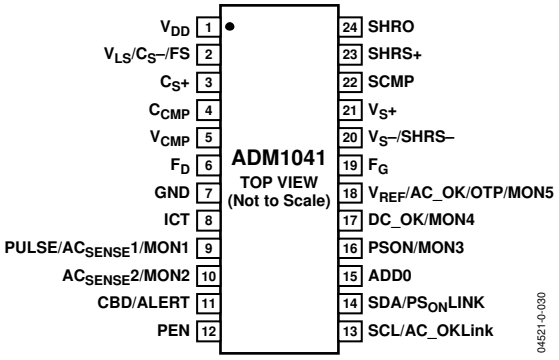

Figure 7. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Positive Supply for the ASIC. Normal range is 4.5 V to 5.5 V. Absolute maximum rating is 6.5 V.
2	$V_{LS}/C_S-/FS$	Inverting Differential Current Sense Input, Local Voltage Sense Pin, and OrFET Source. These three functions are served by a common divider. The local voltage sense input is used for local overvoltage and undervoltage sensing. This pin also provides an input to the false UV clamp that prevents shutdown during an external load overvoltage condition. When supporting an OrFET circuit, this pin represents the FET source and is the inverting input of a differential amplifier looking for the presence of a reverse voltage across the FET, which might indicate a failure mode.
3	C_S+	Noninverting Differential Current Sense Input. The differential sensitivity of C_S+ and C_S- is normally around 10 mV to 40 mV at the input to the ASIC. Nulling any external divider offset is achieved by injecting a trimmable amount of current into either the inverting or noninverting input of the second stage of the current sense amplifier. A compensation circuit is used to ensure the amount of current for zero-offset tracks the common-mode voltage. Nulling of any amplifier offset is done in a similar manner except that it does not track the common-mode voltage.
4	C_{CMP}	Current Error Amplifier Compensation. This pin is the output of the current limit transconductance error amplifier. A series resistor and a capacitor to ground are required for loop compensation.
5	V_{CMP}	Voltage Error Amplifier Compensation. This is the output of a voltage error transconductance amplifier. Compensate with a series capacitor and resistor to ground. An external emitter-follower or buffer is typically used to drive an optocoupler. Output voltage positioning may be obtained by placing a second resistor directly to ground. Refer to Analog Devices applications notes on voltage positioning.
6	FD	A divider from the OrFET drain is connected here. A differential amplifier is then used to detect the presence of a reverse voltage across the FET, which indicates a fault condition and causes the OrFET gate to be pulled low.
7	GND	Ground. This pin is double bonded for extra reliability. If the ground pin goes positive with respect to the remote sense return (V_S-) for a sustained period indicating that the negative remote sense line is disconnected, PEN will be disabled.
8	ICT	Input for Current Transformer. The sensitivity of this pin is suitable for the typical 0.5 V to 1 V signal that is normally available. If this function is enabled, the C_S+ amplifier is disabled. This pin is also used for extended SMBus addressing, i.e., pulled below ground to allow additional SMBus addresses.
9	PULSE/AC_{SENSE}1/MON1	Pulse Present, AC/Bulk Sense 1, or Monitor 1 Input. PULSE: This tells the OrFET circuit that the voltage from the power transformer is normal. A peak hold allows the OrFET circuit to pass through the pulse skipping that occurs with very light loads but turns off the circuit about one second after the last pulse is recognized. AC_{SENSE}1: This sense function also uses the peak voltage on this pin to measure the bulk capacitor voltage. If too low, AC_OK and DC_OK can warn of an imminent loss of power. Threshold level and hysteresis can be trimmed. When not selected, AC_{SENSE}1 defaults to true. MON1: When MON1 is selected for this pin, its input is compared against a 1.25 V comparator that could be used for monitoring a post regulated output; includes overvoltage, undervoltage, and overtemperature conditions.

Pin No.	Mnemonic	Description
10	$AC_{SENSE}2$/MON2	AC/Bulk Sense Input 2 or Monitor 2 Input. $AC_{SENSE}2$: This alternative AC_{SENSE} input can be used when the AC_{SENSE} source must be different from that used for the OrFET. It also allows dc and opto-coupled signals that are not suitable for the OrFET control. MON2: When MON2 is selected for this pin, its input is compared against a 1.25 V comparator that could be used for monitoring a post regulated output; includes overvoltage, undervoltage, and overtemperature conditions.
11	CBD/ALERT	CBD: The crowbar drive pin allows implementation of a fast shutdown in case of a load overvoltage fault. The pin can be configured as an open-drain N-channel or P-channel and is suitable for driving a sensitive gate SCR crowbar. An external transistor is required if a high gate current is needed. Either polarity may be selected. ALERT: This pin can be configured to provide an ALERT function in microprocessor-supported applications whereby any of several ICs in a redundant system that detects a problem can interrupt and shut down the power supply. An alternative use is as a general-purpose logic output signal.
12	PEN	Power Enable. This pin can be configured as an open-drain N-channel or P-channel that typically drives the PEN optocoupler. Providing that the PSON pin has been asserted to turn the output on, and that there are no faults, this pin drives an optocoupler on enabling the primary PWM circuit. Either polarity may be selected.
13	SCL/AC_OKLink	SCL: SMBus Serial Clock Input. AC_OKLink: In non-microprocessor applications, this pin can be programmed to give the status of AC_{SENSE} to all the ICs on the same bus. The main effect is to turn on undervoltage blanking whenever the sense circuit monitoring ac or bulk dc detects a low voltage.
14	SDA/PS_{ON}LINK	SDA: SMBus Serial Data Input and Output. PS_{ON}LINK: In non-microprocessor applications, this pin can be programmed to provide the PSON status to other ICs. This allows just one IC to be the PSON interface to the host system, or the PS_{ON}LINK itself can be the PSON interface.
15	ADD0	Chip Address Pin. There are three addresses possible using this pin, which are achieved by tying ADD0 to ground, tying to V_{DD}, or being left to float. One address bit is available via programming at the device/daughter card level so the total number of addressable ICs can be increased to six.
16	PSON/MON3	PSON: In non-microprocessor configurations, this is power supply on. As a standard I/O, this pin is rugged enough for direct interface with a customer's system. Either polarity may be selected. MON3: When MON3 is selected for this pin, its input is compared against a 1.25 V comparator that could be used for monitoring a post-regulated output; includes overvoltage, undervoltage, and overtemperature conditions.
17	DC_OK/MON4	DC_OK: This pin is the output of a general-purpose digital I/O that can be configured as open-drain N-channel or open-drain P-channel suitable for wire-ORing with other ICs and direct interfacing with a customer's system. Either polarity may be selected. MON4: When MON4 is selected for this pin, its input is compared against a 1.25 V comparator that could be used for overtemperature protection and for monitoring a post-regulated output; includes overvoltage, undervoltage, and overtemperature conditions.
18	V_{REF}/AC_OK/OTP/MON5	Voltage Reference, Buffered Output, Overtemperature Protection, or Monitor 5. V_{REF}: This is a 2.5 V precision reference voltage capable of sourcing 2 mA. This function is continuously monitored, and if the voltage falls below 2.0 V, PEN is disabled. Forcing this pin's voltage does not affect the integrity of the internal reference. AC_OK: This option can be configured as N-channel or P-channel and as normal or inverted polarity. At system level, a true AC_OK is used to indicate that the primary bulk voltage is high enough to support the system, and when false, that dc output is about to fail. MON5: A further option is to configure this as an analog input, MON5, with a flexible hysteresis and trimmable 2.5 V reference that makes this pin particularly suitable for overtemperature protection (OTP) sensing. Since hysteresis uses a switched 100 µA current source, hysteresis can be adjusted via the source impedance of the external circuit. It can also be used for overvoltage and undervoltage functions.
19	F_G	FET Gate Enable. When supporting an OrFET circuit, this is the gate drive pin. Since the open-drain voltage on the chip is limited to V_{DD}, an external level shifter is required to drive the higher gate voltages suitable for the OrFET. This pin is configured as an open-drain N-channel. Either output polarity, low = on or low = off, may be selected.
20	V_S–/SHRS–	This pin is used as the ground input reference for the current share and load voltage sense circuits. It should be tied to ground at the common remote sense location. The input impedance is about 35 kΩ to ground.

Pin No.	Mnemonic	Description
21	V_S+	This pin is the positive remote load voltage sense input and is normally divided down from the power supply output voltage to 2.0 V at no load using an external voltage divider. The input impedance is high.
22	SCMP	Output of the Current Share Transconductance Error Amplifier. Compensation is a series capacitor and resistor to ground. While V_{DD} is normal and PEN is false, this pin is clamped to ground. When the converter is enabled (PEN true) and the clamp is released, the compensation capacitor charges providing a slow walk-in. The error amplifier input has a built-in bias so that all slaves in a parallel supply system do not compete with the master for control of the share bus.
23	SHRS+	Current Share Sense. This is the noninverting input of a differential sense amplifier looking at the voltage on the share bus. For testing purposes, this pin is normally connected to SHRO. Calibration always expects this pin to be at 2.0 V with respect to SHRS−/V_S−. If a higher share voltage is required, a resistor divider from SHRO or an additional gain stage, as shown in the application notes, must be used.
24	SHRO	Current Share Output. This output is capable of driving the share bus of several power supplies between 0 V and V_{DD} − 0.4 V (10 kΩ bus pull-down in each supply). Where a higher share bus voltage is required, an external amplifier is necessary. The current share output from the supply which, when bused with the share output of other power supplies working in parallel, allows each of the supplies to contribute essentially equal currents to the load.

Table 4. Default Pin States during EEPROM Download

Pin No.	Mnemonic	State
11	CBD	High impedance (Hi-Z) at power-up and until the end of the EEPROM download (approximately 20 ms). This pin is reconfigured at the end of the EEPROM download.
12	PEN	High impedance (Hi-Z) at power-up and until the end of the EEPROM download (approximately 20 ms). This pin is reconfigured at the end of the EEPROM download.
17	DC_OK	Active low (low if DC_OK true) at power-up. This pin is reconfigured during the EEPROM download.
18	AC_OK	Active low (low if DC_OK true) at power-up. This pin is reconfigured during the EEPROM download.
19	F_G	High impedance (Hi-Z) at power-up and until the end of the EEPROM download (approximately 20 ms). This pin is reconfigured at the end of the EEPROM download.

TERMINOLOGY

Table 5.

Mnemonic	Description
POR	Power-On Reset. When V_{DD} is initially applied to the ASIC, the POR function clears all latches and puts the logic into a state that allows a clean start-up.
UVL	Undervoltage Lockout. This is used on V_{DD} to prevent spurious modes of operation that might occur if V_{DD} is below a specific voltage.
CVMode	Constant Voltage Mode. This is the normal mode of operation of the power supply main output. The output voltage remains constant over the whole range of current specified.
CCMode	Constant Current Mode. This mode of operation occurs when the output is overloaded until or unless a shutdown event is triggered. The output current control level remains constant down to 0 V.
UVP	Undervoltage Protection. If the output being monitored is detected as going under voltage, the UVP function sends a fault signal. After a delay, PEN goes false, the output is disabled, and either latch-off or an auto-restart occurs, depending on the mode selected. The DC_OK output also goes false immediately to show that the output is out of tolerance.
OVP	Overvoltage Protection. If the output being monitored is detected as going over voltage, the OVP function latches and sends a fault signal, PEN goes false, and CBD goes true. The DC_OK output also goes false immediately. OVP faults are always latching and require the cycling of PSON or V_{DD} or SMBus command to reset the latch.
OCP	Overcurrent Protection. If the output being monitored is detected as going over current for a certain time, the OCP function sends out a fault signal that triggers a shutdown that can be latched or allowed to auto-restart, depending on the mode selected. Prior to shutting down, the DC_OK output goes false warning the system that output will be lost. The latch is the same one used for OVP. For auto-restart, the OCP time out period is configurable.
OTP	Overtemperature Protection. If the temperature being sensed is detected as going over the selected limit, the OTP function sends out a fault signal that triggers a shutdown that can be latched or allowed to auto-restart depending on the mode selected. Prior to shutting down, the DC_OK output goes false warning the system that output will be lost. The latch is the same one used for OVP.
UVB	Undervoltage Blanking. The UVP function is blanked (disabled) during power-up or if the AC_{SENSE} function is false (ac line voltage is low). When in constant current mode, UVB is disabled. The status of AC_{SENSE} must be known to the IC, either by virtue of the on-board AC_{SENSE} or communicated by the SMBus with the help of an external microprocessor or by using AC_OKLink. When in constant current mode, due to an overload, UVB is applied for the overcurrent ride through period.
DC_OK	The DC_OK function advises the system on the status of the power supply. When it is false, the system is assured of at least 1 ms of operation if ac power is lost for any reason. Other turn-off modes provide more warning time. This pin is an open-drain output. It can be configured as a P-channel pull-up or an N-channel pull-down. It may also be configured as positive or negative (inverted) logic.
AC_OK	The AC_OK function advises the system whether or not sufficient bulk voltage is present to allow reliable operation. The system may choose to shut down if this pin is false. The power supply normally tries to maintain normal operation as long as possible, although DC_OK goes false when only a millisecond or so of operation time is left. This pin is an open-drain output. It can be configured as a P-channel pull-up or an N-channel pull-down. It may also be configured as positive or negative (inverted) logic.
DC_OKondelay	The DC_OK output is kept false for typically 100 ms to 900 ms during power-up.
DC_OKoffdelay	When the system is to be shut down in response to PSON going low, or in response to an OCP or OTP event, a signal is first sent to the DC_OK output to go false as a warning that power is about to be lost. PEN is signaled false typically 2 ms later (configurable).
Debounce Digital Noise Filter	All of the inputs to the logic core are first debounced or digitally filtered to improve noise immunity. The debounce period for OV events is in the order of 16 µs, for UV events it is 450 µs, and for PSON it is typically 80 ms (configurable).
$AC_{SENSE}1$	A voltage from the secondary of the power transformer, which can provide an analog of the bulk supply, is rectified and lightly filtered and measured by the ac sense function. At start-up, if this voltage is adequate, this function signals the end user system that it is okay to start. If a brown-out occurs or ac power is removed, this function can provide early warning that power is about to be lost and allow the system to shut down in an orderly manner. While AC_{SENSE} is low, UVB is enabled, which means undervoltage protection is not initiated. If ac power is so low that the converter cannot continue to operate, other protection circuits on the primary side normally shut down the converter. When an adequate voltage level is resumed, a power-up cycle is initiated.

Mnemonic	Description
Pulse_OK	As well as providing ac sense, the preceding connection to the transformer is used to gate the operation of the OrFET circuit. If the output of the transformer is good and has no problems, the OrFET circuit allows gate drive to the OrFET.
AC Hysteresis	AC Sense Hysteresis. Configurable voltage on the ac sense input allows the ac sense upper and lower threshold to be adjusted to suit different amounts of low frequency ripple present on the bulk capacitor.
$AC_{SENSE}2$	An alternate form of ac sense can be accepted by the ASIC. This may in the form of an opto-coupled signal from the primary side where the actual level sensing might be done. As with the above, while ac is low and UVB is disabled, AC_OK is false and DC_OK is true. Any brownout protection that might be required on the primary is done on the primary side.
Soft-start	At start-up, the voltage reference to the voltage error amplifier is brought up slowly in approximately 127 steps to provide a controlled rate of rise of the output voltage.
V_{DD}–OVP	An OVP fault on the auxiliary supply to the ASIC causes a standard OVP operation (see the OVP function).
V_{DD}–UVL	A UVL fault on the auxiliary supply to the IC causes a standard UVP operation (see the UVP function).
AutoRestart Mode	In this mode, the housekeeping circuit attempts to restart the supply after an undervoltage event at about 1 second intervals. No other fault can initiate auto-restart.
V_{REF}–MON	The internal precision reference is monitored by a separate reference for overvoltage and allows truly redundant OVP. The externally available reference is also monitored for an undervoltage that would indicate a short on the pin.
GND–MON	The internal ASIC ground is constantly monitored against the remote sense negative pin. If the chip ground goes positive with respect to this pin, it indicates that the chip ground is open-circuit either inside the ASIC or the external wiring. The ASIC would be latched off, similar to an OV event.

THEORY OF OPERATION

POWER MANAGEMENT

This block contains V_{DD} undervoltage lockout circuitry and a power-on/reset function. It also provides precision references for internal use and a buffered reference voltage, V_{REF}. If V_{REF} is configured to an output pin, overloading, shorting to ground, or shorting to V_{DD} do not effect the internal references. See Figure 8.

During power-on, V_{REF} does not come up until V_{DD} exceeds the upper UVL threshold. Housekeeping functions in this block include reference voltage monitors, V_{DD} overvoltage, and a ground fault detector.

The ground fault detector monitors ADM1041 ground with respect to the remote sense pin V_S-. If GND becomes positive with respect to V_S- an on-chip signal, V_{DD}OK, goes false. V_{DD}OK is true only when all the following conditions are met: ground is negative with respect to V_S-, INTREF and EXTREF are operating normally, V_{DD} > UVLHI, and V_{DD} < V_{DD} OVP threshold.

GAIN TRIMMING AND CONFIGURATION

The various gain settings and configurations throughout the ADM1041 are digitally set up via the SMBus after it has been loaded onto its printed circuit board. There is no need for external trim potentiometers. An initial adjustment process should be carried out in a test system. Other adjustments such as current sense and voltage calibration should be carried out in the completed power supply.

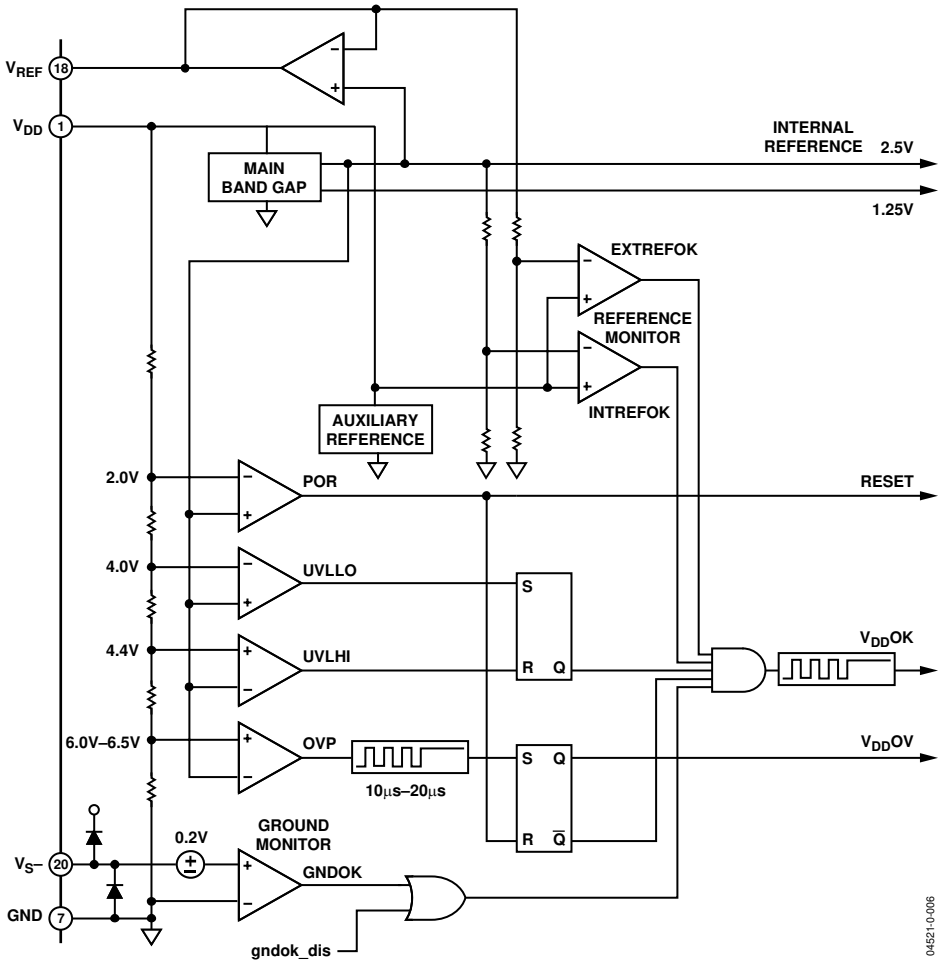

Figure 8. Block Diagram of Power Management Section

DIFFERENTIAL REMOTE SENSE AMPLIFIER

This amplifier senses the load voltage and is the main voltage feedback input. A differential input is used to compensate for the voltage drop on the negative output cable of the power supply. An external voltage divider should be designed to set the V_S+ pin to approximately 2.0 V with respect to V_S-. The amplifier gain is 1.0. See Figure 9.

SET LOAD VOLTAGE

The load voltage may be trimmed via the SMBus by a trim stage at the output of the differential remote sense amplifier. The voltage at the output of the trimmer is 1.50 V when the voltage loop is closed. See Figure 9.

LOAD OVERVOLTAGE (OV)

A comparator at the output of the load voltage trim stage detects load overvoltage. The load OV threshold can be trimmed via the SMBus. The main purpose is to turn off the OrFET when the load voltage rises to an intermediate over-voltage level that is below the local OVP level. This circuit is not latching. See Figure 9.

LOCAL VOLTAGE SENSE

This amplifier senses the output voltage of the power supply just before the OrFET. Its input is derived from one of the pins used for current sensing and is set to 2.0 V by an external voltage divider. The amplifier gain is 1.3. See Figure 9.

LOCAL OVERVOLTAGE PROTECTION (OVP)

This is the main overvoltage detection for the power supply. It is detected locally so that only the faulty power supply shuts down in the event of an OVP condition in an N+1 redundant power system. This occurs only after a load OV event. The local OVP threshold may be trimmed via the SMBus. See Figure 9.

LOCAL UNDERVOLTAGE PROTECTION (UVP)

This is the main undervoltage detection for the power supply. It is also detected locally so that a faulty power supply can be detected in an N+1 redundant power system. The local UVP threshold may be trimmed via the SMBus. See Figure 9.

FALSE UV CLAMP

If a faulty power supply causes an OVP condition on the system bus, the control loops in the good power supplies is driven to zero output. Therefore, a means is required to prevent the good power supplies from indicating an undervoltage, and they must recover quickly after the faulty power supply has shut down. The false UV clamp achieves this by clamping the output voltage just above the local UVP threshold. It may be trimmed via the SMBus. The OCPF signal disables the clamp during overcurrent faults. See Figure 9.

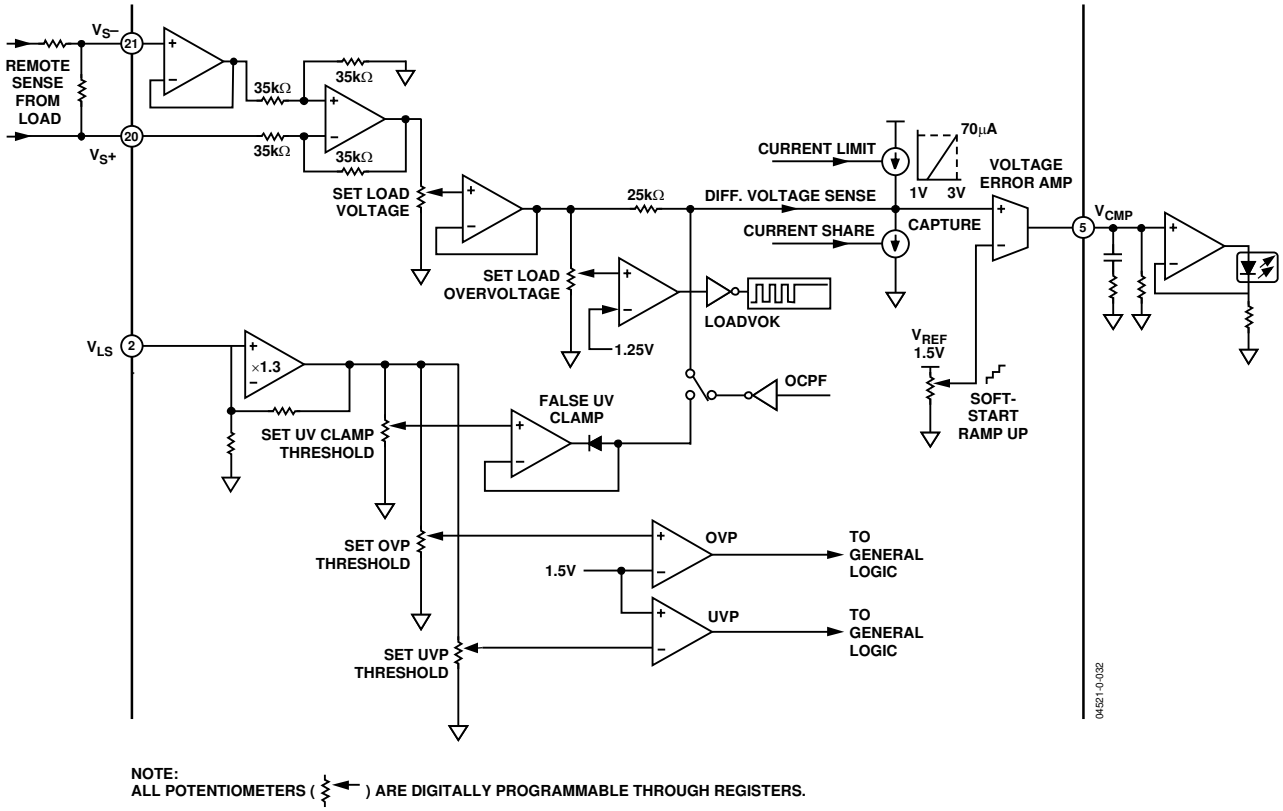

Figure 9. Block Diagram of Voltage Sense Amplifier

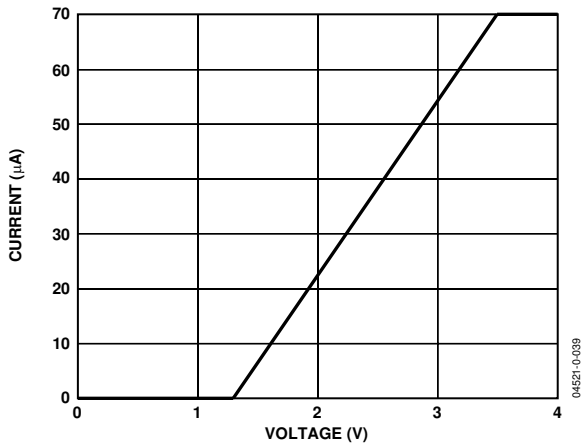

Figure 10. Current Limit

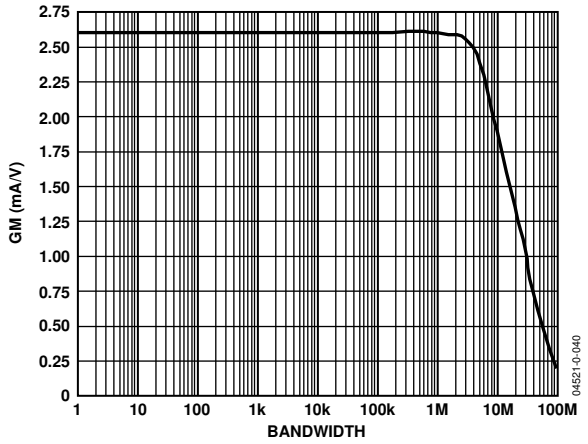

Figure 11. V_{CMP} Transconductance

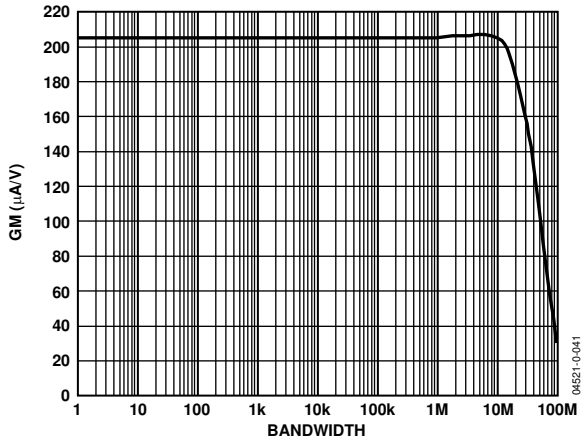

Figure 12. C_{CMP} and S_{CMP} Transconductance

VOLTAGE ERROR AMPLIFIER

This is a high gain transconductance amplifier that takes its input from the load voltage trim stage described previously. The amplifier requires only the output pin for loop compensation, which typically consists of a series RC network-to-common. A parallel resistor may be added to common to reduce the open-loop gain and thereby provide some output voltage droop as output current increases. The output of the amplifier is typically connected to an emitter follower that drives an optocoupler, which in turn controls the duty of the primary side PWM. The emitter follower should have a high gain to minimize loading effects on the amplifier. Alternatively, an op amp voltage follower may be used. See Figure 9, Figure 10, and Figure 11.

MAIN VOLTAGE REFERENCE

A 1.5 V reference is connected to the inverting input of the voltage error amplifier. This 1.5 V reference is the output voltage of the soft-start circuit. Under closed-loop conditions, the voltage at the noninverting input is also controlled to 1.5 V. During start-up, the output voltage should be ramped up in a linear fashion at a rate that is independent of the load current. This is achieved by digitally ramping up the reference voltage by using a counter and a DAC. The ramp rate is configurable via the SMBus. See Figure 14.

CURRENT SENSE AMPLIFIER

This is a two-stage differential amplifier that achieves low offset and accuracy. The amplifier has the option to be chopped to reduce offset or left as a linear amplifier without chopping. Refer to the Register Listing for more details. Its gain may be selected from three ranges. It is followed by a trim stage and then by a low gain buffer stage that can be configured with a gain of 1.0 or 2.1. The result is a total of six overlapping gain ranges (65 to 230), one of which must be selected via the SMBus. This gives ample adjustment to compensate for the poor initial tolerance of the resistance wires typically used for current sensing. It also allows selecting a higher sensitivity for better efficiency or a lower sensitivity for better accuracy (lower offset). The amplifier offset voltage is trimmed to zero in a once-off operation via the SMBus and uses a voltage controlled current source at the output of the first gain stage. A second controlled current source is used to trim out the additional offset due to the mismatch of the external divider resistors. This offset trim is dynamically adjusted according to the common-mode voltage present at the top of the voltage dividers. Six ranges are selectable according to the magnitude and polarity of this offset component. Because the offset compensation circuit itself has some inaccuracies, the best overall current sense accuracy is obtained by using more closely matched external dividers and then selecting a low compensation range. See Figure 14.

CURRENT SENSING

Current is typically sensed by a low value resistor in series with the positive output of the power supply, just before the OrFET or diode. For high voltages (12 V and higher), this resistor is usually placed in the negative load. A pair of closely matched voltage dividers connected to Pins 2 and 3 divide the common-mode voltage down to approximately 2.0 V. The divider ratio must be the same as used in the local and remote voltage sense circuits. Alternatively, current may be sensed by a current transformer (CT) connected to Pin 8. The ADM1041 must be configured via the SMBus to select one or the other. See Figure 13.

CURRENT TRANSFORMER INPUT

The ADM1041 can also be configured to sense current by using a current transformer (CT) connected to Pin 8. In this case, the resistive current sense is disabled. A separate single-ended amplifier has two possible sensitivities that are selected via the SMBus. If the CT option is selected, the gain of the 1.0, 2.1 buffer that follows the gain trim stage is no longer configurable and is fixed at 1.0.

The share driver amplifier has a total of 100 mV positive offset built into it. In order to use the ADM1041 in CT mode, it is necessary to compensate for this additional 100 mV offset. This is achieved by adding in a positive offset on the CT input. This also allows any negative amplifier offsets in the CT chain to be nulled out.

This offset cancellation is achieved by sourcing a current through a resistance on the ICT pin. The resistor value is 40 kΩ and so for 100 mV of offset cancellation a current of 2.5 μA is required. It is possible to fine trim this current via Register 15h, Bits 4–0, step size 170 nA. For example, 2.5 μA ≈ 15 × 170 nA; so the code for Register 15h is decimal 15 or 0Fh. Refer to the Current Transformer parameter in the Specifications table for more details. See Figure 13.

CURRENT SENSE CALIBRATION

Regardless of which means is used to sense the current, the end result of the calibration process should produce the standard current share signal between Pins 20 and 23, that is, 2.0 V at 100% load, excluding any additional share signal offset that might be configured.

CURRENT LIMIT ERROR AMPLIFIER

This is a low gain transconductance amplifier that takes its input from one of the calibrated current stages described previously. The amplifier requires only the output pin for loop compensation, which typically consists of a series RC network to common. A trimmable reference provides a wide range of adjustment for the current limit. When the current signal reaches the reference voltage, the output of the error amplifier comes out of saturation and begins to drive a controlled current source. The control threshold is nominally 1.0 V. This current flows through a resistor in series with the trimmed voltage loop signal and thereby attempts to increase the voltage signal above the 1.5 V reference for that loop. The closed voltage loop reacts by reducing the power supply's output voltage and this results in constant current operation. See Figure 13.

OVERCURRENT PROTECTION

When the current limit threshold is reached, the OCP comparator detects when the current error amplifier comes out of saturation. Its threshold is nominally 0.5 V. This starts a timer that, when it times out, causes an OCP condition to occur and the power supply to shut down. If the current limit disappears before the time has expired, the timer is reset. The time period is configurable via the SMBus. Undervoltage blanking is applied during the timer operation. See Figure 14.

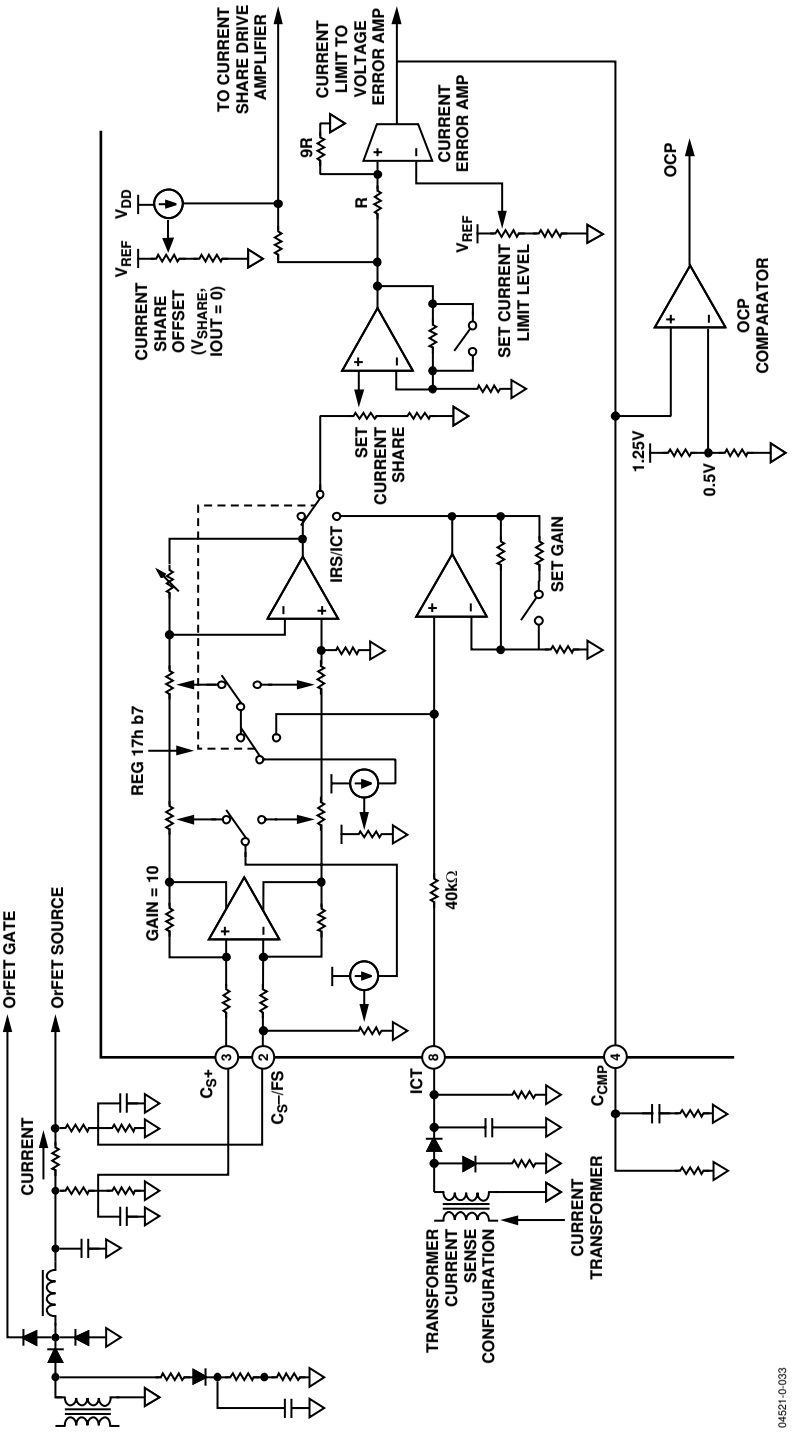

Figure 13. Current Sense

CURRENT SHARE

The current share method is the master–slave type, which means that the power supply with the highest output current automatically becomes the master and controls the share bus signal. All other power supplies become slaves, and the share bus signal causes them to increase their output voltages slightly until their output currents are almost equal to that of the master. This scheme has two major advantages. A failed master power supply simply allows one of the slaves to become the new master. A short circuited share signal disables current sharing, but all power supplies default to their normal voltage setting, allowing a certain degree of passive sharing. Because this chip uses a low voltage process, an external bidirectional amplifier is needed for most existing share bus signal levels. The voltage between Pins 20 and 23 is always controlled to 2.0 V full scale, ignoring any offset. By connecting Pins 20 and 23 together, the chip can produce a 2.0 V share signal directly without any external circuits. To improve accuracy, the share signal is referenced to remote voltage sense negative.

CURRENT SHARE OFFSET

To satisfy some customer specifications, the current share signal can be offset by a fixed amount by using a trimmable current generator and a series resistor. The offset is added on top of the 2.0 V full-scale current share output signal. See Figure 14.

I_{SHARE} DRIVE AMPLIFIER

This amplifier is a buffer with enough current source capability to drive the current share circuits of several slave power supplies. It has negligible current sink capability. Refer to the Differential Sense Amplifier section that follows.

DIFFERENTIAL SENSE AMPLIFIER

This amplifier has unity gain and senses the difference between the share bus voltage and the remote voltage sense negative pin. When the power supply is the master, it forms a closed loop with the I_{SHARE} drive amplifier described above, and therefore it causes the share bus voltage between Pins 20 and 23 to equal the current share signal at the noninverting input of the I_{SHARE} drive amplifier. When the power supply is a slave, the output of the differential sense amplifier exceeds the internal current share signal, which causes the I_{SHARE} drive amplifier to be driven into cutoff. Because it is not possible to trim out negative offsets in the op amps in the current share chain, a 50 mV voltage source is used to provide a known fixed positive offset. The share bus offset controlled current source must be trimmed via the SMBus to take out the resulting overall offset. See Figure 14.

I_{SHARE} ERROR AMPLIFIER

This is a low gain transconductance amplifier that measures the difference between the internal current share voltage and the signal voltage on the external share bus. If two power supplies have almost identical current share signals, a 50 mV voltage source on the inverting input helps arbitrate which power supply becomes the master and prevents "hunting" between master and slave roles. The amplifier requires only the output pin for loop compensation, which typically consists of a series RC network to common. When the power supply is a slave, the output of the error amplifier comes out of saturation and begins to drive a controlled current sink. The control threshold is nominally 1.0 V. This current flows from a resistor in series with the trimmed voltage loop signal and thereby attempts to decrease the voltage signal below the 1.5 V reference for that loop. The closed voltage loop reacts by increasing the power supply's output voltage until current share is achieved. The maximum current sink is limited so that the power supply voltage can be increased only a small amount, which is usually limited to be within the customer's specified voltage regulation limit. This small voltage increase also limits the control range of the current share circuit and is called the capture range. The capture range may be set via the SMBus to one of four values, from 1% to 4% nominal. See Figure 14.

I_{SHARE} CLAMP

This clamp keeps the current share-loop compensation capacitor discharged when the current share is not required to operate. The clamp is released during power-up when the voltage reference and therefore the output voltage of the power supply has risen to either 75% or 88% of its final value. This is configurable via the SMBus. When the clamp is released, the current share loop slowly "walks in" the current share and helps to avoid output voltage spikes during hot swapping. See Figure 14.

Share_OK DETECTOR

Incorrect current sharing is a useful early indicator that there is some sort of non-catastrophic problem with one of the power supplies in a parallel system. Two comparators are used to detect an excessive positive or negative error voltage at the input of the I_{SHARE} error amplifier, which indicates that the current share loop has lost control. One of four possible error levels must be configured via the SMBus. See Figure 14.

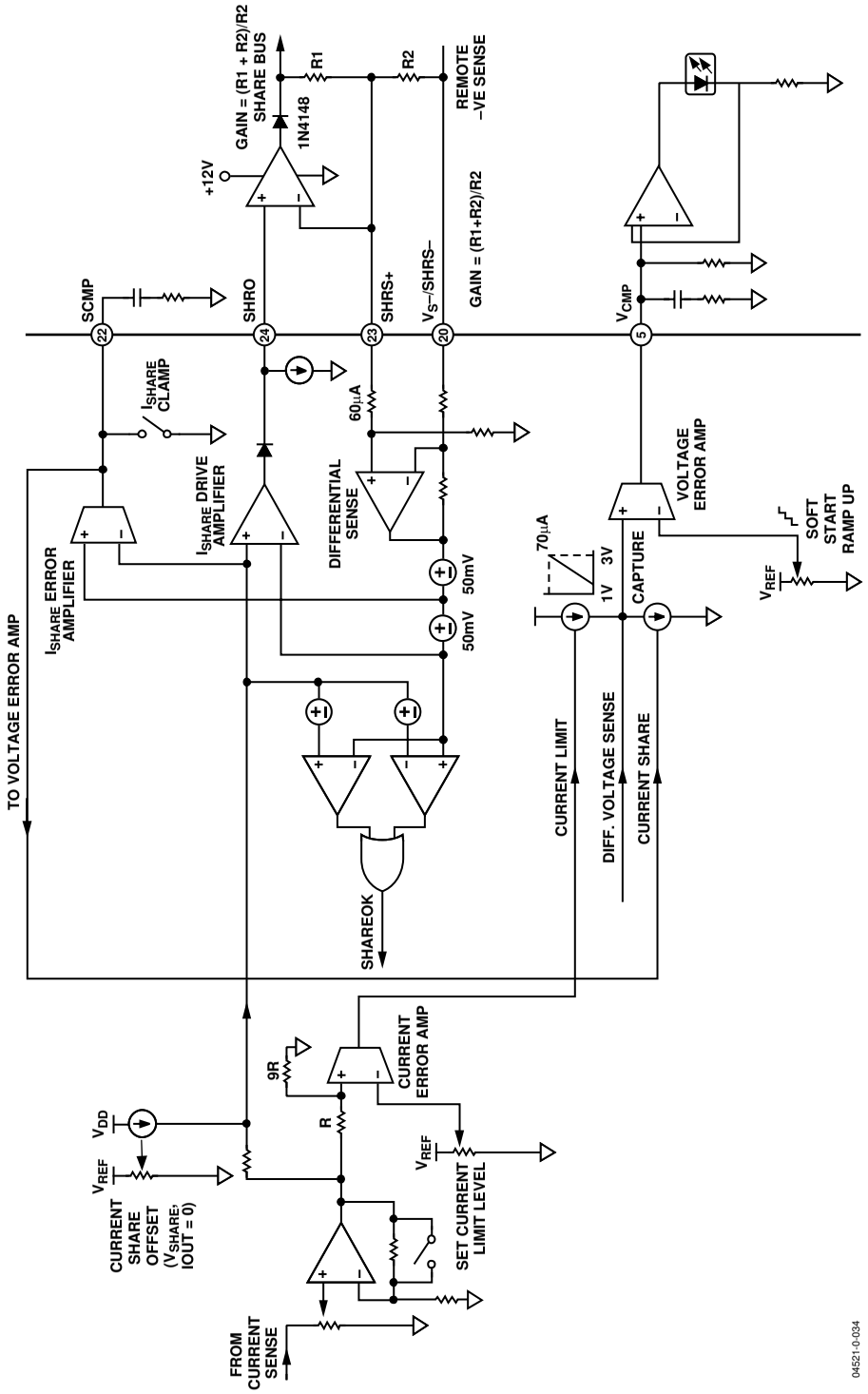

Figure 14. Current Share Circuit and Soft-start