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Multisupply Supervisor/Sequencer with ADC and Temperature Monitoring

Data Sheet

ADM1063

FEATURES

- Complete supervisory and sequencing solution for up to 10 supplies
- 10 supply fault detectors enable supervision of supplies to
  - <0.5% accuracy at all voltages at 25°C
  - <1.0% accuracy across all voltages and temperatures
- 5 selectable input attenuators allow supervision of supplies to
  - 14.4 V on VH
  - 6 V on VP1 to VP4 (VPx)
- 5 dual-function inputs, VX1 to VX5 (VXx)
  - High impedance input to supply fault detector with thresholds between 0.573 V and 1.375 V
  - General-purpose logic input
- 10 programmable driver outputs, PDO1 to PDO10 (PDOx)
  - Open-collector with external pull-up
  - Push/pull output, driven to VDDCAP or VPx
  - Open collector with weak pull-up to VDDCAP or VPx
  - Internally charge-pumped high drive for use with external N-FET (PDO1 to PDO6 only)
- Sequencing engine (SE) implements state machine control of PDOx outputs
  - State changes conditional on input events
  - Enables complex control of boards
  - Power-up and power-down sequence control
  - Fault event handling
  - Interrupt generation on warnings
  - Watchdog function can be integrated in SE
  - Program software control of sequencing through SMBus
- Complete voltage margining solution for 6 voltage rails
- 12-bit ADC for readback of all supervised voltages
- 1 internal and 2 external temperature sensors
- Reference input (REFIN) has 2 input options
  - Driven directly from 2.048 V (±0.25%) REFOUT pin
  - More accurate external reference for improved ADC performance
- Device powered by the highest of VPx, VH for improved redundancy
- User EEPROM: 256 bytes
- Industry-standard, 2-wire bus interface (SMBus)
- Guaranteed PDO low with VH, VPx = 1.2 V
- Available in 40-lead, 6 mm × 6 mm LFCSP and 48-lead, 7 mm × 7 mm TQFP packages

FUNCTIONAL BLOCK DIAGRAM

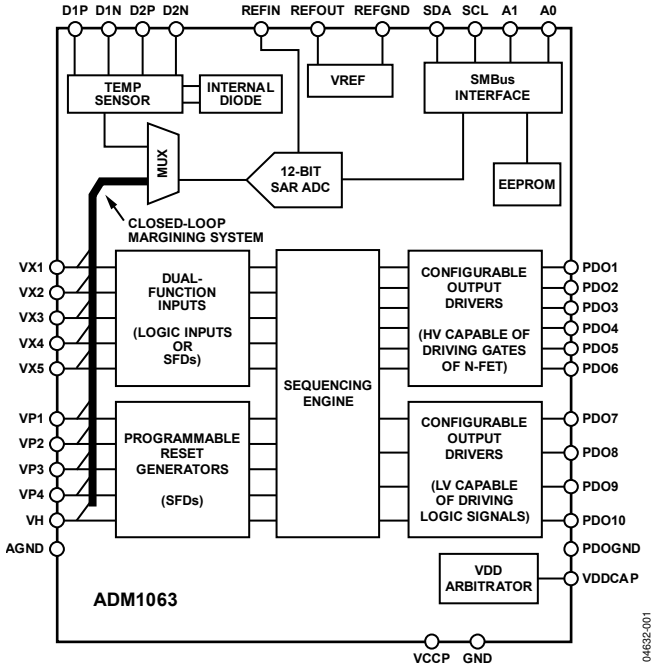

Figure 1.

APPLICATIONS

- Central office systems
- Servers/routers
- Multivoltage system line cards
- DSP/FPGA supply sequencing
- In-circuit testing of margined supplies

GENERAL DESCRIPTION

The ADM1063 is a configurable supervisory/sequencing device that offers a single-chip solution for supply monitoring and sequencing in multiple supply systems. In addition to these functions, the ADM1063 integrates a 12-bit ADC that can be used to accurately read back up to 12 separate voltages.

The device also provides up to 10 programmable inputs for monitoring undervoltage faults, overvoltage faults, or out-of-window faults on up to 10 supplies. In addition, 10 programmable outputs can be used as logic enables. Six of these programmable outputs can provide up to a 12 V output for driving the gate of an N-FET that can be placed in the path of a supply.

For more information about the ADM1063 register map, refer to the AN-698 Application Note.

Rev. D

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

ADM1063* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADM1063 Evaluation Board

DOCUMENTATION

Application Notes

- AN-0973: Erasing and Programming the Sequencing Engine EEPROM
- AN-0975: Automatic Generation of State Diagrams for the ADM1062 to ADM1069 Using Graphviz
- AN-0997: Ping-Pong Configuration Guide for ADM1062 to ADM1069 Devices
- AN-1001: Checksum Calculations
- AN-1009: Block Erasing, Reading and Writing to the ADM106x EEPROM
- AN-1086: Using an ADM106x in a Hot Swap Application
- AN-698: Configuration Registers of ADM1062/ADM1063/ ADM1064/ADM1065/ADM1066/ADM1067/ADM1166
- AN-722: Watchdog Detection Using the ADM106x
- AN-723: Interrupt Generation Using the ADM106x
- AN-780: Monitoring Negative Voltages with the ADM1062 to ADM1069 Super Sequencers
- AN-781: Monitoring Additional Supplies with the ADM1062-ADM1069 Super Sequencers™
- AN-782: Monitoring High Voltages with the ADM1062-ADM1069 Super Sequencers™
- AN-897: ADC Readback Code

Data Sheet

- ADM1063-EP: Enhanced Product Data Sheet
- ADM1063: Multisupply Supervisor/Sequencer with ADC and Temperature Monitoring Data Sheet

User Guides

- SuperSequencer Documentation
- UG-404: USB-SDP-CABLEZ Serial Interface Board

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADMxxxx Common Run-Time
- SuperSequencer Software

REFERENCE MATERIALS

Informational

- Optical and High Speed Networking ICs

Product Selection Guide

- Supervisory Devices Complementary Parts Guide for Altera FPGAs
- Supervisory Devices Complementary Parts Guide for Xilinx FPGAs

Solutions Bulletins & Brochures

- Power Supply Sequencing Bulletin (2007)

Technical Articles

- Temperature monitor measures three thermal zones

DESIGN RESOURCES

- ADM1063 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADM1063 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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TABLE OF CONTENTS

REVISION HISTORY

1/15—Rev. C to Rev. D

Changed Round-Robin Circuit to ADC Round-Robin ..... Throughout
Moved Revision History 3
Moved Absolute Maximum Ratings Section 8
Changes to Figure 4 and Table 4 9
Added Slew Rate Consideration Section 14
Added VP1 Glitch Filtering Section 16
Added SCL Held Low Timeout Section and False Start Detection Section 28
Updated Outline Dimensions 33
Changes to Ordering Guide 33

7/11—Rev. B to Rev. C

Changes to Serial Bus Timing Parameter in Table 1 4
Added Endnote 4 in Table 1 4
Changes to Figure 3 7
Added Exposed Pad Notation to Outline Dimensions 30
Changes to Ordering Guide 31

5/08—Rev. A to Rev. B

Changes to Table 1 4
Changes to Powering the ADM1063 Section 13
Changes to Table 5 14
Changes to Default Output Configuration Section 16
Changes to Sequence Detector Section 19
Changes to Temperature Measurement System Section 21
Changes to Table 10 22
Changes to Configuration Download at Power-Up Section 24
Changes to Table 11 25
Changes to Figure 44 and Error Correction Section 29
Changes to Ordering Guide 31

12/06—Rev. 0 to Rev. A

Updated Format ..... Universal
Changes to Features 1
Changes to Figure 2 3
Changes to Table 1 4
Changes to Table 2 7
Changes to Absolute Maximum Ratings Section 9
Deleted Figure 17 to Figure 19 12
Changes to Programming the Supply Fault Detectors Section 14
Changes to Table 6 14
Changes to Outputs Section 16
Changes to Fault Reporting Section 20
Deleted Supply Margining Section 21
Changes to Table 9 21
Changes to Identifying the ADM1063 on the SMBus Section 28
Changes to Figure 34 and Figure 35 30

4/05—Revision 0: Initial Version

Temperature measurement is possible with the ADM1063. The device contains one internal temperature sensor and two pairs of differential inputs for remote thermal diodes. These are measured by the 12-bit ADC.

The logical core of the device is a sequencing engine. This state-machine-based construction provides up to 63 different states. This design enables very flexible sequencing of the outputs based on the condition of the inputs.

The device is controlled via configuration data that can be programmed into an EEPROM. The entire configuration can be programmed using an intuitive GUI-based software package provided by Analog Devices, Inc.

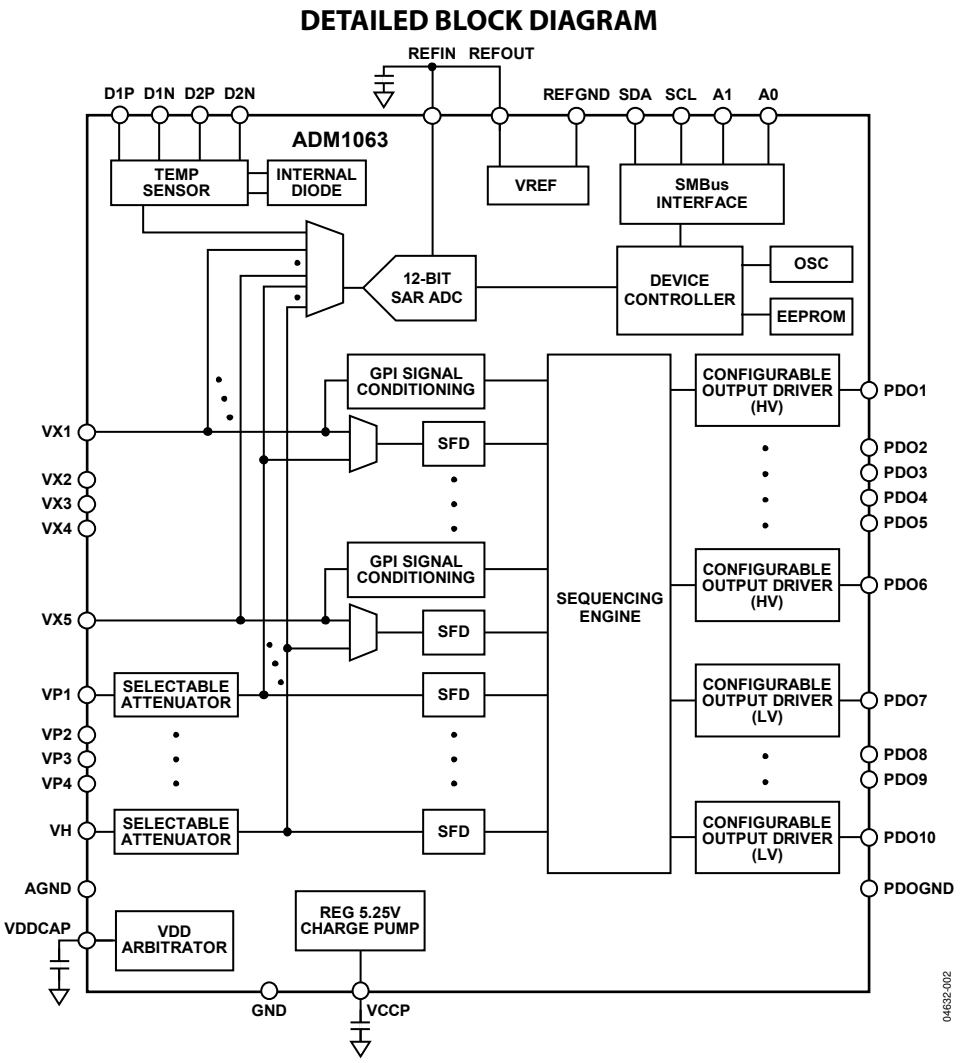

Figure 2.

SPECIFICATIONS

VH = 3.0 V to 14.4 V[1], VPx = 3.0 V to 6.0 V[1], T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY ARBITRATION					
VH, VPx	3.0			V	Minimum supply required on one of VH, VPx
VPx			6.0	V	Maximum VDDCAP = 5.1 V, typical
VH			14.4	V	VDDCAP = 4.75 V
VDDCAP	2.7	4.75	5.4	V	Regulated LDO output
C_{VDDCAP}	10			µF	Minimum recommended decoupling capacitance
POWER SUPPLY					
Supply Current, I_{VH}, I_{VPx}		4.2	6	mA	VDDCAP = 4.75 V, PDO1 to PDO10 off, ADC off
Additional Currents					
All PDO FET Drivers On		1		mA	VDDCAP = 4.75 V, PDO1 to PDO6 loaded with 1 µA each, PDO7 to PDO10 off
Current Available from VDDCAP			2	mA	Maximum additional load that can be drawn from all PDO pull-ups to VDDCAP
ADC Supply Current		1		mA	Running round-robin loop
EEPROM Erase Current		10		mA	1 ms duration only, VDDCAP = 3 V
SUPPLY FAULT DETECTORS					
VH Pin					
Input Impedance		52		kΩ	
Input Attenuator Error		±0.05		%	Midrange and high range
Detection Ranges					
High Range	6		14.4	V	
Midrange	2.5		6	V	
VPx Pins					
Input Impedance		52		kΩ	
Input Attenuator Error		±0.05		%	Low range and midrange
Detection Ranges					
Midrange	2.5		6	V	
Low Range	1.25		3	V	
Ultralow Range	0.573		1.375	V	No input attenuation error
VXx Pins					
Input Impedance	1			MΩ	
Detection Range					
Ultralow Range	0.573		1.375	V	No input attenuation error
Absolute Accuracy			±1	%	VREF error + DAC nonlinearity + comparator offset error + input attenuation error
Threshold Resolution		8		Bits	
Digital Glitch Filter		0		µs	Minimum programmable filter length
		100		µs	Maximum programmable filter length
ANALOG-TO-DIGITAL CONVERTER					
Signal Range	0		V_{REFIN}	V	The ADC can convert signals presented to the VH, VPx, and VXx pins; VPx and VH input signals are attenuated depending on the selected range; a signal at the pin corresponding to the selected range is from 0.573 V to 1.375 V at the ADC input
Input Reference Voltage on REFIN Pin, V_{REFIN}		2.048		V	
Resolution		12		Bits	
INL			±2.5	LSB	Endpoint corrected, V_{REFIN} = 2.048 V
Gain Error			±0.05	%	V_{REFIN} = 2.048 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Conversion Time		0.44		ms	One conversion on one channel
		84		ms	All 12 channels selected, 16× averaging enabled
Offset Error			±2	LSB	V_{REFIN} = 2.048 V
Input Noise		0.25		LSB rms	Direct input (no attenuator)
TEMPERATURE SENSOR[2]					
Local Sensor Accuracy		±3		°C	VDDCAP = 4.75 V
Local Sensor Supply Voltage Coefficient		−1.7		°C/V	
Remote Sensor Accuracy		±3		°C	VDDCAP = 4.75 V
Remote Sensor Supply Voltage Coefficient		−3		°C	
Remote Sensor Current Source		200		µA	High level
		12		µA	Low level
Temperature for Code 0x800		0		°C	VDDCAP = 4.75 V
Temperature for Code 0xC00		128		°C	VDDCAP = 4.75 V
Temperature Resolution per Code		0.125		°C	
REFERENCE OUTPUT					
Reference Output Voltage	2.043	2.048	2.053	V	No load
Load Regulation		−0.25		mV	Sourcing current, $I_{DACxMAX}$ = −100 µA
		0.25		mV	Sinking current, $I_{DACxMAX}$ = 100 µA
Minimum Load Capacitance	1			µF	Capacitor required for decoupling, stability
PSRR		60		dB	DC
PROGRAMMABLE DRIVER OUTPUTS					
High Voltage (Charge Pump) Mode (PDO1 to PDO6)					
Output Impedance		500		kΩ	
V_{OH}	11	12.5	14	V	I_{OH} = 0 µA
	10.5	12	13.5	V	I_{OH} = 1 µA
I_{OUTAVG}		20		µA	2 V < V_{OH} < 7 V
Standard (Digital Output) Mode (PDO1 to PDO10)					
V_{OH}	2.4			V	V_{PU} (pull-up to VDDCAP or VPx) = 2.7 V, I_{OH} = 0.5 mA
			4.5	V	V_{PU} to VPx = 6.0 V, I_{OH} = 0 mA
	V_{PU} − 0.3			V	V_{PU} ≤ 2.7 V, I_{OH} = 0.5 mA
V_{OL}	0		0.50	V	I_{OL} = 20 mA
I_{OL}[3]			20	mA	Maximum sink current per PDOx pin
I_{SINK}[3]			60	mA	Maximum total sink for all PDOx pins
$R_{PULL-UP}$	19	20	29	kΩ	Internal pull-up
I_{SOURCE} (VPx)[3]			2	mA	Current load on any VPx pull-ups, that is, total source current available through any number of PDOx pull-up switches configured onto any one VPx pin
Three-State Output Leakage Current			10	µA	V_{PDO} = 14.4 V
Oscillator Frequency	90	100	110	kHz	All on-chip time delays derived from this clock
DIGITAL INPUTS (VXx, A0, A1)					
Input High Voltage, V_{IH}	2.0			V	Maximum V_{IN} = 5.5 V
Input Low Voltage, V_{IL}			0.8	V	Maximum V_{IN} = 5.5 V
Input High Current, I_{IH}	−1			µA	V_{IN} = 5.5 V
Input Low Current, I_{IL}			1	µA	V_{IN} = 0 V
Input Capacitance		5		pF	
Programmable Pull-Down Current, $I_{PULL-DOWN}$		20		µA	VDDCAP = 4.75 V, T_A = 25°C if known logic state is required
SERIAL BUS DIGITAL INPUTS (SDA, SCL)					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}			0.8	V	
Output Low Voltage, V_{OL}[3]			0.4	V	I_{OUT} = −3.0 mA

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL BUS TIMING[4]					
Clock Frequency, f_{SCLK}			400	kHz	
Bus Free Time, t_{BUF}	1.3			µs	
Start Setup Time, $t_{SU;STA}$	0.6			µs	
Stop Setup Time, $t_{SU;STO}$	0.6			µs	
Start Hold Time, $t_{HD;STA}$	0.6			µs	
SCL Low Time, t_{LOW}	1.3			µs	
SCL High Time, t_{HIGH}	0.6			µs	
SCL, SDA Rise Time, t_R			300	ns	
SCL, SDA Fall Time, t_F			300	ns	
Data Setup Time, $t_{SU;DAT}$	100			ns	
Data Hold Time, $t_{HD;DAT}$	5			ns	
Input Low Current, I_{IL}			1	µA	V_{IN} = 0 V
SEQUENCING ENGINE TIMING					
State Change Time		10		µs	

[1] At least one of the VH, VPx pins must be ≥3.0 V to maintain the device supply on VDDCAP.
[2] All temperature sensor measurements are taken with round-robin loop enabled and at least one other voltage input being measured.
[3] Specification is not production tested but is supported by characterization data at initial product release.
[4] Timing specifications are guaranteed by design and supported by characterization data.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltage on VH Pin	16 V
Voltage on VPx Pins	7 V
Voltage on VXx Pins	−0.3 V to +6.5 V
Voltage on A0, A1 Pins	−0.3 V to +7 V
Voltage on REFIN, REFOUT Pins	5 V
Voltage on VDDCAP, VCCP Pins	6.5 V
Voltage on PDOx Pins	16 V
Voltage on SDA, SCL Pins	7 V
Voltage on GND, AGND, PDOGND, REFGND Pins	−0.3 V to +0.3 V
Voltage on DxN, DxP Pins	−0.3 V to +5 V
Input Current at Any Pin	±5 mA
Package Input Current	±20 mA
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature, Soldering Vapor Phase, 60 sec	215°C
ESD Rating, All Pins	2000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
40-Lead LFCSP	25	°C/W
48-Lead TQFP	50	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

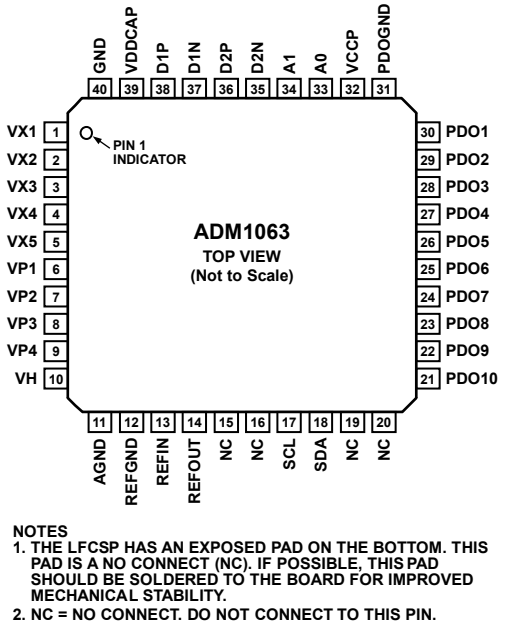

Figure 3. 40- Lead LFCSP Pin Configuration

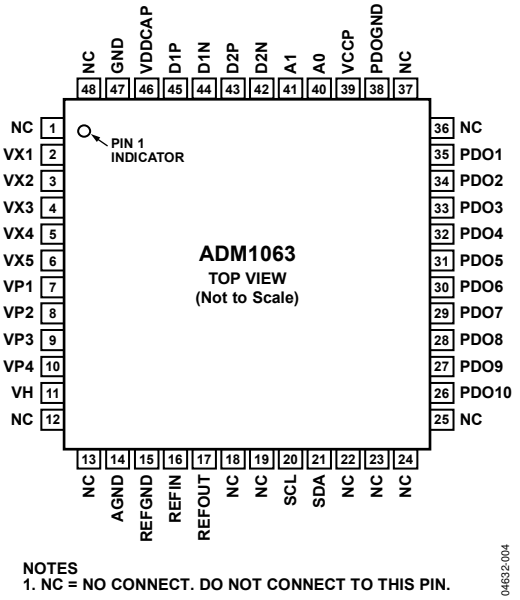

Figure 4. 48-Lead TQFP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.			
40-Lead LFCSP	**48-Lead TQFP**	**Mnemonic**	**Description**
15, 16, 19, 20	1, 12, 13, 18, 19, 22 to 25, 36, 37, 48	NC	No Connect. Do not connect to this pin.
1 to 5	2 to 6	VX1 to VX5 (VXx)	High Impedance Inputs to Supply Fault Detectors. Fault thresholds can be set from 0.573 V to 1.375 V. Alternatively, these pins can be used as general-purpose digital inputs.
6 to 9	7 to 10	VP1 to VP4 (VPx)	Low Voltage Inputs to Supply Fault Detectors. Three input ranges can be set by altering the input attenuation on a potential divider connected to these pins, the output of which connects to a supply fault detector. These pins allow thresholds from 2.5 V to 6.0 V, from 1.25 V to 3.00 V, and from 0.573 V to 1.375 V.
10	11	VH	High Voltage Input to Supply Fault Detectors. Two input ranges can be set by altering the input attenuation on a potential divider connected to this pin, the output of which connects to a supply fault detector. This pin allows thresholds from 6.0 V to 14.4 V and from 2.5 V to 6.0 V.
11	14	AGND[1]	Ground Return for Input Attenuators.
12	15	REFGND[1]	Ground Return for On-Chip Reference Circuits.
13	16	REFIN	Reference Input for ADC. Nominally, 2.048 V. This pin must be driven by a reference voltage. The on-board reference can be used by connecting the REFOUT pin to the REFIN pin.
14	17	REFOUT	Reference Output, 2.048 V. Typically connected to REFIN. Note that the capacitor must be connected between this pin and REFGND. A 10 µF capacitor is recommended for this purpose.
17	20	SCL	SMBus Clock Pin. Bidirectional open drain requires external resistive pull-up.
18	21	SDA	SMBus Data Pin. Bidirectional open drain requires external resistive pull-up.
21 to 30	26 to 35	PDO10 to PDO1	Programmable Output Drivers.
31	38	PDOGND[1]	Ground Return for Output Drivers.
32	39	VCCP	Central Charge Pump Voltage of 5.25 V. A reservoir capacitor must be connected between this pin and GND. A 10 µF capacitor is recommended for this purpose.
33	40	A0	Logic Input. This pin sets the seventh bit of the SMBus interface address.
34	41	A1	Logic Input. This pin sets the sixth bit of the SMBus interface address.
35	42	D2N	External Temperature Sensor 2 Cathode Connection.
36	43	D2P	External Temperature Sensor 2 Anode Connection.

Pin No.			
40-Lead LFCSP	48-Lead TQFP	Mnemonic	Description
37	44	D1N	External Temperature Sensor 1 Cathode Connection.
38	45	D1P	External Temperature Sensor 1 Anode Connection.
39	46	VDDCAP	Device Supply Voltage. Linearly regulated from the highest of the VPx, VH pins to a typical of 4.75 V. Note that the capacitor must be connected between this pin and GND. A 10 µF capacitor is recommended for this purpose.
40	47	GND[1]	Supply Ground.
	N/A[2]	EPAD	Exposed Pad. The LFCSP has an exposed pad on the bottom. This pad is a no connect (NC). If possible, this pad should be soldered to the board for improved mechanical stability.

[1] In a typical application, all ground pins are connected together.
[2] N/A is not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

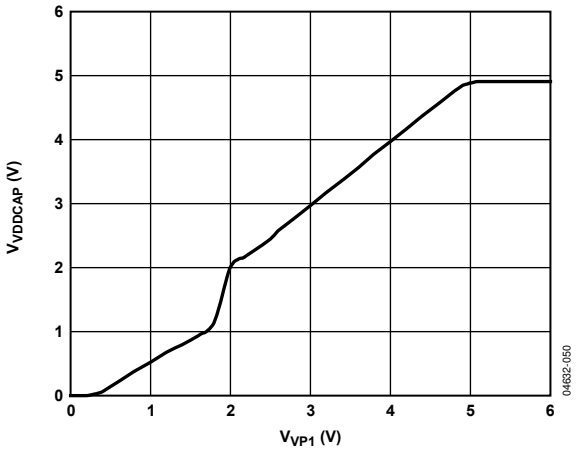

Figure 5. V_{VDDCAP} vs. V_{VP1}

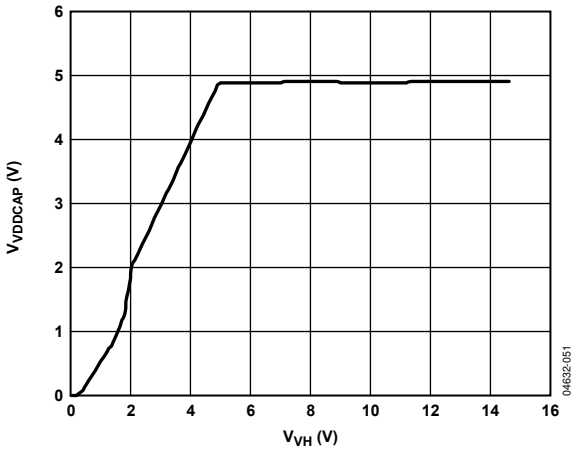

Figure 6. V_{VDDCAP} vs. V_{VH}

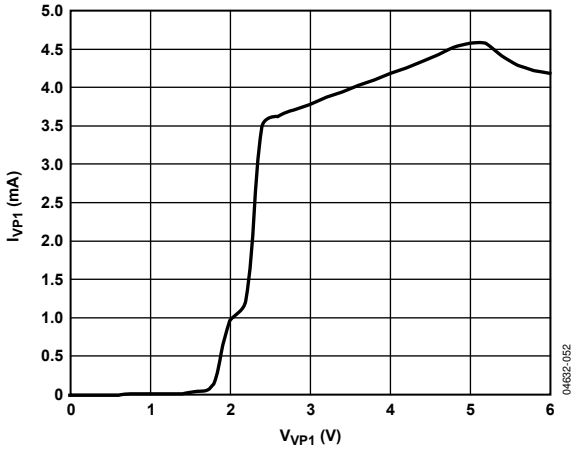

Figure 7. I_{VP1} vs. V_{VP1} (VP1 as Supply)

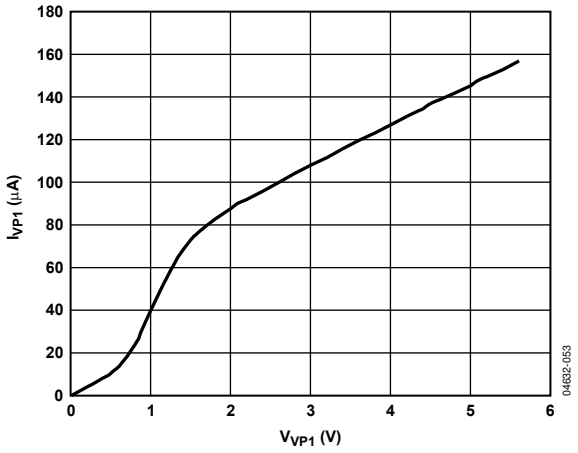

Figure 8. I_{VP1} vs. V_{VP1} (VP1 Not as Supply)

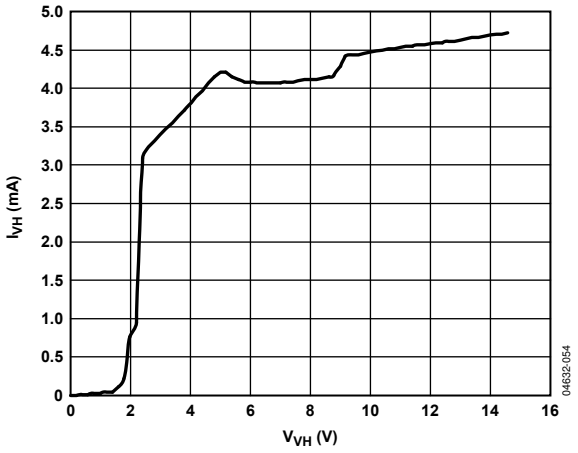

Figure 9. I_{VH} vs. V_{VH} (VH as Supply)

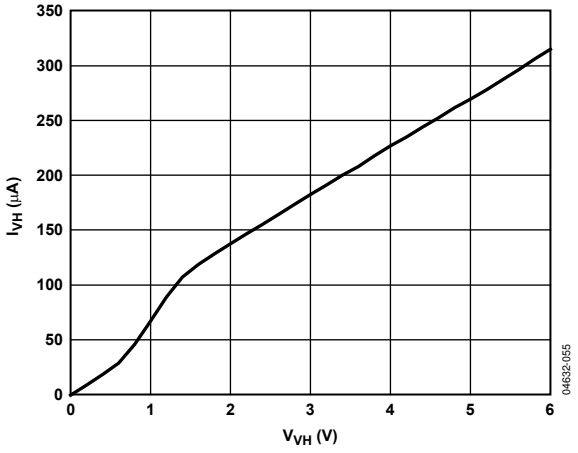

Figure 10. I_{VH} vs. V_{VH} (VH Not as Supply)

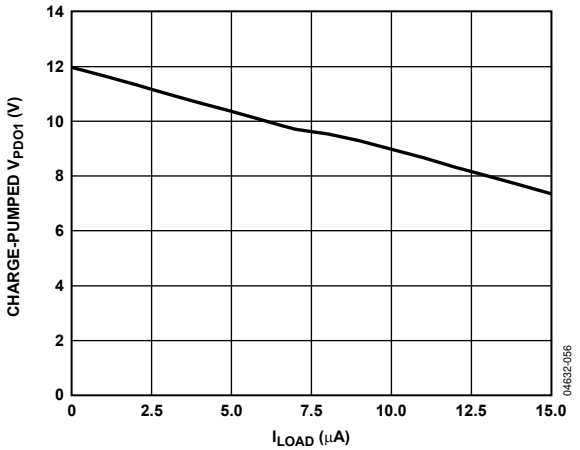

Figure 11. Charge-Pumped V_{PDO1} (FET Drive Mode) vs. I_{LOAD}

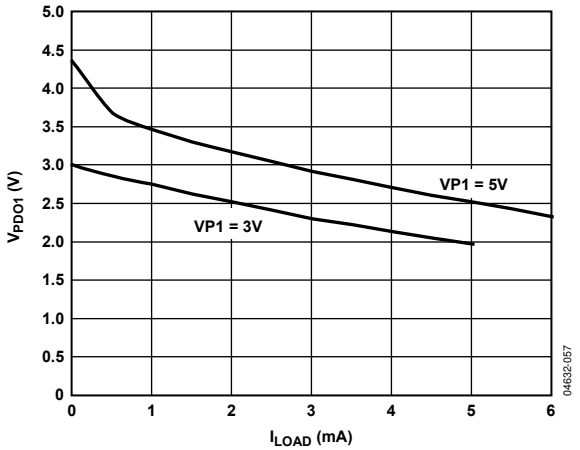

Figure 12. V_{PDO1} (Strong Pull-Up to VPx) vs. I_{LOAD}

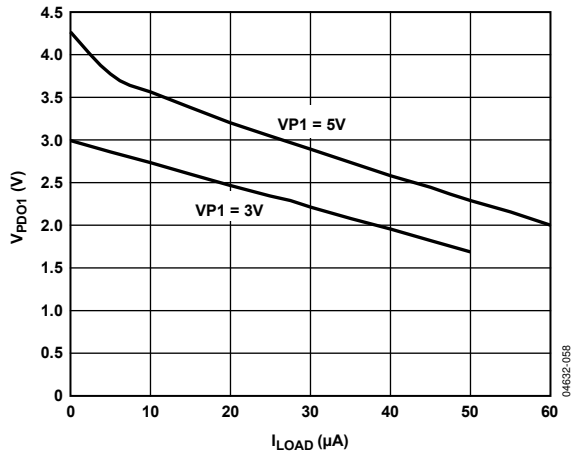

Figure 13. V_{PDO1} (Weak Pull-Up to VPx) vs. I_{LOAD}

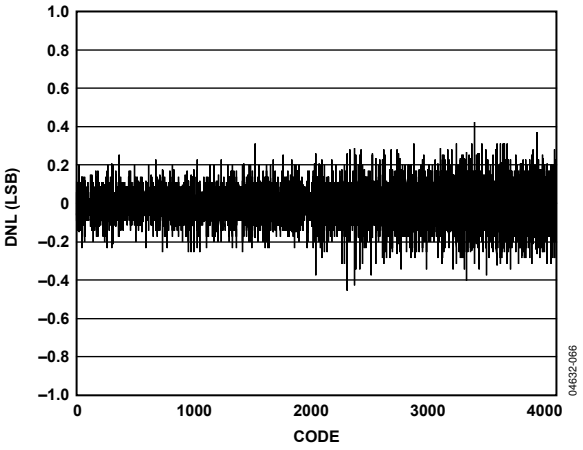

Figure 14. DNL for ADC

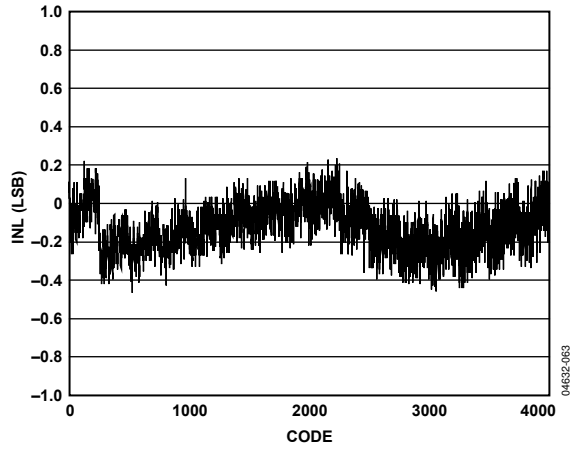

Figure 15. INL for ADC

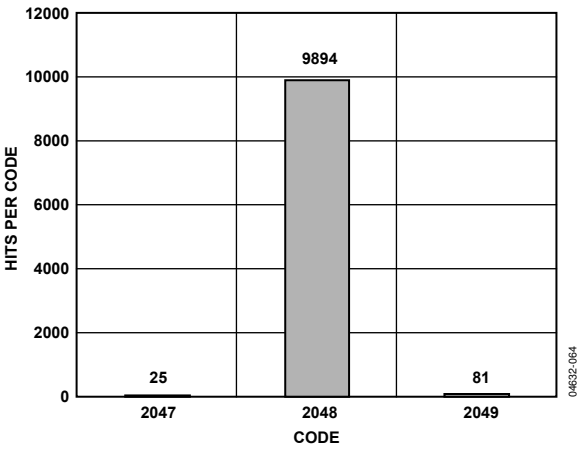

Figure 16. ADC Noise, Midcode Input, 10,000 Reads

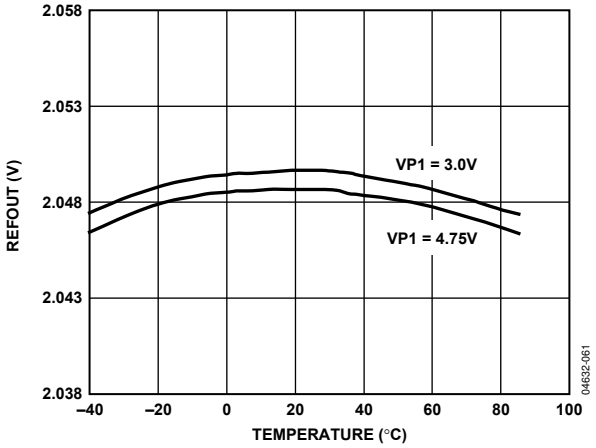

Figure 17. REFOUT vs. Temperature

POWERING THE ADM1063

The ADM1063 is powered from the highest voltage input on either the positive-only supply inputs (VPx) or the high voltage supply input (VH). This technique offers improved redundancy because the device is not dependent on any particular voltage rail to keep it operational. The same pins are used for supply fault detection (see the Supply Supervision section). A V_{DD} arbitrator on the device chooses which supply to use. The arbitrator can be considered an OR'ing of five low dropout regulators (LDOs) together. A supply comparator chooses the highest input to provide the on-chip supply. There is minimal switching loss with this architecture (~0.2 V), resulting in the ability to power the ADM1063 from a supply as low as 3.0 V. Note that the supply on the VXx pins cannot be used to power the device.

An external capacitor to GND is required to decouple the on-chip supply from noise. This capacitor should be connected to the VDDCAP pin, as shown in Figure 18. The capacitor has another use during brownouts (momentary loss of power). Under these conditions, when the input supply (VPx or VH) dips transiently below V_{DD}, the synchronous rectifier switch immediately turns off so that it does not pull V_{DD} down. The V_{DD} capacitor can then act as a reservoir to keep the device active until the next highest supply takes over the powering of the device. A 10 µF capacitor is recommended for this reservoir/decoupling function.

The VH input pin can accommodate supplies up to 14.4 V, which allows the ADM1063 to be powered using a 12 V backplane supply. In cases where this 12 V supply is hot swapped, it is recommended that the ADM1063 not be connected directly to the supply. Suitable precautions, such as the use of a hot swap controller, should be taken to protect the device from transients that could cause damage during hot swap events.

When two or more supplies are within 100 mV of each other, the supply that first takes control of V_{DD} keeps control. For example, if VP1 is connected to a 3.3 V supply, V_{DD} powers up to approximately 3.1 V through VP1. If VP2 is then connected to another 3.3 V supply, VP1 still powers the device, unless VP2 goes 100 mV higher than VP1.

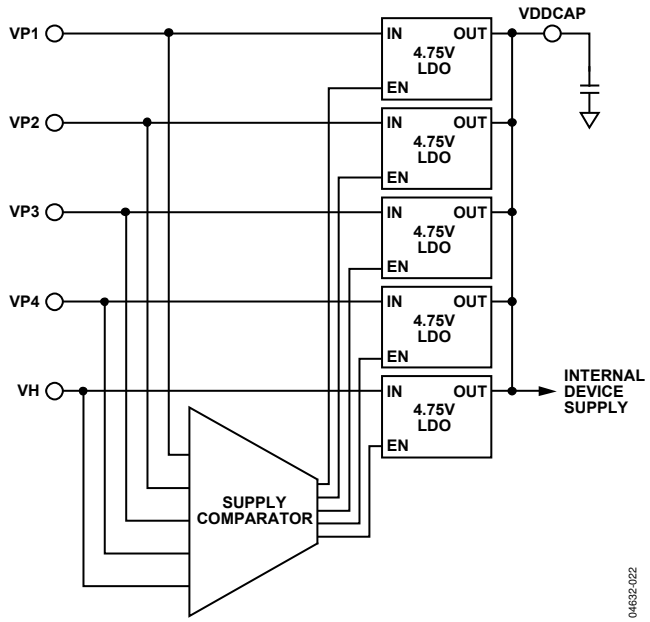

Figure 18. V_{DD} Arbitrator Operation

SLEW RATE CONSIDERATION

When the ambient temperature of operation is less than approximately −20°C, and in the event of a power loss where all supply inputs fail for less than a few hundreds of milliseconds (for example, due to a system supply brownout), it is recommended that the supply voltage recover with a ramp rate of at least 1.5 V/ms or less than 0.5 V/ms.

INPUTS

SUPPLY SUPERVISION

The ADM1063 has 10 programmable inputs. Five of these are dedicated supply fault detectors (SFDs). These dedicated inputs are called VH and VPx (VP1 to VP4) by default. The other five inputs are labeled VXx (VX1 to VX5) and have dual functionality. They can be used either as SFDs, with functionality similar to VH and VPx, or as CMOS-/TTL-compatible logic inputs to the device. Therefore, the ADM1063 can have up to 10 analog inputs, a minimum of five analog inputs and five digital inputs, or a combination thereof. If an input is used as an analog input, it cannot be used as a digital input. Therefore, a configuration requiring 10 analog inputs has no available digital inputs. Table 6 shows the details of each input.

PROGRAMMING THE SUPPLY FAULT DETECTORS

The ADM1063 can have up to 10 SFDs on its 10 input channels. These highly programmable reset generators enable the supervision of up to 10 supply voltages. The supplies can be as low as 0.573 V and as high as 14.4 V. The inputs can be configured to detect an undervoltage fault (the input voltage drops below a preprogrammed value), an overvoltage fault (the input voltage rises above a preprogrammed value), or an out-of-window fault (the input voltage is outside a preprogrammed range). The thresholds can be programmed to an 8-bit resolution in registers provided in the ADM1063. This translates to a voltage resolution that is dependent on the range selected.

The resolution is given by

$$Step\ Size = Threshold\ Range/255$$

Therefore, if the high range is selected on VH, the step size can be calculated as follows:

$$(14.4\ V - 6.0\ V)/255 = 32.9\ mV$$

Table 5 lists the upper and lower limits of each available range, the bottom of each range (V_B), and the range itself (V_R).

Table 5. Voltage Range Limits

Voltage Range (V)	V_B (V)	V_R (V)
0.573 to 1.375	0.573	0.802
1.25 to 3.00	1.25	1.75
2.5 to 6.0	2.5	3.5
6.0 to 14.4	6.0	8.4

The threshold value required is given by

$$V_T = (V_R \times N)/255 + V_B$$

where:
V_T is the desired threshold voltage (undervoltage or overvoltage).
V_R is the voltage range.
N is the decimal value of the 8-bit code.
V_B is the bottom of the range.

Reversing the equation, the code for a desired threshold is given by

$$N = 255 \times (V_T - V_B)/V_R$$

For example, if the user wants to set a 5 V overvoltage threshold on VP1, the code to be programmed in the PS1OVTH register (as discussed in the AN-698 Application Note) is given by

$$N = 255 \times (5 - 2.5)/3.5$$

Therefore, N = 182 (1011 0110 or 0xB6).

INPUT COMPARATOR HYSTERESIS

The UV and OV comparators shown in Figure 19 are always monitoring VPx. To avoid chatter (multiple transitions when the input is very close to the set threshold level), these comparators have digitally programmable hysteresis. The hysteresis can be programmed up to the values shown in Table 6.

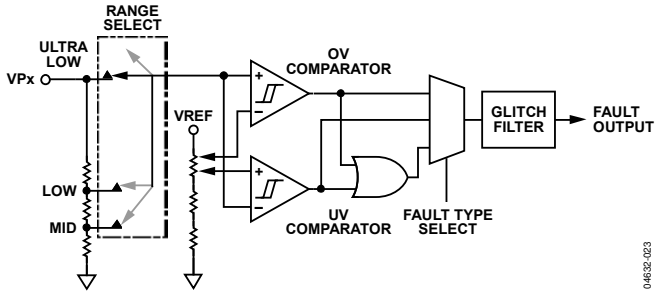

Figure 19. Supply Fault Detector Block

The hysteresis is added after a supply voltage goes out of tolerance. Therefore, the user can program the amount above the undervoltage threshold to which the input must rise before an undervoltage fault is deasserted. Similarly, the user can program the amount below the overvoltage threshold to which an input must fall before an overvoltage fault is deasserted.

Table 6. Input Functions, Thresholds, and Ranges

Input	Function	Voltage Range (V)	Maximum Hysteresis	Voltage Resolution (mV)	Glitch Filter (µs)
VH	High Voltage Analog Input	2.5 to 6.0	425 mV	13.7	0 to 100
		6.0 to 14.4	1.02 V	32.9	0 to 100
VPx	Positive Analog Input	0.573 to 1.375	97.5 mV	3.14	0 to 100
		1.25 to 3.00	212 mV	6.8	0 to 100
		2.5 to 6.0	425 mV	13.7	0 to 100
VXx	High-Z Analog Input	0.573 to 1.375	97.5 mV	3.14	0 to 100
	Digital Input	0 to 5.0	N/A	N/A	0 to 100

The hysteresis value is given by

$$V_{HYST} = V_R \times N_{THRESH}/255$$

where:
V_{HYST} is the desired hysteresis voltage.
N_{THRESH} is the decimal value of the 5-bit hysteresis code.

Note that N_{THRESH} has a maximum value of 31. The maximum hysteresis for the ranges is listed in Table 6.

INPUT GLITCH FILTERING

The final stage of the SFDs is a glitch filter. This block provides time-domain filtering on the output of the SFD comparators, which allows the user to remove any spurious transitions, such as supply bounce at turn-on. The glitch filter function is in addition to the digitally programmable hysteresis of the SFD comparators. The glitch filter timeout is programmable up to 100 µs.

For example, when the glitch filter timeout is 100 µs, any pulse appearing on the input of the glitch filter block that is less than 100 µs in duration is prevented from appearing on the output of the glitch filter block. Any input pulse that is longer than 100 µs appears on the output of the glitch filter block. The output is delayed with respect to the input by 100 µs. The filtering process is shown in Figure 20.

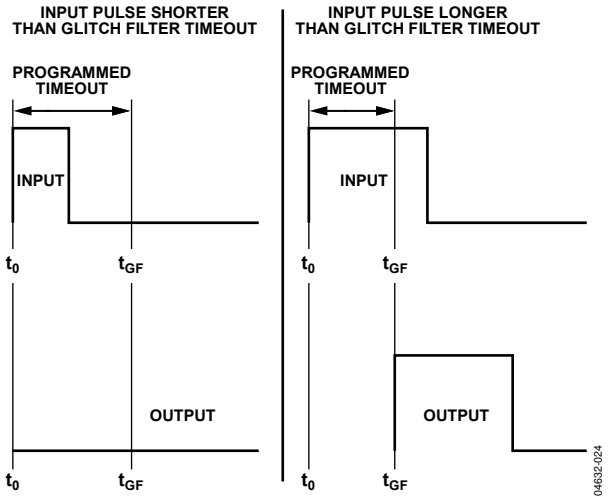

Figure 20. Input Glitch Filter Function

VP1 Glitch Filtering

If the ADC round-robin is used, it is recommended to enable glitch filtering on VP1 because the ADC input mux is connected to VP1 when the ADC round-robin stops. When the ADC round-robin stops, a small internal glitch on the VP1 monitor rail occurs, and if the rail is close to the UV threshold, it may be enough to trip the VP1 UV comparator. Use any value of glitch filter greater than 0 µs to avoid false UV triggers. For more information about the ADC round-robin, see the Voltage Readback section.

SUPPLY SUPERVISION WITH VXx INPUTS

The VXx inputs have two functions. They can be used as either supply fault detectors or digital logic inputs. When selected as analog (SFD) inputs, the VXx pins have functionality that is very similar to the VH and VPx pins. The primary difference is that the VXx pins have only one input range: 0.573 V to 1.375 V. Therefore, these inputs can directly supervise only the very low supplies. However, the input impedance of the VXx pins is high, allowing an external resistor divide network to be connected to the pin. Thus, potentially any supply can be divided down into the input range of the VXx pin and supervised, enabling the ADM1063 to monitor other supplies, such as +24 V, +48 V, and −5 V.

An additional supply supervision function is available when the VXx pins are selected as digital inputs. In this case, the analog function is available as a second detector on each of the dedicated analog inputs, VPx and VH. The analog function of VX1 is mapped to VP1, VX2 is mapped to VP2, and so on; VX5 is mapped to VH. In this case, these SFDs can be viewed as secondary or warning SFDs.

The secondary SFDs are fixed to the same input range as the primary SFDs. They are used to indicate warning levels rather than failure levels. This allows faults and warnings to be generated on a single supply using only one pin. For example, if VP1 is set to output a fault when a 3.3 V supply drops to 3.0 V, VX1 can be set to output a warning at 3.1 V. Warning outputs are available for readback from the status registers. They are also OR'ed together and fed into the SE, allowing warnings to generate interrupts on the PDOs. Therefore, in this example, if the supply drops to 3.1 V, a warning is generated and remedial action can be taken before the supply drops out of tolerance.

VXx PINS AS DIGITAL INPUTS

As discussed in the Supply Supervision with VXx Inputs section, the VXx input pins on the ADM1063 have dual functionality. The second function is as a digital logic input to the device. Therefore, the ADM1063 can be configured for up to five digital inputs. These inputs are TTL-/CMOS-compatible. Standard logic signals can be applied to the pins: RESET from reset generators, PWRGD signals, fault flags, manual resets, and so on. These signals are available as inputs to the SE and, therefore, can be used to control the status of the PDOs. The inputs can be configured to detect either a change in level or an edge.

When configured for level detection, the output of the digital block is a buffered version of the input. When configured for edge detection, a pulse of programmable width is output from the digital block once the logic transition is detected. The width is programmable from 0 µs to 100 µs.

The digital blocks feature the same glitch filter function that is available on the SFDs. This enables the user to ignore spurious transitions on the inputs. For example, the filter can be used to debounce a manual reset switch.

When configured as digital inputs, each VXx pin has a weak (10 µA) pull-down current source available for placing the input into a known condition, even if left floating. The current source, if selected, weakly pulls the input to GND.

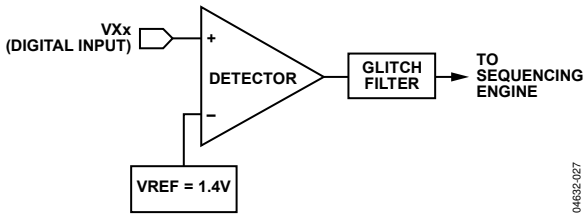

Figure 21. VXx Digital Input Function

OUTPUTS

SUPPLY SEQUENCING THROUGH CONFIGURABLE OUTPUT DRIVERS

Supply sequencing is achieved with the ADM1063 using the programmable driver outputs (PDOs) on the device as control signals for supplies. The output drivers can be used as logic enables or as FET drivers.

The sequence in which the PDOs are asserted (and, therefore, the supplies are turned on) is controlled by the sequencing engine (SE). The SE determines what action is taken with the PDOs, based on the condition of the ADM1063 inputs. Therefore, the PDOs can be set up to assert when the SFDs are in tolerance, the correct input signals are received on the VXx digital pins, no warnings are received from any of the inputs of the device, and at other times. The PDOs can be used for a variety of functions. The primary function is to provide enable signals for LDOs or dc-to-dc converters that generate supplies locally on a board. The PDOs can also be used to provide a PWRGD signal, when all the SFDs are in tolerance, or a RESET output if one of the SFDs goes out of specification (this can be used as a status signal for a DSP, FPGA, or other microcontroller).

The PDOs can be programmed to pull up to a number of different options. The outputs can be programmed as follows:

- Open drain (allowing the user to connect an external pull-up resistor).
- Open drain with weak pull-up to V_{DD}.
- Open drain with strong pull-up to V_{DD}.
- Open drain with weak pull-up to VPx.
- Open drain with strong pull-up to VPx.
- Strong pull-down to GND.
- Internally charge-pumped high drive (12 V, PDO1 to PDO6 only).

The last option (available only on PDO1 to PDO6) allows the user to directly drive a voltage high enough to fully enhance an external N-FET, which is used to isolate, for example, a card-side voltage from a backplane supply (a PDO can sustain greater than 10.5 V into a 1 µA load). The pull-down switches can also be used to drive status LEDs directly.

The data driving each of the PDOs can come from one of three sources. The source can be enabled in the PDOxCFG configuration register (see the AN-698 Application Note for details).

The data sources are as follows:

- Output from the SE.
- Directly from the SMBus. A PDO can be configured so that the SMBus has direct control over it. This enables software control of the PDOs. Therefore, a microcontroller can be used to initiate a software power-up/power-down sequence.
- On-chip clock. A 100 kHz clock is generated on the device. This clock can be made available on any of the PDOs. It can be used, for example, to clock an external device such as an LED.

DEFAULT OUTPUT CONFIGURATION

All of the internal registers in an unprogrammed ADM1063 device from the factory are set to 0. Because of this, the PDOx pins are pulled to GND by a weak (20 kΩ) on-chip pull-down resistor.

As the input supply to the ADM1063 ramps up on VPx or VH, all PDOx pins behave as follows:

- Input supply = 0 V to 1.2 V. The PDOs are high impedance.
- Input supply = 1.2 V to 2.7 V. The PDOs are pulled to GND by a weak (20 kΩ) on-chip pull-down resistor.
- Supply > 2.7 V. Factory programmed devices continue to pull all PDOs to GND by a weak (20 kΩ) on-chip pull-down resistor. Programmed devices download current EEPROM configuration data, and the programmed setup is latched. The PDO then goes to the state demanded by the configuration. This provides a known condition for the PDOs during power-up.

The internal pull-down can be overdriven with an external pull-up of suitable value tied from the PDOx pin to the required pull-up voltage. The 20 kΩ resistor must be accounted for in calculating a suitable value. For example, if PDOx must be pulled up to 3.3 V, and 5 V is available as an external supply, the pull-up resistor value is given by

$$3.3\ V = 5\ V \times 20\ k\Omega/(R_{UP} + 20\ k\Omega)$$

Therefore,

$$R_{UP} = (100\ k\Omega - 66\ k\Omega)/3.3\ V = 10\ k\Omega$$

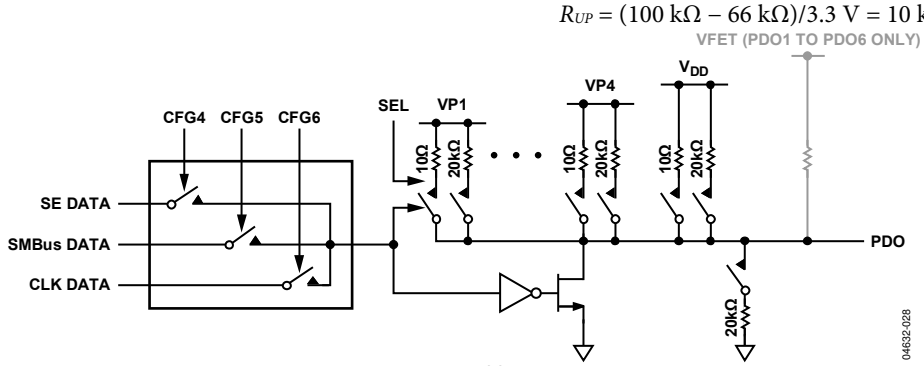

Figure 22. Programmable Driver Output

SEQUENCING ENGINE

OVERVIEW

The ADM1063 sequencing engine (SE) provides the user with powerful and flexible control of sequencing. The SE implements a state machine control of the PDO outputs, with state changes conditional on input events. SE programs can enable complex control of boards such as power-up and power-down sequence control, fault event handling, interrupt generation on warnings, and so on. A watchdog function that verifies the continued operation of a processor clock can be integrated into the SE program. The SE can also be controlled via the SMBus, giving software or firmware control of the board sequencing.

The SE state machine comprises 63 state cells. Each state has the following attributes:

- Monitors signals indicating the status of the 10 input pins, VP1 to VP4, VH, and VX1 to VX5.
- Can be entered from any other state.
- Three exit routes move the state machine onto a next state: sequence detection, fault monitoring, and timeout.
- Delay timers for the sequence and timeout blocks can be programmed independently and changed with each state change. The range of timeouts is from 0 ms to 400 ms.
- Output condition of the 10 PDO pins is defined and fixed within a state.
- Transition from one state to the next is made in less than 20 µs, which is the time needed to download a state definition from EEPROM to the SE.

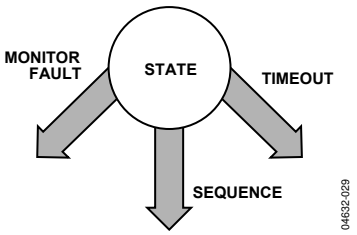

Figure 23. State Cell

The ADM1063 offers up to 63 state definitions. The signals monitored to indicate the status of the input pins are the outputs of the SFDs.

WARNINGS

The SE also monitors warnings. These warnings can be generated when the ADC readings violate their limit register value or when the secondary voltage monitors on VPx and VH are triggered. The warnings are OR'ed together and are available as a single warning input to each of the three blocks that enable exiting a state.

SMBus JUMP (UNCONDITIONAL JUMP)

The SE can be forced to advance to the next state unconditionally. This enables the user to force the SE to advance. Examples of the use of this feature include moving to a margining state or debugging a sequence. The SMBus jump or go-to command can be seen as another input to sequence and timeout blocks to provide an exit from each state.

Table 7. Sample Sequence State Entries

State	Sequence	Timeout	Monitor
IDLE1	If VX1 is low, go to State IDLE2.		
IDLE2	If VP1 is okay, go to State EN3V3.		
EN3V3	If VP2 is okay, go to State EN2V5.	If VP2 is not okay after 10 ms, go to State DIS3V3.	If VP1 is not okay, go to State IDLE1.
DIS3V3	If VX1 is high, go to State IDLE1.		
EN2V5	If VP3 is okay, go to State PWRGD.	If VP3 is not okay after 20 ms, go to State DIS2V5.	If VP1 or VP2 is not okay, go to State FSEL2.
DIS2V5	If VX1 is high, go to State IDLE1.		
FSEL1	If VP3 is not okay, go to State DIS2V5.		If VP1 or VP2 is not okay, go to State FSEL2.
FSEL2	If VP2 is not okay, go to State DIS3V3.		If VP1 is not okay, go to State IDLE1.
PWRGD	If VX1 is high, go to State DIS2V5.		If VP1, VP2, or VP3 is not okay, go to State FSEL1.

SEQUENCING ENGINE APPLICATION EXAMPLE

The application in this section demonstrates the operation of the SE. Figure 25 shows how the simple building block of a single SE state can be used to build a power-up sequence for a three-supply system. Table 8 lists the PDO outputs for each state in the same SE implementation. In this system, a good 5 V supply on VP1 and the VX1 pin held low are the triggers required to start a power-up sequence. The sequence next turns on the 3.3 V supply, then the 2.5 V supply (assuming successful turn-on of the 3.3 V supply). When all three supplies have turned on correctly, the PWRGD state is entered, where the SE remains until a fault occurs on one of the three supplies, or until it is instructed to go through a power-down sequence by VX1 going high.

Faults are dealt with throughout the power-up sequence on a case-by-case basis. The following three sections (the Sequence Detector section, the Monitoring Fault Detector section, and the Timeout Detector section) describe the individual blocks and use the sample application shown in Figure 25 to demonstrate the actions of the state machine.

Sequence Detector

The sequence detector block is used to detect when a step in a sequence has been completed. It looks for one of the SE inputs to change state and is most often used as the gate for successful progress through a power-up or power-down sequence. A timer block that is included in this detector can insert delays into a power-up or power-down sequence, if required. Timer delays can be set from 10 µs to 400 ms. Figure 24 is a block diagram of the sequence detector.

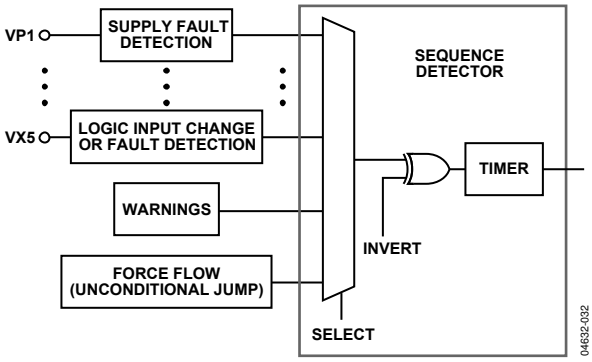

Figure 24. Sequence Detector Block Diagram

If a timer delay is specified, the input to the sequence detector must remain in the defined state for the duration of the timer delay. If the input changes state during the delay, the timer is reset.

The sequence detector can also help to identify monitoring faults. In the sample application shown in Figure 25, the FSEL1 and FSEL2 states first identify which of the VP1, VP2, or VP3 pins has faulted, and then they take appropriate action.

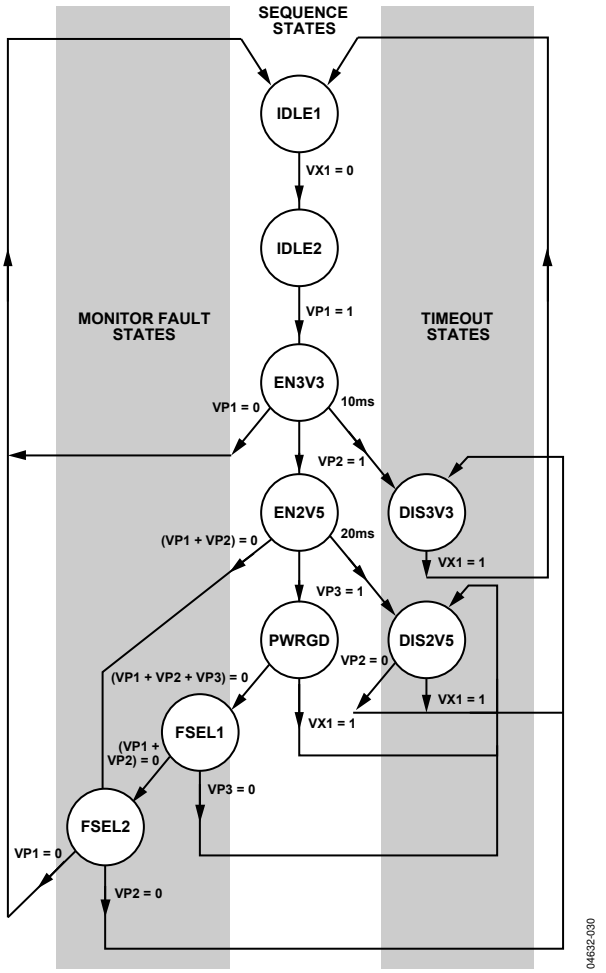

Figure 25. Sample Application Flow Diagram

Table 8. PDO Outputs for Each State

PDO Outputs	IDLE1	IDLE2	EN3V3	EN2V5	DIS3V3	DIS2V5	PWRGD	FSEL1	FSEL2
PDO1 = 3V3ON	0	0	1	1	0	1	1	1	1
PDO2 = 2V5ON	0	0	0	1	1	0	1	1	1
PDO3 = FAULT	0	0	0	0	1	1	0	1	1

Monitoring Fault Detector

The monitoring fault detector block is used to detect a failure on an input. The logical function implementing this is a wide OR gate that can detect when an input deviates from its expected condition. The clearest demonstration of the use of this block is in the PWRGD state, where the monitor block indicates that a failure on one or more of the VP1, VP2, or VP3 inputs has occurred.

No programmable delay is available in this block because the triggering of a fault condition is likely to be caused by a supply falling out of tolerance. In this situation, the device needs to react as quickly as possible. Some latency occurs when moving out of this state because it takes a finite amount of time (~20 µs) for the state configuration to download from EEPROM into the SE. Figure 26 is a block diagram of the monitoring fault detector.

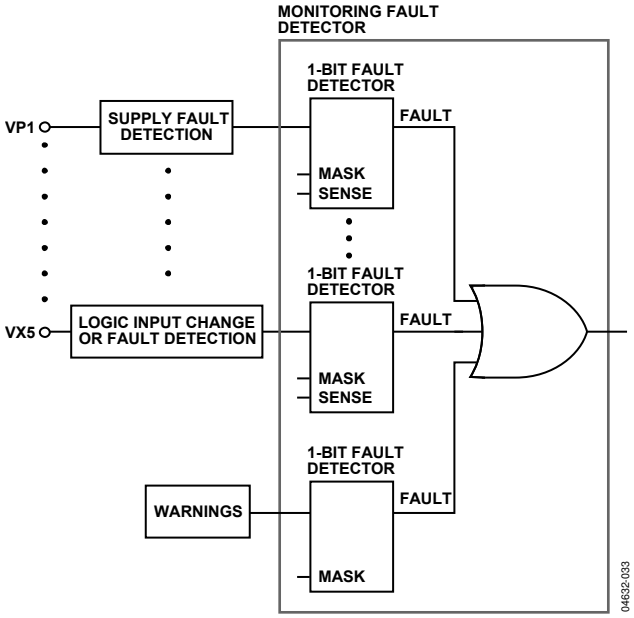

Figure 26. Monitoring Fault Detector Block Diagram

Timeout Detector

The timeout detector allows the user to trap a failure to ensure proper progress through a power-up or power-down sequence.

In the sample application shown in Figure 25, the timeout next-state transition is from the EN3V3 and EN2V5 states. For the EN3V3 state, the signal 3V3ON is asserted on the PDO1 output pin upon entry to this state to turn on a 3.3 V supply. This supply rail is connected to the VP2 pin, and the sequence detector looks for the VP2 pin to go above its undervoltage threshold, which is set in the supply fault detector (SFD) attached to that pin.

The power-up sequence progresses when this change is detected. If, however, the supply fails (perhaps due to a short circuit overloading this supply), the timeout block traps the problem. In this example, if the 3.3 V supply fails within 10 ms, the SE moves to the DIS3V3 state and turns off this supply by bringing PDO1 low. It also indicates that a fault has occurred by taking PDO3 high. Timeout delays of 100 µs to 400 ms can be programmed.

FAULT AND STATUS REPORTING

The ADM1063 has a fault latch for recording faults. Two registers, FSTAT1 and FSTAT2, are set aside for this purpose. A single bit is assigned to each input of the device, and a fault on that input sets the relevant bit. The contents of the fault register can be read out over the SMBus to determine which input(s) faulted. The fault register can be enabled/disabled in each state. To latch data from one state, ensure that the fault latch is disabled in the following state. This ensures that only real faults are captured and not, for example, undervoltage conditions that may be present during a power-up or power-down sequence.

The ADM1063 also has a number of status registers. These include more detailed information, such as whether an undervoltage or overvoltage fault is present on a particular input. The status registers also include information on ADC limit faults. Note that the data in the status registers is not latched in any way and, therefore, is subject to change at any time.

See the AN-698 Application Note for full details about the ADM1063 registers.

VOLTAGE READBACK

The ADM1063 has an on-board, 12-bit, accurate ADC for voltage readback over the SMBus. The ADC has a 13-channel analog mux on the front end. The 13 channels consist of the 10 SFD inputs (VH, VPx, and VXx), plus three channels for temperature readback (see the Temperature Measurement System section). Any or all of these inputs can be selected to be read, in turn, by the ADC. The circuit controlling this operation is called the ADC round-robin. This circuit can be selected to run through its loop of conversions once or continuously. Averaging is also provided for each channel. In this case, the ADC round-robin runs through its loop of conversions 16 times before returning a result for each channel. At the end of this cycle, the results are written to the output registers.

The ADC samples single-sided inputs with respect to the AGND pin. A 0 V input gives out Code 0, and an input equal to the voltage on REFIN gives out full code (4095 decimal).

The inputs to the ADC come directly from the VXx pins and from the back of the input attenuators on the VPx and VH pins, as shown in Figure 27 and Figure 28.

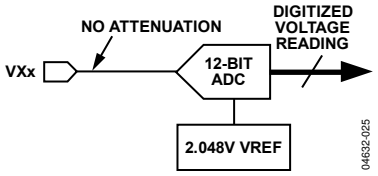

Figure 27. ADC Reading on VXx Pins

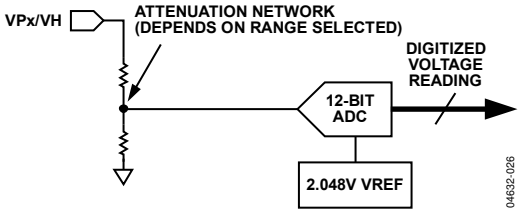

Figure 28. ADC Reading on VPx/VH Pins

The voltage at the input pin can be derived from the following equation:

$$V = \frac{ADC\,Code}{4095} \times Attenuation\ Factor \times V_{REFIN}$$

where V_{REFIN} = 2.048 V when the internal reference is used (that is, the REFIN pin is connected to the REFOUT pin).

The ADC input voltage ranges for the SFD input ranges are listed in Table 9.

Table 9. ADC Input Voltage Ranges

SFD Input Range (V)	Attenuation Factor	ADC Input Voltage Range (V)
0.573 to 1.375	1	0 to 2.048
1.25 to 3.00	2.181	0 to 4.46
2.5 to 6.0	4.363	0 to 6.0[1]
6.0 to 14.4	10.472	0 to 14.4[1]

[1] The upper limit is the absolute maximum allowed voltage on the VPx and VH pins.

The typical way to supply the reference to the ADC on the REFIN pin is to connect the REFOUT pin to the REFIN pin. REFOUT provides a 2.048 V reference. As such, the supervising range covers less than half the normal ADC range. It is possible, however, to provide the ADC with a more accurate external reference for improved readback accuracy.

Supplies can also be connected to the input pins purely for ADC readback, even though these pins may go above the expected supervisory range limits (but not above the absolute maximum ratings on these pins). For example, a 1.5 V supply connected to the VX1 pin can be correctly read out as an ADC code of approximately 3/4 full scale, but it always sits above any supervisory limits that can be set on that pin. The maximum setting for the REFIN pin is 2.048 V.

SUPPLY SUPERVISION WITH THE ADC

In addition to the readback capability, another level of supervision is provided by the on-chip, 12-bit ADC. The ADM1063 has limit registers with which the user can program a maximum or minimum allowable threshold. Exceeding the threshold generates a warning that can either be read back from the status registers or input into the SE to determine what sequencing action the ADM1063 should take. Only one register is provided for each input channel. Therefore, either an undervoltage threshold or overvoltage threshold (but not both) can be set for a given channel. The ADC round-robin can be enabled via an SMBus write, or it can be programmed to turn on in any state in the SE program. For example, it can be set to start after a power-up sequence is complete, and all supplies are known to be within expected tolerance limits.

Note that a latency is built into this supervision, dictated by the conversion time of the ADC. With all 12 channels selected, the total time for the round-robin operation (averaging off) is approximately 6 ms (500 µs per channel selected). Supervision using the ADC, therefore, does not provide the same real-time response as the SFDs.

TEMPERATURE MEASUREMENT SYSTEM

The ADM1063 contains an on-chip, band gap temperature sensor, whose output is digitized by the on-chip, 12-bit ADC. Theoretically, the temperature sensor and the ADC can measure temperatures from −128°C to +128°C with a resolution of 0.125°C. Because this exceeds the operating temperature range of the device, local temperature measurements outside this range are not possible. Temperature measurements from −128°C to +128°C are possible using a remote sensor. The output code is in offset binary format, with −128°C given by Code 0x400, 0°C given by Code 0x800, and +128°C given by Code 0xC00.

As with the other analog inputs to the ADC, a limit register is provided for each of the temperature input channels. Therefore, a temperature limit can be set such that if it is exceeded, a warning is generated and available as an input to the sequencing engine. This enables users to control their sequence or monitor functions based on an overtemperature or undertemperature event.

REMOTE TEMPERATURE MEASUREMENT

The ADM1063 can measure the temperature of two remote diode sensors or diode-connected transistors connected to the DxN and DxP pins.

The forward voltage of a diode or diode-connected transistor operated at a constant current exhibits a negative temperature coefficient of about −2 mV/°C. Unfortunately, the absolute value of V_{BE} varies from device to device, and individual calibration is required to null it, making the technique unsuitable for mass production. The technique used in the ADM1063 is to measure the change in V_{BE} when the device is operated at two different currents.

The change in V_{BE} is given by

$$\Delta V_{BE} = kT/q \times ln(N)$$

where:
k is Boltzmann's constant.
q is the charge on the carrier.
T is the absolute temperature in Kelvin.
N is the ratio of the two currents.

Figure 31 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor provided for temperature monitoring on some microprocessors, but it could equally be a discrete transistor such as a 2N3904 or 2N3906.

If a discrete transistor is used, the collector is not grounded and should be linked to the base. If a PNP transistor is used, the base is connected to the DxN input and the emitter is connected to the DxP input. If an NPN transistor is used, the emitter is connected to the DxN input and the base is connected to the DxP input. Figure 29 and Figure 30 show how to connect the ADM1063 to an NPN or PNP transistor for temperature measurement. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground but is biased above ground by an internal diode at the DxN input.

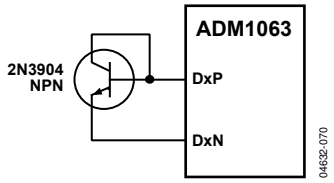

Figure 29. Measuring Temperature Using an NPN Transistor

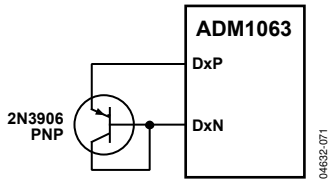

Figure 30. Measuring Temperature Using a PNP Transistor

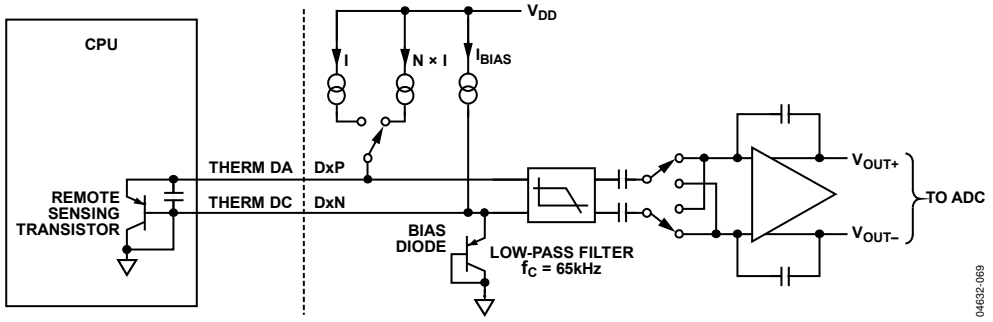

Figure 31. Signal Conditioning for Remote Diode Temperature Sensors

To measure ΔV_{BE}, the sensor is switched between operating currents of I and N × I. The resulting waveform is passed through a 65 kHz low-pass filter to remove noise and through a chopper-stabilized amplifier that amplifies and rectifies the waveform to produce a dc voltage proportional to ΔV_{BE}. This voltage is measured by the ADC to produce a temperature output in 12-bit offset binary. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles. A remote temperature measurement takes nominally 600 ms. The results of remote temperature measurements are stored in 12-bit, offset binary format, as shown in Table 10. This format provides temperature readings with a resolution of 0.125°C.

Table 10. Temperature Data Format

Temperature	Digital Output (Hex)	Digital Output (Binary)
−128°C	0x400	010000000000
−125°C	0x418	010000011000
−100°C	0x4E0	010011100000
−75°C	0x5A8	010110101000
−50°C	0x670	011001110000
−25°C	0x738	011100111000
−10°C	0x7B0	011110110000
0°C	0x800	100000000000
+10.25°C	0x852	100001010010
+25.5°C	0x8CC	100011001100
+50.75°C	0x996	100110010110
+75°C	0xA58	101001011000
+100°C	0XB20	101100100000
+125°C	0xBE8	101111101000
+128°C	0xC00	110000000000