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–48 V Hot Swap Controller and Digital Power Monitor with PMBus Interface

Data Sheet **ADM1075**

FEATURES

- **Constant power foldback for FET SOA protection**
- **Precision (<1.0%) current and voltage measurement**
- **Controls inrush and faults for negative supply voltages**
- **Suitable for wide input range due to internal shunt regulator**
- **25 mV/50 mV full-scale sense voltage**
- **Fine tune current limit to allow use of standard sense resistor**
- **Soft start inrush current limit profiling**
- **1% accurate UVH and OV pins, 1.5% accurate UVL pin**
- **PMBus/I²C interface for control, telemetry, and fault recording**
- **28-lead LFCSP and TSSOP**
- **–40°C to 105°C junction temperature (T_J) operating range**

APPLICATIONS

- **Telecommunication and data communication equipment**
- **Central office switching**
- **–48 V distributed power systems**
- **Negative power supply control**
- **High availability servers**

PRODUCT HIGHLIGHTS

1. Constant Power Foldback.
   Maximum FET power set by a PLIM resistor divider. This eases complexity when designing to maintain FET SOA.
2. Adjustable Current Limit.
   The current limit is adjustable via the ISET pin allowing for the use of a standard value sense resistor.
3. 12-Bit ADC.
   Accurate voltage, current, and power measurements. Also enables calculation of energy consumption over time.
4. PMBus/I²C Interface.
   PMBus fast mode compliant interface used to read back status and data registers and set warning and fault limits.
5. Fault Recording.
   Latched status registers provide useful debugging information to help trace faults in high reliability systems.
6. Built-In Soft Start.
   Soft start capacitor controls inrush current profile with di/dt control.

FUNCTIONAL BLOCK DIAGRAM

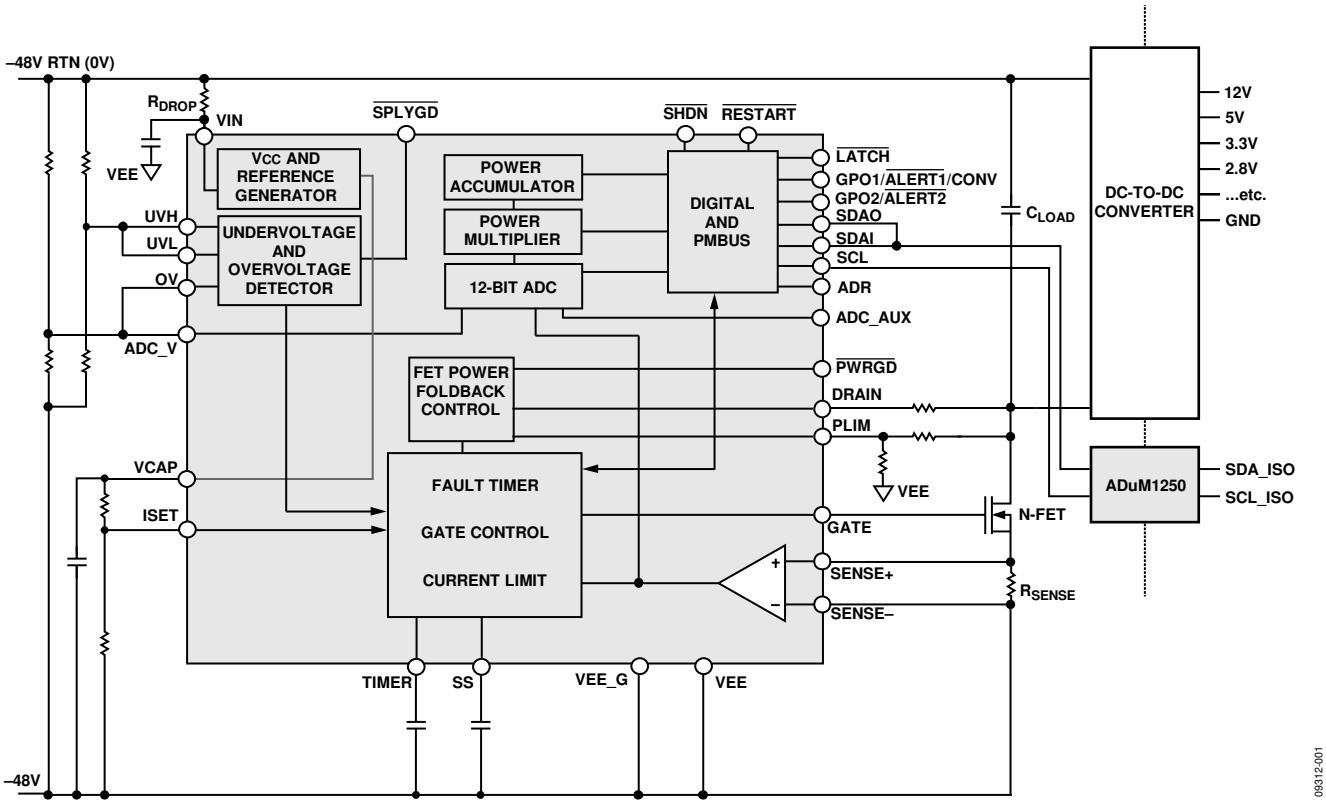

Figure 1.

Rev. C **Document Feedback**

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ADM1075* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADM1075 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1135: ADC Sampling Information ADM1275/ ADM1276/ADM1075
- AN-1343: Energy Metering on Hot Swap and Power Monitor Devices

Data Sheet

- ADM1075: –48 V Hot Swap Controller and Digital Power Monitor with PMBus Interface Data Sheet

User Guides

- UG-304: Evaluating the ADM1075 –48 V Hot-Swap Controller and Digital Power Monitor with PMBus Interface
- UG-353: Hot Swap and Power Monitor Software
- UG-404: USB-SDP-CABLEZ Serial Interface Board
- UG-548: ADM1075 Mini Evaluation Board User Guide
- UG-733: ISO-CABLEZ User Guide

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADMxxxx Common Run-Time
- Hot-Swap & Power Monitoring Evaluation Software

DESIGN RESOURCES

- ADM1075 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADM1075 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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4/14—Rev. B to Rev. C

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4/13—Rev. A to Rev. B

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Added I Partial Transactions on I^2C Bus Section 28
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3/12—Rev. 0 to Rev. A

Added 28-Lead LFCSP ..... Universal
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Added Figure 4; Renumbered Sequentially; and changes to Table 5 11
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10/11—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADM1075 is a full feature, negative voltage, hot swap controller with constant power foldback and high accuracy digital current and voltage measurement that allows boards to be safely inserted and removed from a live −48 V backplane. The part provides precise and robust current limiting and protection against both transient and nontransient short circuits and overvoltage and undervoltage conditions. The ADM1075 typically operates from a negative voltage of −35 V to −80 V and, due to shunt regulation, has excellent voltage transient immunity. The operating range of the part is flexible due to the shunt regulator, and the part can be powered directly by a 10 V rail to save shunt power dissipation (see the Powering the ADM1075 section for more details).

A full-scale current limit of 25 mV or 50 mV can be selected by choosing the appropriate model. The maximum current limit is set by the combination of the sense resistor, R_{SENSE}, and the input voltage on the ISET pin, using external resistors. This allows fine tuning of the trip voltage so that standard sense resistors can be used. Inrush current is limited to this programmable value by controlling the gate drive of an external N-channel FET. A built-in soft start function allows control of the inrush current profile by an external capacitor on the soft start (SS) pin.

An external capacitor on the TIMER pin determines the maximum allowed on-time for when the system is in current limit. This is based on the safe operating area (SOA) limits of the MOSFET. A constant power foldback scheme is used to control the power dissipation in the MOSFET during power-up and fault conditions. The ADM1075 regulates the current dynamically to ensure that the power in the MOSFET is within SOA limits as V_{DS} changes. After the timer has expired, the device shuts down the MOSFET. The level of this power, along with the TIMER regulation time, can be set to ensure that the MOSFET remains within the SOA limits.

The ADM1075 employs a limited consecutive retry scheme when the $\overline{\text{LATCH}}$ pin is tied to the $\overline{\text{SHDN}}$ pin. In this mode, if the load current reaches the limit, the FET gate is pulled low after the timer expires and retries after a cooling period for seven attempts only. If the fault remains, the device latches off, and the MOSFET is disabled until a manual restart is initiated. Alternatively, the ADM1075 can be set to retry only once by isolating the $\overline{\text{LATCH}}$ pin from the $\overline{\text{SHDN}}$ pin. The part can also be configured to retry an infinite number of times with a 10 second interval between restarts by connecting the GPO2 pin to the $\overline{\text{RESTART}}$ pin.

The ADM1075 has separate UVx and OV pins for undervoltage and overvoltage detection. The FET is turned off if a nontransient voltage less than the undervoltage threshold (typically −35 V) is detected on the UVx pins or if greater than the overvoltage threshold (typically −80 V) is detected on the OV pin. The operating voltage range of the ADM1075 is programmable via resistor networks on the UVx and OV pins. The hysteresis levels on the overvoltage detectors can also be altered by selecting the appropriate resistors. There are two separate UVx pins to allow accurate programming of hysteresis.

In the case of a short circuit, the ADM1075 has a fast response circuit to detect and respond adequately to this event. If the sense voltage exceeds 1.5 times the normal current limit, a high current (750 mA minimum) gate pull-down switch is activated to shut down the MOSFET as quickly as possible. There is a default internal glitch filter of 900 ns. If a longer filter time or different severe overcurrent limit is required, these parameters can be adjusted via the PMBus™ interface.

The ADM1075 also includes a 12-bit ADC to provide digital measurement of the voltage and load current. The current is measured at the output of the internal current sense amplifier and the voltage from the ADC_V input. This data can be read across the PMBus interface.

The PMBus interface allows a controller to read current, voltage, and power measurements from the ADC. Measurements can be initiated by a PMBus command or can be set up to run continuously. The user can read the latest conversion data whenever it is required. A power accumulator is also provided to report total power consumed in a user specified period (total energy). Up to four unique I^2C addresses can be created, depending on the configuration of the ADR pin.

The GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$ outputs can be used as a flag to warn a microcontroller or FPGA of one or more fault/warning conditions becoming active. The fault type and level is programmed across the PMBus, and the user can select which faults/warnings activate the alert.

Other functions include

- $\overline{\text{PWRGD}}$ output, which can be used to enable a power module (the DRAIN and GATE pins are monitored to determine when the load capacitance is fully charged)
- $\overline{\text{SHDN}}$ input to manually disable the GATE drive
- $\overline{\text{RESTART}}$ input to remotely initiate a 10 second shutdown

SPECIFICATIONS

VEE = −48 V, V_{SENSE} = (V_{SENSE+} − V_{SENSE-}) = 0 mV, shunt regulation current = 10 mA, T_J = −40°C to +105°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYSTEM SUPPLY					
Voltage Transient Immunity		−200		V	
Typical Operating Voltage	−80		−35	V	Determined by external component, R_{SHUNT}
SHUNT REGULATOR					
Operating Supply Voltage Range, VIN	11.5	12.3	13	V	Shunt regulation voltage, I_{IN} = 5.5 mA to 30 mA, maximum I_{IN} dependent on T_A, θ_{JA} (see the Powering the ADM1075 section)
Quiescent Supply Current			5.5	mA	VIN = 13 V
Undervoltage Lockout, V_{UVLO_RISING}			9.2	V	
Undervoltage Lockout Hysteresis			600	mV	
Power Directly Without Shunt	9.2		11.5	V	
UV PINS—UNDERVOLTAGE DETECTION					
Undervoltage Rising Threshold, V_{UVH}	0.99	1.0	1.01	V	
Undervoltage Falling Threshold, V_{UVL}	0.887	0.9	0.913	V	
Total Undervoltage Hysteresis		100		mV	When UVL and UVH are tied together
Undervoltage Fault Filter	3.5		7.5	µs	
UV Propagation Delay		5	8	µs	UV low to GATE pull-down active
UVL/UVH Input Current		1	50	nA	
OV PIN—OVERVOLTAGE DETECTION					
Overvoltage Rising Threshold, V_{OVR}	0.99	1.0	1.01	V	
Overvoltage Hysteresis Current	4.3	5	5.7	µA	
Overvoltage Fault Filter	1.75		3.75	µs	
OV Propagation Delay		2	4	µs	OV high to GATE pull-down active
OV Input Current		1	50	nA	
GATE PIN					
Gate Voltage High	11	12	13	V	I_{GATE} = −1.0 µA
Gate Voltage Low		10	100	mV	I_{GATE} = 100 µA
Pull-Up Current	−50		−30	µA	V_{GATE} = 0 V to 8 V; V_{SS} = 2 V
Pull-Down Current (Regulation)	100			µA	V_{GATE} ≥ 2 V
Pull-Down Current (UV/OV/OC)	5	10		mA	V_{GATE} ≥ 2 V
Pull-Down Current (Severe OC)	750	1500	2000	mA	V_{GATE} ≥ 6 V
Pull-Down On-Time (Severe OC)	8		16	µs	
Gate Hold-Off Resistance		20		Ω	0 V ≤ VIN ≤ 9.2 V
SENSE+, SENSE−					
SENSE+, SENSE− Input Current, I_{SENSEx}			100	µA	V_{SENSE} ≤ 65 mV for ADM1075-1, per individual pin; V_{SENSE} ≤ 130 mV for ADM1075-2, per individual pin
SENSE+, SENSE− Input Imbalance, $I_{\Delta SENSEx}$			1	µA	$I_{\Delta SENSEx}$ = I_{SENSE+} − I_{SENSE-}
VCAP					
Internally Regulated Voltage, V_{VCAP}	2.66	2.7	2.74	V	0 ≤ I_{VCAP} ≤ 100 µA; C_{VCAP} = 1 µF
ISET					
ISET Reference Select Threshold, $V_{ISETRSTH}$	1.35	1.5	1.65	V	If V_{ISET} > $V_{ISETRSTH}$ an internal 1 V reference (V_{CLREF}) is used
ISET Internal Reference, V_{CLREF}		1		V	Accuracies included in total sense voltage accuracies
Gain of Current Sense Amplifier, AV_{CSAMP}		50/25		V/V	Accuracies included in total sense voltage accuracies
ISET Input Current, I_{ISET}			100	nA	V_{ISET} ≤ VCAP
ADM1075-1 ONLY (GAIN = 50)					
Hot Swap Sense Voltage					
Hot Swap Sense Voltage Current Limit, $V_{SENSECL}$	19.4	20	20.6	mV	V_{ISET} > 1.65 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0 V
	24.5	25	25.5	mV	V_{ISET} = 1.25 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0 V
	19.5	20	20.5	mV	V_{ISET} = 1.0 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0 V
	14.5	15	15.5	mV	V_{ISET} = 0.75 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Constant Power Active	9.4	10	11.0	mV	V_{ISET} > 1.65 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0.2 V
	4.5	5	5.7	mV	V_{ISET} > 1.65 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0.4 V
	1.4	2	2.6	mV	V_{ISET} > 1.65 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 1.2 V
Circuit Breaker Offset, V_{CBOS}	0.6	0.75	0.95	mV	Circuit breaker voltage, $V_{CB} = V_{SENSECL} - V_{CBOS}$
Severe Overcurrent					Activates high current gate pull-down
Voltage Threshold, $V_{SENSEOC}$	23	25	27	mV	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; optional select through PMBus
	28	30	32	mV	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; default at power-up
	38	40	42	mV	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; optional select through PMBus
	43	45	47	mV	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; optional select through PMBus
Response Time					
Glitch Filter Duration	50		200	ns	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 18 mV to 52 mV; optional select through PMBus
	500		900	ns	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 18 mV to 52 mV; default at power-up
	6.2		10.7	µs	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 18 mV to 52 mV; optional select through PMBus
	44		57	µs	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 18 mV to 52 mV; optional select through PMBus
Total Response Time	180		300	ns	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 18 mV to 52 mV; optional select through PMBus
	610		950	ns	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 18 mV to 52 mV; default at power-up
	7		13	µs	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 18 mV to 52 mV; optional select through PMBus
	45		60	µs	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 18 mV to 52 mV; optional select through PMBus
ADM1075-2 ONLY (GAIN = 25)					
Hot Swap Sense Voltage					
Hot Swap Sense Voltage Current Limit, $V_{SENSECL}$	39.2	40	40.8	mV	V_{ISET} > 1.65 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0 V
	49.2	50	50.8	mV	V_{ISET} = 1.25 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0 V
	39.2	40	40.8	mV	V_{ISET} = 1.0 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0 V
	29.2	30	30.8	mV	V_{ISET} = 0.75 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0 V
Constant Power Active	19	20	21.9	mV	V_{ISET} > 1.65 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0.2 V
	9.2	10	11.2	mV	V_{ISET} > 1.65 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0.4 V
	3	4	5.0	mV	V_{ISET} > 1.65 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 1.2 V
Circuit Breaker Offset, V_{CBOS}	1.1	1.5	1.9	mV	Circuit breaker voltage, $V_{CB} = V_{SENSECL} - V_{CBOS}$
Severe Overcurrent					Activates high current gate pull-down
Voltage Threshold, $V_{SENSEOC1}$	46	50	54	mV	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; optional select through PMBus
	56	60	64	mV	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; default at power-up
	76	80	84	mV	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; optional select through PMBus
	86	90	94	mV	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; optional select through PMBus
Response Time					
Glitch Filter Duration	50		200	ns	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 36 mV to 104 mV; optional select through PMBus
	400		900	ns	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 36 mV to 104 mV; default at power-up
	6.2		10.7	µs	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 36 mV to 104 mV; optional select through PMBus
	44		57	µs	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 36 mV to 104 mV; optional select through PMBus

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Total Response Time	180		300	ns	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 36 mV to 104 mV; optional select through PMBus
	610		950	ns	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 36 mV to 104 mV; default at power-up
	7		13	µs	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 36 mV to 104 mV; optional select through PMBus
	45		60	µs	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 36 mV to 104 mV; optional select through PMBus
SOFT START					
SS Pull-Up Current, I_{SS}	−11.5	−10	−8.5	µA	V_{SS} = 0V
Default $V_{SENSECL}$ Limit	0.6	1.25	1.9	mV	When V_{SENSE} reaches this level, I_{SS} is enabled, ramping; V_{SS} = 0 V; ADM1075-1 only (gain = 50)
	1.2	2.5	3.8	mV	When V_{SENSE} reaches this level, I_{SS} is enabled, ramping; V_{SS} = 0 V; ADM1075-2 only (gain = 25)
SS Pull-Down Current		100		µA	V_{SS} = 1 V
TIMER					
Timer Pull-Up Current (POR), $I_{TIMERUPPOR}$	−4	−3	−2	µA	Initial power-on reset; V_{TIMER} = 0.5 V
Timer Pull-Up Current (OC Fault), $I_{TIMERUPFLT}$	−63	−60	−57	µA	Overcurrent fault; 0.05 V ≤ V_{TIMER} ≤ 1 V
Timer Pull-Down Current (Retry), $I_{TIMERDNRT}$	1.7	2	2.3	µA	After a fault when GATE is off; V_{TIMER} = 0.5 V
Timer Retry/OC Fault Current Ratio		3.33		%	Defines the limits of the autoretry duty cycle
Timer Pull-Down Current (Hold), $I_{TIMERDNHOLD}$		100		µA	Holds TIMER at 0 V when inactive; V_{TIMER} = 0.5 V
Timer High Threshold, V_{TIMERH}	0.98	1.0	1.02	V	
Timer Low Threshold, V_{TIMERL}	0.03	0.05	0.07	V	
PLIM					
PLIM Active Threshold	0.08	0.09	0.1	V	V_{ISET} > 1.65 V
Input Current, I_{PLIM}			100	nA	V_{PLIM} ≤ 1 V
Minimum Current Clamp, V_{ICLAMP}	75	100	125	mV	V_{PLIM} = 1.2 V; V_{SENSE_IMIN} = (V_{ICLAMP} ÷ gain) = minimum allowed current control
DRAIN					
DRAIN Voltage at Which $\overline{PWRGD}$ Asserts	1.9	2	2.1	V	I_{DRAIN} ≤ 50 µA
ADC_AUX/ADC_V					
Input Current			100	nA	0 V ≤ V_{ADC} ≤ 1.5 V
$\overline{SHDN}$ PIN					
Input High Voltage, V_{IH}	1.1			V	
Input Low Voltage, V_{IL}			0.8	V	
Glitch Filter		1		µs	
Internal Pull-Up Current		8		µA	Pull-up to VIN
$\overline{RESTART}$ PIN					
Input High Voltage, V_{IH}	1.1			V	
Input Low Voltage, V_{IL}			0.8	V	
Glitch Filter		1		µs	
Internal Pull-Up Current		8		µA	Pull-up to VIN
$\overline{SPLYGD}$ PIN					
Output Low Voltage, V_{OL_LATCH}			0.4	V	I_{SPLYGD} = 1 mA
			1.5	V	I_{SPLYGD} = 5 mA
Leakage Current			100	nA	V_{SPLYGD} ≤ 2 V; $\overline{SPLYGD}$ pin disabled
			1	µA	V_{SPLYGD} ≤ 14 V; $\overline{SPLYGD}$ pin disabled
$\overline{LATCH}$ PIN					
Output Low Voltage, V_{OL_LATCH}			0.4	V	I_{LATCH} = 1 mA
			1.5	V	I_{LATCH} = 5 mA
Leakage Current			100	nA	V_{LATCH} ≤ 2 V; $\overline{LATCH}$ pin disabled
			1	µA	V_{LATCH} ≤ 14 V; $\overline{LATCH}$ pin disabled
GPO1/$\overline{ALERT1}$/CONV PIN					
Output Low Voltage, V_{OL_GPO1}			0.4	V	I_{GPO} = 1 mA
			1.5	V	I_{GPO} = 5 mA

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Leakage Current			100	nA	V_{GPO} ≤ 2 V; GPO disabled
			1	µA	V_{GPO} = 14 V; GPO disabled
Input High Voltage, V_{IH}	1.1			V	Configured as CONV pin
Input Low Voltage, V_{IL}			0.8	V	Configured as CONV pin
Glitch Filter		1		µs	Configured as CONV pin
GPO2/$\overline{\text{ALERT2}}$ PIN					
Output Low Voltage, V_{OL_GPO2}			0.4	V	I_{GPO} = 1 mA
			1.5	V	I_{GPO} = 5 mA
Leakage Current			100	nA	V_{GPO} ≤ 2 V; GPO disabled
			1	µA	V_{GPO} = 14 V; GPO disabled
$\overline{\text{PWRGD}}$ PIN					
Output Low Voltage, V_{OL_PWRGD}			0.4	V	I_{PWRGD} = 1 mA
			1.5	V	I_{PWRGD} = 5 mA
VIN That Guarantees Valid Output	1			V	I_{SINK} = 100 µA; V_{OL_PWRGD} = 0.4 V
Leakage Current			100	nA	V_{PWRGD} ≤ 2 V; $\overline{\text{PWRGD}}$ active
			1	µA	V_{PWRGD} = 14 V; $\overline{\text{PWRGD}}$ active
CURRENT AND VOLTAGE MONITORING					
Current Sense Absolute Error (ADM1075-1)					25 mV input range; 128 sample averaging (unless otherwise noted)
		−0.01	±0.7	%	V_{SENSE} = 25 mV
		0.05	±0.85	%	V_{SENSE} = 20 mV
		0.07	±0.85	%	V_{SENSE} = 20 mV; 16 sample averaging
		0.04	±2.8	%	V_{SENSE} = 20 mV; 1 sample averaging
			±1.0	%	V_{SENSE} = 15 mV
			±1.4	%	V_{SENSE} = 10 mV
			±2.7	%	V_{SENSE} = 5 mV
			±5.9	%	V_{SENSE} = 2.5 mV
Current Sense Absolute Error (ADM1075-2)					50 mV input range; 128 sample averaging (unless otherwise noted)
		−0.03	±0.65	%	V_{SENSE} = 50 mV
		−0.03	±0.7	%	V_{SENSE} = 40 mV
		−0.03	±0.7	%	V_{SENSE} = 40 mV; 16 sample averaging
		−0.04	±1.35	%	V_{SENSE} = 40 mV; 1 sample averaging
			±0.75	%	V_{SENSE} = 30 mV
			±0.9	%	V_{SENSE} = 20 mV
			±1.7	%	V_{SENSE} = 10 mV
			±3.0	%	V_{SENSE} = 5 mV
ADC_V/ADC_AUX Absolute Accuracy	−0.8		+0.8	%	0.6 V ≤ V_{ADC} ≤ 1.5 V
ADC Conversion Time					1 sample of voltage and current; from command received to valid data in register
		191	219	µs	VAUX disabled
		263	301	µs	VAUX enabled
					16 samples of voltage and current averaged; from command received to valid data in register
		2.830	3.243	ms	VAUX disabled
		3.987	4.568	ms	VAUX enabled
					128 samples of voltage and current averaged; from command received to valid data in register
		22.54	25.83	ms	VAUX disabled (default on power-up)
		31.79	36.43	ms	VAUX enabled
Power Multiplication Time		14		µs	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADR PIN					See Table 6
Address Set to 00	0		0.8	V	Connect to VEE
Input Current for Address 00	−40	−22		µA	V_{ADR} = 0 V to 0.8 V
Address Set to 01	135	150	165	kΩ	Resistor to VEE
Address Set to 10	−1		+1	µA	No connect state; maximum leakage current allowed
Address Set to 11	2.1			V	Connect to VCAP
Input Current for Address 11		3	10	µA	V_{ADR} = 2.0 V to VCAP; must not exceed the maximum allowable current draw from VCAP
SERIAL BUS DIGITAL INPUTS (SDAI/SDAO, SCL)					
Input High Voltage, V_{IH}	1.1			V	
Input Low Voltage, V_{IL}			0.8	V	
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 4 mA, SDAO only
Input Leakage, $I_{LEAK-PIN}$	−10		+10	µA	
	−5		+5	µA	Device is not powered
Nominal Bus Voltage, V_{DD}	2.7		5.5	V	3 V to 5 V ±10%
Capacitive Load per Bus Segment, C_{BUS}			400	pF	
Capacitance for SDAI, SDAO, or SCL Pin, C_{PIN}		5		pF	
Input Glitch Filter, t_{SP}	0		50	ns	

SERIAL BUS TIMING

Table 2.

Parameter	Description	Min	Typ	Max	Unit	Test Conditions/Comments
f_{SCLK}	Clock frequency			400	kHz	
t_{BUF}	Bus free time	1.3			µs	
$t_{HD;STA}$	Start hold time	0.6			µs	
$t_{SU;STA}$	Start setup time	0.6			µs	
$t_{SU;STO}$	Stop setup time	0.6			µs	
$t_{HD;DAT}$	SDA[1] hold time	300		900	ns	
$t_{SU;DAT}$	SDA[1] setup time	100			ns	
t_{LOW}	SCL low time	1.3			µs	
t_{HIGH}	SCL high time	0.6			µs	
t_R[2]	SCL, SDA[1] rise time	20		300	ns	
t_F	SCL, SDA[1] fall time	20		300	ns	
t_{OF}	SCL, SDA[1] output fall time	20 + 0.1 × C_{BUS}		250	ns	

[1] SDAI and SDAO tied together.
[2] t_R = ($V_{IL(MAX)}$ − 0.15) to (V_{IH3V3} + 0.15) and t_F = 0.9 V_{DD} to ($V_{IL(MAX)}$ − 0.15); where V_{IH3V3} = 2.1 V, and V_{DD} = 3.3 V.

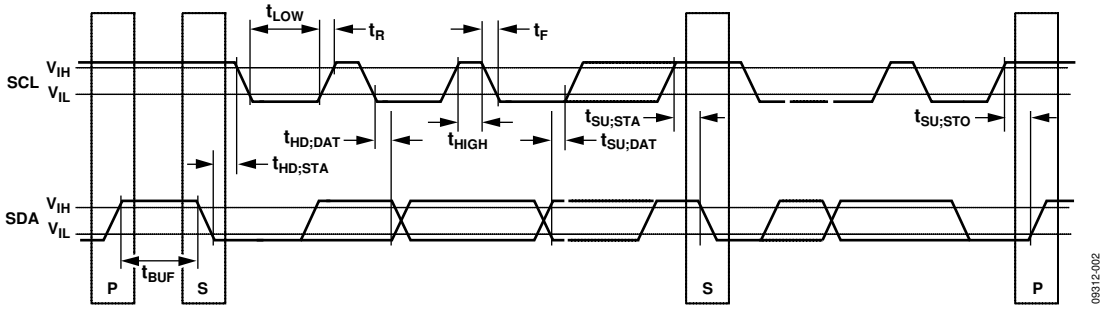

Figure 2. Serial Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN Pin to VEE	−0.3 V to +14 V
UVL Pin to VEE	−0.3 V to +4 V
UVH Pin to VEE	−0.3 V to +4 V
OV Pin to VEE	−0.3 V to +4 V
ADC_V Pin to VEE	−0.3 V to +4 V
ADC_AUX Pin to VEE	−0.3 V to +4 V
SS Pin to VEE	−0.3 V to (VCAP + 0.3 V)
TIMER Pin to VEE	−0.3 V to (VCAP + 0.3 V)
VCAP Pin to VEE	−0.3 V to +4 V
ISET Pin to VEE	−0.3 V to +4 V
$\overline{\text{SPLYGD}}$ Pin to VEE	−0.3 V to +18 V
$\overline{\text{LATCH}}$ Pin to VEE	−0.3 V to +18 V
$\overline{\text{RESTART}}$ Pin to VEE	−0.3 V to +18 V
$\overline{\text{SHDN}}$ Pin to VEE	−0.3 V to +18 V
$\overline{\text{PWRGD}}$ Pin to VEE	−0.3 V to +18 V
DRAIN Pin to VEE	−0.3 V to (VCAP + 0.3 V)
SCL Pin to VEE	−0.3 V to +6.5 V
SDAI Pin to VEE	−0.3 V to +6.5 V
SDAO Pin to VEE	−0.3 V to +6.5 V
ADR Pin to VEE	−0.3 V to (VCAP + 0.3 V)
GPO1/$\overline{\text{ALERT1}}$/CONV Pin to VEE	−0.3 V to +18 V
GPO2/$\overline{\text{ALERT2}}$ Pin to VEE	−0.3 V to +18 V
PLIM Pin to VEE	−0.3 V to +4 V
GATE Pin to VEE	−0.3 V to +18 V
SENSE+ Pin to VEE	−0.3 V to +4 V
SENSE− Pin to VEE	−0.3 V to +0.3 V
VEE to VEE_G	−0.3 V to +0.3 V
Continuous Current into Any Pin	±10 mA
Storage Temperature Range	−65°C to +125°C
Operating Junction Temperature Range	−40°C to +105°C
Lead Temperature, Soldering (10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
28-Lead TSSOP	68	20	°C/W
28-Lead LFCSP	35	4	°C/W

[1] Measured on JEDEC 4-layer board in still air.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

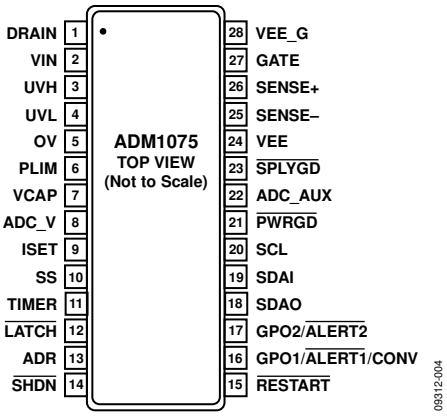

Figure 3. TSSOP Pin Configuration

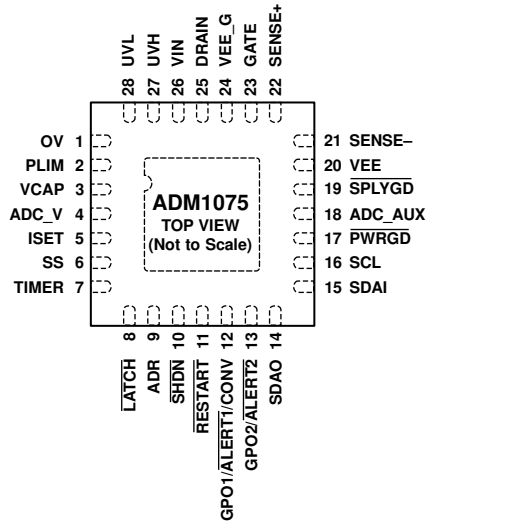

Figure 4. LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	25	DRAIN	Connect to the drain pin of the FET through a resistor. The current in this resistor is used to determine the V_{DS} of the MOSFET. This is used for $\overline{PWRGD}$.
2	26	VIN	Shunt Regulated Positive Supply to Chip. Connect to the positive supply rail via a shunt resistor. A 1 µF capacitor to VEE is recommended on the VIN pin.
3	27	UVH	Undervoltage Rising Input Pin. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect if the supply is under the UVH limit.
4	28	UVL	Undervoltage Falling Input Pin. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect if the supply is under the UVL limit.
5	1	OV	Overvoltage Input Pin. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect if the supply is above the OV limit.
6	2	PLIM	The voltage on this pin is proportional to the V_{DS} voltage of the FET. As the PLIM voltage changes, the current limit automatically adjusts to maintain constant power across the FET.
7	3	VCAP	A capacitor with a value of 1 µF or greater should be placed on this pin to maintain good accuracy. This is an internal regulated supply. This pin can be used as a reference to program the ISET pin voltage.
8	4	ADC_V	This pin is used to read back the input voltage using the internal ADC. It can be connected to the OV string or a separate divider.
9	5	ISET	This pin allows the current limit threshold to be programmed. The default limit is set when this pin is connected directly to VCAP. Alternatively, using a resistor divider from VCAP, the current limit can be adjusted to achieve a user defined sense voltage. An external reference can also be used.
10	6	SS	A capacitor is used on this pin to set the inrush current soft start ramp profile. The voltage on the soft start pin controls the current sense voltage limit, allowing control over the inrush current profile.
11	7	TIMER	Timer Pin. An external capacitor, C_{TIMER}, sets an initial timing cycle delay and a fault delay. The GATE pin turns off when the voltage on the TIMER pin exceeds the upper threshold.
12	8	$\overline{LATCH}$	This pin signals the device latching off after an overcurrent fault. This pin is also used to configure the desired retry scheme. See the Hot Swap Fault Retry section for additional details.
13	9	ADR	PMBus Address Pin. This pin can be tied low, tied to VCAP, left floating, or tied low through a resistor to set four different PMBus addresses.

Pin No.			
TSSOP	LFCSP	Mnemonic	Description
14	10	$\overline{\text{SHDN}}$	Drive this pin low to shut down the gate. Internal weak pull-up to VIN. This pin is also used to configure the desired retry scheme. See the Hot Swap Fault Retry section for additional details.
15	11	$\overline{\text{RESTART}}$	Falling Edge Triggered 10 sec Automatic Restart. The gate remains off for 10 seconds, and then powers back up. Internal weak pull-up to VIN. This pin is also used to configure the desired retry scheme. See the Hot Swap Fault Retry section for additional details.
16	12	GPO1/$\overline{\text{ALERT1}}$ /CONV	General-Purpose Digital Output (GPO1). Alert ($\overline{\text{ALERT1}}$). This pin can be configured to generate an alert signal when one or more fault or warning conditions have been detected. Conversion (CONV). This pin can be used as an input signal to control when a power monitor ADC sampling cycle begins. This pin defaults to indicate FET health mode at power-up. There is no internal pull-up on this pin.
17	13	GPO2/$\overline{\text{ALERT2}}$	General-Purpose Digital Output (GPO2). Alert ($\overline{\text{ALERT2}}$). This pin can be configured to generate an alert signal when one or more fault or warning conditions have been detected. This pin is also used to configure the desired retry scheme. See the Hot Swap Fault Retry section for further details. This pin defaults to indicate a seven-attempt fail at power-up. There is no internal pull-up on this pin.
18	14	SDAO	PMBus Serial Data Output. This is a split version of the SDA for easy use with optocouplers.
19	15	SDAI	PMBus Serial Data Input. This is a split version of the SDA for easy use with optocouplers.
20	16	SCL	PMBus Clock Pin. Open-drain input requires an external resistive pull-up.
21	17	$\overline{\text{PWRGD}}$	Power-Good Signal. This pin is used to indicate that the FET is no longer in the linear region and capacitors are fully charged. See the $\overline{\text{PWRGD}}$ section for details on assert and deassert.
22	18	ADC_AUX	This pin is used to read back a voltage using the internal ADC.
23	19	$\overline{\text{SPLYGD}}$	This pin asserts low when the supply is within the UV and OV limits set by the UVx and OV pins.
24	20	VEE	Chip Ground Pin. Must connect to –VIN rail (lowest potential).
25	21	SENSE–	Negative Current Sense Input Pin. A sense resistor between the SENSE+ pin and the SENSE– pin sets the analog current limit. The hot swap operation controls the external FET gate to maintain the ($V_{SENSE+} - V_{SENSE-}$) sense voltage. This pin also connects to the VEE node, but should be routed separately.
26	22	SENSE+	Positive Current Sense Input Pin. A sense resistor between the SENSE+ pin and the SENSE– pin sets the analog current limit. The hot swap operation controls the external FET gate to maintain the ($V_{SENSE+} - V_{SENSE-}$) sense voltage. This pin also connects to the FET source node.
27	23	GATE	Gate Output Pin. This pin is the gate drive of an external N-channel FET. It is driven by the FET drive controller. The FET drive controller regulates to a maximum load current by regulating the GATE pin. GATE is held low while the supply is out of the voltage range.
28	24	VEE_G	Chip Ground Pin. Must connect to –VIN rail (lowest potential). The PCB layout should configure this pin as the gate pull-down return.
	EPAD	EPAD	Exposed Pad. Solder the exposed pad to the board to improve thermal dissipation. The exposed pad can be connected to VEE.

TYPICAL PERFORMANCE CHARACTERISTICS

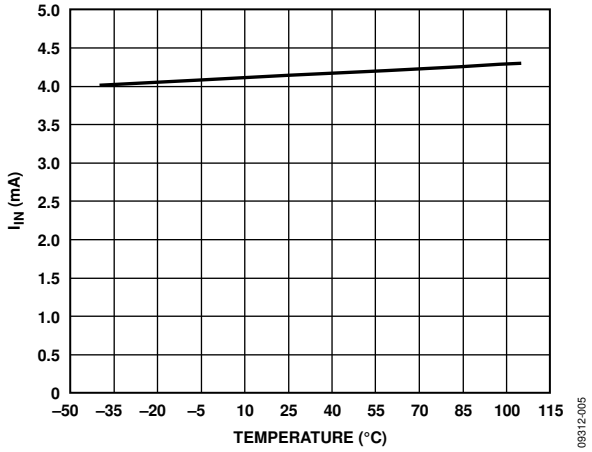

Figure 5. I_{IN} vs. Temperature

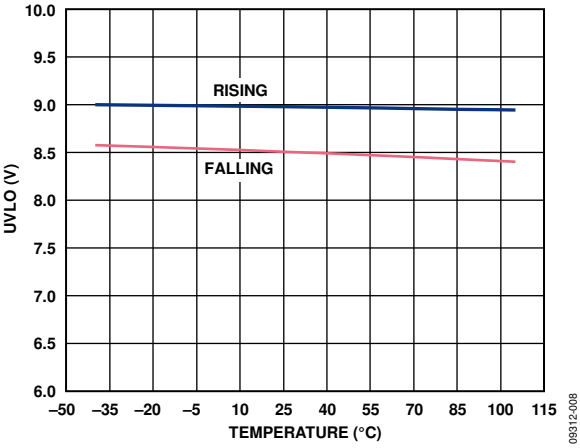

Figure 8. UVLO vs. Temperature

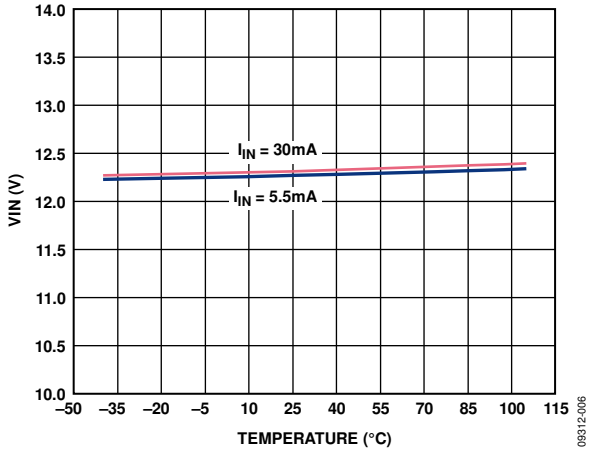

Figure 6. VIN vs. Temperature

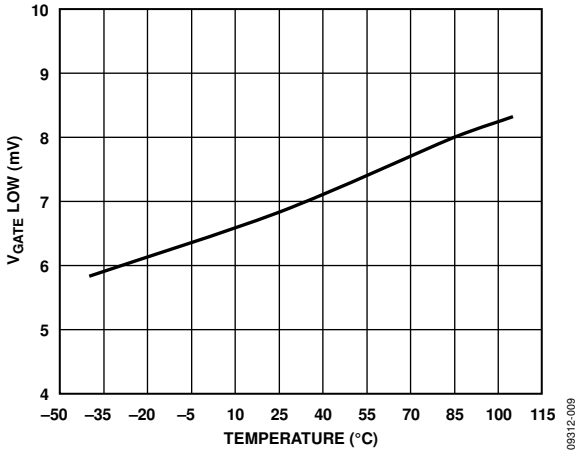

Figure 9. V_{GATE} Low vs. Temperature (I_{GATE} = 100 µA)

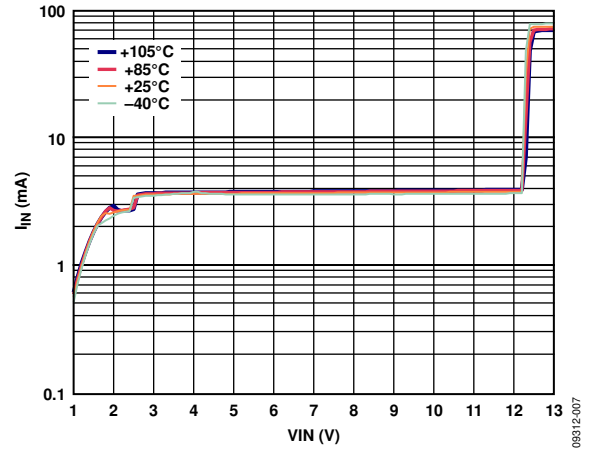

Figure 7. I_{IN} vs. VIN

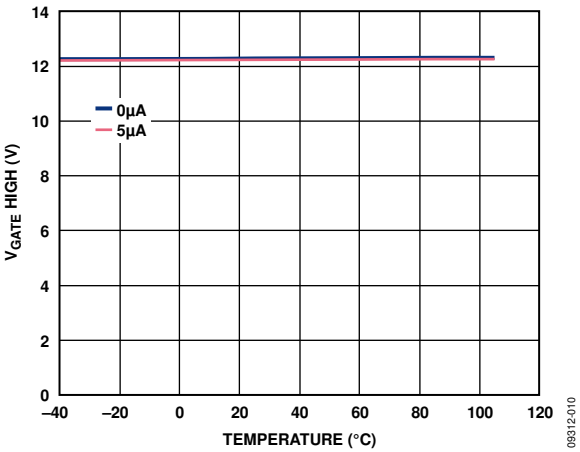

Figure 10. V_{GATE} High vs. Temperature

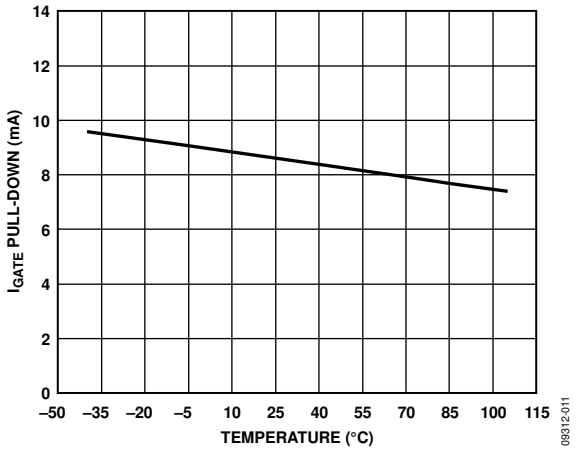

Figure 11. I_{GATE} Pull-Down vs. Temperature

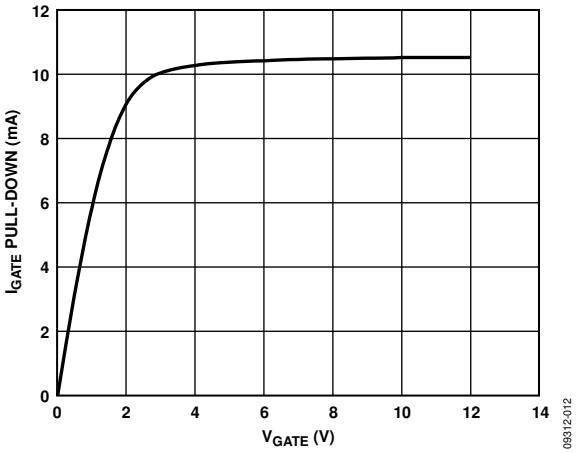

Figure 12. I_{GATE} Pull-Down vs. V_{GATE}

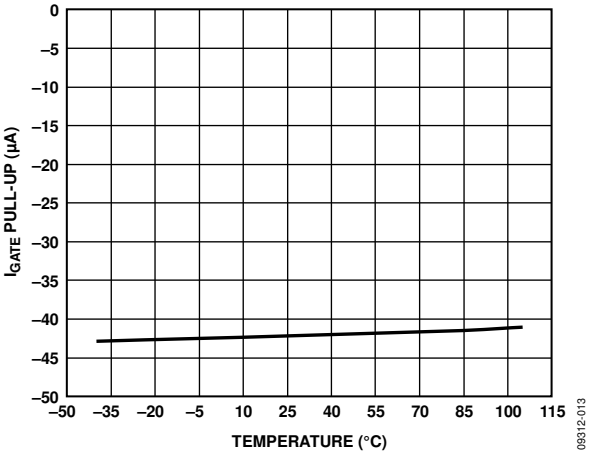

Figure 13. I_{GATE} Pull-Up vs. Temperature

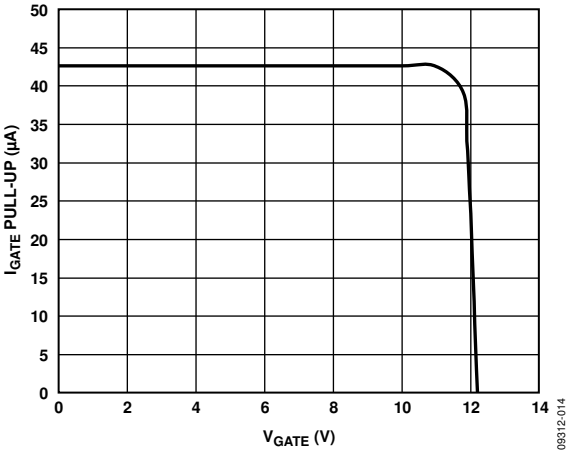

Figure 14. I_{GATE} Pull-Up vs. V_{GATE}

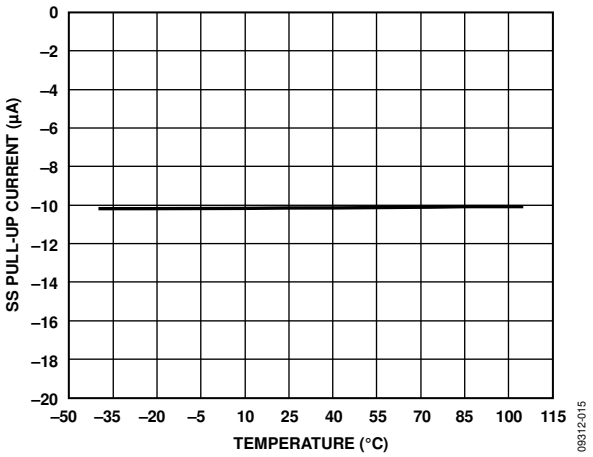

Figure 15. SS Pull-Up Current vs. Temperature

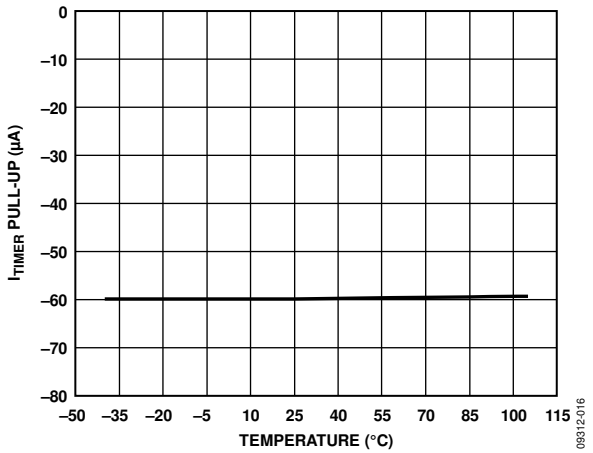

Figure 16. I_{TIMER} Pull-Up vs. Temperature

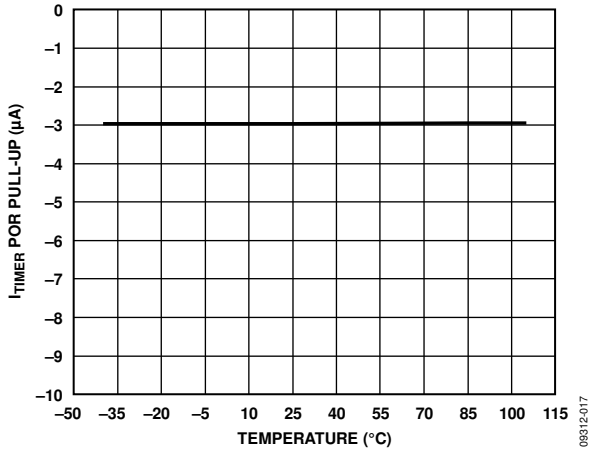

Figure 17. I_{TIMER} POR Pull-Up vs. Temperature

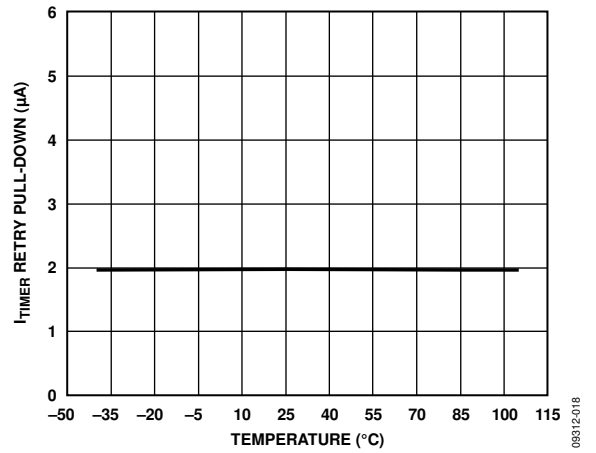

Figure 18. I_{TIMER} Retry Pull-Down vs. Temperature

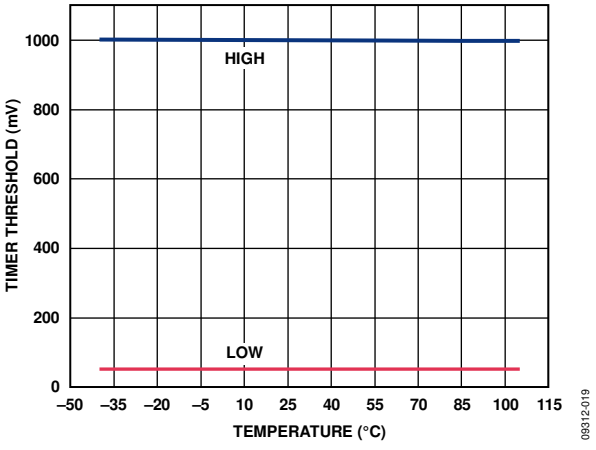

Figure 19. TIMER Threshold vs. Temperature

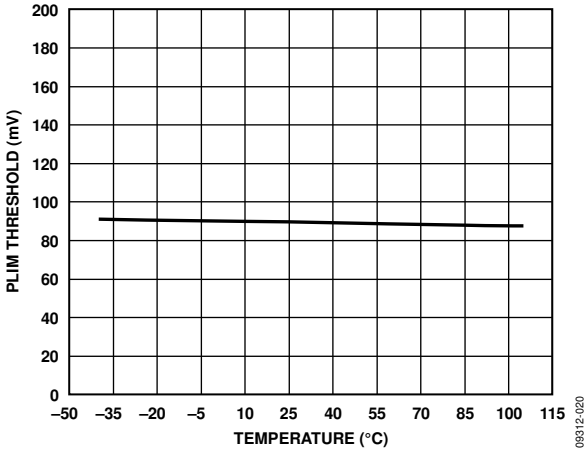

Figure 20. PLIM Threshold vs. Temperature

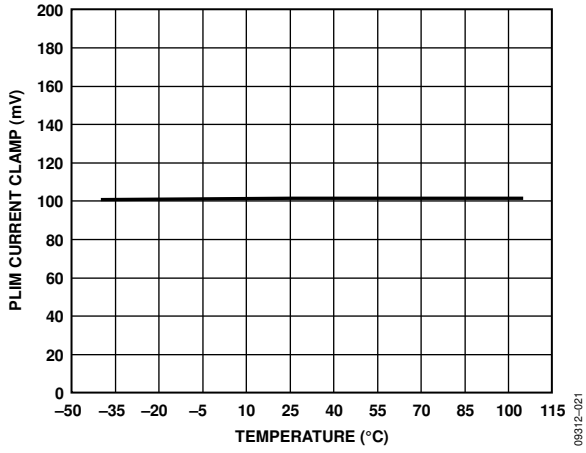

Figure 21. PLIM Current Clamp vs. Temperature

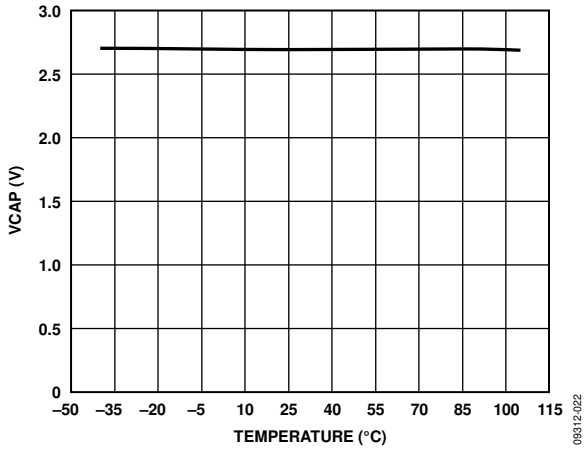

Figure 22. VCAP vs. Temperature (I_{VCAP} = 100 µA)

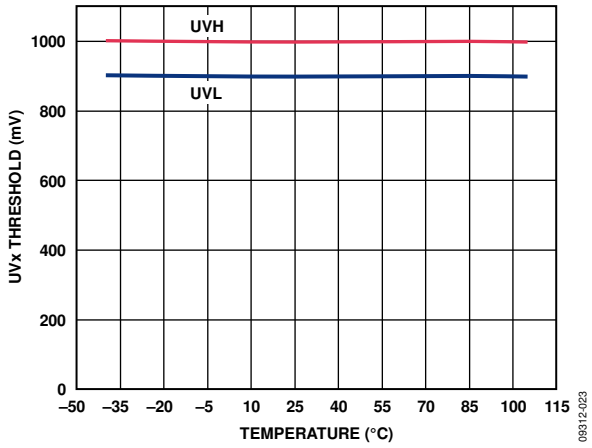

Figure 23. UVx Threshold vs. Temperature

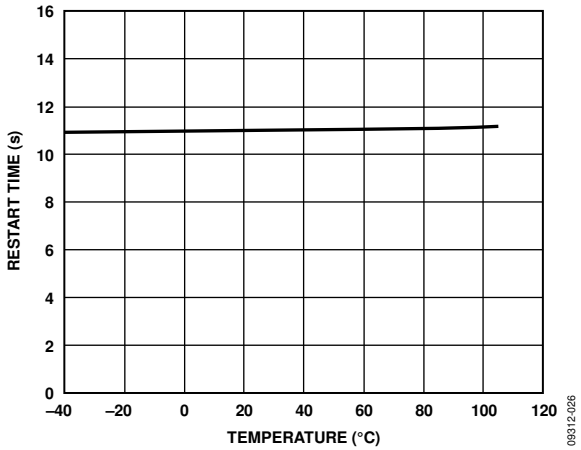

Figure 26. Restart Time vs. Temperature

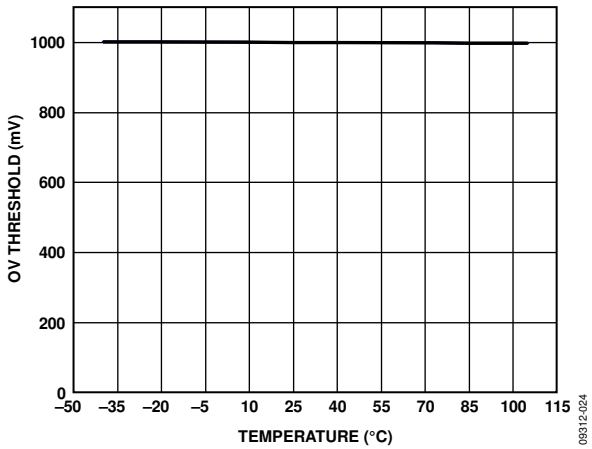

Figure 24. OV Threshold vs. Temperature

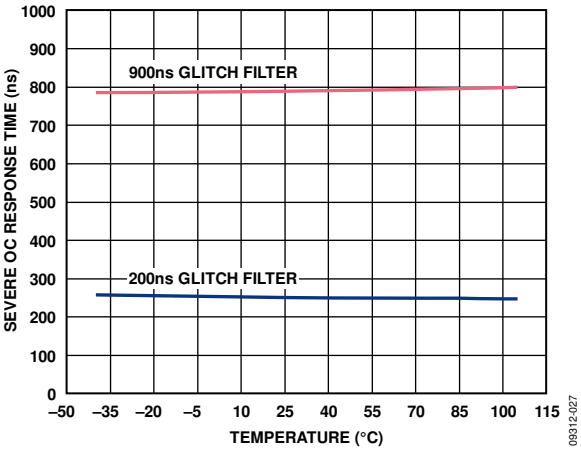

Figure 27. Severe OC Response vs. Temperature

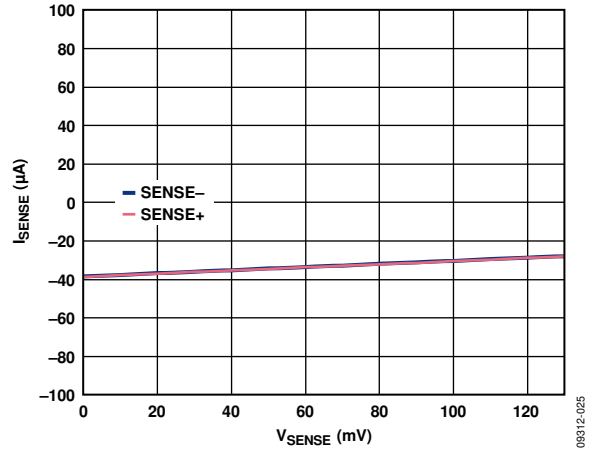

Figure 25. I_{SENSE} vs. V_{SENSE}

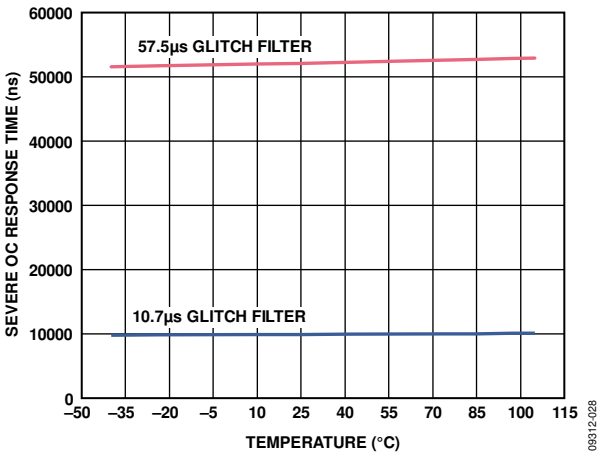

Figure 28. Severe OC Response vs. Temperature

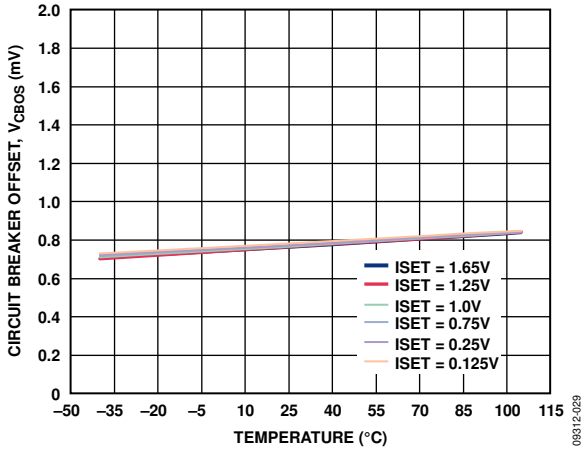

Figure 29. Circuit Breaker Offset vs. Temperature, ADM1075-1

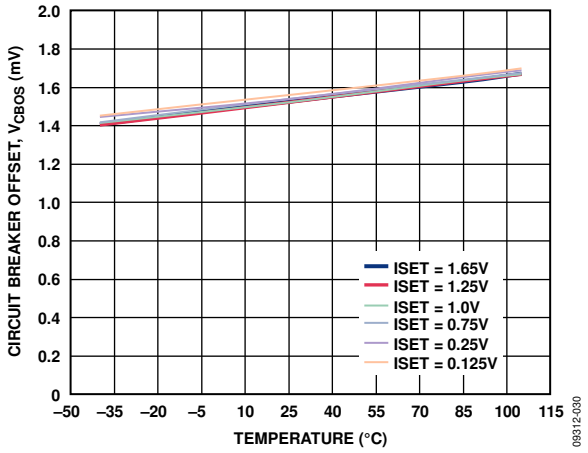

Figure 30. Circuit Breaker Offset vs. Temperature, ADM1075-2

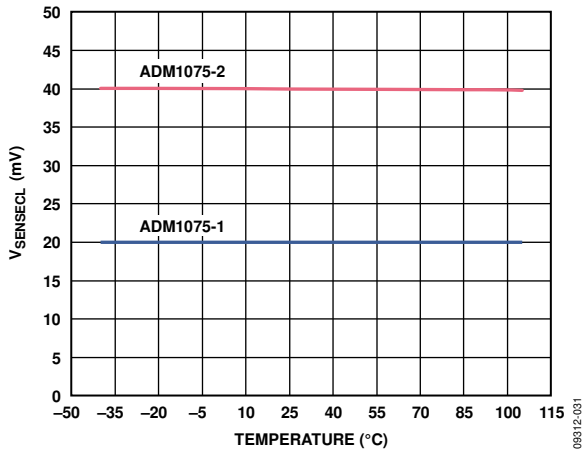

Figure 31. $V_{SENSECL}$ vs. Temperature, ISET = 1.65 V

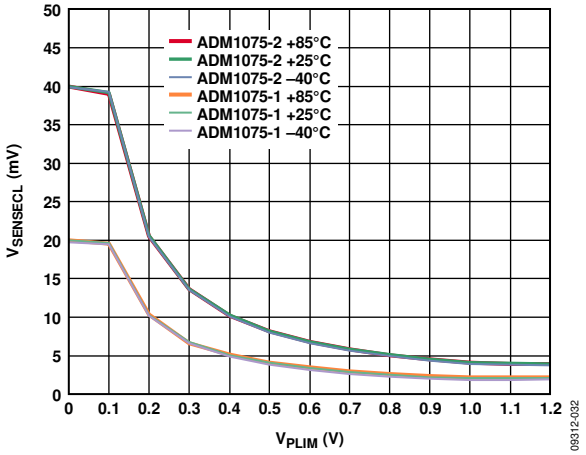

Figure 32. $V_{SENSECL}$ vs. PLIM

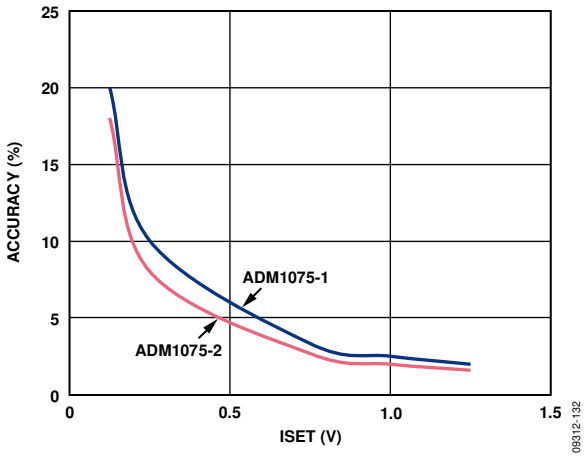

Figure 33. Worst-Case Hot Swap V_{SENSE} Accuracy vs. ISET

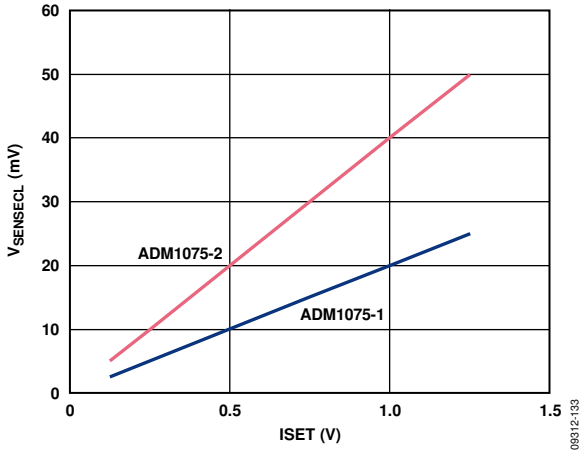

Figure 34. Typical Hot Swap $V_{SENSECL}$ vs. ISET

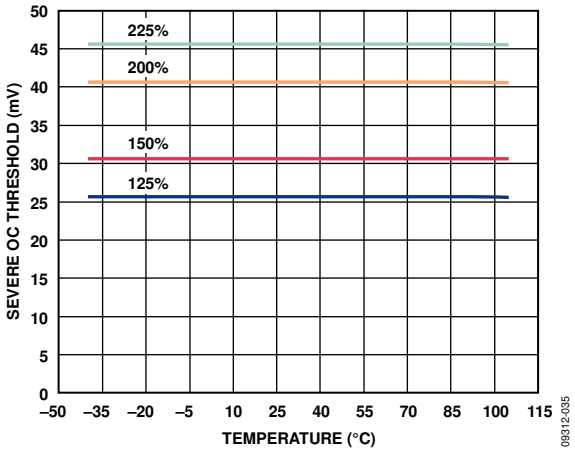

Figure 35. Severe OC Threshold vs. Temperature, ADM1075-1, ISET = 1.65 V

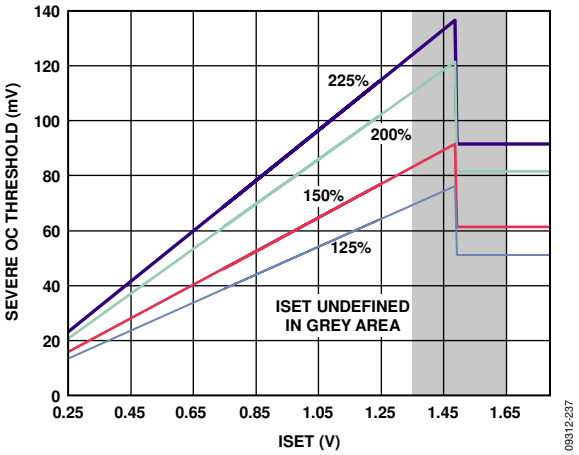

Figure 38. Severe OC Threshold vs. ISET, ADM1075-2

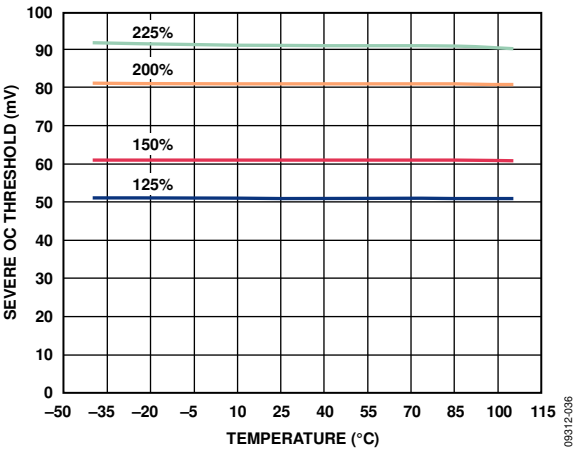

Figure 36. Severe OC Threshold vs. Temperature, ADM1075-2, ISET = 1.65 V

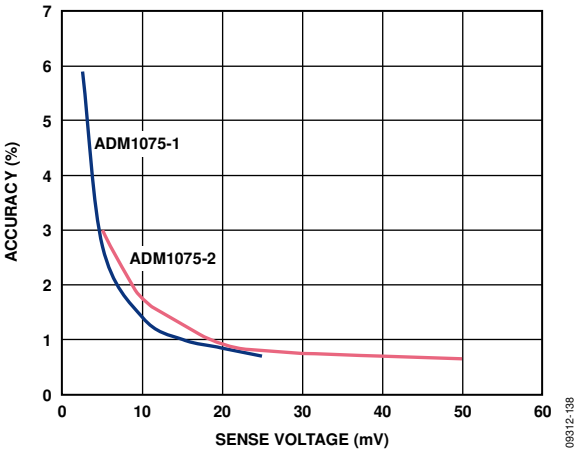

Figure 39. Worst-Case Current Sense Power Monitor Error vs. Current Sense Voltage (V_{SENSE})

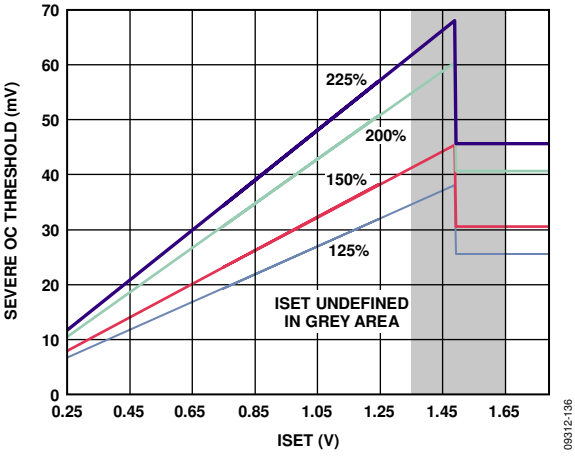

Figure 37. Severe OC Threshold vs. ISET, ADM1075-1

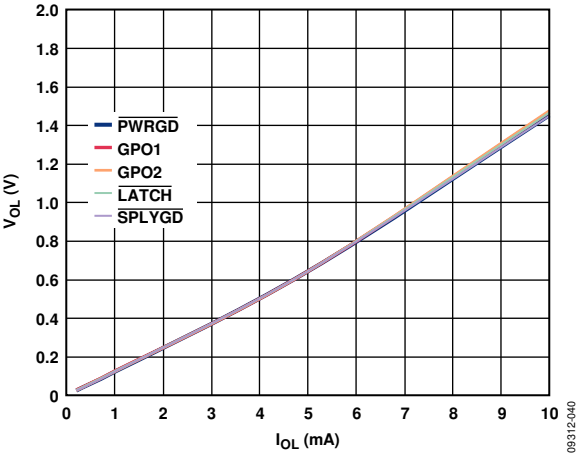

Figure 40. V_{OL} vs. I_{OL}

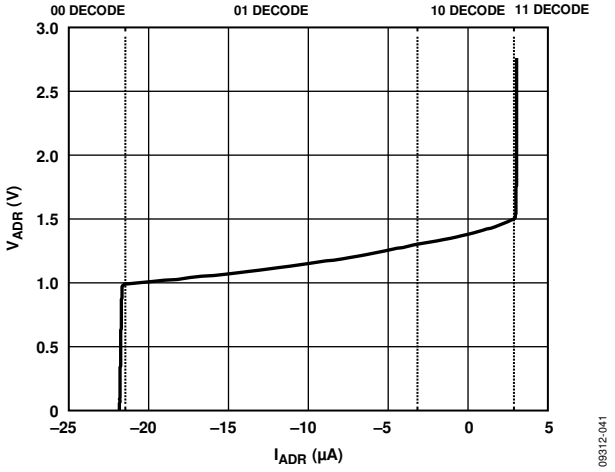

Figure 41. V_{ADR} vs. I_{ADR}

THEORY OF OPERATION

When circuit boards are inserted into a live backplane, discharged supply bypass capacitors draw large transient currents from the backplane power bus as they charge. Such transient currents can cause permanent damage to connector pins, as well as dips on the backplane supply that can reset other boards in the system.

The ADM1075 is intended to control the powering on and off of a board in a controlled manner, allowing the board to be removed from, or inserted into, a live backplane by protecting it from excess currents. The ADM1075 can reside either on the backplane or on the removable board.

A minimal load current requirement is assumed when charging the load capacitance. If the load current is too large relative to the regulation current, it may not be possible to charge the load capacitance. The $\overline{\text{PWRGD}}$ pin can be used to disable the load until the load capacitance is fully charged.

POWERING THE ADM1075

The ADM1075 typically operates from a negative supply of −35 V to −80 V and can tolerate transient voltages of up to −200 V. The VIN pin is a positive supply pin with respect to chip ground. It is a current-driven supply and is shunt regulated to 12 V internally. It should be connected to the most positive supply terminal (usually −48 V RTN or 0 V) through a dropper resistor. The resistor should be chosen such that it always supplies enough current to overcome the maximum quiescent supply current of the chip while not exceeding the maximum allowable shunt current. After the system supply range has been established, an appropriate value for the dropper resistor can be calculated.

$$R_{SHUNT\_MIN} = \frac{V_{IN\_MAX} - V_{SHUNT\_MIN}}{I_{SHUNT\_MAX}}$$

$$R_{SHUNT\_MAX} = \frac{V_{IN\_MIN} - V_{SHUNT\_MAX}}{I_{SHUNT\_MIN}}$$

where:

V_{IN_MIN} and V_{IN_MAX} are the supply voltage extremes (that is, 35 V, 80 V).

V_{SHUNT_MIN} and V_{SHUNT_MAX} are the shunt regulator voltage data sheet specifications (see Table 1).

I_{SHUNT_MIN} is the maximum quiescent supply current (minimum shunt current).

I_{SHUNT_MAX} is the maximum shunt input current.

I_{SHUNT_MAX} can be calculated based on the maximum ambient temperature ($T_{A(MAX)}$) in the application, the maximum junction temperature ($T_{J(MAX)}$ = 105°C), and the θ_{JA} value of the package from Table 4. Worst-case internal power is at $VIN_{(MAX)}$ from Table 1.

$$I_{SHUNT\_MAX} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA} \times VIN_{(MAX)}}$$

For example, the maximum shunt current with a TSSOP device at 80°C maximum ambient can be calculated as

$$I_{SHUNT\_MAX} = \frac{105°C - 80°C}{68°C/W \times 13\ V} = 28\ mA$$

Tolerance of supplies and resistors should also be accounted for to ensure that the shunt current is always within the desired range.

Care must be taken to ensure that the power rating of the shunt resistor is sufficient. The power may be as high as 2 W at extreme supply conditions. Multiple shunt resistors can be used in series or in parallel to share power between resistors.

$$P_{R\_SHUNT} = VI = (V_{IN\_MAX} - V_{SHUNT\_MIN}) \times I_{MAX}$$

where:

$$I_{MAX} = \frac{V_{IN\_MAX} - V_{SHUNT\_MIN}}{R_{SHUNT}}$$

The power dissipation in the shunt resistor can be saved if a suitable voltage rail is available to power the chip directly. This voltage rail must be well regulated to ensure that it is always greater than the UVLO threshold but less than the minimum shunt regulation voltage. The power directly without shunt specification in Table 1 shows the limits this voltage rail must meet. Note that this voltage is referenced to VEE.

The VIN pin provides the majority of the bias current for the device. The remainder of the current needed to control the gate drive and to best regulate the V_{GS} voltage is supplied by the SENSE± pins. The VEE and SENSE− pins are connected to the same voltage rail, although through separate traces to prevent accuracy loss in the sense voltage measurement (see Figure 42).

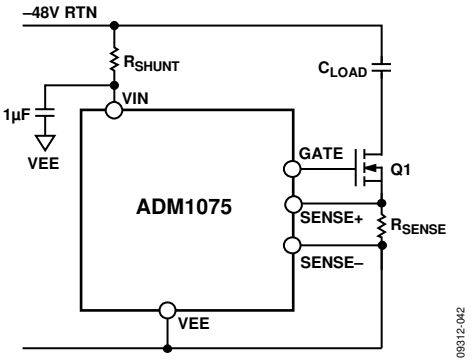

Figure 42. Powering the ADM1075

The available shunt current range should be wide enough to accommodate most telecommunication input voltage ranges. In an application where a wider input voltage range is possible, some external circuitry may be required to meet the shunt regulation current specifications. The applications diagram in Figure 43 shows an example of such a circuit, using a Zener diode and a bipolar junction transistor (BJT) device as an external pre-regulator on the −48 V supply. This ensures that the shunt regulation current is always within specification even at the extremes of supply voltage.

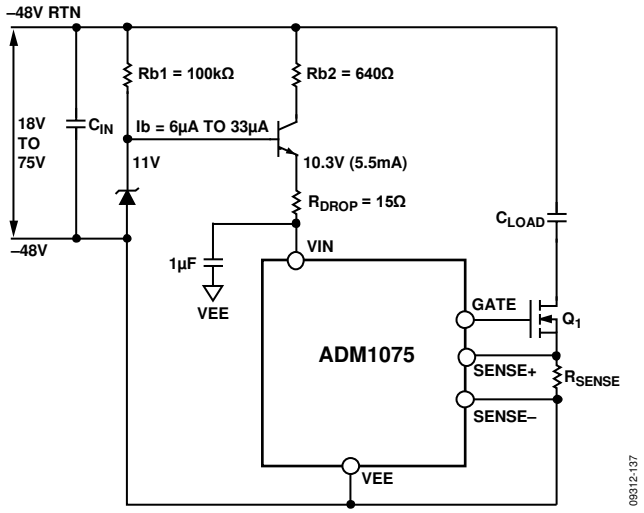

Figure 43. Wide Input Supply Range

CURRENT SENSE INPUTS

The load current is monitored by measuring the voltage drop across an external sense resistor, R_{SENSE}. An internal current sense amplifier provides a gain of 25 or 50 (depending on the model) to the voltage drop detected across R_{SENSE}. The result is compared to an internal reference and detects when an overcurrent condition occurs.

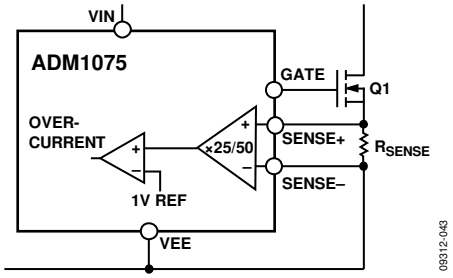

Figure 44. Hot-Swap Current Sense Amplifier

The SENSE± inputs can be connected to multiple parallel sense resistors, which can affect the voltage drop detected by the ADM1075. The current flowing through the sense resistors creates an offset, resulting in reduced accuracy. To achieve better accuracy, averaging resistors should be used to sum the sense nodes of each sense resistor, as shown in Figure 45. The typical value for the averaging resistors is 10 Ω. The value of the averaging resistors is chosen to be much greater than the trace resistance between the sense resistor terminals and the inputs to the ADM1075. This greatly reduces the effects of differences in the trace resistances.

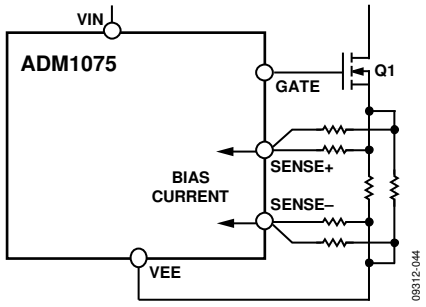

Figure 45. Connection of Multiple Sense Resistors to SENSE± Pins

CURRENT LIMIT REFERENCE

The current limit reference voltage determines the load current level to which the ADM1075 limits the current during an overcurrent event. This is the reference voltage to which the gained up current sense voltage is compared to determine if the limit is reached. This current limit voltage, shown in Figure 46, is then converted to a gate current to regulate the GATE pin.

$$I_{GATE} = V_{CURR\_LIM} \times g_m$$

where g_m, the gate transconductance, = 660 µS.

An internal current limit reference selector block continuously compares the ISET, soft start, and foldback (derived from PLIM) voltages, determines which is the lowest at any given time, and uses it as the current limit reference. This ensures that the programmed current limit, ISET, is used in normal operation and the soft start and foldback features reduce the current limit when required.

The foldback and soft start voltages change during different stages of operation and are clamped to a lower level of 100 mV (typical) to prevent zero current flow due to the current limit being too low.

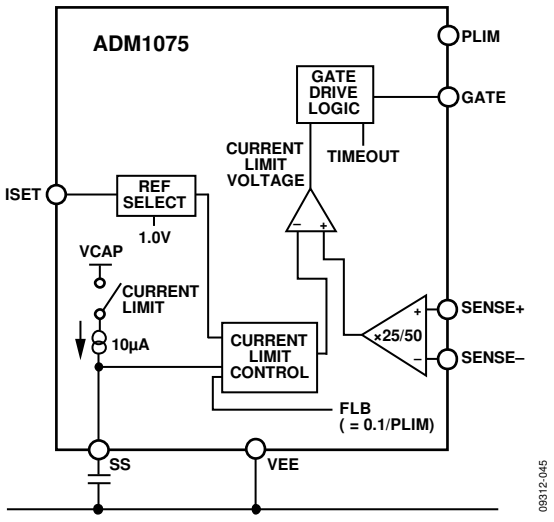

Figure 46. Current Limit Reference Selection

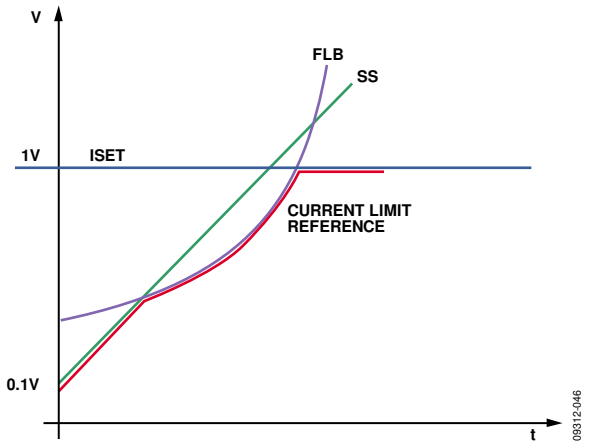

Figure 47. Interaction of Soft Start, Foldback, and ISET Current Limits

SETTING THE CURRENT LIMIT (ISET)

The maximum current limit is partially determined by selecting a sense resistor to match the current sense voltage limit on the controller for the desired load current. However, as currents become larger, the sense resistor value becomes smaller and resolution can be difficult to achieve when selecting the appropriate sense resistor value. The ADM1075 provides an adjustable sense voltage limit to deal with this issue. The device allows the user to program the required current sense voltage limit from 15 mV to 25 mV for the ADM1075-1 and from 30 mV to 50 mV for the ADM1075-2.

The default value of 20 mV/40 mV is achieved by connecting the ISET pin directly to the VCAP pin (VCAP > 1.65 V ISET reference select threshold). This configures the device to use an internal 1 V reference, which equates to 20 mV/40 mV at the sense inputs (see Figure 48(a)).

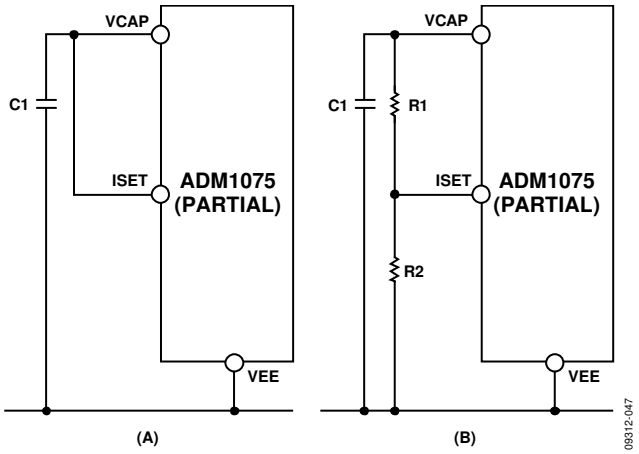

Figure 48. (a) Fixed 20 mV/40 mV Current Sense Limit
(b) Adjustable 15 mV to 50 mV Current Sense Limit

To set the sense voltage in the 15 mV to 50 mV range, a resistor divider is used to apply a reference voltage to the ISET pin (see Figure 48(b)). The VCAP pin has a 2.7 V internally generated voltage that can be used to set a voltage at the ISET pin.

Assuming V_{ISET} equals the voltage on the ISET pin, the resistor divider should be sized to set the ISET voltage as follows:

$V_{ISET} = (V_{SENSE} \times 50)$ for ADM1075-1 or

$V_{ISET} = (V_{SENSE} \times 25)$ for ADM1075-2

where V_{SENSE} is the sense voltage limit. The VCAP rail can also be used as the pull-up supply for setting the I^2C address. The VCAP pin should not be used for any other purpose. To guarantee accuracy specifications, care must be taken to not load the VCAP pin by more than 100 µA.

SOFT START

A capacitor connected to the SS pin determines the inrush current profile. Before the FET is enabled, the output voltage of the current limit reference selector block is clamped at 100 mV. This, in turn, holds the current limit reference at approximately 2 mV for the ADM1075-1 or 4 mV for the ADM1075-2. When the FET is requested to turn on, the SS pin is held at ground until the voltage between the SENSE+ and SENSE− pins (V_{SENSE}) reaches the circuit breaker voltage, V_{CB}.

$$V_{CB} = V_{SENSECL} - V_{CBOS}$$

When the load current generates a sense voltage equal to V_{CB}, a 10 µA current source is enabled, which charges the SS capacitor and results in a linear ramping voltage on the SS pin. The current limit reference also ramps up accordingly, allowing the regulated load current to ramp up, while avoiding sudden transients during power-up. The SS capacitor value is given by

$$C_{SS} = \frac{I_{SS} \times t}{V_{ISET}}$$

where I_{SS} = 10 µA, and t is the SS ramp time.

For example, a 10 nF capacitor gives a soft start time of 1 ms.

Note that the SS voltage may intersect with the PLIM or foldback (FLB) voltage, and the current limit reference may change to follow PLIM (see Figure 47). This has minimal impact on startup because the output voltage rises at a similar rate to SS.

CONSTANT POWER FOLDBACK (PLIM)

Foldback is a method that actively reduces the current limit as the voltage drop across the FET increases. It keeps the power across the FET below the programmed value during power-up, overcurrent, or short-circuit events. This allows a smaller FET to be used, resulting in significant cost savings. The foldback method employed is a constant power foldback scheme, meaning power in the FET is held constant regardless of the V_{DS} of the FET. This simplifies the task of ensuring that the FET is always operating within the SOA region.

The ADM1075 detects the voltage drop across the FET by monitoring the voltage on the drain of the FET (via the PLIM pin). The device relies on the principle that the source of the FET is at the most negative expected supply voltage, and the magnitude of the drain voltage is relative to that of the V_{DS} of the FET. Using a resistor divider from the drain of the FET to

the PLIM pin, the relationship of V_{DS} to V_{PLIM} can be controlled. The foldback voltage, V_{FLB}, is the input to the current limit reference selector block and is defined as

$$V_{FLB} = 0.1/V_{PLIM}$$

The resistor divider should be designed to generate a V_{FLB} voltage equal to I_{SET} when the V_{DS} of the FET (and thus V_{PLIM}) rises above the desired power level. If I_{SET} = 1 V, V_{PLIM} needs to be 0.1 V at the point where constant power takes over (V_{FLB} = I_{SET}). For example, to generate a 200 W constant power limit at 10 A current limit, the maximum V_{DS} is required to be 20 V at the current limit. Therefore, the resistor divider must be 200:1 to generate a 0.1 V PLIM voltage at V_{DS} = 20 V. As V_{PLIM} continues to increase, the current limit reference follows V_{FLB} because it is now the lowest voltage input to the current limit reference selector block. This results in a reduction of the current limit, and, therefore, the regulated load current. To prevent complete current flow restriction, a clamp becomes active when the current limit reference reaches 100 mV. The current limit cannot drop below this level. This 200 W constant power example is illustrated in terms of FET SOA and real scope plots in Figure 49 and Figure 50.

When V_{FLB} has control of the current limit reference, the regulation current through the FET is

$$I_D = V_{FLB}/(Gain \times R_{SENSE})$$

where I_D is the external FET drain current, and *Gain* is the sense amplifier gain.

$$I_D = 0.1/(V_{PLIM} \times Gain \times R_{SENSE})$$

$$I_D = 0.1/(V_{DS} \times D \times Gain \times R_{SENSE})$$

where *D* is the resistor divider factor on PLIM.

Therefore, the FET power is calculated as

$$P_{FET} = I_D \times V_{DS} = 0.1/(D \times Gain \times R_{SENSE})$$

Because P_{FET} does not have any dependency on V_{DS}, it remains constant. Therefore, the FET power for a given system can be set by adjusting the divider (D) driving the PLIM pin.

The limits to the constant power system are when $V_{FLB} > I_{SET}$ (or 1 V if $V_{ISET} > V_{ISETRSTH}$) or when $V_{FLB} < 100$ mV (100 mV max clamp on V_{CLREF}). With an I_{SET} voltage of 1 V, this gives a 10:1 foldback current range.

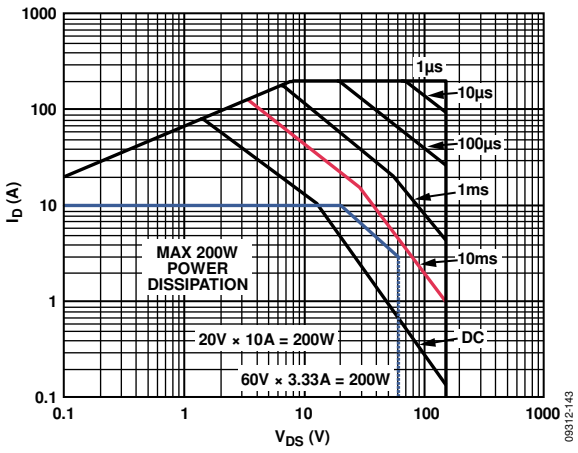

Figure 49. FET SOA

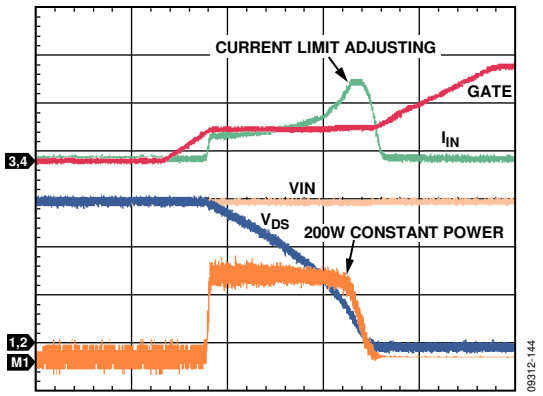

Figure 50. 200 W Constant Power Scope Plot, CH1 = VIN; CH2 = V_{DS}; CH3 = GATE; CH4 = System Current; M1 = FET Power

TIMER

The TIMER pin handles several timing functions with an external capacitor, C_{TIMER}. There are two comparator thresholds: V_{TIMERH} (1.0 V) and V_{TIMERL} (0.05 V). The four timing current sources are a 3 µA pull-up, a 60 µA pull-up, a 2 µA pull-down, and a 100 µA pull-down.

These current and voltage levels, together with the value of C_{TIMER} chosen by the user, determine the initial timing cycle time, the fault current limit time, and the hot swap retry duty cycle. The TIMER capacitor value is determined using the following equation:

$$C_{TIMER} = (t_{ON} \times 60\ \mu A)/V_{TIMERH}$$

where t_{ON} is the time that the FET is allowed to spend in regulation. The choice of C_{TIMER} is based on matching this time with the SOA requirements of the FET. Foldback can be used here to simplify selection.

When V_{IN} is connected to the backplane supply, the internal supply of the ADM1075 must be charged up. A very short time later when the internal supply is fully up and above the undervoltage lockout voltage (UVLO), the device comes out of reset. During this first short reset period, the GATE and TIMER pins are both held low. The ADM1075 then goes through an initial

timing cycle. The TIMER pin is pulled up with 3 µA. When the TIMER reaches the V_{TIMERH} threshold (1.0 V), the first portion of the initial cycle is complete. The 100 µA current source then pulls down the TIMER pin until it reaches V_{TIMERL} (0.05 V). The initial cycle duration is related to C_{TIMER} by the following equation:

$$t_{INITIAL} = \frac{V_{TIMERH} \times C_{TIMER}}{3\,\mu A} + \frac{(V_{TIMERH} - V_{TIMERL}) \times C_{TIMER}}{100\,\mu A}$$

For example, a 470 nF capacitor results in a power-up delay of approximately 160 ms. Provided the UV and OV detectors are inactive when the initial timing cycle terminates, the device is ready to start a hot swap operation.

When the voltage across the sense resistor reaches the circuit breaker trip voltage, V_{CB}, the 60 µA timer pull-up current is activated, and the gate begins to regulate the current at the current limit. This initiates a ramp-up on the TIMER pin. If the sense voltage falls below this circuit breaker trip voltage before the TIMER pin reaches V_{TIMERH} (1.0 V), the 60 µA pull-up is disabled, and the 2 µA pull-down is enabled.

The circuit breaker trip voltage is not the same as the hot swap sense voltage current limit. There is a small circuit breaker offset, V_{CBOS}, which means that the timer actually starts a short time before the current reaches the defined current limit.

However, if the overcurrent condition is continuous and the sense voltage remains above the circuit breaker trip voltage, the 60 µA pull-up remains active and the FET remains in regulation. This allows the TIMER pin to reach V_{TIMERH} and initiate the GATE shutdown. The $\overline{\text{LATCH}}$ pin is pulled low immediately.

In latch-off mode, the TIMER pin is switched to the 2 µA pull-down when it reaches the V_{TIMERH} threshold. The $\overline{\text{LATCH}}$ pin remains low. While the TIMER pin is being pulled down, the hot swap controller is kept off and cannot be turned back on.

When the voltage on the TIMER pin goes below the V_{TIMERL} threshold, the hot swap controller can be reenabled by toggling the UVx pin or by using the PMBus OPERATION command to toggle the ON bit from on to off and then on again.

SETTING A LINEAR OUTPUT VOLTAGE RAMP AT POWER-UP

The ADM1075 standard method of operation is to control a constant power in the MOSFET during power-up into the load. This can result in non-linear output voltage ramps and often requires many retry attempts to charge larger load capacitances, due to MOSFET SOA limitations. However, there is a way to configure a single linear voltage ramp on the output which allows a constant inrush current to be maintained. For a typical power-up using constant power, as the output voltage increases in magnitude, the controlled current also increases to maintain a constant power in the pass MOSFET. This can be a challenge for maintaining MOSFET SOA, where higher drain currents limit energy transfer more than lower currents. However, if the output voltage is programmed to result in a linear ramp, the inrush into the load capacitance remains somewhat constant. This can have the advantage of setting very low inrush currents where required by combination of large output capacitance and FET SOA limitations.

The object of such a design is to allow a linear monotonic power-up event without the restrictions of the system fault timer. To achieve this, a power-up ramp is set so that the inrush is low enough not to reach the circuit breaker current limit, or constant power current limit. This allows power-up to continue without the timer running. When using this method, take separate care to ensure the power in the MOSFET during this event meets the SOA requirements. The components labeled R_{GD}, C_{GD} and C_G on the gate pin in Figure 51 show the required extra components.

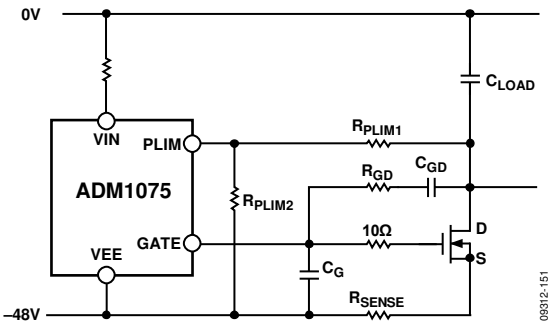

Figure 51. Required Extra Components

To ensure the inrush current does not approach or exceed the active current limit level, the output voltage ramp can be set by selecting the appropriate value for C_{GD} as follows:

$$C_{GD} = (I_{GATEUP}/I_{INRUSH}) \times C_{LOAD}$$

where I_{GATEUP} is the gate pull-up current specified.

Add margin and tolerance as necessary to ensure a robust design. Subtract any parasitic C_{GD} of the MOSFETS from the total to determine the additional external capacitance required.

The power-up ramp time can now be approximated by:

$$t_{RAMP} = (V_{IN} \times C_{LOAD})/I_{INRUSH}$$

Check the SOA of the MOSFET for conditions and the duration of this power-up ramp.

R_{GD} and C_G are used to limit the impact of sudden transients on the MOSFET Drain pin being coupled to the GATE pin through C_{GD}. R_G is chosen such that I_{GATEUP} has minimal voltage drop impact. Typical values would be 1 K. As a rule, C_G is recommended to be about 10× the value of C_{GD}, to a maximum of 470 nF. C_G must be minimized and must not exceed 470 nF to avoid slowing down gate shutdown in response to severe overcurrent events. This capacitance results in slowing down the gate ramp through V_{TH} and therefore the trans-conductance current ramp. This delay must also be considered when checking SOA during power-up into a fault. When using this method, always remove the SS cap, and TIMER can be minimized to provide a simple fault filtering solution.