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### FEATURES

- Complete supervisory and sequencing solution for up to 8 supplies**
  - 16-event deep black box nonvolatile fault recording**
  - 8 supply fault detectors enable supervision of supplies to <0.5% accuracy at all voltages at 25°C**
  - <1.0% accuracy across all voltages and temperatures**
  - 4 selectable input attenuators allow supervision of supplies to 14.4 V on VH and 6 V on VP1 to VP3 (VPx)**
  - 4 dual-function inputs, VX1 to VX4 (VXx)**
    - High impedance input to supply fault detector with thresholds between 0.573 V and 1.375 V
    - General-purpose logic input
  - 8 programmable driver outputs, PDO1 to PDO8 (PDOx)**
    - Open-collector with external pull-up
    - Push/pull output, driven to VDDCAP or VPx
    - Open-collector with weak pull-up to VDDCAP or VPx
    - Internally charge-pumped high drive for use with external NFET (PDO1 to PDO6 only)
  - SE implements state machine control of PDO outputs**
    - State changes conditional on input events
    - Enables complex control of boards
    - Power-up and power-down sequence control
    - Fault event handling
    - Interrupt generation on warnings
    - Watchdog function can be integrated in SE
    - Program software control of sequencing through SMBus
  - Complete voltage margining solution for 4 voltage rails**
  - 4 voltage output 8-bit DACs (0.300 V to 1.551 V) allow voltage adjustment via dc-to-dc converter trim/feedback node**
  - 12-bit ADC for readback of all supervised voltages**
  - Reference input (REFIN) has 2 input options**
    - Driven directly from 2.048 V ( $\pm 0.25\%$ ) REFOUT pin
    - More accurate external reference for improved ADC performance
  - Device powered by the highest of VPx, VH for improved redundancy**
  - User EEPROM: 256 bytes**
  - Industry-standard 2-wire bus interface (SMBus)**
  - Guaranteed PDO low with VH, VPx = 1.2 V**
  - Available in 32-lead LQFP and 40-lead LFCSP packages**
- ### APPLICATIONS
- Central office systems
  - Servers/routers
  - Multivoltage system line cards
  - DSP/FPGA supply sequencing
  - In-circuit testing of margined supplies

Rev. B

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### FUNCTIONAL BLOCK DIAGRAM

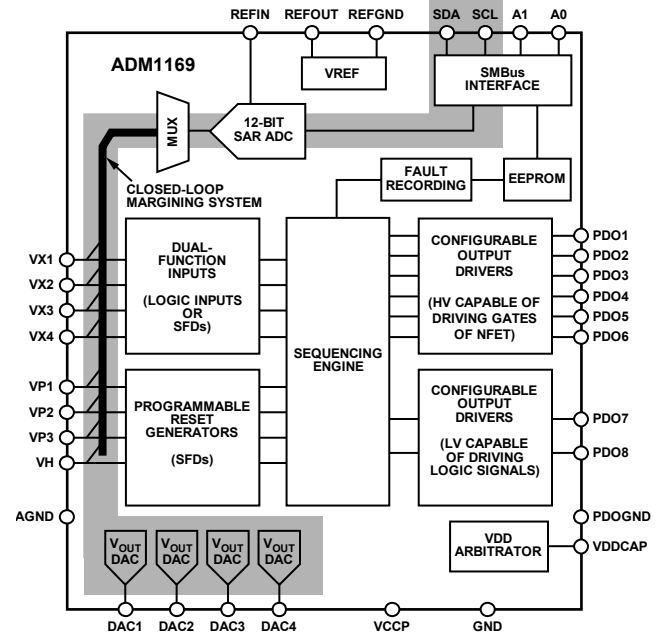


Figure 1.

### GENERAL DESCRIPTION

The **ADM1169** Super Sequencer® is a configurable supervisory/sequencing device that offers a single-chip solution for supply monitoring and sequencing in multiple supply systems. In addition to these functions, the **ADM1169** integrates a 12-bit ADC and four 8-bit voltage output DACs. These circuits can be used to implement a closed-loop margining system that enables supply adjustment by altering either the feedback node or reference of a dc-to-dc converter using the DAC outputs.

Supply margining can be performed with a minimum of external components. The margining loop can be used for in-circuit testing of a board during production (for example, to verify board functionality at  $-5\%$  of nominal supplies), or it can be used dynamically to accurately control the output voltage of a dc-to-dc converter.

For more information about the **ADM1169** register map, refer to the [AN-721 Application Note](#).

# ADM1169\* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

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## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- ADM1169 Evaluation Board

## DOCUMENTATION

### Application Notes

- AN-0973: Erasing and Programming the Sequencing Engine EEPROM
- AN-0975: Automatic Generation of State Diagrams for the ADM1062 to ADM1069 Using Graphviz
- AN-0997: Ping-Pong Configuration Guide for ADM1062 to ADM1069 Devices
- AN-1001: Checksum Calculations
- AN-1009: Block Erasing, Reading and Writing to the ADM106x EEPROM
- AN-1086: Using an ADM106x in a Hot Swap Application
- AN-721: ADM1068/ADM1069/ADM1168/ADM1169 Configuration Registers
- AN-722: Watchdog Detection Using the ADM106x
- AN-723: Interrupt Generation Using the ADM106x
- AN-780: Monitoring Negative Voltages with the ADM1062 to ADM1069 Super Sequencers
- AN-781: Monitoring Additional Supplies with the ADM1062-ADM1069 Super Sequencers™
- AN-782: Monitoring High Voltages with the ADM1062-ADM1069 Super Sequencers™
- AN-897: ADC Readback Code

### Data Sheet

- ADM1169: Super Sequencer with Margining Control and Nonvolatile Fault Recording Data Sheet

### User Guides

- SuperSequencer Documentation
- UG-404: USB-SDP-CABLEZ Serial Interface Board

## SOFTWARE AND SYSTEMS REQUIREMENTS

- ADMxxxx Common Run-Time
- SuperSequencer Software

## DESIGN RESOURCES

- ADM1169 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all ADM1169 EngineerZone Discussions.

## SAMPLE AND BUY

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## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

Submit feedback for this data sheet.

## TABLE OF CONTENTS

Features .....	1	Sequencing Engine Application Example .....	19
Applications .....	1	Fault and Status Reporting .....	20
Functional Block Diagram .....	1	Nonvolatile Black Box Fault Recording .....	20
General Description .....	1	Black Box Writes with No External Supply .....	21
Revision History .....	2	Voltage Readback .....	22
Detailed Block Diagram .....	3	Supply Supervision with the ADC .....	22
Specifications .....	4	Supply Margining .....	23
Absolute Maximum Ratings .....	7	Overview .....	23
Thermal Resistance .....	7	Open-Loop Supply Margining .....	23
ESD Caution .....	7	Closed-Loop Supply Margining .....	23
Pin Configurations and Function Descriptions .....	8	Writing to the DACs .....	24
Typical Performance Characteristics .....	10	Choosing the Size of the Attenuation Resistor .....	24
Powering the ADM1169 .....	13	DAC Limiting and Other Safety Features .....	24
Slew Rate Consideration .....	13	Applications Diagram .....	25
Inputs .....	14	Communicating with the ADM1169 .....	26
Supply Supervision .....	14	Configuration Download at Power-Up .....	26
Programming the Supply Fault Detectors .....	14	Updating the Configuration .....	26
Input Comparator Hysteresis .....	15	Updating the Sequencing Engine .....	27
Input Glitch Filtering .....	15	Internal Registers .....	27
Supply Supervision with VXx Inputs .....	16	EEPROM .....	27
VXx Pins as Digital Inputs .....	16	Serial Bus Interface .....	28
Outputs .....	17	SMBus Protocols for RAM and EEPROM .....	29
Supply Sequencing Through Configurable Output Drivers .....	17	Write Operations .....	30
Default Output Configuration .....	17	Read Operations .....	31
Sequencing Engine .....	18	Outline Dimensions .....	33
Overview .....	18	Ordering Guide .....	33
Warnings .....	18		
SMBus Jump (Unconditional Jump) .....	18		

## REVISION HISTORY

### 1/15—Rev. A to Rev. B

Changes to Table 4 .....	8
Added Slew Rate Consideration Section .....	13

### 8/13—Rev. 0 to Rev. A

Change to Table 12 .....	28
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### 4/11—Revision 0: Initial Version



## SPECIFICATIONS

V<sub>H</sub> = 3.0 V to 14.4 V,<sup>1</sup> V<sub>Px</sub> = 3.0 V to 6.0 V,<sup>1</sup> T<sub>A</sub> = -40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
<b>POWER SUPPLY ARBITRATION</b>					
V <sub>H</sub> , V <sub>Px</sub>	3.0			V	Minimum supply required on one of V <sub>H</sub> , V <sub>Px</sub>
V <sub>Px</sub>			6.0	V	Maximum VDDCAP = 5.1 V, typical
V <sub>H</sub>			14.4	V	VDDCAP = 4.75 V
VDDCAP	2.7	4.75	5.4	V	Regulated LDO output
C <sub>VDDCAP</sub>	10			μF	Minimum recommended decoupling capacitance
<b>POWER SUPPLY</b>					
Supply Current, I <sub>VH</sub> , I <sub>VPx</sub>		4.2	6	mA	VDDCAP = 4.75 V, PDO1 to PDO8 off, DACs off, ADC off
Additional Currents					
All PDOx FET Drivers On		1		mA	VDDCAP = 4.75 V, PDO1 to PDO6 loaded with 1 μA each, PDO7 to PDO8 off
Current Available from VDDCAP			2	mA	Maximum additional load that can be drawn from all PDO pull-ups to VDDCAP
DAC Supply Currents		2.2		mA	Four DACs on with 100 μA maximum load on each
ADC Supply Current		1		mA	Running round-robin loop
EEPROM Erase Current		10		mA	1 ms duration only, VDDCAP = 3 V
<b>SUPPLY FAULT DETECTORS</b>					
V <sub>H</sub> Pin					
Input Impedance		52		kΩ	Midrange and high range
Input Attenuator Error		±0.05		%	
Detection Ranges					
High Range	6		14.4	V	
Midrange	2.5		6	V	
V <sub>Px</sub> Pins					
Input Impedance		52		kΩ	Low range and midrange
Input Attenuator Error		±0.05		%	
Detection Ranges					
Midrange	2.5		6	V	No input attenuation error
Low Range	1.25		3	V	
Ultralow Range	0.573		1.375	V	
V <sub>Xx</sub> Pins					
Input Impedance	1			MΩ	No input attenuation error
Ultralow Range	0.573		1.375	V	
Absolute Accuracy			±1	%	Internal reference VREF error + DAC nonlinearity + comparator offset error
Threshold Resolution		8		Bits	
Digital Glitch Filter		0		μs	Minimum programmable filter length
		100		μs	Maximum programmable filter length

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
<b>ANALOG-TO-DIGITAL CONVERTER</b>					
Signal Range	0		$V_{REFIN}$	V	The ADC can convert signals presented to the VH, VPx, and VXx pins; VPx and VH input signals are attenuated depending on the selected range; a signal at the pin corresponding to the selected range is from 0.573 V to 1.375 V at the ADC input
Input Reference Voltage on REFIN Pin, $V_{REFIN}$		2.048		V	
Resolution		12		Bits	
INL			$\pm 2.5$	LSB	Endpoint corrected, $V_{REFIN} = 2.048$ V
Gain Error			$\pm 0.05$	%	$V_{REFIN} = 2.048$ V
Conversion Time		0.44		ms	One conversion on one channel
Offset Error		84		ms	All eight channels selected, averaging enabled
Input Noise		0.25		LSB <sub>rms</sub>	$V_{REFIN} = 2.048$ V Direct input (no attenuator)
<b>BUFFERED VOLTAGE OUTPUT DACS</b>					
Resolution		8		Bits	
Code 0x80 Output Voltage					Four DACs are individually selectable for centering on one of four output voltage ranges
Range 1	0.592	0.6	0.603	V	
Range 2	0.796	0.8	0.803	V	
Range 3	0.996	1	1.003	V	
Range 4	1.246	1.25	1.253	V	
Output Voltage Range		601.25		mV	Same range, independent of center point
LSB Step Size		2.36		mV	
INL			$\pm 0.75$	LSB	Endpoint corrected
DNL			$\pm 0.4$	LSB	
Gain Error			1	%	
Maximum Load Current (Source)		100		$\mu$ A	
Maximum Load Current (Sink)		100		$\mu$ A	
Maximum Load Capacitance			50	pF	
Settling Time into 50 pF Load			2	$\mu$ s	
Load Regulation		2.5		mV	Per mA
PSRR		60		dB	DC
		40		dB	100 mV step in 20 ns with 50 pF load
<b>REFERENCE OUTPUT</b>					
Reference Output Voltage	2.043	2.048	2.053	V	No load
Load Regulation		-0.25		mV	Sourcing current, $I_{DACxMAX} = -100$ $\mu$ A
		+0.25		mV	Sinking current, $I_{DACxMAX} = +100$ $\mu$ A
Minimum Load Capacitance	1			$\mu$ F	Capacitor required for decoupling, stability
PSRR		60		dB	DC

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
<b>PROGRAMMABLE DRIVER OUTPUTS</b>					
High Voltage (Charge Pump) Mode (PDO1 to PDO6)					
Output Impedance		500		kΩ	
V <sub>OH</sub>	11	12.5	14	V	I <sub>OH</sub> = 0 μA
	10.5	12	13.5	V	I <sub>OH</sub> = 1 μA
I <sub>OUTAVG</sub>		20		μA	2 V < V <sub>OH</sub> < 7 V
<b>Standard (Digital Output) Mode (PDO1 to PDO8)</b>					
V <sub>OH</sub>	2.4			V	V <sub>PU</sub> (pull-up to VDDCAP or VPx) = 2.7 V, I <sub>OH</sub> = 0.5 mA
			4.5	V	V <sub>PU</sub> to VPx = 6.0 V, I <sub>OH</sub> = 0 mA
	V <sub>PU</sub> - 0.3			V	V <sub>PU</sub> ≤ 2.7 V, I <sub>OH</sub> = 0.5 mA
V <sub>OL</sub>	0		0.50	V	I <sub>OL</sub> = 20 mA
I <sub>OL</sub> <sup>2</sup>			20	mA	Maximum sink current per PDOx pin
I <sub>SINK</sub> <sup>2</sup>			60	mA	Maximum total sink for all PDOx pins
R <sub>PULL-UP</sub>	16	20	29	kΩ	Internal pull-up
I <sub>SOURCE</sub> (VPx) <sup>2</sup>			2	mA	Current load on any VPx pull-ups, that is, total source current available through any number of PDO pull-up switches configured onto any one VPx pin
Three-State Output Leakage Current			10	μA	V <sub>PDO</sub> = 14.4 V
Oscillator Frequency	90	100	110	kHz	All on-chip time delays derived from this clock
<b>DIGITAL INPUTS (VXx, A0, A1)</b>					
Input High Voltage, V <sub>IH</sub>	2.0			V	Maximum V <sub>IN</sub> = 5.5 V
Input Low Voltage, V <sub>IL</sub>			0.8	V	Maximum V <sub>IN</sub> = 5.5 V
Input High Current, I <sub>IH</sub>	-1			μA	V <sub>IN</sub> = 5.5 V
Input Low Current, I <sub>IL</sub>			1	μA	V <sub>IN</sub> = 0 V
Input Capacitance		5		pF	
Programmable Pull-Down Current, I <sub>PULL-DOWN</sub>		20		μA	VDDCAP = 4.75 V, T <sub>A</sub> = 25°C, if known logic state is required
<b>SERIAL BUS DIGITAL INPUTS (SDA, SCL)</b>					
Input High Voltage, V <sub>IH</sub>	2.0			V	
Input Low Voltage, V <sub>IL</sub>			0.8	V	
Output Low Voltage, V <sub>OL</sub> <sup>2</sup>			0.4	V	I <sub>OUT</sub> = -3.0 mA
<b>SERIAL BUS TIMING</b>					
Clock Frequency, f <sub>SCLK</sub>			400	kHz	See Figure 38
Bus Free Time, t <sub>BUF</sub>	1.3			μs	
Start Setup Time, t <sub>SU;STA</sub>	0.6			μs	
Stop Setup Time, t <sub>SU;STO</sub>	0.6			μs	
Start Hold Time, t <sub>HD;STA</sub>	0.6			μs	
SCL Low Time, t <sub>LOW</sub>	1.3			μs	
SCL High Time, t <sub>HIGH</sub>	0.6			μs	
SCL, SDA Rise Time, t <sub>R</sub>			300	ns	
SCL, SDA Fall Time, t <sub>F</sub>			300	ns	
Data Setup Time, t <sub>SU;DAT</sub>	100			ns	
Data Hold Time, t <sub>HD;DAT</sub>	250			ns	
Input Low Current, I <sub>IL</sub>			1	μA	V <sub>IN</sub> = 0 V
<b>SEQUENCING ENGINE TIMING</b>					
State Change Time		10		μs	

<sup>1</sup> At least one of the VH, VPx pins must be ≥3.0 V to maintain the device supply on VDDCAP.

<sup>2</sup> Specification is not production tested but is supported by characterization data at initial product release.



## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltage on VH Pin	16 V
Voltage on VPx Pins	7 V
Voltage on VXx Pins	-0.3 V to +6.5 V
Voltage on A0, A1 Pins	-0.3 V to +7 V
Voltage on REFIN, REFOUT Pins	5 V
Voltage on VDDCAP, VCCP Pins	6.5 V
Voltage on DACx Pins	6.5 V
Voltage on PDOx Pins	16 V
Voltage on SDA, SCL Pins	7 V
Voltage on GND, AGND, PDOGND, REFGND Pins	-0.3 V to +0.3 V
Input Current at Any Pin	±5 mA
Package Input Current	±20 mA
Maximum Junction Temperature (T <sub>j</sub> max)	150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature	
Soldering Vapor Phase, 60 sec	215°C
ESD Rating, All Pins	2000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	$\theta_{JA}$	Unit
32-Lead LQFP	54	°C/W
40-Lead LFCSP	26.5	°C/W

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

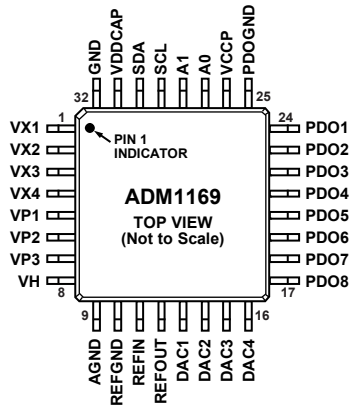
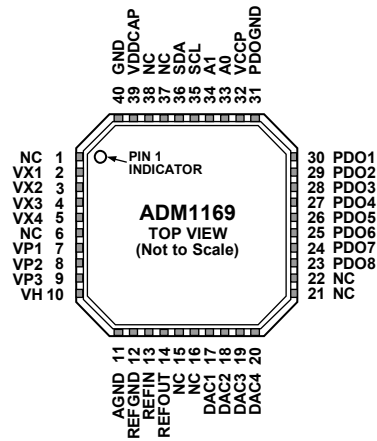


Figure 3. 32-Lead LQFP Pin Configuration



NOTES  
 1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.  
 2. THE LFCSP HAS AN EXPOSED PAD ON THE BOTTOM. THIS PAD IS A NO CONNECT (NC). IF POSSIBLE, THIS PAD SHOULD BE SOLDERED TO THE BOARD FOR IMPROVED MECHANICAL STABILITY.

Figure 4. 40-Lead LFCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.		Mnemonic	Description
32-Lead LQFP	40-Lead LFCSP		
N/A <sup>1</sup>	1, 6, 15, 16, 21, 22, 37, 38	NC	No Connect. Do not connect to this pin.
1 to 4	2 to 5	VX1 to VX4 (VXx)	High Impedance Inputs to Supply Fault Detectors. Fault thresholds can be set from 0.573 V to 1.375 V. Alternatively, these pins can be used as general-purpose digital inputs.
5 to 7	7 to 9	VP1 to VP3 (VPx)	Low Voltage Inputs to Supply Fault Detectors. Three input ranges can be set by altering the input attenuation on a potential divider connected to these pins, the output of which connects to a supply fault detector. These pins allow thresholds from 2.5 V to 6 V, from 1.25 V to 3 V, and from 0.573 V to 1.375 V.
8	10	VH	High Voltage Input to Supply Fault Detectors. Three input ranges can be set by altering the input attenuation on a potential divider connected to this pin, the output of which connects to a supply fault detector. This pin allows thresholds from 6 V to 14.4 V and from 2.5 V to 6 V.
9	11	AGND <sup>2</sup>	Ground Return for Input Attenuators.
10	12	REFGND <sup>2</sup>	Ground Return for On-Chip Reference Circuits.
11	13	REFIN	Reference Input for ADC. Nominally, 2.048 V. This pin must be driven by a reference voltage. The on-board reference can be used by connecting the REFOUT pin to the REFIN pin. This is the normal configuration.
12	14	REFOUT	2.048 V Reference Output. A reservoir capacitor must always be connected between this pin and GND, even if the REFIN pin is driven by an external reference. A 10 µF capacitor is recommended for this purpose.
13 to 16	17 to 20	DAC1 to DAC4	Voltage Output DACs. These pins default to high impedance at power-up.
17 to 24	23 to 30	PDO8 to PDO1	Programmable Output Drivers.
25	31	PDOGND <sup>2</sup>	Ground Return for Output Drivers.
26	32	VCCP	Central Charge-Pump Voltage of 5.25 V. A reservoir capacitor must be connected between this pin and GND. A 10 µF capacitor is recommended for this purpose.
27	33	A0	Logic Input. This pin sets the seventh bit of the SMBus interface address.
28	34	A1	Logic Input. This pin sets the sixth bit of the SMBus interface address.
29	35	SCL	SMBus Clock Pin. Bidirectional open drain requires external resistive pull-up.
30	36	SDA	SMBus Data Pin. Bidirectional open drain requires external resistive pull-up.

Pin No.		Mnemonic	Description
32-Lead LQFP	40-Lead LFCSP		
31	39	VDDCAP	Device Supply Voltage. Linearly regulated from the highest of the VPx and VH pins to a typical of 4.75 V. Note that a capacitor must be connected between this pin and GND. A 10 $\mu$ F capacitor is recommended for this purpose.
32	40	GND <sup>2</sup>	Supply Ground.
N/A <sup>1</sup>		EPAD	Exposed Pad. This pad is a no connect (NC). If possible, this pad should be soldered to the board for improved mechanical stability.

<sup>1</sup> N/A is not applicable.

<sup>2</sup> In a typical application, all ground pins are connected together.

TYPICAL PERFORMANCE CHARACTERISTICS

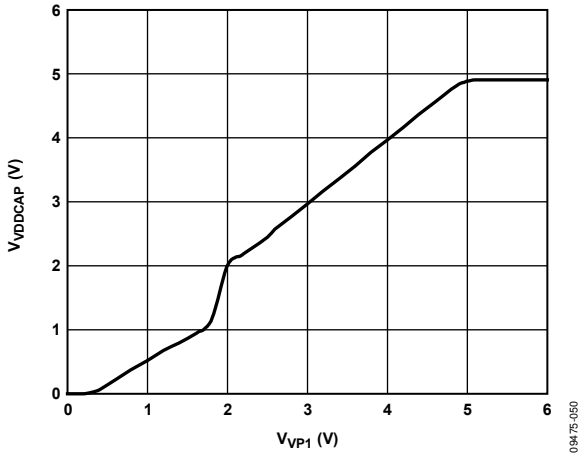


Figure 5.  $V_{DDCAP}$  vs.  $V_{VP1}$

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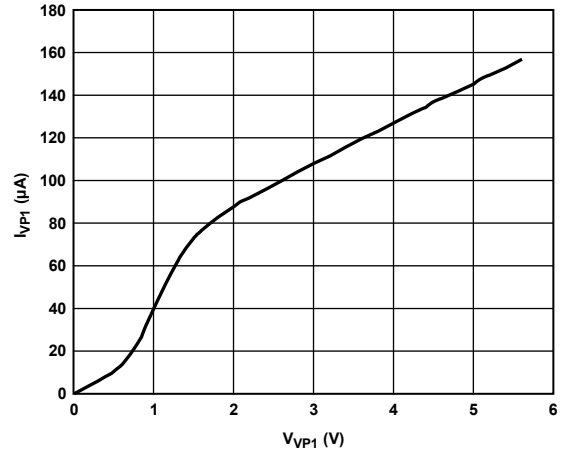


Figure 8.  $I_{VP1}$  vs.  $V_{VP1}$  (VP1 Not as Supply)

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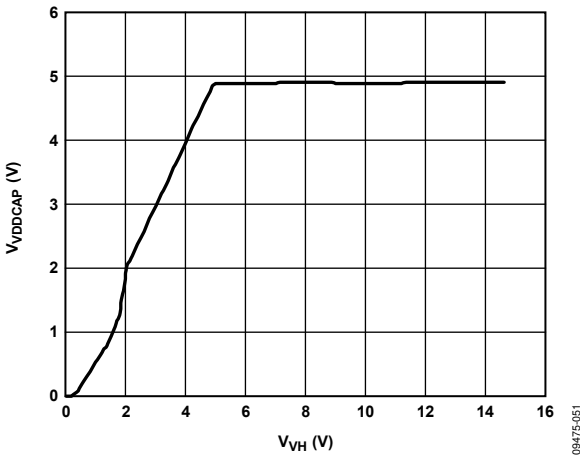


Figure 6.  $V_{DDCAP}$  vs.  $V_{VH}$

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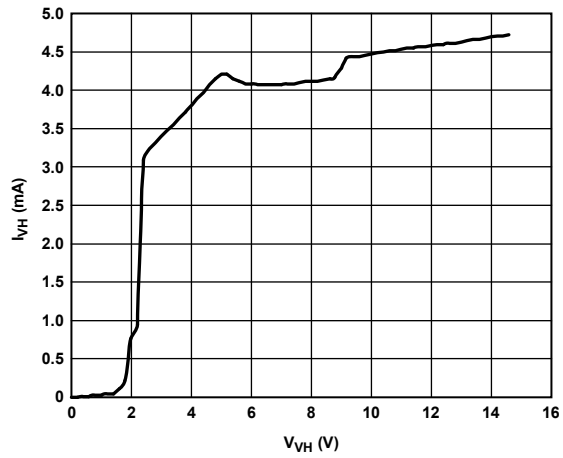


Figure 9.  $I_{VH}$  vs.  $V_{VH}$  (VH as Supply)

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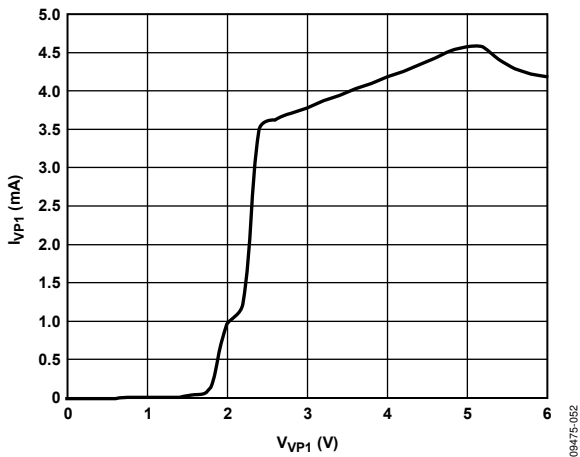


Figure 7.  $I_{VP1}$  vs.  $V_{VP1}$  (VP1 as Supply)

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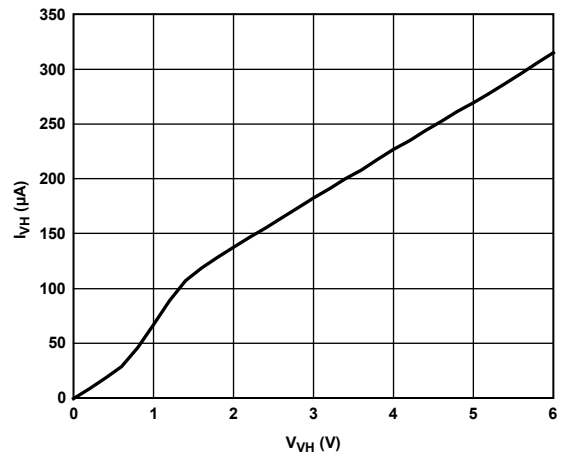


Figure 10.  $I_{VH}$  vs.  $V_{VH}$  (VH Not as Supply)

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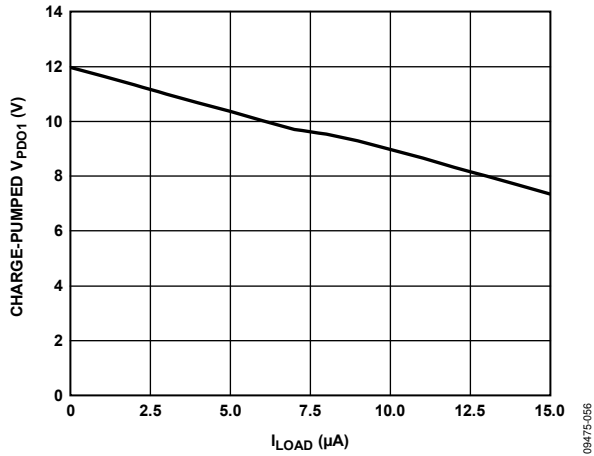


Figure 11. Charge-Pumped  $V_{PDO1}$  (FET Drive Mode) vs.  $I_{LOAD}$

09475-056

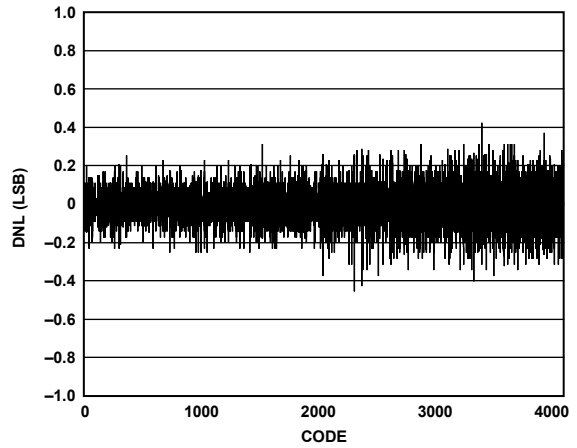


Figure 14. DNL for ADC

09475-066

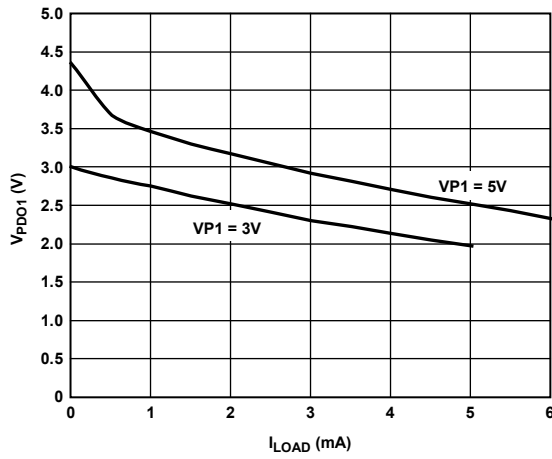


Figure 12.  $V_{PDO1}$  (Strong Pull-Up to  $VPx$ ) vs.  $I_{LOAD}$

09475-057

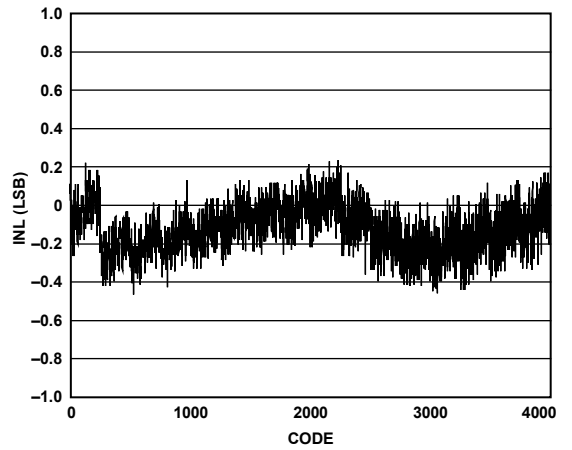


Figure 15. INL for ADC

09475-063

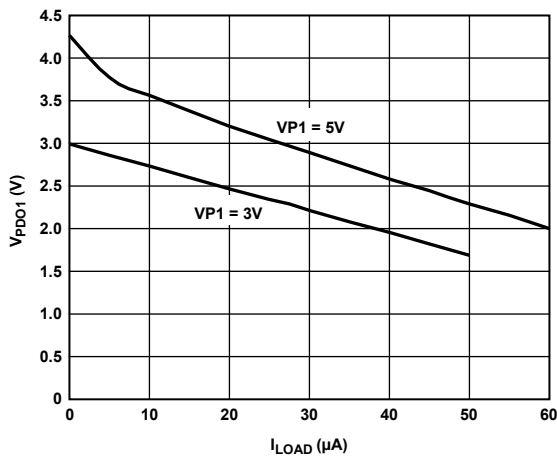


Figure 13.  $V_{PDO1}$  (Weak Pull-Up to  $VPx$ ) vs.  $I_{LOAD}$

09475-058

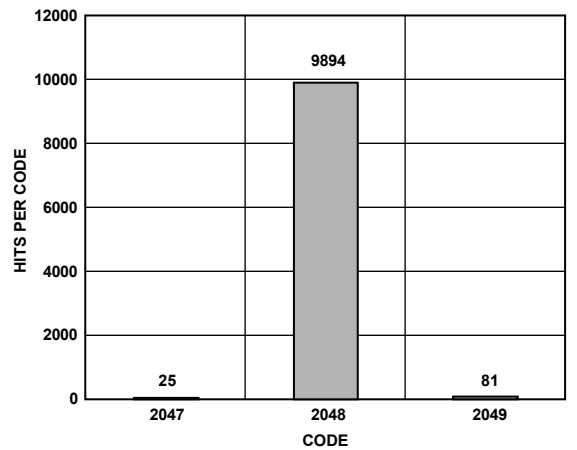


Figure 16. ADC Noise, Midcode Input, 10,000 Reads

09475-064

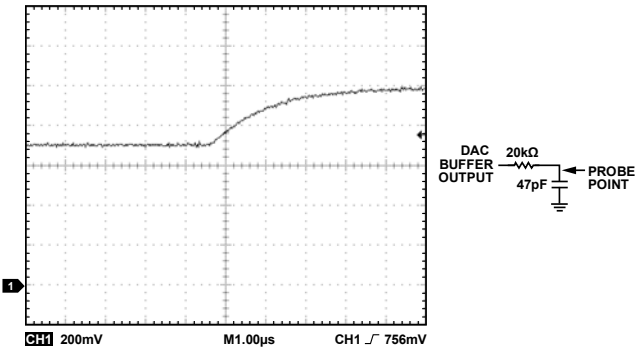


Figure 17. Transient Response of DAC Code Change into Typical Load

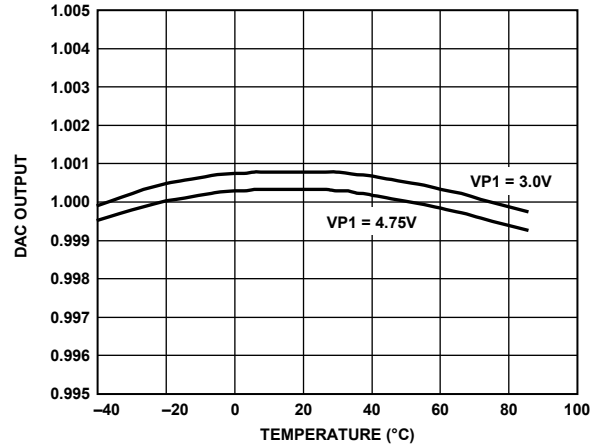


Figure 19. DAC Output vs. Temperature

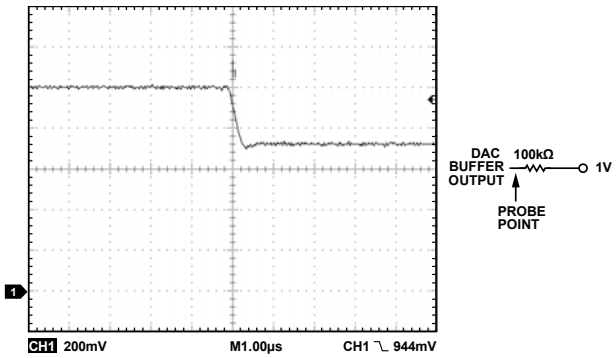


Figure 18. Transient Response of DAC to Turn-On from High-Z State

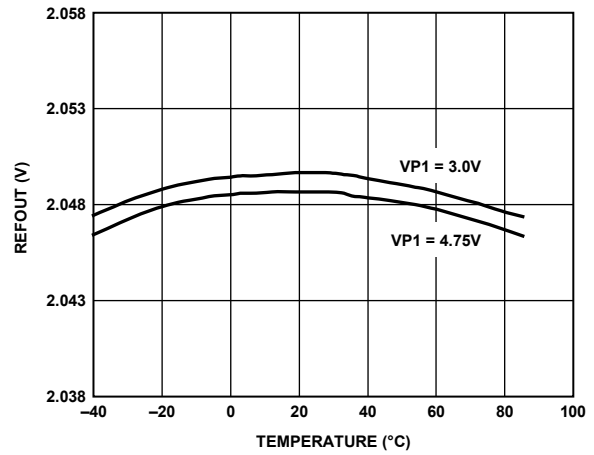


Figure 20. REFOUT vs. Temperature

## POWERING THE ADM1169

The ADM1169 is powered from the highest voltage input on either the positive-only supply inputs (VPx) or the high voltage supply input (VH). This technique offers improved redundancy because the device is not dependent on any particular voltage rail to keep it operational. The same pins are used for supply fault detection (see the Supply Supervision section). A V<sub>DD</sub> arbitrator on the device chooses which supply to use. The arbitrator can be considered an OR'ing of four low dropout regulators (LDOs) together. A supply comparator chooses the highest input to provide the on-chip supply. There is minimal switching loss with this architecture (~0.2 V), resulting in the ability to power the ADM1169 from a supply as low as 3.0 V. Note that the supply on the VXx pins cannot be used to power the device.

An external capacitor to GND is required to decouple the on-chip supply from noise. This capacitor should be connected to the VDDCAP pin, as shown in Figure 21. The capacitor has another use during brownouts (momentary loss of power). Under these conditions, when the input supply (VPx or VH) dips transiently below V<sub>DD</sub>, the synchronous rectifier switch immediately turns off so that it does not pull V<sub>DD</sub> down. The V<sub>DD</sub> capacitor can then act as a reservoir to keep the device active until the next highest supply takes over the powering of the device. A 10 μF capacitor is recommended for this reservoir/decoupling function.

The VH input pin can accommodate supplies up to 14.4 V, which allows the ADM1169 to be powered using a 12 V backplane supply. In cases where this 12 V supply is hot swapped, it is recommended that the ADM1169 not be connected directly to the supply. Suitable precautions, such as the use of a hot swap controller or RC filter network, should be taken to protect the device from transients that may cause damage during hot swap events.

When two or more supplies are within 100 mV of each other, the supply that first takes control of V<sub>DD</sub> keeps control. For example, if VP1 is connected to a 3.3 V supply, V<sub>DD</sub> powers up to approximately 3.1 V through VP1. If VP2 is then connected to another 3.3 V supply, VP1 still powers the device unless VP2 goes 100 mV higher than VP1.

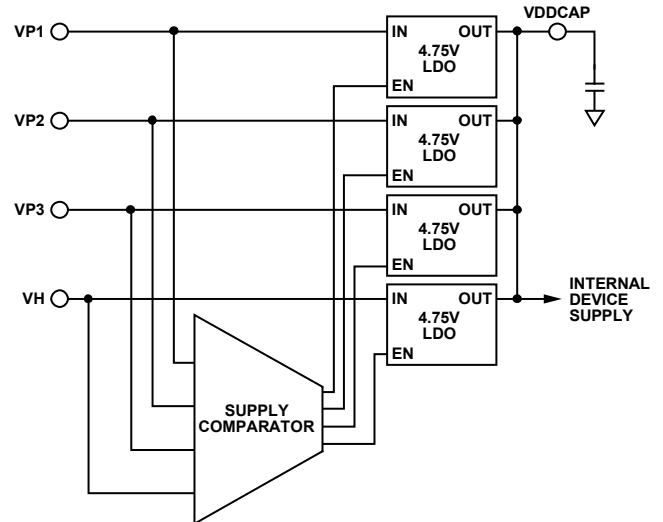


Figure 21. V<sub>DD</sub> Arbitrator Operation

## SLEW RATE CONSIDERATION

When the ambient temperature of operation is less than approximately -20°C, and in the event of a power loss where all supply inputs fail for less than a few hundreds of milliseconds (for example, due to a system supply brownout), it is recommended that the supply voltage recover with a ramp rate of at least 1.5 V/ms or less than 0.5 V/ms.

## INPUTS

### SUPPLY SUPERVISION

The ADM1169 has eight programmable inputs. Four of these are dedicated supply fault detectors (SFDs). These dedicated inputs are called VH and VPx (VP1 to VP3) by default. The other four inputs are labeled VXx (VX1 to VX4) and have dual functionality. They can be used either as SFDs, with functionality similar to the VH and VPx, or as CMOS-/TTL-compatible logic inputs to the device. Therefore, the ADM1169 can have up to eight analog inputs, a minimum of four analog inputs and four digital inputs, or a combination thereof. If an input is used as an analog input, it cannot be used as a digital input. Therefore, a configuration requiring eight analog inputs has no available digital inputs. Table 6 shows the details of each input.

### PROGRAMMING THE SUPPLY FAULT DETECTORS

The ADM1169 can have up to eight SFDs on its eight input channels. These highly programmable reset generators enable the supervision of up to eight supply voltages. The supplies can be as low as 0.573 V and as high as 14.4 V. The inputs can be configured to detect an undervoltage fault (the input voltage drops below a preprogrammed value), an overvoltage fault (the input voltage rises above a preprogrammed value), or an out-of-window fault (the input voltage is outside a preprogrammed range). The thresholds can be programmed to an 8-bit resolution in registers provided in the ADM1169. This translates to a voltage resolution that is dependent on the range selected. The resolution is given by

$$\text{Step Size} = \text{Threshold Range}/255$$

Therefore, if the high range is selected on VH, the step size can be calculated as follows:

$$(14.4 \text{ V} - 6.0 \text{ V})/255 = 32.9 \text{ mV}$$

Table 5 lists the upper and lower limits of each available range, the bottom of each range ( $V_B$ ), and the range itself ( $V_R$ ).

**Table 5. Voltage Range Limits**

Voltage Range (V)	$V_B$ (V)	$V_R$ (V)
0.573 to 1.375	0.573	0.802
1.25 to 3.00	1.25	1.75
2.5 to 6.0	2.5	3.5
6.0 to 14.4	6.0	8.4

The threshold value required is given by

$$V_T = (V_R \times N)/255 + V_B$$

where:

$V_T$  is the desired threshold voltage (undervoltage or overvoltage).

$V_R$  is the voltage range.

$N$  is the decimal value of the 8-bit code.

$V_B$  is the bottom of the range.

Reversing the equation, the code for a desired threshold is given by

$$N = 255 \times (V_T - V_B)/V_R$$

For example, if the user wants to set a 5 V overvoltage threshold on VP1, the code to be programmed in the PS1OVTH register (as described in the [AN-721 Application Note](#)) is given by

$$N = 255 \times (5 - 2.5)/3.5$$

Therefore,  $N = 182$  (1011 0110 or 0xB6).



**INPUT COMPARATOR HYSTERESIS**

The UV and OV comparators shown in Figure 23 are always monitoring VPx. To avoid chatter (multiple transitions when the input is very close to the set threshold level), these comparators have digitally programmable hysteresis. The hysteresis can be programmed up to the values shown in Table 6.

The hysteresis is added after a supply voltage goes out of tolerance. Therefore, the user can program the amount above the undervoltage threshold to which the input must rise before an undervoltage fault is deasserted. Similarly, the user can program the amount below the overvoltage threshold to which an input must fall before an overvoltage fault is deasserted.

The hysteresis value is given by

$$V_{HYST} = V_R \times N_{THRESH}/255$$

where:

$V_{HYST}$  is the desired hysteresis voltage.

$N_{THRESH}$  is the decimal value of the 5-bit hysteresis code.

Note that  $N_{THRESH}$  has a maximum value of 31. The maximum hysteresis for the ranges is listed in Table 6.

**INPUT GLITCH FILTERING**

The final stage of the SFDs is a glitch filter. This block provides time-domain filtering on the output of the SFD comparators, which allows the user to remove any spurious transitions such as supply bounce at turn-on. The glitch filter function is in addition to the digitally programmable hysteresis of the SFD comparators. The glitch filter timeout is programmable up to 100  $\mu$ s.

For example, when the glitch filter timeout is 100  $\mu$ s, any pulse appearing on the input of the glitch filter block that is less than 100  $\mu$ s in duration is prevented from appearing on the output of the glitch filter block. Any input pulse that is longer than 100  $\mu$ s appears on the output of the glitch filter block. The output is delayed with respect to the input by 100  $\mu$ s. The filtering process is shown in Figure 22.

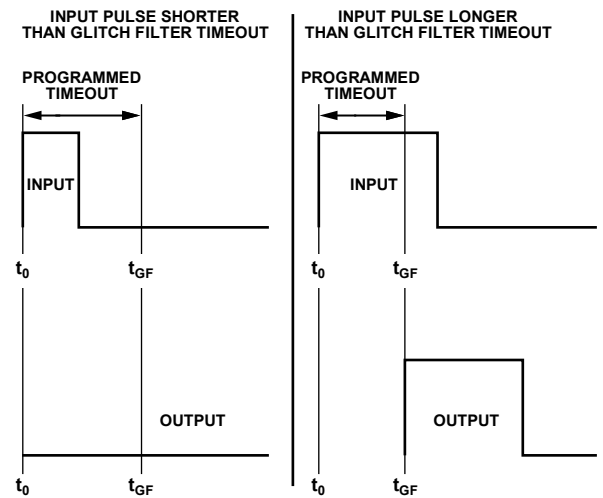


Figure 22. Input Glitch Filter Function

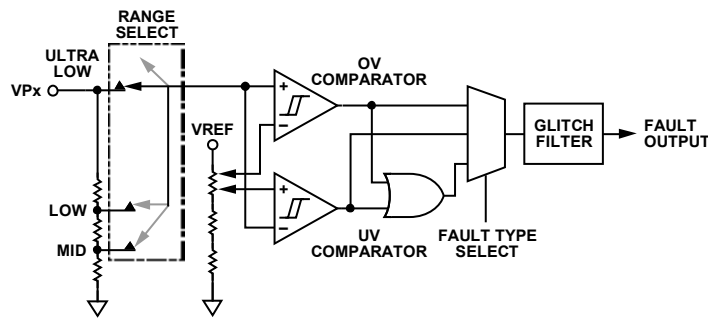


Figure 23. Supply Fault Detector Block

Table 6. Input Functions, Thresholds, and Ranges

Input	Function	Voltage Range (V)	Maximum Hysteresis	Voltage Resolution (mV)	Glitch Filter ( $\mu$ s)
VH	High voltage analog input	2.5 to 6.0	425 mV	13.7	0 to 100
		6.0 to 14.4	1.02 V	32.9	0 to 100
VPx	Positive analog input	0.573 to 1.375	97.5 mV	3.14	0 to 100
		1.25 to 3.00	212 mV	6.8	0 to 100
		2.5 to 6.0	425 mV	13.7	0 to 100
VXx	High-Z analog input	0.573 to 1.375	97.5 mV	3.14	0 to 100
	Digital input	0 to 5.0	Not applicable	Not applicable	0 to 100

## SUPPLY SUPERVISION WITH VXx INPUTS

The VXx inputs have two functions. They can be used as either supply fault detectors or digital logic inputs. When selected as analog (SFD) inputs, the VXx pins have functionality that is very similar to the VH and VPx pins. The primary difference is that the VXx pins have only one input range: 0.573 V to 1.375 V. Therefore, these inputs can directly supervise only the very low supplies. However, the input impedance of the VXx pins is high, allowing an external resistor divide network to be connected to the pin. Thus, potentially any supply can be divided down into the input range of the VXx pin and supervised. This enables the ADM1169 to monitor other supplies, such as +24 V, +48 V, and -5 V.

An additional supply supervision function is available when the VXx pins are selected as digital inputs. In this case, the analog function is available as a second detector on each of the dedicated analog inputs, VPx and VH. The analog function of VX1 is mapped to VP1, VX2 is mapped to VP2, and so on. VX4 is mapped to VH. In this case, these SFDs can be viewed as secondary or warning SFDs.

The secondary SFDs are fixed to the same input range as the primary SFDs. They are used to indicate warning levels rather than failure levels. This allows faults and warnings to be generated on a single supply using only one pin. For example, if VP1 is set to output a fault when a 3.3 V supply drops to 3.0 V, VX1 can be set to output a warning at 3.1 V. Warning outputs are available for readback from the status registers. They are also ORed together and fed into the SE, allowing warnings to generate interrupts on the PDOs. Therefore, in this example, if the supply drops to 3.1 V, a warning is generated, and remedial action can be taken before the supply drops out of tolerance.

## VXx PINS AS DIGITAL INPUTS

As described in the Supply Supervision with VXx Inputs section, the VXx input pins on the ADM1169 have dual functionality. The second function is as a digital logic input to the device. Therefore, the ADM1169 can be configured for up to four digital inputs. These inputs are TTL-/CMOS-compatible inputs. Standard logic signals can be applied to the pins: RESET from reset generators, PWRGD signals, fault flags, manual resets, and so on. These signals are available as inputs to the SE and, therefore, can be used to control the status of the PDOs. The inputs can be configured to detect either a change in level or an edge.

When configured for level detection, the output of the digital block is a buffered version of the input. When configured for edge detection, a pulse of programmable width is output from the digital block when the logic transition is detected. The width is programmable from 0  $\mu$ s to 100  $\mu$ s.

The digital blocks feature the same glitch filter function that is available on the SFDs. This enables the user to ignore spurious transitions on the inputs. For example, the filter can be used to debounce a manual reset switch.

When configured as digital inputs, each VXx pin has a weak (10  $\mu$ A) pull-down current source available for placing the input into a known condition, even if left floating. The current source, if selected, weakly pulls the input to GND.

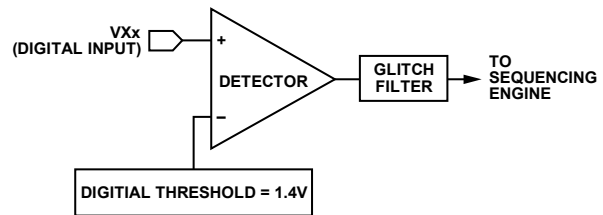


Figure 24. VXx Digital Input Function

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## OUTPUTS

### SUPPLY SEQUENCING THROUGH CONFIGURABLE OUTPUT DRIVERS

Supply sequencing is achieved with the [ADM1169](#) using the programmable driver outputs (PDOs) on the device as control signals for supplies. The output drivers can be used as logic enables or as FET drivers.

The sequence in which the PDOs are asserted (and, therefore, the supplies are turned on) is controlled by the SE. The SE determines what action is taken with the PDOs based on the condition of the [ADM1169](#) inputs. Therefore, the PDOs can be set up to assert when the SFDs are in tolerance, the correct input signals are received on the V<sub>X</sub> digital pins, and no warnings are received from any of the inputs of the devices. The PDOs can be used for a variety of functions. The primary function is to provide enable signals for LDOs or dc-to-dc converters that generate supplies locally on a board. The PDOs can also be used to provide a PWRGD signal when all the SFDs are in tolerance or a RESET output if one of the SFDs goes out of specification (this can be used as a status signal for a DSP, FPGA, or other microcontroller).

The PDOs can be programmed to pull up to a number of different options. The outputs can be programmed as follows:

- Open-drain (allowing the user to connect an external pull-up resistor)
- Open-drain with weak pull-up to V<sub>DD</sub>
- Open-drain with strong pull-up to V<sub>DD</sub>
- Open-drain with weak pull-up to V<sub>Px</sub>
- Open-drain with strong pull-up to V<sub>Px</sub>.
- Strong pull-down to GND
- Internally charge-pumped high drive (12 V, PDO1 to PDO6 only)

The last option (available only on PDO1 to PDO6) allows the user to directly drive a voltage high enough to fully enhance an external NFET, which is used to isolate, for example, a card-side voltage from a backplane supply (a PDO can sustain greater than 10.5 V into a 1 μA load). The pull-down switches can also be used to drive status LEDs directly.

The data driving each of the PDOs can come from one of three sources. The source can be enabled in the PDOxCFG configuration register (see the [AN-721 Application Note](#) for details).

The data sources are as follows:

- Output from the SE.
- Directly from the SMBus. A PDO can be configured so that the SMBus has direct control over it. This enables software control of the PDOs. Therefore, a microcontroller can be used to initiate a software power-up/power-down sequence.
- On-chip clock. A 100 kHz clock is generated on the device. This clock can be made available on any of the PDOs. It can be used, for example, to clock an external device such as an LED.

### DEFAULT OUTPUT CONFIGURATION

All of the internal registers in an unprogrammed [ADM1169](#) device from the factory are set to 0. Because of this, the PDOx pins are pulled to GND by a weak (20 kΩ), on-chip, pull-down resistor.

As the input supply to the [ADM1169](#) ramps up on V<sub>Px</sub> or V<sub>H</sub>, all PDOx pins behave as follows:

- Input supply = 0 V to 1.2 V. The PDOs are high impedance.
- Input supply = 1.2 V to 2.7 V. The PDOs are pulled to GND by a weak (20 kΩ), on-chip, pull-down resistor.
- Supply > 2.7 V. Factory programmed devices continue to pull all PDOs to GND by a weak (20 kΩ), on-chip, pull-down resistor. Programmed devices download current EEPROM configuration data, and the programmed setup is latched. The PDO then goes to the state demanded by the configuration. This provides a known condition for the PDOs during power-up.

The internal pull-down can be overdriven with an external pull-up of suitable value tied from the PDOx pin to the required pull-up voltage. The 20 kΩ resistor must be accounted for in calculating a suitable value. For example, if PDOx must be pulled up to 3.3 V, and 5 V is available as an external supply, the pull-up resistor value is given by

$$3.3 \text{ V} = 5 \text{ V} \times 20 \text{ k}\Omega / (R_{UP} + 20 \text{ k}\Omega)$$

Therefore,

$$R_{UP} = (100 \text{ k}\Omega - 66 \text{ k}\Omega) / 3.3 \text{ V} = 10 \text{ k}\Omega$$

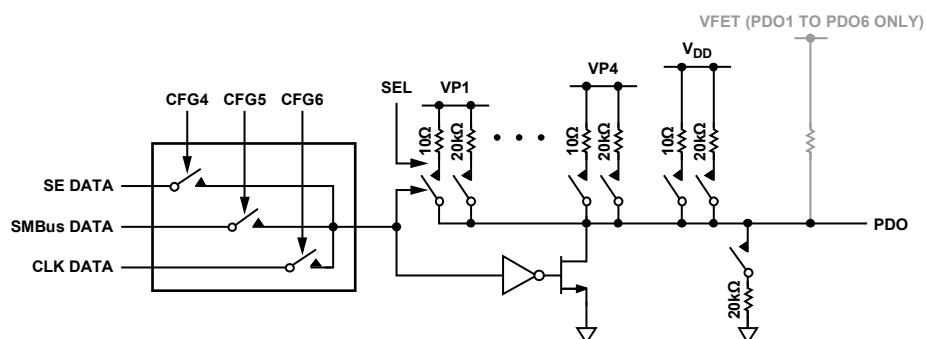


Figure 25. Programmable Driver Output

# SEQUENCING ENGINE

## OVERVIEW

The ADM1169 SE provides the user with powerful and flexible control of sequencing. The SE implements a state machine control of the PDO outputs, with state changes conditional on input events. SE programs can enable complex control of boards such as power-up and power-down sequence control, fault event handling, and interrupt generation on warnings. A watchdog function that verifies the continued operation of a processor clock can be integrated into the SE program. The SE can also be controlled via the SMBus, giving software or firmware control of the board sequencing.

The SE state machine comprises 63 state cells. Each state has the following attributes:

- It monitors signals indicating the status of the eight input pins: VP1 to VP3, VH, and VX1 to VX4.
- It can be entered from any other state.
- Three exit routes move the state machine onto a next state: sequence detection, fault monitoring, and timeout.
- Delay timers for the sequence and timeout blocks can be programmed independently and changed with each state change. The range of timeouts is from 0 ms to 400 ms.
- Output condition of the eight PDO pins is defined and fixed within a state.
- It transitions from one state to the next in less than 20 μs, which is the time needed to download a state definition from EEPROM to the SE.
- It can trigger a write of the black box fault and status registers into the black box section of EEPROM.

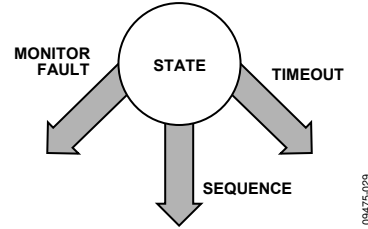


Figure 26. State Cell

The ADM1169 offers up to 63 state definitions. The signals monitored to indicate the status of the input pins are the outputs of the SFDs.

## WARNINGS

The SE also monitors warnings. These warnings can be generated when the ADC readings violate their limit register value or when the secondary voltage monitors on VPx and VH are triggered. The warnings are ORed together and are available as a single warning input to each of the three blocks that enable exiting a state.

## SMBus JUMP (UNCONDITIONAL JUMP)

The SE can be forced to advance to the next state unconditionally. This enables the user to force the SE to advance. Examples of the use of this feature include moving to a margining state or debugging a sequence. The SMBus jump or go-to command can be seen as another input to sequence and timeout blocks to provide an exit from each state.

Table 7. Sample Sequence State Entries

State	Sequence	Timeout	Monitor
IDLE1	If VX1 is low, go to State IDLE2.		
IDLE2	If VP1 is okay, go to State EN3V3.		
EN3V3	If VP2 is okay, go to State EN2V5.	If VP2 is not okay after 10 ms, go to State DIS3V3.	If VP1 is not okay, go to State IDLE1.
DIS3V3	If VX1 is high, go to State IDLE1.		
EN2V5	If VP3 is okay, go to State PWRGD.	If VP3 is not okay after 20 ms, go to State DIS2V5.	If VP1 or VP2 is not okay, go to State FSEL2.
DIS2V5	If VX1 is high, go to State IDLE1.		
FSEL1	If VP3 is not okay, go to State DIS2V5.		If VP1 or VP2 is not okay, go to State FSEL2.
FSEL2	If VP2 is not okay, go to State DIS3V3.		If VP1 is not okay, go to State IDLE1.
PWRGD	If VX1 is high, go to State DIS2V5.		If VP1, VP2, or VP3 is not okay, go to State FSEL1.

**SEQUENCING ENGINE APPLICATION EXAMPLE**

The application in this section demonstrates the operation of the SE. Figure 28 shows how the simple building block of a single SE state can be used to build a power-up sequence for a three-supply system. Table 8 lists the PDO outputs for each state in the same SE implementation. In this system, a good 5 V supply on the VP1 pin and the VX1 pin held low are the triggers required to start a power-up sequence. The sequence next turns on the 3.3 V supply, then the 2.5 V supply (assuming successful turn-on of the 3.3 V supply). When all three supplies have turned on correctly, the PWRGD state is entered, where the SE remains until a fault occurs on one of the three supplies, or until it is instructed to go through a power-down sequence by VX1 going high.

Faults are dealt with throughout the power-up sequence on a case-by-case basis. The following three sections (the Sequence Detector section, the Monitoring Fault Detector section, and the Timeout Detector section) describe the individual blocks and use the sample application shown in Figure 28 to demonstrate the actions of the state machine.

**Sequence Detector**

The sequence detector block is used to detect when a step in a sequence has been completed. It looks for one of the SE inputs to change state, and it is most often used as the gate for successful progress through a power-up or power-down sequence. A timer block that is included in this detector can insert delays into a power-up or power-down sequence, if required. Timer delays can be set from 10 μs to 400 ms. Figure 27 is a block diagram of the sequence detector.

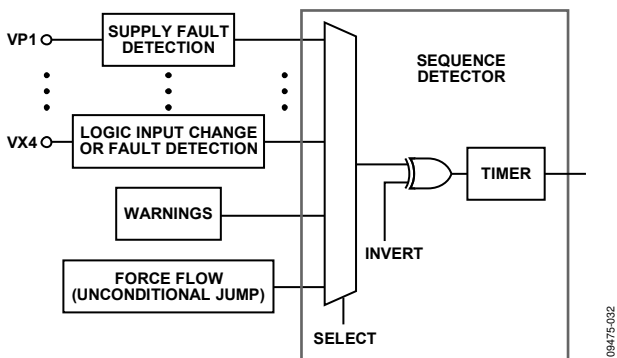


Figure 27. Sequence Detector Block Diagram

If a timer delay is specified, the input to the sequence detector must remain in the defined state for the duration of the timer delay. If the input changes state during the delay, the timer is reset.

The sequence detector can also help to identify monitoring faults. In the sample application shown in Figure 28, the FSEL1 and FSEL2 states first identify which of the VP1, VP2, or VP3 pins has faulted, and then they take appropriate action.

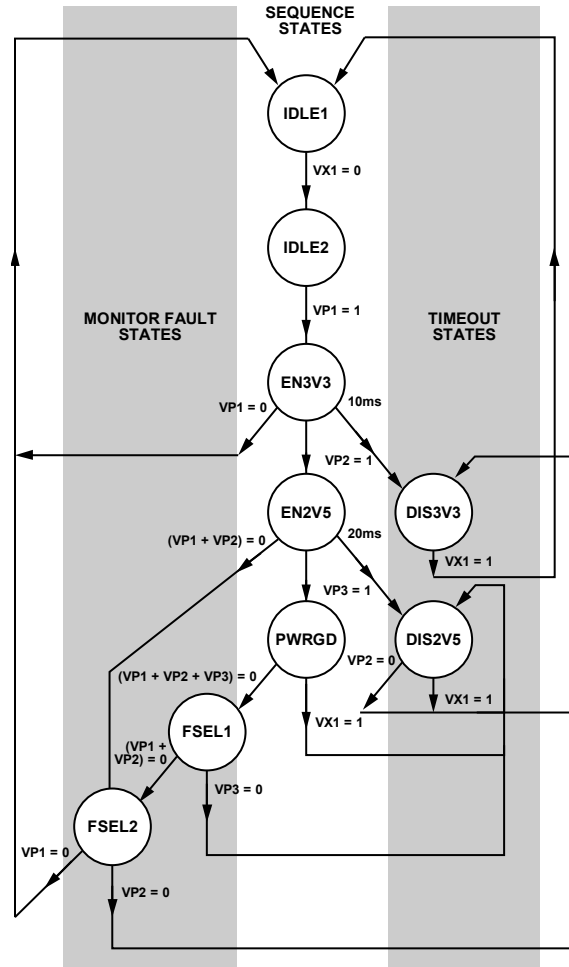


Figure 28. Sample Application Flow Diagram

**Table 8. PDO Outputs for Each State**

PDO Outputs	IDLE1	IDLE2	EN3V3	EN2V5	DIS3V3	DIS2V5	PWRGD	FSEL1	FSEL2
PDO1 = 3V3ON	0	0	1	1	0	1	1	1	1
PDO2 = 2V5ON	0	0	0	1	1	0	1	1	1
PDO3 = FAULT	0	0	0	0	1	1	0	1	1

### Monitoring Fault Detector

The monitoring fault detector block is used to detect a failure on an input. The logical function implementing this is a wide OR gate that can detect when an input deviates from its expected condition. The clearest demonstration of the use of this block is in the PWRGD state, where the monitor block indicates that a failure on one or more of the VPx, VXx, or VH inputs has occurred.

No programmable delay is available in this block because the triggering of a fault condition is likely to be caused by a supply falling out of tolerance. In this situation, the device needs to react as quickly as possible. Some latency occurs when moving out of this state because it takes a finite amount of time (~20  $\mu$ s) for the state configuration to download from EEPROM into the SE. Figure 29 is a block diagram of the monitoring fault detector.

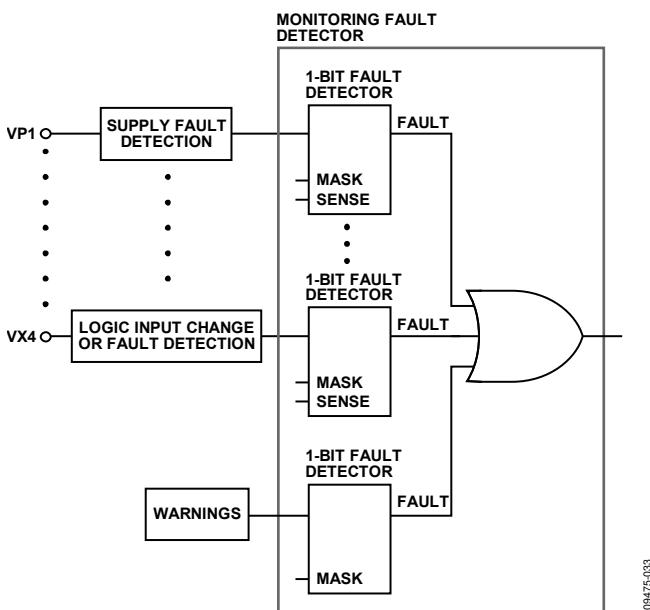


Figure 29. Monitoring Fault Detect or Block Diagram

### Timeout Detector

The timeout detector allows the user to trap a failure to ensure proper progress through a power-up or power-down sequence.

In the sample application shown in Figure 28, the timeout next-state transition is from the EN3V3 and EN2V5 states. For the EN3V3 state, the signal 3V3ON is asserted on the PDO1 output pin upon entry to this state to turn on a 3.3 V supply.

This supply rail is connected to the VP2 pin, and the sequence detector looks for the VP2 pin to go above its undervoltage threshold, which is set in the supply fault detector (SFD) attached to that pin.

The power-up sequence progresses when this change is detected. If, however, the supply fails (perhaps due to a short circuit overloading this supply), the timeout block traps the problem. In this example, if the 3.3 V supply fails within 10 ms, the SE moves to the DIS3V3 state and turns off this supply by bringing PDO1 low. It also indicates that a fault has occurred by taking PDO3 high. Timeout delays of 100  $\mu$ s to 400 ms can be programmed.

### FAULT AND STATUS REPORTING

The ADM1169 has a fault latch for recording faults. Two registers, FSTAT1 and FSTAT2, are set aside for this purpose. A single bit is assigned to each input of the device, and a fault on that input sets the relevant bit. The contents of the fault register can be read out over the SMBus to determine which input(s) faulted. The fault register can be enabled/disabled in each state. To latch data from one state, ensure that the fault latch is disabled in the following state. This ensures that only real faults are captured and not, for example, undervoltage conditions that may be present during a power-up or power-down sequence.

The ADM1169 also has a number of status registers. These include more detailed information, such as whether an undervoltage or overvoltage fault is present on a particular input. The status registers also include information on ADC limit faults.

There are two sets of these registers with different behaviors. The first set of status registers is not latched in any way and, therefore, can change at any time in response to changes on the inputs. These registers provide information such as the UV and OV state of the inputs, the digital state of the GPI VXx inputs, and also the ADC warning limit status.

The second set of registers update each time the sequence engine changes state and are latched until the next state change. The second set of registers provides the same information as the first set, but in a more compact form. The reason for this is that these registers are used by the black box feature when writing status information for the previous state into EEPROM.

See the AN-721 Application Note for full details about the ADM1169 registers.

### NONVOLATILE BLACK BOX FAULT RECORDING

A section of EEPROM, from Address 0xF900 to Address 0xF9FF, is provided that by default can be used to store user-defined settings and information. Part of this section of EEPROM, Address 0xF980 to Address 0xF9FF, can instead be used to store up to 16 fault records.

Any sequencing engine state can be designated as a black box write state. Each time the sequence engine enters that state, a fault record is written into EEPROM. The fault record provides a snapshot of the entire ADM1169 state at the point in time when the last state was exited, just prior to entering the designated black box write state. A fault record contains the following information:

- A flag bit set to 0 after the fault record has been written.
- The state number of the previous state prior to the fault record write state.
- Did a sequence, timeout, or monitor condition cause the previous state to exit?
- UVSTATx and OVSTATx input comparator status.
- VXx GPISTAT status.
- LIMSTATx status.
- A checksum byte.

Each fault record contains eight bytes, with each byte taking typically about 250  $\mu$ s to write to EEPROM, for a total write time of about 2 ms. After the black box begins to write a fault record into EEPROM, the ADM1169 ensures that is complete before attempting to write any additional fault records. This means that if consecutive sequencing engine states are designated as black box write states, then a time delay must be used in the first state to ensure that the fault record is written before moving to the next state.

When the ADM1169 powers on initially, it performs a search to find the first fault record that has not been written to. It does this by checking the flag bit in each fault record until it finds one where the flag bit is 1. The first fault record is stored at Address 0xF980, and at multiples of eight bytes after that, with the last record stored at Address 0xF9F8.

The fault recorder is only able to write in the EEPROM. It is not able to erase the EEPROM prior to writing the fault record. Therefore, to ensure correct operation, it is important that the fault record EEPROM is erased prior to use. When all the EEPROM locations for the fault records are used, no more fault records are written. This ensures that the first fault in any cascading fault is stored and not overwritten and lost.

To avoid the fault recorder filling up and fault records being lost, an application can periodically poll the ADM1169 to determine if there are fault records to be read. Alternatively, one of the PDOx outputs can be used to generate an interrupt for a processor in the fault record write state to signal the need to come and read one or more fault records.

After reading fault records during normal operation, two things must be done before the fault recorder is able to reuse the EEPROM locations. First, the EEPROM section must be erased. The fault recorder must then be reset so that it performs its search again for the first unused location of EEPROM that is available to store a fault record.

### BLACK BOX WRITES WITH NO EXTERNAL SUPPLY

In cases where all the input supplies fail, for example, if the card has been removed from a powered backplane, the state machine can be programmed to trigger a write into the black box EEPROM. The decoupling capacitors on the rail that power the ADM1169 and other loads on the board form an energy reservoir. Depending on the other loads on the board and their behavior as the supply rails drop, there may be sufficient energy in the decoupling capacitors to allow the ADM1169 to write a complete fault record (eight bytes of data).

Typically, it takes 2 ms to write to the eight bytes of a fault record. If the ADM1169 is powered using a 12 V supply on the VH pin, then a UV threshold at 6 V can be set and used as the state machine trigger to start writing a fault record to EEPROM. The higher the threshold is, the earlier the black box write begins, and the more energy available in the decoupling capacitors to ensure it completes successfully.

Provided the VH supply, or another supply connected to a VPx pin, remains above 3.0 V during the time to write, the entire fault record is always written to the EEPROM. In many cases, there should be sufficient decoupling capacitors on a board to power the ADM1169 as it writes into the EEPROM.

In cases where the decoupling capacitors are not able to supply sufficient energy after the board is removed to ensure a complete fault record is written, the value of the capacitor on VDDCAP may be increased. In the worst case, assuming that no energy is supplied to the ADM1169 by the external decoupling capacitors, but that VDDCAP has 4.75 V on it, then a 47  $\mu$ F is sufficient to guarantee that a single complete black box record can be written to the EEPROM.

## VOLTAGE READBACK

The ADM1169 has an on-board, 12-bit, accurate ADC for voltage readback over the SMBus. The ADC has an 8-channel analog mux on the front end. The eight channels consist of the eight SFD inputs (VH, VPx, and VXx). Any or all of these inputs can be selected to be read, in turn, by the ADC. The circuit controlling this operation is called the round-robin circuit. This circuit can be selected to run through its loop of conversions once or continuously. Averaging is also provided for each channel. In this case, the round-robin circuit runs through its loop of conversions 16 times before returning a result for each channel. At the end of this cycle, the results are written to the output registers.

The ADC samples single-sided inputs with respect to the AGND pin. A 0 V input produces Code 0, and an input equal to the voltage on REFIN produces full code (4095 decimal).

The inputs to the ADC come directly from the VXx pins and from the back of the input attenuators on the VPx and VH pins, as shown in Figure 30 and Figure 31.

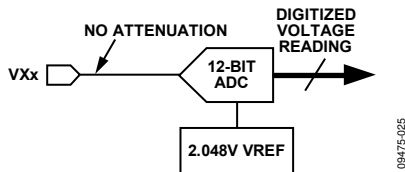


Figure 30. ADC Reading on VXx Pins

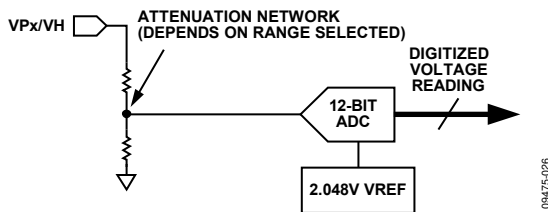


Figure 31. ADC Reading on VPx/VH Pins

The voltage at the input pin can be derived from the following equation:

$$V = \frac{ADC\ Code}{4095} \times Attenuation\ Factor \times V_{REFIN}$$

where  $V_{REFIN} = 2.048\ V$  when the internal reference is used (that is, the REFIN pin is connected to the REFOUT pin).

The ADC input voltage ranges for the SFD input ranges are listed in Table 9.

Table 9. ADC Input Voltage Ranges

SFD Input Range (V)	Attenuation Factor	ADC Input Voltage Range (V)
0.573 to 1.375	1	0 to 2.048
1.25 to 3.00	2.181	0 to 4.46
2.5 to 6.0	4.363	0 to 6.0 <sup>1</sup>
6.0 to 14.4	10.472	0 to 14.4 <sup>1</sup>

<sup>1</sup> The upper limit is the absolute maximum allowed voltage on the VPx and VH pins.

The typical way to supply the reference to the ADC on the REFIN pin is to connect the REFOUT pin to the REFIN pin. REFOUT provides a 2.048 V reference. As such, the supervising range covers less than half the normal ADC range. It is possible, however, to provide the ADC with a more accurate external reference for improved readback accuracy.

Supplies can also be connected to the input pins purely for ADC readback, even though these pins may go above the expected supervisory range limits (but not above the absolute maximum ratings on these pins). For example, a 1.5 V supply connected to the VX1 pin can be correctly read out as an ADC code of approximately  $\frac{3}{4}$  full scale, but it always sits above any supervisory limits that can be set on that pin. The maximum setting for the REFIN pin is 2.048 V.

## SUPPLY SUPERVISION WITH THE ADC

In addition to the readback capability, another level of supervision is provided by the on-chip, 12-bit ADC. The ADM1169 has limit registers with which the user can program a maximum or minimum allowable threshold. Exceeding the threshold generates a warning that can either be read back from the status registers or input into the SE to determine what sequencing action the ADM1169 should take. Only one register is provided for each input channel. Therefore, either an undervoltage threshold or overvoltage threshold (but not both) can be set for a given channel. The round-robin circuit can be enabled via an SMBus write, or it can be programmed to turn on in any state in the SE program. For example, it can be set to start after a power-up sequence is complete, and all supplies are known to be within expected tolerance limits.

Note that a latency is built into this supervision, dictated by the conversion time of the ADC. With all 12 channels selected, the total time for the round-robin operation (averaging off) is approximately 6 ms (500  $\mu$ s per channel selected). Supervision using the ADC, therefore, does not provide the same real-time response as the SFDs.



# SUPPLY MARGINING

## OVERVIEW

It is often necessary for the system designer to adjust supplies, either to optimize their level or force them away from nominal values to characterize the system performance under these conditions. This is a function typically performed during an in-circuit test (ICT), such as when a manufacturer wants to guarantee that a product under test functions correctly at nominal supplies minus 10%.

## OPEN-LOOP SUPPLY MARGINING

The simplest method of margining a supply is to implement an open-loop technique (see Figure 32). A popular way to do this is to switch extra resistors into the feedback node of a power module, such as a dc-to-dc converter or low dropout regulator (LDO). The extra resistor alters the voltage at the feedback or trim node and forces the output voltage to margin up or down by a certain amount.

The ADM1169 can perform open-loop margining for up to four supplies. The four on-board voltage DACs (DAC1 to DAC4) can drive into the feedback pins of the power modules to be margined. The simplest circuit to implement this function is an attenuation resistor that connects the DACx pin to the feedback node of a dc-to-dc converter. When the DACx output voltage is set equal to the feedback voltage, no current flows into the attenuation resistor, and the dc-to-dc converter output voltage does not change. Taking DACx above the feedback voltage forces current into the feedback node, and the output of the dc-to-dc converter is forced

to fall to compensate for this. The dc-to-dc converter output can be forced high by setting the DACx output voltage lower than the feedback node voltage. The series resistor can be split in two, and the node between them can be decoupled with a capacitor to ground. This can help to decouple any noise picked up from the board. Decoupling to a ground local to the dc-to-dc converter is recommended.

The ADM1169 can be commanded to margin a supply up or down over the SMBus by updating the values on the relevant DAC output.

## CLOSED-LOOP SUPPLY MARGINING

A more accurate and comprehensive method of margining is to implement a closed-loop system (see Figure 33). The voltage on the rail to be margined can be read back to accurately margin the rail to the target voltage. The ADM1169 incorporates all the circuits required to do this, with the 12-bit successive approximation ADC used to read back the level of the supervised voltages, and the six voltage output DACs, implemented as described in the Open-Loop Supply Margining section, used to adjust supply levels. These circuits can be used along with other intelligence, such as a microcontroller, to implement a closed-loop margining system that allows any dc-to-dc converter or LDO supply to be set to any voltage, accurate to within  $\pm 0.5\%$  of the target.

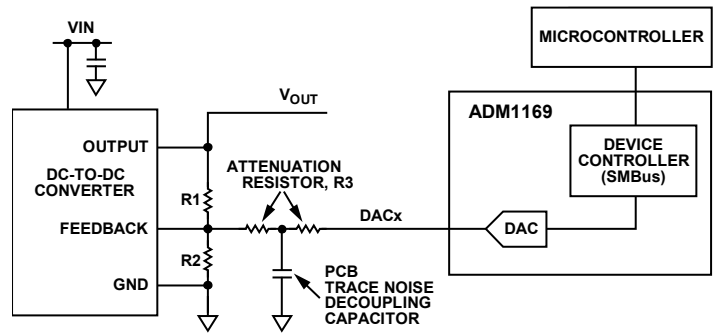


Figure 32. Open-Loop Margining System Using the ADM1169

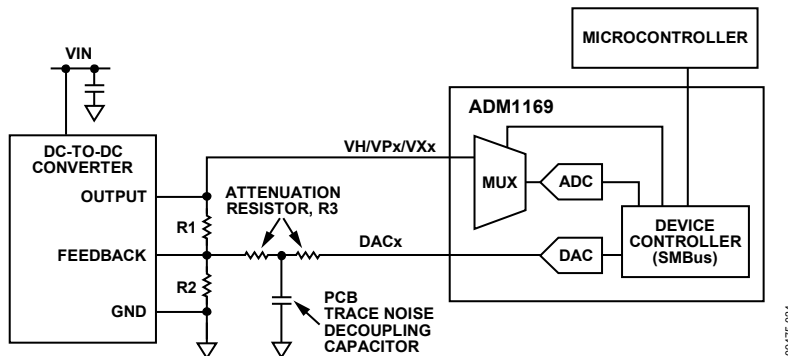


Figure 33. Closed-Loop Margining System Using the ADM1169

To implement closed-loop margining,

1. Disable the four DACx outputs.
2. Set the DAC output voltage equal to the voltage on the feedback node.
3. Enable the DAC.
4. Read the voltage at the dc-to-dc converter output that is connected to one of the VPx, VH, or VXx pins.
5. If necessary, modify the DACx output code up or down to adjust the dc-to-dc converter output voltage. Otherwise, stop because the target voltage has been reached.
6. Set the DAC output voltage to a value that alters the supply output by the required amount (for example,  $\pm 5\%$ ).
7. Repeat Step 4 through Step 6 until the measured supply reaches the target voltage.

Step 1 to Step 3 ensures that when the DACx output buffer is turned on, it has little effect on the dc-to-dc converter output. The DAC output buffer is designed to power up without glitching by first powering up the buffer to follow the pin voltage. It does not drive out onto the pin at this time. When the output buffer is properly enabled, the buffer input is switched over to the DAC, and the output stage of the buffer is turned on. Output glitching is negligible.

## WRITING TO THE DACS

Four DAC ranges are offered. They can be placed with midcode (Code 0x7F) at 0.6 V, 0.8 V, 1.0 V, and 1.25 V. These voltages are placed to correspond to the most common feedback voltages. Centering the DAC outputs in this way provides the best use of the DAC resolution. For most supplies, it is possible to place the DAC midcode at the point where the dc-to-dc converter output is not modified, thereby giving half of the DAC range to margin up and the other half to margin down.

The DAC output voltage is set by the code written to the DACx register. The voltage is linear with the unsigned binary number in this register. Code 0x7F is placed at the midcode voltage, as described previously. The output voltage is given by

$$DAC\ Output = (DACx - 0x7F)/255 \times 0.6015 + V_{OFF}$$

where  $V_{OFF}$  is one of the four offset voltages.

There are 256 DAC settings available. The midcode value is located at DAC Code 0x7F, as close as possible to the middle of the 256 code range. The full output swing of the DACs is +302 mV (+128 codes) and -300 mV (-127 codes) around the selected midcode voltage. The voltage range for each midcode voltage is shown in Table 10.

**Table 10. Ranges for Midcode Voltages**

Midcode Voltage (V)	Minimum Voltage Output (V)	Maximum Voltage Output (V)
0.6	0.300	0.902
0.8	0.500	1.102
1.0	0.700	1.302
1.25	0.950	1.552

## CHOOSING THE SIZE OF THE ATTENUATION RESISTOR

The size of the attenuation resistor, R3, determines how much the DAC voltage swing affects the output voltage of the dc-to-dc converter that is being margined (see Figure 33).

Because the voltage at the feedback pin remains constant, the current flowing from the feedback node to GND through R2 is a constant. In addition, the feedback node itself is high impedance. This means that the current flowing through R1 is the same as the current flowing through R3. Therefore, a direct relationship exists between the extra voltage drop across R1 during margining and the voltage drop across R3.

This relationship is given by

$$\Delta V_{OUT} = \frac{R1}{R3} (V_{FB} - V_{DACOUT})$$

where:

$\Delta V_{OUT}$  is the change in  $V_{OUT}$ .

$V_{FB}$  is the voltage at the feedback node of the dc-to-dc converter.

$V_{DACOUT}$  is the voltage output of the margining DAC.

This equation demonstrates that if the user wants the output voltage to change by  $\pm 300$  mV, then  $R1 = R3$ . If the user wants the output voltage to change by  $\pm 600$  mV,  $R1 = 2 \times R3$ , and so on.

It is best to use the full DAC output range to margin a supply. Choosing the attenuation resistor in this way provides the most resolution from the DAC, meaning that with one DAC code change, the smallest effect on the dc-to-dc converter output voltage is induced. If the resistor is sized up to use a code such as 27 decimal to 227 decimal to move the dc-to-dc converter output by  $\pm 5\%$ , it takes 100 codes to move 5% (each code moves the output by 0.05%). This is beyond the readback accuracy of the ADC, but it should not prevent the user from building a circuit to use the most resolution.

## DAC LIMITING AND OTHER SAFETY FEATURES

Limit registers (called DPLIMx and DNLIMx) on the device offer the user some protection from firmware bugs that can cause catastrophic board problems by forcing supplies beyond their allowable output ranges. Essentially, the DAC code written into the DACx register is clipped such that the code used to set the DAC voltage is given by

DAC Code

$$= DACx, \quad DACx \geq DNLIMx \text{ and } DACx \leq DPLIMx$$

$$= DNLIMx, \quad DACx < DNLIMx$$

$$= DPLIMx, \quad DACx > DPLIMx$$

In addition, the DAC output buffer is three-stated if  $DNLIMx > DPLIMx$ . By programming the limit registers this way, the user can make it very difficult for the DAC output buffers to be turned on during normal system operation. The limit registers are among the registers downloaded from EEPROM at startup.