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### FEATURES

- Complete supervisory and sequencing solution for up to 10 supplies per device**
- Interchip bus (ICB) simplifies multidevice connections and sequencing system operation**
- Supports up to 4 devices**
- 16 event deep black box nonvolatile fault recording**
- 10 supply fault detectors enable supervision of supplies**
  - <0.5% accuracy at all voltages at 25°C
  - <1.0% accuracy across all voltages and temperatures
- 5 selectable input attenuators allow supervision of supplies**
  - 14.4 V on VH and 6.0 V on VP1 to VP4 (VPx)
- 5 dual function inputs: VX1 to VX5 (VXx)**
  - High impedance input to supply fault detector with thresholds between 0.573 V and 1.375 V
  - General-purpose logic input
- 10 programmable driver outputs: PDO1 to PDO10 (PDOx)**
  - Open-collector with an external pull-up resistor
  - Push/pull output, driven to VDDCAP or VPx
  - Open-collector with weak pull-up to VDDCAP or VPx
  - Internally charge pumped high drive for use with external N-FET (PDO1 to PDO6 only)
- Sequencing engine (SE) implements state machine control of the PDOx outputs**
  - State changes conditional on input events
  - Enables complex control of boards
  - Power-up and power-down sequence control
  - Fault event handling
  - Interrupt generation on warnings
  - Watchdog function can be integrated in the SE
  - Program software control of sequencing through the SMBus
- Complete voltage margining solution for 6 voltage rails**
- 6 output voltage 8-bit DACs (0.300 V to 1.552 V) allow voltage adjustment via dc-to-dc converter trim/feedback node**
- 12-bit ADC for readback of all supervised voltages**
- Reference input (REFIN) with two input options**
  - Driven directly from the 2.048 V ( $\pm 0.25\%$ ) REFOUT pin
  - External reference for improved ADC performance
- Powered by the highest voltage on either VPx or VH**
  - Voltage on VPx or VH must be greater than the undervoltage lockout (UVLO) threshold
- Electronically erasable programmable read-only memory (EEPROM)**
- Industry-standard, 2-wire bus interface (SMBus)**
- PDOx pins guaranteed low with VH and VPx = 1.2 V**
- Available in a 40-lead, 6 mm  $\times$  6 mm LFCSP package**

### FUNCTIONAL BLOCK DIAGRAM

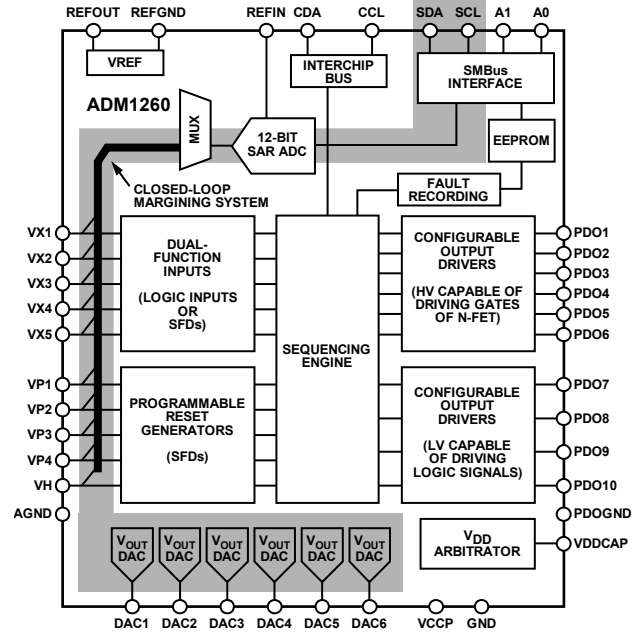


Figure 1.

### APPLICATIONS

- Central office systems
- Servers/routers
- Multivoltage system line cards
- Digital signal processor (DSP)/field programmable gate array (FPGA) supply sequencing
- In-circuit testing of margined supplies

# ADM1260\* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

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## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- ADM1260 Evaluation Board

## DOCUMENTATION

### Application Notes

- AN-1418: Programming the ADM1260 Using a Hexadecimal (HEX) File and Restarting the Sequence

### Data Sheet

- ADM1260: Super Sequencer with Interchip Bus and Nonvolatile Fault Recording Data Sheet

### User Guides

- UG-932: Evaluating the ADM1260 Super Sequencer with Interchip Bus and Nonvolatile Fault Recording

## DESIGN RESOURCES

- ADM1260 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all ADM1260 EngineerZone Discussions.

## SAMPLE AND BUY

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**REVISION HISTORY**

4/16—Revision 0: Initial Version

## GENERAL DESCRIPTION

The **ADM1260** Super Sequencer® is a configurable supervisory/sequencing device that offers a single-chip solution for supply monitoring and sequencing in multiple supply systems.

A high speed interchip bus (ICB) allows multiple devices to be easily linked together. It is possible to create a system capable of sequencing up to 40 supplies and monitoring up to 37 supplies. Using the **ADI Power Studio™** software, the operation of the ICB is transparent to the user, making multiple devices appear to operate as a single virtual sequencer.

In addition to these functions, the **ADM1260** integrates a 12-bit analog-to-digital converter (ADC) and six 8-bit voltage output digital-to-analog converters (DACs). Use the ADC and the DACs to implement a closed-loop margining system that enables supply adjustment by altering either the feedback node or the reference of a dc-to-dc converter using the DAC outputs.

Supply margining can be performed with a minimum of external components. The margining loop can be used for in-circuit testing of a board during production (for example, to verify board functionality at -5% of nominal supplies), or it can be used dynamically to accurately control the output voltage of a dc-to-dc converter.

The device also provides up to 10 programmable inputs for monitoring undervoltage faults, overvoltage faults, or out of window faults on up to 10 supplies. In addition, 10 programmable outputs can be used as logic enables. Six of these programmable outputs can also provide an output of up to 12 V for driving the gate of an N-FET that can be placed in the path of a supply.

The logical core of the device is a sequencing engine (SE). This state machine-based construction provides up to 61 different states. This design enables very flexible sequencing of the outputs, based on the condition of the inputs.

A block of nonvolatile EEPROM is available that can be used to store user defined information and can also be used to hold a number of fault records that are written by the sequencing engine, as defined by the user when a particular fault or sequence occurs.

The device is controlled via configuration data that can be programmed into an EEPROM. The entire configuration can be programmed using an intuitive graphical user interface (GUI)-based software package provided by Analog Devices, Inc., the **ADI Power Studio** software.

### DETAILED FUNCTIONAL BLOCK DIAGRAM

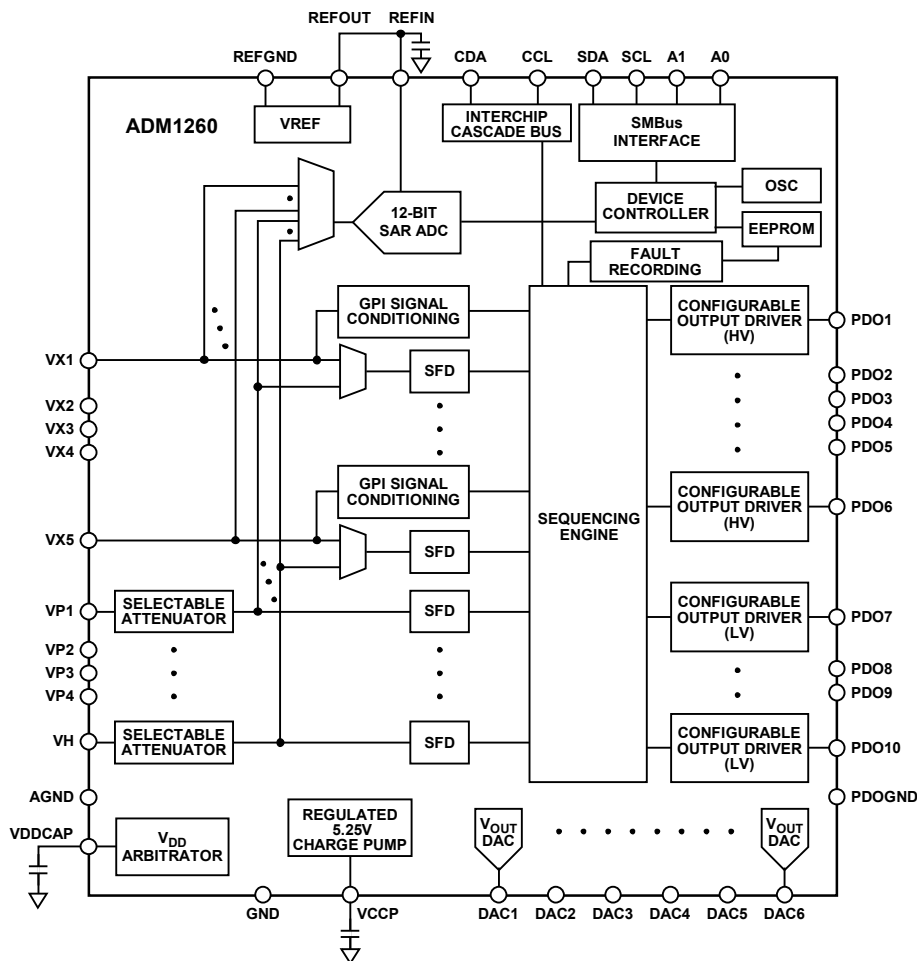


Figure 2. Detailed Functional Block Diagram

## SPECIFICATIONS

V<sub>H</sub> = 3.0 V to 14.4 V,<sup>1</sup> V<sub>Px</sub> = 3.0 V to 6.0 V,<sup>1</sup> T<sub>A</sub> = -40°C to +85°C, unless otherwise noted.

**Table 1.**

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
<b>POWER SUPPLY ARBITRATION</b>					
V <sub>H</sub> , V <sub>Px</sub>	3.0			V	Minimum supply required on one of V <sub>Px</sub> or V <sub>H</sub> pins
V <sub>Px</sub>			6.0	V	Maximum V <sub>DDCAP</sub> = 5.1 V, typical
V <sub>H</sub>			14.4	V	V <sub>DDCAP</sub> = 4.75 V
V <sub>DDCAP</sub>	2.7	4.75	5.4	V	Regulated low dropout (LDO) output
C <sub>VDDCAP</sub>	10			μF	Minimum recommended decoupling capacitance
<b>POWER SUPPLY</b>					
Supply Current, I <sub>VH</sub> , I <sub>VPx</sub>		4.5	6.5	mA	V <sub>DDCAP</sub> = 4.75 V, PDO1 to PDO10 off, DACs off, ADC off
Additional Currents					
All PDOx FET Drivers On		1		mA	V <sub>DDCAP</sub> = 4.75 V, PDO1 to PDO6 loaded with 1 μA each, PDO7 to PDO10 off
Current Available from V <sub>DDCAP</sub>			2	mA	Maximum additional load that can be drawn from all PDO pull-ups to V <sub>DDCAP</sub>
DAC Supply Currents		2.2		mA	Six DACs on with 100 μA maximum load on each
ADC Supply Current		1		mA	Running round robin loop
EEPROM Erase Current		10		mA	1 ms duration only, V <sub>DDCAP</sub> = 3 V
<b>SUPPLY FAULT DETECTORS</b>					
<b>V<sub>H</sub></b>					
Input Impedance		52		kΩ	
Input Attenuator Error		±0.05		%	Midrange and high range
Detection Ranges					
High Range	6.0		14.4	V	
Midrange	2.5		6.0	V	
<b>V<sub>Px</sub></b>					
Input Impedance		52		kΩ	
Input Attenuator Error		±0.05		%	Low range and midrange
Detection Ranges					
Midrange	2.5		6.0	V	
Low Range	1.25		3.00	V	
Ultralow Range	0.573		1.375	V	No input attenuation error
<b>V<sub>Xx</sub></b>					
Input Impedance	1			MΩ	
Detection Range					
Ultralow Range	0.573		1.375	V	No input attenuation error
Absolute Accuracy			±1	%	V <sub>REF</sub> error + DAC nonlinearity + comparator offset error + input attenuation error (±0.5% at 25°C)
Threshold Resolution		8		Bits	
Digital Glitch Filter		0		μs	Minimum programmable filter length
		100		μs	Maximum programmable filter length

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments	
<b>ANALOG-TO-DIGITAL CONVERTER</b>						
Signal Range	0		$V_{REFIN}$	V	The ADC can convert signals presented to the VH, VPx, and VXx pins; the VPx and VH input signals are attenuated depending on the selected range; a signal at the pin corresponding to the selected range is from 0.573 V to 1.375 V at the ADC input	
Input Reference Voltage on REFIN Pin, $V_{REFIN}$		2.048		V		
Resolution		12		Bits		
Integral Nonlinearity (INL)			$\pm 2.5$	LSB		Endpoint corrected, $V_{REFIN} = 2.048$ V
Gain Error			$\pm 0.05$	%		$V_{REFIN} = 2.048$ V
Conversion Time		0.44		ms		One conversion on one channel
Offset Error		84		ms		All 12 channels selected, 16x averaging enabled
Input Noise		0.25	$\pm 2$	LSB	$V_{REFIN} = 2.048$ V	
				LSB rms	Direct input (no attenuator)	
<b>BUFFERED VOLTAGE OUTPUT DACs</b>						
Resolution		8		Bits	Six DACs are individually selectable for centering on one of four output voltage ranges	
Code 0x7F Output Voltage						
Range 1	0.592	0.6	0.603	V		
Range 2	0.796	0.8	0.803	V		
Range 3	0.996	1	1.003	V		
Range 4	1.246	1.25	1.253	V		
Output Voltage		601.25		mV		Reflects the DAC output voltage range, independent of center point
LSB Step Size		2.36		mV		
INL			$\pm 0.75$	LSB		Endpoint corrected
DNL			$\pm 0.4$	LSB		
Gain Error			1	%		
Maximum Load Current						
Source		100		$\mu$ A		
Sink		100		$\mu$ A		
Maximum Load Capacitance			50	pF		
Settling Time to 50 pF Load			2	$\mu$ s		
Load Regulation		2.5		mV	Per mA	
Power Supply Rejection Ratio (PSRR)		60		dB	DC	
		40		dB	100 mV step in 20 ns with 50 pF load	
<b>REFERENCE OUTPUT</b>						
Reference Output Voltage	2.043	2.048	2.053	V	No load	
Load Regulation		-0.25		mV	Sourcing current, $I_{DACMAX} = -100$ $\mu$ A	
		0.25		mV	Sinking current, $I_{DACMAX} = 100$ $\mu$ A	
Minimum Load Capacitance	1			$\mu$ F	Capacitor required for decoupling, stability	
PSRR		60		dB	DC	
<b>PROGRAMMABLE DRIVER OUTPUTS</b>						
High Voltage Charge Pump Mode (PDO1 to PDO6)						
Output Impedance		500		k $\Omega$		
Output Voltage When PDOx is High ( $V_{OH}$ )	11	12.5	14	V	Current drawn when PDOx is high ( $I_{OH}$ ) = 0 $\mu$ A	
	10.5	12	13.5	V	$I_{OH} = 1$ $\mu$ A	
	8	10	13.5	V	$I_{OH} = 7$ $\mu$ A <sup>2</sup>	
Average Output Current ( $I_{OUTAVG}$ )		20		$\mu$ A	$2$ V < $V_{OH}$ < 7 V	



Parameter	Min	Typ	Max	Unit	Test Conditions/Comments	
Standard (Digital Output) Mode (PDO1 to PDO10) $V_{OH}$	2.4		4.5	V	Pull-up resistor to VDDCAP or VPx ( $V_{PU}$ ) = 2.7 V, $I_{OH}$ = 0.5 mA $V_{PU}$ to VPx = 6.0 V, $I_{OH}$ = 0 mA $V_{PU} \leq 2.7$ V, $I_{OH}$ = 0.5 mA	
	$V_{PU} - 0.3$			V		
Output Voltage When PDOx is Low ( $V_{OL}$ )	0		0.50	V		
Output Sink Current When PDOx is Low ( $I_{OL}^2$ )			20	mA	Maximum sink current per PDOx pin	
Total Sink Current of PDOx Pins ( $I_{SINK}^2$ )			60	mA	Maximum total sink for all PDOx pins	
$R_{PULL-UP}$	16	20	29	k $\Omega$	Internal pull-up resistor	
Maximum Current Drawn from VPx When PDOx is Internally Pulled Up to VPx ( $I_{SOURCE}^2$ )			2	mA	Current load on any VPx pull-up resistors, that is, the total source current available through any number of the PDOx pull-up switches configured onto any one VPx pin	
Three-State Output Leakage Current			10	$\mu$ A	$V_{PDO} = 14.4$ V	
Oscillator Frequency	90	100	110	kHz	All on-chip time delays are derived from this clock	
<b>DIGITAL INPUTS (VXx, A0, A1)</b>						
Input Voltage High, $V_{IH}$	2.0			V	Maximum $V_{IN} = 5.5$ V Maximum $V_{IN} = 5.5$ V	
Input Voltage Low, $V_{IL}$			0.8	V		
Input Current High, $I_{IH}$	-1			$\mu$ A	$V_{IN} = 5.5$ V $V_{IN} = 0$ V	
Input Current Low, $I_{IL}$			1	$\mu$ A		
Input Capacitance		5		pF	$V_{DDCAP} = 4.75$ V, $T_A = 25^\circ\text{C}$ , if known logic state is required	
Programmable Pull-Down Current, $I_{PULL-DOWN}$		20		$\mu$ A		
<b>SERIAL BUS, ICB DIGITAL INPUTS/ OUTPUT (SDA, SCL, CDA, CCL)</b>						
Input Voltage High, $V_{IH}$	2.0			V	$V_{IN} = 0$ V $I_{OUT} = -3.0$ mA	
Input Voltage Low, $V_{IL}$			0.8	V		
Input Low Current, $I_{IL}$			1	$\mu$ A		
Output Low Voltage, $V_{OL}^2$			0.4	V	$V_{OL} = 0.4$ V	
CDA, CCL Input Glitch Filter, $t_{SP}$		50		ns		
CDA, CCL Output Low Current, $I_{OL}$			5	mA		
<b>SDA, SCL SERIAL BUS TIMING<sup>3</sup></b>						
Clock Frequency, $f_{SCLK}$			400	kHz	See Figure 40	
Bus Free Time, $t_{BUF}$				$\mu$ s		
Start Setup Time, $t_{SU,STA}$	1.3			$\mu$ s		
Stop Setup Time, $t_{SU,STO}$	0.6			$\mu$ s		
Start Hold Time, $t_{HD,STA}$	0.6			$\mu$ s		
SCL Low Time, $t_{LOW}$	0.6			$\mu$ s		
SCL High Time, $t_{HIGH}$	1.3			$\mu$ s		
SCL, SDA Rise Time, $t_R$	0.6		300	ns		
SCL, SDA Fall Time, $t_F$			300	ns		
Data Setup Time, $t_{SU,DAT}$	100			ns		
Data Hold Time, $t_{HD,DAT}$	250			ns		
<b>CDA, CCL SERIAL BUS<sup>3</sup></b>						
Clock Frequency, $f_{SCLK}$			400	kHz		$I_{OL} = 5$ mA
Bus Capacitance			240	pF		
Pin Capacitance			10	pF		

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SEQUENCING ENGINE TIMING					
State Change Time		45		μs	
Black Box (Exit)		350		μs	With delay or timeout configured as 0 μs in the state

<sup>1</sup> At least one of the VH and VPx pins must be  $\geq 3.0$  V to maintain the device supply on VDDCAP.

<sup>2</sup> Specification is not production tested but is supported by characterization data at initial product release.

<sup>3</sup> Guaranteed by design.

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VH	16 V
VPx	7 V
VXx	-0.3 V to +6.5 V
A0, A1	-0.3 V to +7 V
REFIN, REFOUT	5 V
VDDCAP, VCCP	6.5 V
DACx	6.5 V
PDOx	16 V
SDA, SCL, CDA, CCL	7 V
GND, AGND, PDOGND, REFGND	-0.3 V to +0.3 V
Input Current at Any Pin	±5 mA
Package Input Current	±20 mA
Maximum Junction Temperature (T <sub>JMAX</sub> )	150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature	
Soldering Vapor Phase, 60 sec	215°C
ESD Rating, All Pins	2000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

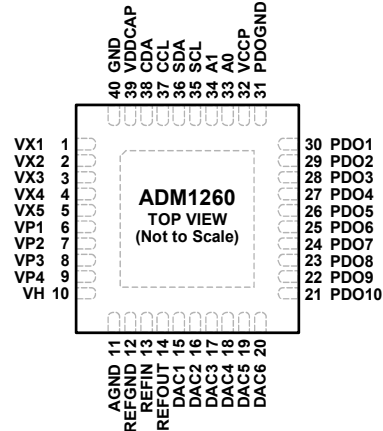
Package Type	$\theta_{JA}$	Unit
40-Lead LFCSP	26.5	°C/W

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



## NOTES

1. EXPOSED PAD. THIS PAD IS A NO CONNECT (NC). IF POSSIBLE, SOLDER THIS PAD TO THE BOARD FOR IMPROVED MECHANICAL STABILITY. THE EXPOSED PAD MAY BE CONNECTED TO GROUND, THOUGH THIS CONNECTION IS NOT REQUIRED.

12445-003

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 5	VX1 to VX5 (VXx)	High Impedance Inputs to Supply the Fault Detectors. Fault thresholds can be set from 0.573 V to 1.375 V. Alternatively, use these pins as general-purpose logic inputs.
6 to 9	VP1 to VP4 (VPx)	Low Voltage Inputs to Supply the Fault Detectors. Three input ranges can be set by altering the input attenuation on a potential divider connected to these pins, the output of which connects to a supply fault detector. These pins allow thresholds from 2.5 V to 6.0 V, from 1.25 V to 3.00 V, and from 0.573 V to 1.375 V.
10	VH	High Voltage Input to Supply the Fault Detectors. Two input ranges can be set by altering the input attenuation on a potential divider connected to this pin, the output of which connects to a supply fault detector. This pin allows thresholds from 6.0 V to 14.4 V and from 2.5 V to 6.0 V.
11	AGND <sup>1</sup>	Ground Return for Input Attenuators.
12	REFGND <sup>1</sup>	Ground Return for On-Chip Reference Circuits.
13	REFIN	Reference Input for the ADC. This pin is nominally 2.048 V and must be driven by a reference voltage. Use the on-board reference by connecting the REFOUT pin to the REFIN pin.
14	REFOUT	Reference Output, 2.048 V. This pin is typically connected to REFIN. Note that the recommended 10 $\mu$ F capacitor must be connected between this pin and REFGND.
15 to 20	DAC1 to DAC6	Voltage Output DACs. These pins default to high impedance at power-up.
21 to 30	PDO10 to PDO1	Programmable Driver Outputs.
31	PDOGND <sup>1</sup>	Ground Return for Driver Outputs.
32	VCCP	Central Charge Pump Voltage of 5.25 V (Positive/Negative). A reservoir capacitor must be connected between this pin and GND. A 10 $\mu$ F capacitor is recommended for this purpose.
33	A0	Logic Input 0. This pin sets the seventh bit of the SMBus interface address.
34	A1	Logic Input 1. This pin sets the sixth bit of the SMBus interface address.
35	SCL	SMBus Clock. This pin is a bidirectional, open-drain pin that requires an external pull-up resistor.
36	SDA	SMBus Data. This pin is a bidirectional, open-drain pin that requires an external pull-up resistor.
37	CCL	ICB Clock. This pin is a bidirectional, open-drain pin that requires an external pull-up resistor.
38	CDA	ICB Data. This pin is a bidirectional, open-drain pin that requires an external pull-up resistor.
39	VDDCAP	Device Supply Voltage. This pin is linearly regulated from the highest of the VPx and VH pins to a typical of 4.75 V. Note that the minimum 10 $\mu$ F capacitor must be connected between this pin and GND.
40	GND <sup>1</sup> EPAD	Supply Ground. Exposed Pad. This pad is a no connect (NC). If possible, solder this pad to the board for improved mechanical stability. The exposed pad may be connected to ground, though this connection is not required.

<sup>1</sup> In a typical application, all ground pins are connected together.

TYPICAL PERFORMANCE CHARACTERISTICS

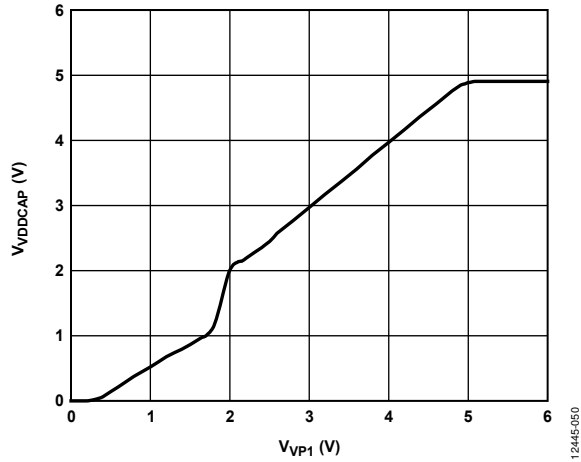


Figure 4.  $V_{DDCAP}$  vs.  $V_{VP1}$

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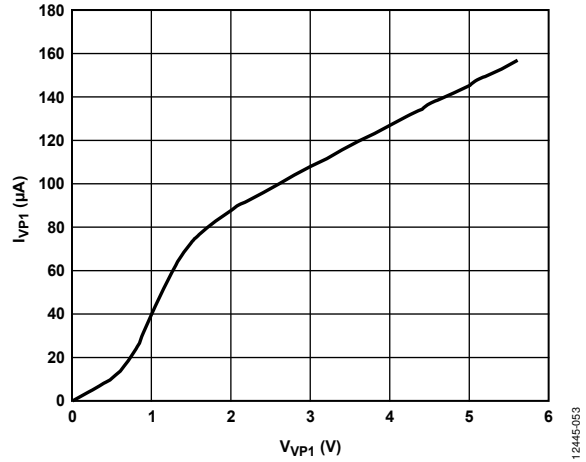


Figure 7.  $I_{VP1}$  vs.  $V_{VP1}$  (VP1 Not the Supply)

12445-053

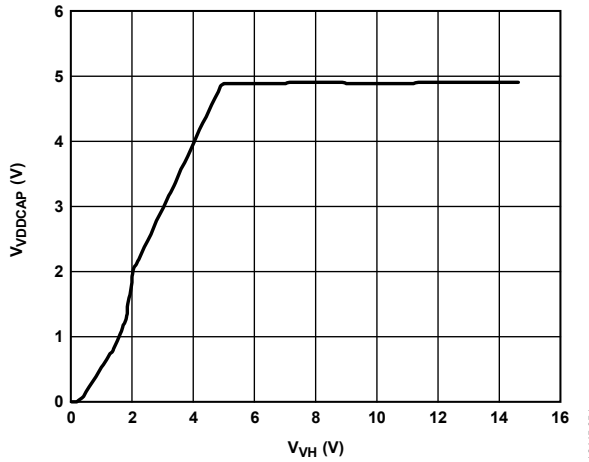


Figure 5.  $V_{DDCAP}$  vs.  $V_{VH}$

12445-051

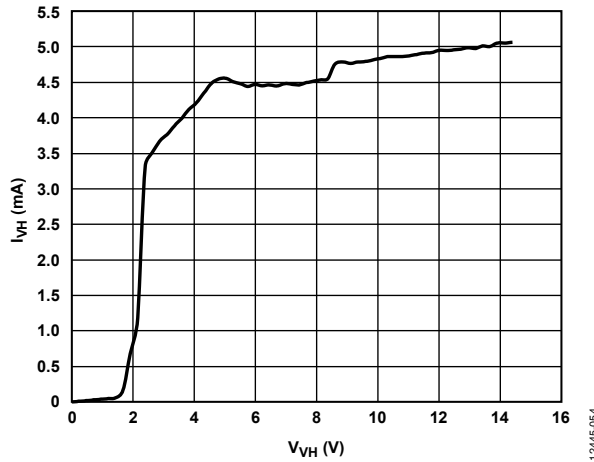


Figure 8.  $I_{VH}$  vs.  $V_{VH}$  (VH as the Supply)

12445-054

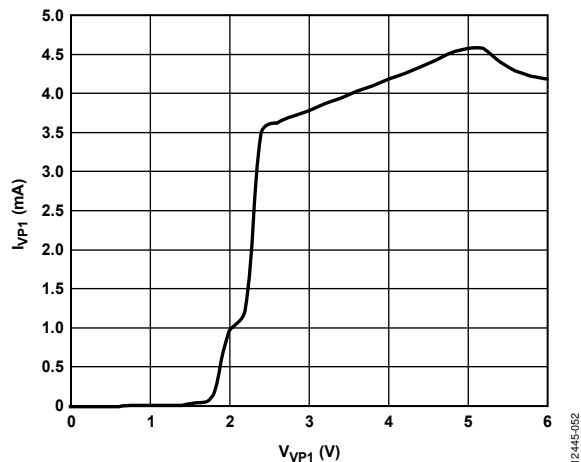


Figure 6.  $I_{VP1}$  vs.  $V_{VP1}$  (VP1 as the Supply)

12445-052

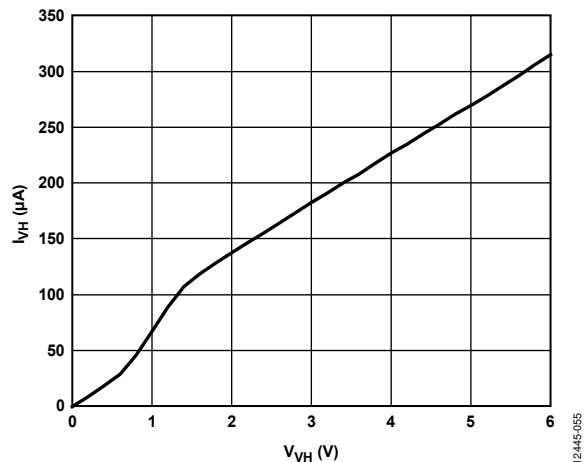


Figure 9.  $I_{VH}$  vs.  $V_{VH}$  (VH Not the Supply)

12445-055

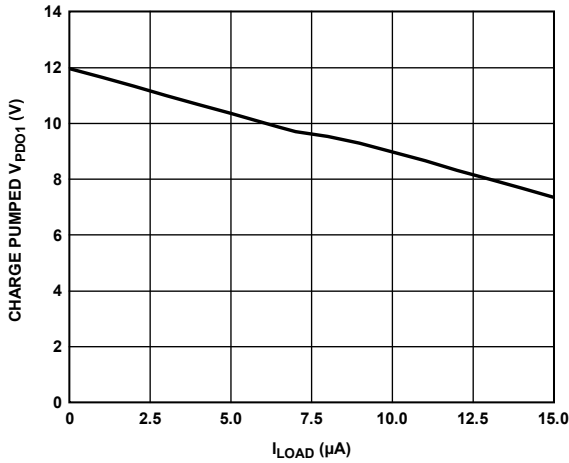


Figure 10. Charge Pumped  $V_{PDO1}$  (FET Drive Mode) vs.  $I_{LOAD}$

12445-056

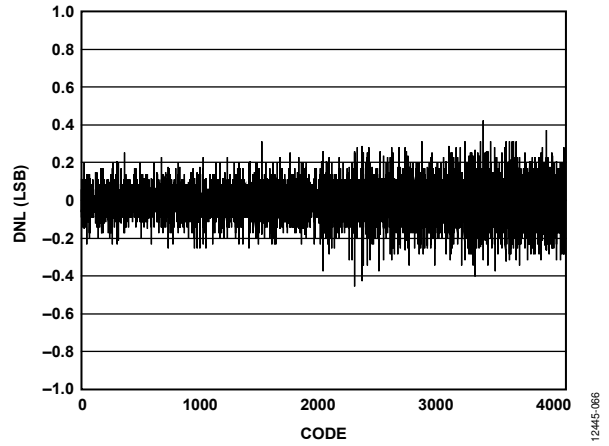


Figure 13. DNL for the ADC

12445-066

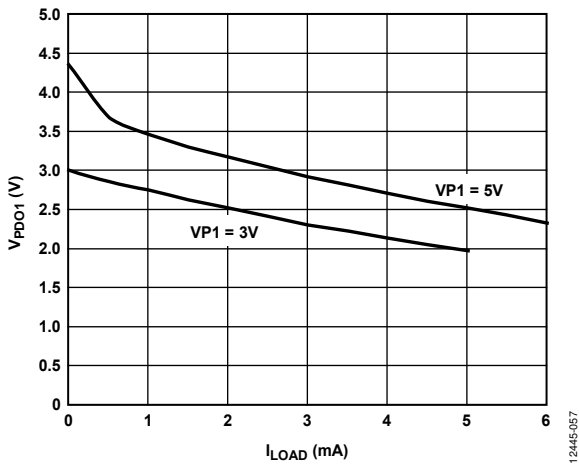


Figure 11.  $V_{PDO1}$  (Strong Pull-Up to  $VPX$ ) vs.  $I_{LOAD}$

12445-057

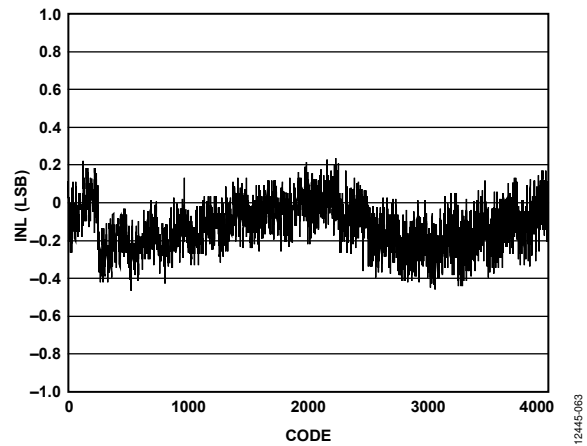


Figure 14. INL for the ADC

12445-063

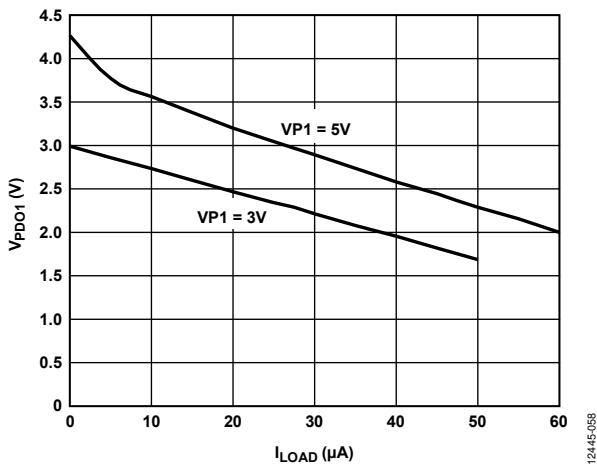


Figure 12.  $V_{PDO1}$  (Weak Pull-Up to  $VPX$ ) vs.  $I_{LOAD}$

12445-058

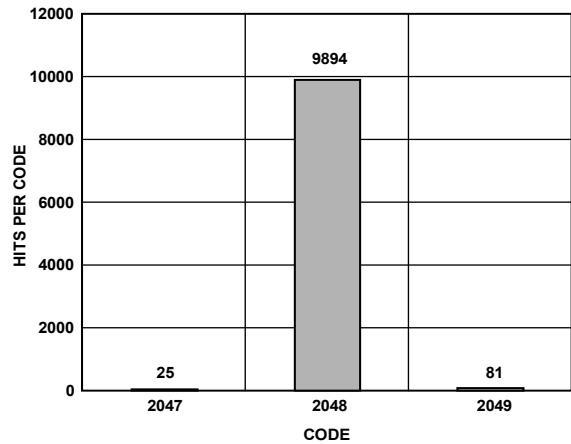


Figure 15. ADC Noise, Midcode Input, 10,000 Reads

12445-064

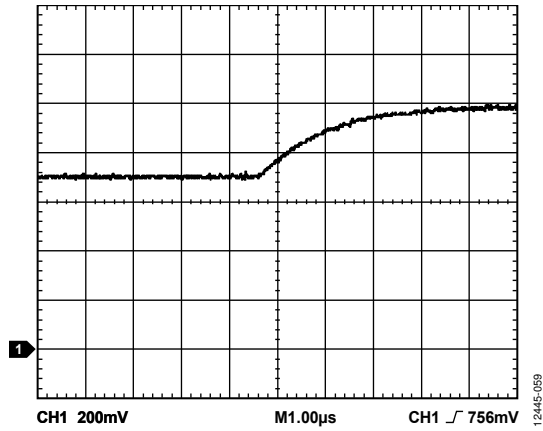


Figure 16. Transient Response of the DAC Code Change into a Typical Load (See Figure 20 for the Corresponding Probe Point Diagram)

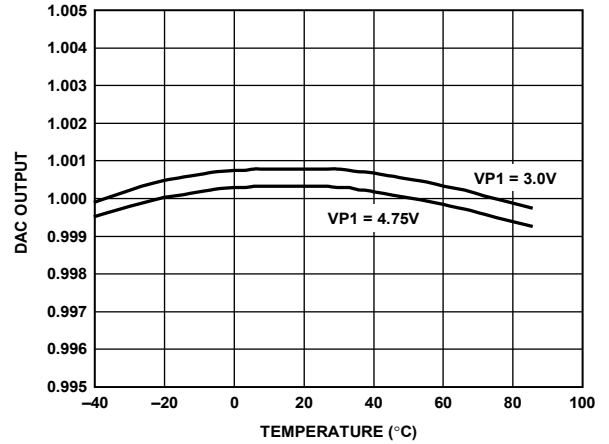


Figure 18. DAC Output vs. Temperature

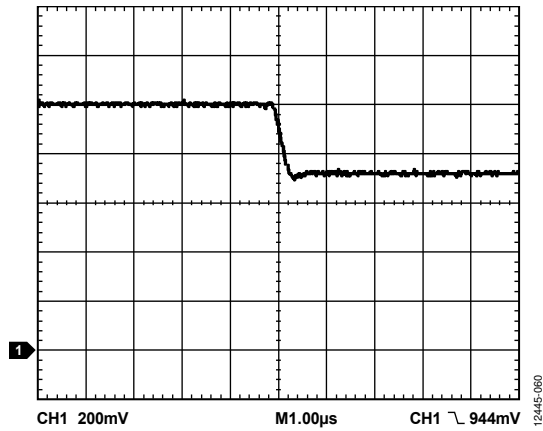


Figure 17. Transient Response of a DAC to Turn On from a High-Z State (See Figure 21 for the Corresponding Probe Point Diagram)

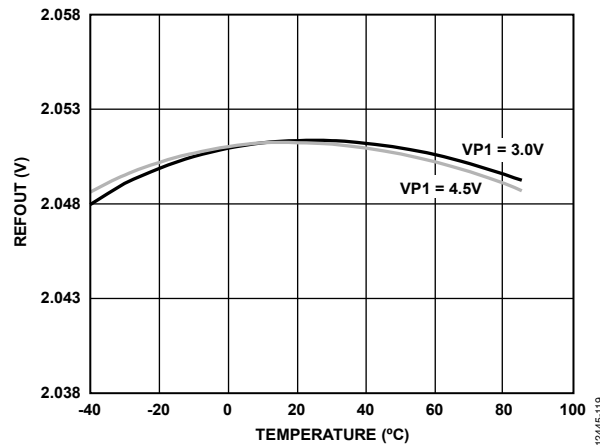


Figure 19. REFOUT vs. Temperature

TEST CIRCUITS

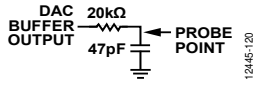


Figure 20. Probe Point for Transient Response of the DAC Code Change into a Typical Load (See Figure 16 for the Corresponding Graph)

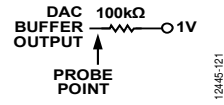


Figure 21. Probe Point for Transient Response of a DAC to Turn On from a High-Z State (See Figure 17 for the Corresponding Graph)



## POWERING THE ADM1260

The **ADM1260** is powered from the highest voltage input on either the positive only supply inputs (VPx) or the high voltage supply input (VH). This technique offers improved redundancy because the device is not dependent on any particular voltage rail to keep it operational. The same pins are used for supply fault detection (see the Supply Supervision section). A  $V_{DD}$  arbitrator on the device chooses which supply to use. The arbitrator can be considered an OR'ing of five low dropout regulators (LDOs) together. A supply comparator chooses the highest input to provide the on-chip supply. There is minimal switching loss with this architecture ( $\sim 0.2$  V), resulting in the ability to power the **ADM1260** from a supply as low as 3.0 V. Note that the supply on the VXX pins cannot be used to power the device.

An external capacitor to GND is required to decouple the on-chip supply from noise. Connect this capacitor to the VDDCAP pin, as shown in Figure 22. The capacitor has another use during a brownout (a momentary loss of power). Under these conditions, when the input supply (VPx or VH) dips transiently below  $V_{DD}$ , the synchronous rectifier switch immediately turns off so that it does not pull  $V_{DD}$  down. The  $V_{DD}$  capacitor can then act as a reservoir to keep the device active until the next highest supply takes over the powering of the device. A 10  $\mu$ F capacitor is recommended for this reservoir/decoupling function.

The value of the VDDCAP capacitor may be increased if it is necessary to guarantee that a complete fault record is written into the EEPROM if all supplies fail. The value of the recommended capacitor is discussed in the Black Box Writes with No External Supply section.

The VH input pin accommodates supplies of up to 14.4 V, which allows the **ADM1260** to be powered using a 12 V backplane supply. In cases where this 12 V supply is hot swapped, it is recommended that the **ADM1260** not be connected directly to the supply. Take suitable precautions, such as the use of a hot swap controller or RC filter network, to protect the device from transients that can cause damage during hot swap events.

When two or more supplies are within 100 mV of each other, the supply that first takes control of  $V_{DD}$  maintains control. For example, if VP1 is connected to a 3.3 V supply,  $V_{DD}$  powers up to approximately 3.1 V through VP1. If VP2 is then connected to another 3.3 V supply, VP1 still powers the device, unless VP2 goes 100 mV higher than VP1.

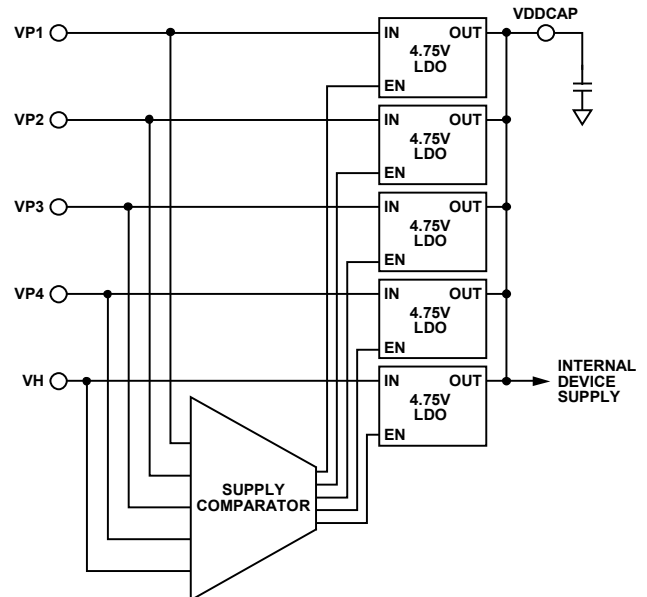


Figure 22.  $V_{DD}$  Arbitrator Operation

In a system where multiple **ADM1260** devices are on the same ICB, these devices must power up using the same supply rail. This simultaneous power-up is due to the requirement that all the devices on the same ICB be synchronized before they start sequencing.

### SLEW RATE CONSIDERATIONS

When the ambient operating temperature is less than approximately  $-20^{\circ}\text{C}$ , and in the event of a power loss where all the supply inputs fail for less than a few hundreds of milliseconds (for example, due to a system supply brownout), it is recommended that the supply voltage recover with a ramp rate of at least 1.5 V/ms or less than 0.5 V/ms.

# INPUTS

## SUPPLY SUPERVISION

The ADM1260 has 10 programmable inputs. Five of these inputs are dedicated supply fault detectors (SFDs). These dedicated inputs are VH and VPx (VP1 to VP4) by default. The other five inputs are VXx (VX1 to VX5) and have dual functionality. These dual function inputs can be used either as SFDs, with functionality similar to that of VH and VPx, or as CMOS-/TTL-compatible logic inputs to the device. Therefore, the ADM1260 can have up to 10 analog inputs, a minimum of five analog inputs and five digital inputs, or a combination thereof. If an input is used as an analog input, it cannot be used as a digital input. Therefore, a configuration requiring 10 analog inputs has no available digital inputs. Table 6 shows the details of each input.

## PROGRAMMING THE SUPPLY FAULT DETECTORS

The ADM1260 can have up to 10 SFDs on its 10 input channels. These highly programmable reset generators enable the supervision of up to 10 supply voltages. The supplies can be as low as 0.573 V and as high as 14.4 V. The inputs can be configured to detect an undervoltage fault (the input voltage drops below a preprogrammed value), an overvoltage fault (the input voltage rises above a preprogrammed value), or an out of window fault (the input voltage is outside a preprogrammed range). The thresholds can be programmed to an 8-bit resolution in registers provided in the ADM1260. This 8-bit resolution translates to a voltage resolution that is dependent on the range selected.

The resolution is given by

$$\text{Step Size} = \text{Threshold Range}/255$$

Therefore, if the high range is selected on VH, calculate the step size as

$$(14.4 \text{ V} - 6.0 \text{ V})/255 = 32.9 \text{ mV}$$

Table 5 lists the upper and lower limits of each available range, the bottom of each range ( $V_B$ ), and the range itself ( $V_R$ ).

Table 5. Voltage Range Limits

Voltage Range (V)	$V_B$ (V)	$V_R$ (V)
0.573 to 1.375	0.573	0.802
1.25 to 3.00	1.25	1.75
2.5 to 6.0	2.5	3.5
6.0 to 14.4	6.0	8.4

The threshold value required is given by

$$V_T = (V_R \times N)/255 + V_B$$

where:

$V_T$  is the desired threshold voltage (undervoltage or overvoltage).

$V_R$  is the voltage range.

$N$  is the decimal value of the 8-bit code.

$V_B$  is the bottom of the range.

Reversing the equation, the code for a desired threshold is given by

$$N = 255 \times (V_T - V_B)/V_R$$

For example, if the user wants to set a 5 V overvoltage threshold on VP1, the code to be programmed in the PS1OVTH register is given by

$$N = 255 \times (5 - 2.5)/3.5$$

Therefore,  $N = 182$  (1011 0110 or 0xB6).

## INPUT COMPARATOR HYSTERESIS

The undervoltage and overvoltage comparators shown in Figure 23 are always monitoring VPx. To avoid chatter (multiple transitions when the input is very close to the set threshold level), these comparators have digitally programmable hysteresis. The hysteresis can be programmed up to the values shown in Table 6.

The hysteresis is added after a supply voltage goes out of tolerance. Therefore, the user can program the amount above the undervoltage threshold to which the input must rise before an undervoltage fault is deasserted. Similarly, the user can program the amount below the overvoltage threshold to which an input must fall before an overvoltage fault is deasserted.

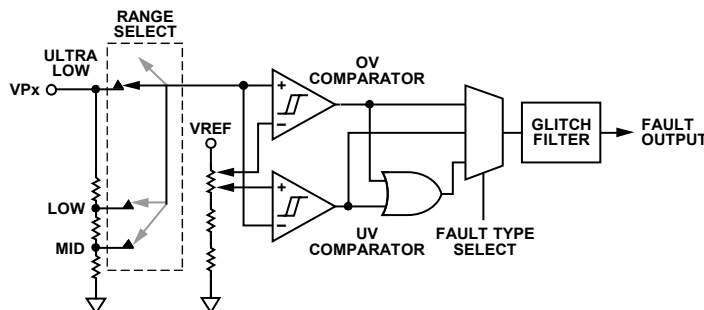


Figure 23. Supply Fault Detector Block

12445-023

Table 6. Input Functions, Thresholds, and Ranges

Input	Function	Voltage Range (V)	Maximum Hysteresis	Voltage Resolution (mV)	Glitch Filter ( $\mu$ s)
VH	High voltage analog input	2.5 to 6.0	425 mV	13.7	0 to 100
		6.0 to 14.4	1.02 V	32.9	0 to 100
VPx	Positive analog input	0.573 to 1.375	97.5 mV	3.14	0 to 100
		1.25 to 3.00	212 mV	6.8	0 to 100
		2.5 to 6.0	425 mV	13.7	0 to 100
VXx	High-Z analog input	0.573 to 1.375	97.5 mV	3.14	0 to 100
	Digital input	0 to 5.0	Not applicable	Not applicable	0 to 100

The hysteresis value is given by

$$V_{HYST} = V_R \times N_{THRESH}/255$$

where:

$V_{HYST}$  is the desired hysteresis voltage.

$V_R$  is the voltage range.

$N_{THRESH}$  is the decimal value of the 5-bit hysteresis code.

Note that  $N_{THRESH}$  has a maximum value of 31. The maximum hysteresis for the ranges is listed in Table 6.

### INPUT GLITCH FILTERING

The final stage of the SFDs is a glitch filter. This block provides time domain filtering on the output of the SFD comparators, which allows the user to remove any spurious transitions, such as supply bounce, at turn on. The glitch filter function is in addition to the digitally programmable hysteresis of the SFD comparators. The glitch filter timeout is programmable up to 100  $\mu$ s.

For example, when the glitch filter timeout is 100  $\mu$ s, any pulse appearing on the input of the glitch filter block that is less than 100  $\mu$ s in duration is prevented from appearing on the output of the glitch filter block. Any input pulse that is longer than 100  $\mu$ s appears on the output of the glitch filter block. The output is delayed by 100  $\mu$ s with respect to the input. The filtering process is shown in Figure 24.

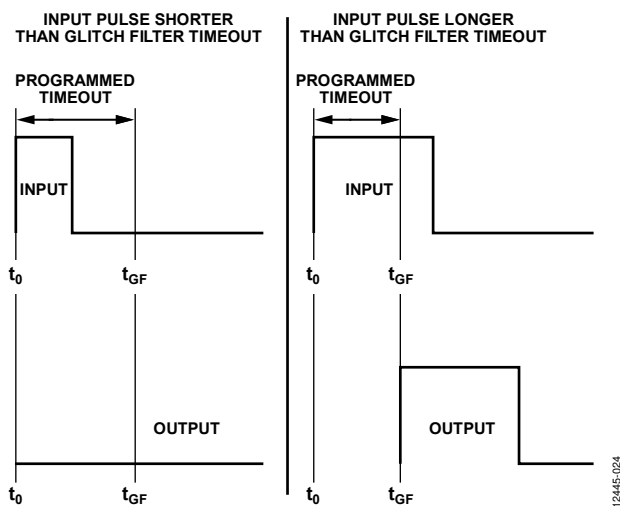


Figure 24. Input Glitch Filter Function

### SUPPLY SUPERVISION WITH THE VXx INPUTS

The VXx inputs have two functions: they can be used as either supply fault detectors or digital logic inputs. When selected as analog (SFD) inputs, the VXx pins have functionality that is very similar to the VH and VPx pins. The primary difference is that the VXx pins have only one input range, 0.573 V to 1.375 V. Therefore, the VXx inputs can directly supervise only the very low supplies. However, the input impedance of the VXx pins is high, allowing an external resistor divider network to be connected to the pin. Thus, potentially any supply can be divided down into the input range of the VXx pin and supervised. This enables the ADM1260 to monitor other supplies, such as  $-5$  V,  $+24$  V, and  $+48$  V.

An additional supply supervision function is available when the VXx pins are selected as digital inputs. In this case, the analog function is available as a second detector on each of the dedicated analog inputs, VPx and VH. The analog function of VX1 is mapped to VP1, VX2 is mapped to VP2, and so on. VX5 is mapped to VH. In this case, these SFDs can be viewed as secondary or warning SFDs.

The secondary SFDs are fixed to the same input range as the primary SFDs. They indicate warning levels rather than failure levels. The primary and secondary SFDs allows faults and warnings to be generated on a single supply using only one pin. For example, if VP1 is set to output a fault when a 3.3 V supply drops to 3.0 V, VX1 can be set to output a warning at 3.1 V. Warning outputs are available for readback from the status registers. These outputs are also ORed together and fed into the SE, allowing warnings to generate interrupts on the PDOs. Therefore, in this example, if the supply drops to 3.1 V, a warning is generated, and remedial action can be taken before the supply drops out of tolerance.

### VXx PINS AS DIGITAL INPUTS

As described in the Supply Supervision with the VXx Inputs section, the VXx input pins on the ADM1260 have dual functionality. The second function is as a digital logic input to the device. Therefore, the ADM1260 can be configured for up to five digital inputs. These inputs are TTL-/CMOS-compatible inputs. Standard logic signals can be applied to the pins: reset from reset generators, power-good (PWRGD) signals, fault flags, and manual resets. These signals are available as inputs to the SE and, therefore, can be used to control the status of the PDOs. The inputs can be configured to detect either a change in level or an edge.

When configured for level detection, the output of the digital block is a buffered version of the input. When configured for edge detection, a pulse of programmable width is output from the digital block once the logic transition is detected. The width is programmable from 0  $\mu$ s to 100  $\mu$ s. The digital blocks feature the same glitch filter function that is available on the SFDs. This

function enables the user to ignore spurious transitions on the inputs. For example, the filter can be used to debounce a manual reset switch.

When configured as digital inputs, each VXx pin has a weak (10  $\mu$ A) pull-down current source available for placing the input into a known condition, even if left floating. The current source, if selected, weakly pulls the input to GND.

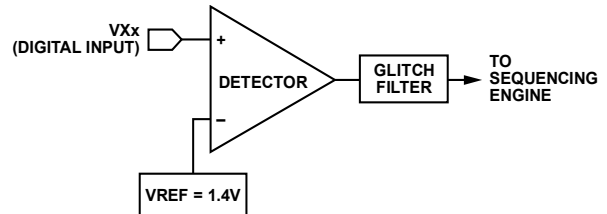


Figure 25. VXx Digital Input Function

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## OUTPUTS

### SUPPLY SEQUENCING THROUGH CONFIGURABLE OUTPUT DRIVERS

Supply sequencing is achieved with the [ADM1260](#) using the programmable driver outputs (PDOs) on the device as control signals for supplies. The output drivers can be used as logic enables or as FET drivers.

The sequence in which the PDOs are asserted (and, therefore, the supplies are turned on) is controlled by the sequencing engine (SE). The SE determines what action is taken with the PDOs, based on the condition of the [ADM1260](#) inputs. Therefore, the PDOs can be set up to assert when the SFDs are in tolerance, the correct input signals are received on the VXx digital pins, and no warnings are received from any of the inputs of the device. The PDOs can be used for a variety of functions. The primary function is to provide enable signals for LDOs or dc-to-dc converters that generate supplies locally on a board. The PDOs can also provide a power-good signal when all the SFDs are in tolerance, or a reset output if one of the SFDs goes out of specification (this output from the PDO can be used as a status signal for a DSP, FPGA, or other microcontroller).

The PDOs can be programmed to pull up to a number of different options. The outputs can be programmed as follows:

- Open drain (allowing the user to connect an external pull-up resistor).
- Open drain with a weak pull-up to  $V_{DD}$ .
- Open drain with a strong pull-up to  $V_{DD}$ .
- Open drain with a weak pull-up to  $VPx$ .
- Open drain with a strong pull-up to  $VPx$ .
- Strong pull-down to GND.
- Internally charge pumped high drive (12 V, PDO1 to PDO6 only).

The last option (available only on PDO1 to PDO6) allows the user to directly drive a voltage high enough to fully enhance an external N-FET, which is used to isolate, for example, a card side voltage from a backplane supply (a PDO can sustain greater than 10.5 V into a 1  $\mu$ A load). The pull-down switches can also be used to drive status LEDs directly.

The data driving each of the PDOs comes from one of three sources. Enable the specific source in the PDOxCFG configuration register.

The data sources are as follows:

- Output from the SE.
- Directly from the SMBus. A PDO can be configured so that the SMBus has direct control over it. This configuration enables software control of the PDOs. Therefore, a microcontroller can be used to initiate a software power-up/power-down sequence.
- On-chip clock. A 100 kHz clock is generated on the device. This clock can be made available on any of the PDOs. It can be used, for example, to clock an external device, such as an LED.

### DEFAULT OUTPUT CONFIGURATION

All of the internal registers in an unprogrammed [ADM1260](#) device from the factory are set to 0. Because of this factory setting, the PDOx pins are pulled to GND by a weak (20 k $\Omega$ ), on-chip pull-down resistor.

As the input supply to the [ADM1260](#) ramps up on  $VPx$  or  $VH$ , all the PDOx pins behave as follows:

- Input supply = 0 V to 1.2 V. The PDOs are high impedance.
- Input supply = 1.2 V to 2.7 V. The PDOs are pulled to GND by a weak (20 k $\Omega$ ), on-chip pull-down resistor.
- Supply > 2.7 V. The factory programmed devices continue to pull all PDOs to GND by a weak (20 k $\Omega$ ), on-chip, pull-down resistor. The programmed devices download current EEPROM configuration data, and the programmed setup is latched. The PDO then goes to the state demanded by the configuration, which provides a known condition for the PDOs during power-up.

The internal pull-down resistor can be overdriven with an external pull-up resistor of suitable value tied from the PDOx pin to the required pull-up voltage. The 20 k $\Omega$  resistor must be accounted for in calculating a suitable value. For example, if PDOx must be pulled up to 3.3 V, and 5 V is available as an external supply, the pull-up resistor value ( $R_{UP}$ ) is given by

$$3.3 \text{ V} = 5 \text{ V} \times 20 \text{ k}\Omega / (R_{UP} + 20 \text{ k}\Omega)$$

Therefore,

$$R_{UP} = (100 \text{ k}\Omega - 66 \text{ k}\Omega) / 3.3 \text{ V} = 10 \text{ k}\Omega$$

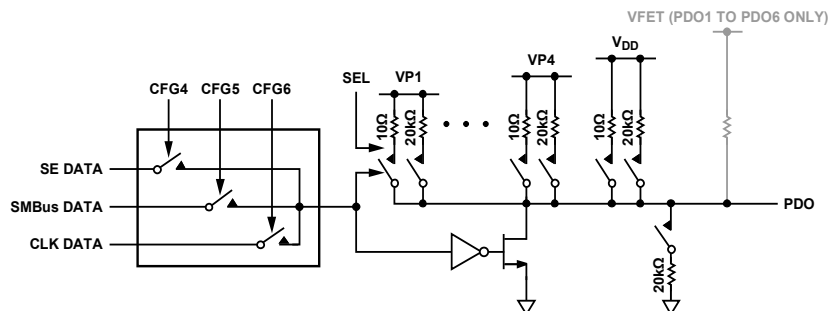


Figure 26. Programmable Driver Output

## SEQUENCING ENGINE

### OVERVIEW

The ADM1260 SE provides the user with powerful and flexible control of sequencing. The SE implements state machine control of the PDO outputs, with state changes conditional on input events. SE programs can enable complex control of boards such as power-up and power-down sequence control, fault event handling, and interrupt generation on warnings. A watchdog function that verifies the continued operation of a processor clock can be integrated into the SE program. The SE can also be controlled via the SMBus, giving software or firmware control of the board sequencing.

The SE state machine comprises 61 free state cells in each ADM1260. Each state has the following attributes:

- Monitors signals indicating the status of the 10 input pins, VP1 to VP4, VH, and VX1 to VX5.
- Can respond to and generate messages on the ICB to provide transparent, multidevice sequencing and monitoring
- Can be entered from any other state.
- Three exit routes move the state machine onto a next state: sequence detection, fault monitoring, and timeout.
- Delay timers for the sequence and timeout blocks can be programmed independently and changed with each state change. The range of timeouts is from 100 ms to 400 ms.
- Output condition of the 10 PDO pins is defined and fixed within a state.
- The transition from one state to the next is made in approximately 45  $\mu$ s (except when exiting out of Blackbox write state), which is the time taken to send one byte of message over the ICB and to download a state definition from the EEPROM to the SE.
- Can trigger a write of the black box fault and status registers into the black box section of the EEPROM.

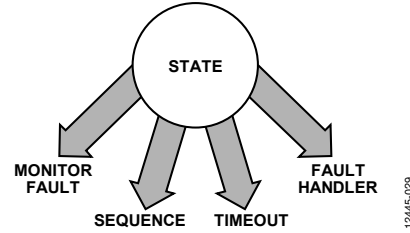


Figure 27. State Cell

The ADM1260 offers up to 61 state definitions. The signals monitored to indicate the status of the input pins are the outputs of the SFDs. In a multidevice system the number of user programmable states varies depending on the number of states used for ping-pong between devices.

### WARNINGS

The SE also monitors warnings. These warnings can be generated when the ADC readings violate their limit register value or when the secondary voltage monitors on VPx or VH are triggered. The warnings are ORed together and are available as a single warning input to each of the three blocks that enable exiting a state.

### SMBUS JUMP (UNCONDITIONAL JUMP)

The SE can be forced to advance to the next state unconditionally, which enables the user to force the SE to advance. Examples of the use of this feature include moving to a margining state or debugging a sequence. The SMBus jump or go to command can be seen by the user as another input to sequence and timeout blocks to provide an exit from each state.

Table 7. Sample Sequence State Entries

State	Sequence	Timeout	Monitor
IDLE1	If VX1 is low, go to State IDLE2.		
IDLE2	If VP1 is good, go to State EN3V3.		
EN3V3	If VP2 is good, go to State EN2V5.	If VP2 is not good after 10 ms, go to State DIS3V3.	If VP1 is not good, go to State IDLE1.
DIS3V3	If VX1 is high, go to State IDLE1.		
EN2V5	If VP3 is good, go to State PWRGD.	If VP3 is not good after 20 ms, go to State DIS2V5.	If VP1 or VP2 is not good, go to State FSEL2.
DIS2V5	If VX1 is high, go to State IDLE1.		
FSEL1	If VP3 is not good, go to State DIS2V5.		If VP1 or VP2 is not good, go to State FSEL2.
FSEL2	If VP2 is not good, go to State DIS3V3.		If VP1 is not good, go to State IDLE1.
PWRGD	If VX1 is high, go to State DIS2V5.		If VP1, VP2, or VP3 is not good, go to State FSEL1.

# ADM1260

## INTERCHIP BUS

In addition to local device conditions, a number of different ICB messages can affect the operation of the SE. These messages are used by the ADM1260 to coordinate the sequencing activities, and to inform other devices of faults within the system.

There are four basic types of ICB messages.

- Sequence action
- Timeout fault
- Monitor fault
- Black box trigger

The sequence action message has two forms. In a device to device form (the first form), this message is used to hand over sequencing responsibility from one device to the another. The transfer of sequencing control is done using a ping-pong handshake to ensure a robust handover of control. In the second form, the message is broadcast to all devices and instructs them to execute the sequence condition of the active SE state. All devices connected by the ICB advance their state machines together in lock step to maintain a coherent overall system state.

The sequence condition can be set to generate a sequence action message that is sent to a specific device, or is broadcast to all devices.

The sequence condition in the SE state must be set to wait for a ping (from a specific device or from a broadcast) for the device to receive and act upon it.

The timeout and monitor fault messages are always broadcast messages. They are used by one device to inform all other devices connected to the ICB that a timeout or monitor fault has occurred, and to follow the exit state defined in the active SE state.

The timeout and monitor messages are always active on the ADM1260. The timeout and monitor conditions do not need to be programmed as part of the SE definition to respond to the messages being received on the ICB.

The black box trigger is a broadcast message automatically sent by an ADM1260 when a sequence condition causes the device to enter a state where the black box trigger is enabled.

In normal operation, the ADM1260 evaluation software, ADI Power Studio, generates a virtual sequence for all the devices that share the same ICB. The software automatically inserts the necessary ICB messages and generates the sequence engine of each device connected to the ICB. In practice, the end user does not need to insert the ICB message handling into the SE.

The ICB must be pulled up for the SE to progress; otherwise, the devices remain in a reserved state.

The SE follows the fault handler path in case of an ICB bus fault or ping-pong fault if one of the devices in the sequence is non-operational.

### ICB Message Address

Each device on the ICB is assigned a 4-bit address, which is automatically configured by the GUI. This address is used for device to device sequence action messages. The ADM1260 supports up to four devices on the ICB.

### SE APPLICATION EXAMPLE

The application in this section demonstrates the operation of the SE. Figure 29 shows how the simple building block of a single SE state can be used to build a power-up sequence for a three-supply system. Table 8 lists the PDOx outputs for each state in the same SE implementation. In this system, a good 5 V supply on the VP1 pin and the VX1 pin held low are the triggers required to start a power-up sequence. Next, the sequence turns on the 3.3 V supply, then the 2.5 V supply (assuming successful turn on of the 3.3 V supply). When all three supplies turn on correctly, the power-good state is entered, where the SE remains until a fault occurs on one of the three supplies or until it is instructed to go through a power-down sequence by VX1 going high. Faults are dealt with throughout the power-up sequence on a case by case basis. The following three sections in this data sheet (the Sequence Detector section, the Monitoring Fault Detector section, and the Timeout Detector section) describe the individual blocks and use the sample application shown in Figure 29 to demonstrate the actions of the SE.

Table 8. PDO Outputs for Each State

PDOx Output	Sequence State <sup>1</sup>								
	IDLE1	IDLE2	EN3V3	EN2V5	DIS3V3	DIS2V5	PWRGD	FSEL1	FSEL2
PDO1 = 3V3ON <sup>2</sup>	0	0	1	1	0	1	1	1	1
PDO2 = 2V5ON <sup>3</sup>	0	0	0	1	1	0	1	1	1
PDO3 = FAULT <sup>4</sup>	0	0	0	0	1	1	0	1	1

<sup>1</sup> The various sequence states are described in Table 7.

<sup>2</sup> 3V3ON means that a particular PDOx pin enables the signal of the 3.3 V LDO.

<sup>3</sup> 2V5ON means that a particular PDOx pin enables the signal of the 2.5 V LDO.

<sup>4</sup> PDO3 is used to send a fault signal to the microcontroller or FPGA.

**Sequence Detector**

The sequence detector block detects when a step in a sequence is complete. The sequence detector looks for one of the SE inputs to change state, and is most often used as the gate for successful progress through a power-up or power-down sequence. A timer block included in this detector inserts delays into a power-up or power-down sequence, if required. Timer delays can be set from 0  $\mu$ s to 400 ms. Figure 28 shows a block diagram of the sequence detector.

If a timer delay is specified, the input to the sequence detector must remain in the defined state for the duration of the timer delay. If the input changes state during the delay, the timer is reset.

The sequence detector can also help to identify monitoring faults. In the sample application shown in Figure 29, the FSEL1 and FSEL2 states first identify which of the VP1, VP2, or VP3 pins faulted; then, the states take the appropriate action.

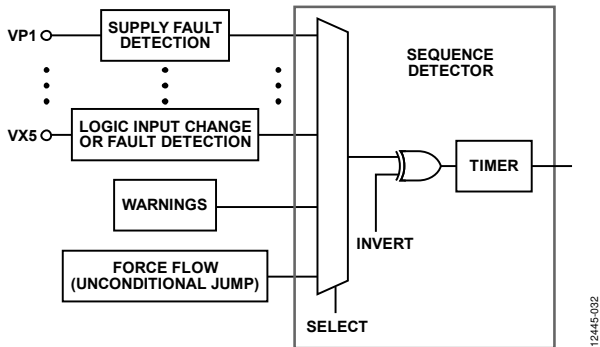


Figure 28. Sequence Detector Block Diagram

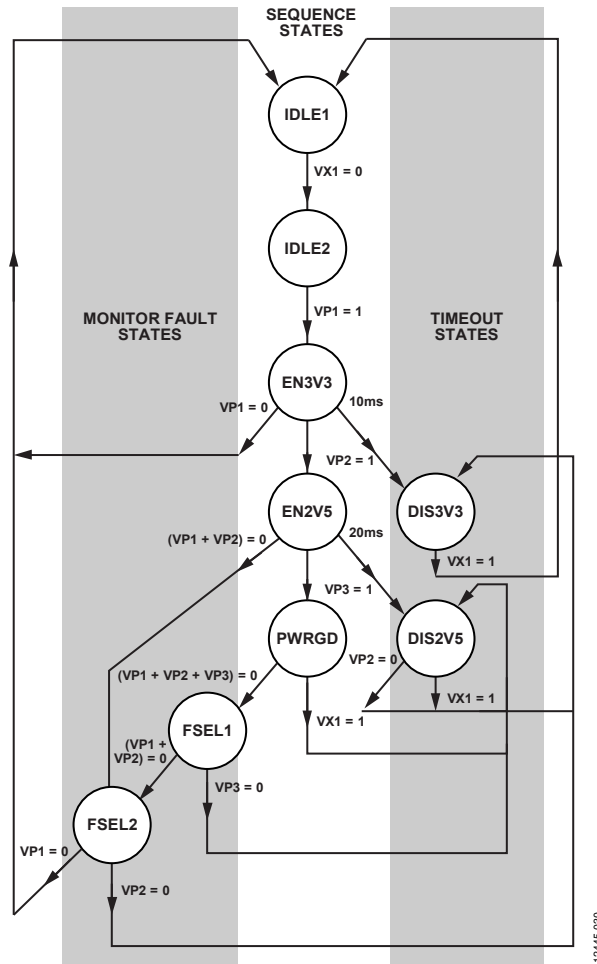


Figure 29. Sample Application Flow Diagram



### Monitoring Fault Detector

The monitoring fault detector block detects a failure on an input. The logical function implementing this is a wide OR gate that can detect when an input deviates from its expected condition. The clearest demonstration of the use of this block is in the PWRGD state, where the monitor block indicates that a failure on one or more of the VPx, VXx, or VH inputs occurred.

No programmable delay is available in this block because the triggering of a fault condition is likely caused by a supply falling out of tolerance. In this situation, the device must react as quickly as possible. Some latency occurs when moving out of this state because it takes a finite amount of time (~45  $\mu$ s) for the state configuration to download from the EEPROM into the SE. Figure 30 is a block diagram of the monitoring fault detector.

If multiple ADM1260 devices are connected through the interchip bus and a monitor fault is detected on any of the devices, the device where the fault occurred transmits a broadcast message on the interchip bus. Because this is a broadcast message, all the devices see the monitor event message and transition their own local SE by following the monitor exit state programmed in their active local state.

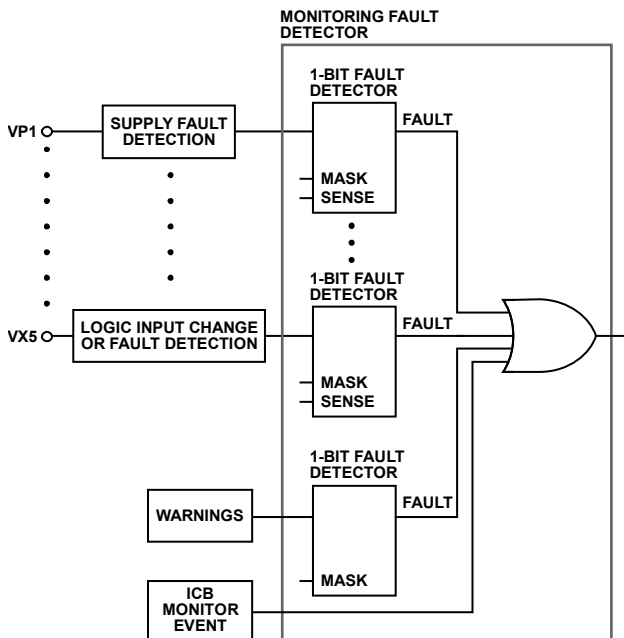


Figure 30. Monitoring Fault Detector Block Diagram

### Timeout Detector

The timeout detector allows the user to trap a failure to ensure proper progress through a power-up or power-down sequence.

In the sample application shown in Figure 29, the timeout next state transition is from the EN3V3 and EN2V5 states. For the EN3V3 state, the 3V3ON signal is asserted on the PDO1 output pin upon entry to this state to turn on a 3.3 V supply.

This 3.3 V supply rail is connected to the VP2 pin, and the sequence detector looks for the VP2 pin to go above its undervoltage threshold, which is set in the SFD attached to that pin.

The power-up sequence progresses when it is detected that the VP2 pin went above the undervoltage threshold. If, however, the supply fails (perhaps due to a short circuit overloading this supply), the timeout block traps the problem. In this example, if the 3.3 V supply fails within 10 ms, the SE moves to the DIS3V3 state and turns off this supply by bringing PDO1 low. It also indicates that a fault has occurred by taking PDO3 high. Timeout delays of 100  $\mu$ s to 400 ms are programmable.

If multiple ADM1260 devices are connected through the interchip bus and a timeout is detected in any of the devices, the device transmits a broadcast timeout message on the interchip bus. Because this is a broadcast message, all the devices see the timeout event message and transition their own local state machine by following the timeout exit state programmed in their active local state.

### FAULT AND STATUS REPORTING

The ADM1260 has a number of input status registers. These registers include more detailed information, such as whether an undervoltage or overvoltage fault is present on a particular input. The status registers also include information on the ADC limit faults. The contents of the fault register can be read out over the SMBus.

There are two sets of these registers with different behaviors. The first set of status registers is not latched in any way and, therefore, can change at any time in response to changes on the inputs. These registers provide information on the undervoltage (UV) and overvoltage (OV) state of the inputs, the digital state of the general-purpose input (GPI) VXx input pins, and also the ADC warning limit status.

The second set of registers update each time the sequence engine changes state and are latched until the next state change. The second set of registers provides the same information as the first set, but in a more compact form. The reason for this compact form is that these registers are used by the black box feature when writing status information for the previous state into EEPROM.

## NONVOLATILE BLACK BOX FAULT RECORDING

A section of EEPROM, Address 0xF980 to Address 0xF9FF, can be used to store up to 16 fault records instead of user data.

The user can designate any sequencing engine state as a black box write trigger state. Each time the sequence engine enters that state, a fault record is written into EEPROM. The fault record provides a snapshot of the entire [ADM1260](#) state at the point in time when the last state exited, just prior to entering the designated black box write state. A fault record contains the following information:

- A flag bit set to 0 after the fault record is written.
- The state number of the previous state prior to the fault record write state.
- Whether a sequence/timeout/monitor condition caused the previous state to exit.
- Whether the transition was caused by the reception of an ICB message.
- The UVSTATx and OVSTATx input comparator status.
- The VXx GPISTAT status.
- The LIMSTATx status.
- A checksum byte.

Each fault record contains eight bytes, with each byte taking typically approximately 250  $\mu$ s to write to EEPROM, for a total write time of approximately 2 ms. After the black box begins to write a fault record into EEPROM, the [ADM1260](#) ensures that the write is complete before attempting to write any additional fault records. This means that if consecutive sequencing engine states are designated as black box write states, a time delay must be used in the first state to ensure that the fault record is written before moving to the next state.

When the [ADM1260](#) powers on initially, it performs a search to find the first fault record that is not written to. The device does this by checking the flag bit in each fault record until it finds a record where the flag bit is 1. The first fault record is stored at Address 0xF980 and at multiples of eight bytes after that, with the last record stored at Address 0xF9F8.

The fault recorder is only able to write in the EEPROM. It is unable to erase the EEPROM prior to writing the fault record. Therefore, to ensure correct operation, it is important that the fault record EEPROM be erased prior to use. After all EEPROM locations for the fault records are used, no more fault records can be written. This limitation ensures that the first fault in any cascading fault is stored and not overwritten and lost.

To avoid the fault recorder filling up and fault records being lost, an application can periodically poll the [ADM1260](#) to determine if there are fault records to be read. Alternatively, one of the PDOx outputs can be used to generate an interrupt for a processor in the fault record write state to signal the need to read one or more fault records.

After reading fault records during normal operation, the following two things must be done before the fault recorder can reuse the EEPROM locations:

- The EEPROM section must be erased.
- The fault recorder must be reset so that it performs its search again for the first unused location of EEPROM that is available to store a fault record.

In a multiple device system, when one of the [ADM1260](#) devices moves to a black box state due to a sequence, monitor, or timeout condition, it generates an ICB message on the bus with the black box bit asserted. This assertion causes a black box write on all the devices on the ICB. This write enables the ability to capture the status of all the devices when a fault occurs. The devices have the same number of black box records that are on the same ICB. The devices that perform the black box write due to the ICB message is stated in the black box record.

## BLACK BOX WRITES WITH NO EXTERNAL SUPPLY

In cases where all the input supplies fail, for example, if the card is removed from a powered backplane, the state machine can be programmed to trigger a write into the black box EEPROM. The decoupling capacitors on the rail that power the [ADM1260](#) and the other loads on the board form an energy reservoir. Depending on the other loads on the board and their behavior as the supply rails drop, there may be sufficient energy in the decoupling capacitors to allow the [ADM1260](#) to write a complete fault record (8 bytes of data). CCL and CDA must be pulled up, at least for the duration required for the SE to transition to the black box trigger state.

Typically, it takes 2 ms to write to the eight bytes of a fault record. If the [ADM1260](#) is powered using a 12 V supply on the VH pin, a UV threshold at 6 V can be set and used as the state machine trigger to start writing a fault record to EEPROM. The higher the threshold, the earlier the black box write begins, and the more energy is available in the decoupling capacitors to ensure that the write completes successfully.

Provided that the VH supply, or another supply connected to a VPx pin, remains above 3.0 V during the time to write, the entire fault record is always written to EEPROM. In many cases, there are sufficient decoupling capacitors on a board to power the [ADM1260](#) as it writes into EEPROM.

In cases where the decoupling capacitors are not able to supply sufficient energy for a complete fault record to be written after the board is removed, the value of the capacitor on VDDCAP may be increased. In a worst case scenario, assuming that no energy is supplied to the [ADM1260](#) by external decoupling capacitors, and that the VDDCAP capacitor has 4.75 V across it at the start of the black box write to EEPROM, a VDDCAP value of 68  $\mu$ F is sufficient to guarantee that a single, complete black box record can be written to EEPROM.