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High Voltage Positive Hot Swap Controller and Digital Power Monitor with PMBus

Data Sheet

ADM1272

FEATURES

- Controls supply voltages from 16 V to 80 V (absolute maximum 120 V)
- High voltage (80 V) IPC-9592 compliant packaging
- <500 ns response time to short circuit
- FET energy monitoring for adaptable FET SOA protection
- Gate boost mode for fast recovery from OC transients
- Programmable random start mode to stagger power-on
- FET fault detection
- Remote temperature sensing with programmable warning and shutdown thresholds
- Programmable 2.5 mV to 30 mV system current-limit setting range
- ±0.85% accurate current measurement with 12-bit ADC
- I_{LOAD}, V_{IN}, V_{OUT}, temperature, power, and energy telemetry
- Programmable start-up current limit
- Programmable linear output voltage soft start
- 1% accurate UV and OV thresholds
- Programmable hot swap restart function
- 2 programmable GPIO pins
- Reports power and energy consumption
- Peak detect registers for current, voltage, and power
- PMBus fast mode compliant interface
- 48-lead 7 mm × 8 mm LFCSP

APPLICATIONS

- 48 V/54 V systems
- Servers
- Power monitoring and control/power budgeting
- Central office equipment
- Telecommunication and data communication equipment
- Industrial applications

GENERAL DESCRIPTION

The ADM1272 is a hot swap controller that allows a circuit board to be removed from or inserted into a live backplane. It also features current, voltage, and power readback via an integrated 12-bit analog-to-digital converter (ADC), accessed using a PMBus™ interface. This device is able to withstand up to 120 V, which makes it very robust in surviving surges and transients commonly associated with high voltage systems, usually clamped using protection devices such as transient voltage suppressors (TVSs) that can often exceed 100 V.

The load current, I_{LOAD}, is measured using an internal current sense amplifier that measures the voltage across a sense resistor in the power path via the SENSE+ and SENSE− pins. A default current limit sense voltage of 30 mV is set, but this limit can be adjusted down, if required, using a resistor divider network from the VCAP regulator output voltage to the ISET pin. An additional resistor can also be placed from ISET to V_{IN} (or V_{OUT}) to allow the current limit to track inversely with the rail voltage. This resistor allows an approximate system power limit to be used.

The ADM1272 limits the current through the sense resistor by controlling the gate voltage of an external N channel field effect transistor (FET) in the power path. The sense voltage, and therefore the load current, is maintained below the preset maximum. The ADM1272 protects the external FET by monitoring and limiting the energy transfer through the FET while the current is being controlled. This energy limit is set by the choice of components connected to the EFAULT pin (for fault protection mode) and the ESTART pin during startup. Therefore, different energy limits can be set for start-up and normal fault conditions. During startup, inrush currents are maintained very low and different areas of the safe operating area (SOA) curve are of interest, whereas during fault conditions, the currents can be much higher.

The controller uses the drain to source voltage (V_{DS}) across the FET to set the current profile of the EFAULT and ESTART pins and, therefore, the amount of much energy allowed to be transferred in the FET. This energy limit ensures the MOSFET remains within the SOA limits. Optionally, use a capacitor on the DVDT pin to set the output voltage ramp rate, if required. In case of a short-circuit event, a fast internal overcurrent detector responds in hundreds of ns and signals the gate to shut down. A 1.5 A pull-down device ensures a fast FET response. The gate then recovers control within 50 µs to ensure minimal disruption during conditions, such as line steps and surges. The ADM1272 features overvoltage (OV) and undervoltage (UV) protection, programmed using external resistor dividers on the UVH, UVL, and OV pins. The use of two pins for undervoltage allows independent accurate rising and falling thresholds. The PWRGD output pin signals when the output voltage is valid and the gate is sufficiently enhanced. The validity of VOUT is determined using the PWGIN pin.

The 12-bit ADC measures the voltage across the sense resistor, the supply voltage on the SENSE+ pin, the output voltage, and the temperature using an external NPN/PNP device. A PMBus interface allows a controller to read data from the ADC. As many as 16 unique I^2C addresses can be selected, depending on how the two ADRx pins are connected. The ADM1272 is available in a custom 48-lead LFCSP (7 mm × 8 mm) with a pinstrap mode that allows the device to be configured for automatic retry or latchoff when an overcurrent (OC) fault occurs.

Rev. 0 Document Feedback

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REVISION HISTORY

4/2017—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

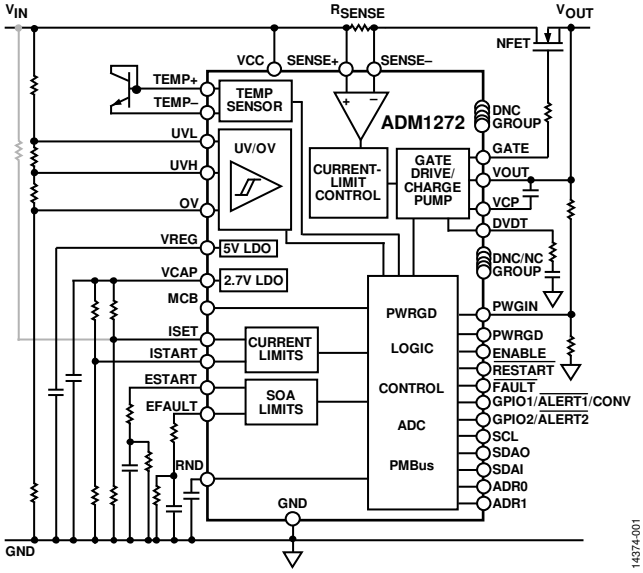


Figure 1.

SPECIFICATIONS

V_{CC} = 16 V to 80 V, $V_{CC} \geq V_{SENSE+}$, V_{SENSE+} = 16 V to 80 V, $V_{\Delta SENSE} = (V_{SENSE+} - V_{SENSE-})$ = 0 V, T_J= −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY						
Operating Voltage Range[1]	V_{CC}	16		80	V	
Undervoltage Lockout	V_{CCUV}	13		16	V	V_{CC} rising
Undervoltage Hysteresis	$V_{CCUVHYS}$		70	115	mV	
Quiescent Current	I_{CC}			6	mA	GATE on and power monitor running
Power-On Reset (POR)	t_{POR}		27		ms	
UVL AND UVH PINS						
Input Current	I_{UV}		1	50	nA	UVL ≤ 3.6 V, when UVL and UVH are tied together
UVH Threshold	UVH_{TH}	0.99	1.0	1.01	V	UV rising
UVL Threshold	UVL_{TH}	0.887	0.9	0.913	V	UV falling
UVx Threshold Hysteresis	UV_{HYST}		100		mV	When UVL and UVH are tied together
UVx Glitch Filter	UV_{GF}	3.5		7.5	µs	50 mV overdrive
UVx Propagation Delay	UV_{PD}		5	8	µs	UVx low to GATE pull-down active
OV PIN						
Input Current	I_{OV}			50	nA	OV ≤ 3.6 V
OV Threshold	OV_{TH}	0.99	1.0	1.01	V	OV rising
OV Hysteresis Current	I_{OVHYST}	4.5	5.25	6	µA	
OV Glitch Filter	OV_{GF}	1.75		3.75	µs	50 mV overdrive
OV Propagation Delay	OV_{PD}		3	4.5	µs	OV high to GATE pull-down active
SENSE+ AND SENSE− PINS						
Current-Limit Setting Range	$V_{SENSECL}$	2.5		30	mV	Adjustable using ISET and ISTART pins
Input Current	I_{SENSEx}		130	170	µA	Per individual pin
Input Imbalance	$I_{\Delta SENSE}$			5	µA	$I_{\Delta SENSE} = (I_{SENSE+}) - (I_{SENSE-})$
VREG PIN						
Internally Regulated Voltage	V_{VREG}	4.5	5	5.5	V	0 µA ≤ I_{VREG} ≤ 100 µA; C_{VREG} = 1 µF
VCAP PIN						
Internally Regulated Voltage	V_{VCAP}	2.68	2.7	2.72	V	0 µA ≤ I_{VCAP} ≤ 100 µA; C_{VCAP} = 1 µF
ISET PIN						
Reference High Limit[1]	V_{CLREF_HI}		1.2		V	V_{CLREF}[2] = $V_{VCAP} - V_{ISET}$; $V_{SENSECL}$ = 30 mV; internally clamped with falling V_{ISET}
Reference Low Limit[1]	V_{CLREF_LO}		100		mV	Internally clamped with rising V_{ISET} or V_{ISTART} < 100 mV, $V_{CLREF} = V_{VCAP} - V_{ISET}$; $V_{SENSECL}$ = 2.5 mV
Gain of Current Sense Amplifier[1]	AV_{CSAMP}		40		V/V	
Input Current	I_{ISET}			100	nA	$V_{ISET} \leq V_{VCAP}$
ISTART PIN						
Reference Select Threshold	$V_{ISTARTRSTH}$	1.35	1.5	1.65	V	If $V_{ISTART} > V_{ISTARTRSTH}$, internal 1 V reference ($V_{CLREF1V}$) is used
Internal Reference[1]	$V_{CLREF1V}$		1		V	
Input Current	I_{ISTART}			100	nA	$V_{ISTART} \leq V_{VCAP}$
GATE PIN[3]						
Gate Drive Voltage	ΔV_{GATE}					$\Delta V_{GATE} = V_{GATE} - V_{OUT}$
		10	12	14	V	80 V ≥ V_{CC} ≥ 20 V; I_{GATE} ≤ 5 µA
		4.5			V	20 V ≥ V_{CC} ≥ 16 V; I_{GATE} ≤ 5 µA

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Gate Pull-Up Current	I_{GATEUP}	−20		−30	µA	ΔV_{GATE} = 0 V
Gate Recovery Rate			0.12		V/µs	Following severe OC shutdown
Gate Pull-Down Current						
Regulation	I_{GATEDN_REG}	35	60	75	µA	4 V > ΔV_{GATE} ≥ 2 V; V_{ISET} = 1.7 V; $V_{\Delta SENSE}$ = 30 mV
		50	70	90		ΔV_{GATE} ≥ 4 V; V_{ISET} = 1.7 V; $V_{\Delta SENSE}$ = 30 mV
Slow	I_{GATEDN_SLOW}	8	15	25	mA	ΔV_{GATE} ≥ 2 V; V_{ENABLE} = 0 V
Fast	I_{GATEDN_FAST}	1.1	1.5	1.9	A	ΔV_{GATE} ≥ 10 V
VCP PIN						
VCP Capacitor Ratio			10			C_{VCP} must be 10 times larger than C_{DVDT} + $C_{GATETOTAL}$
DVDT PIN						
Switch Resistance	$DVDT_{SWG}$		40		Ω	V_{GATE} − V_{DVDT} = 100 mV; V_{GATE} ≤ (V_{VOUT} + 5 V); V_{CC} > 20 V
	$DVDT_{SWVO}$		40		Ω	V_{DVDT} − V_{OUT} = 100 mV
HOT SWAP SENSE VOLTAGE						
Hot Swap Sense Voltage Current Limit						ΔV_{GATE} = 3 V; I_{GATE} = 0 µA
	$V_{SENSECL}$	29.4	30	30.3	mV	V_{ISET} < 1 V; internally clamped
		24.3	25	25.4	mV	V_{ISET} = 1.7 V
		19.3	20	20.4	mV	V_{ISET} = 1.9 V
		14.3	15	15.4	mV	V_{ISET} = 2.1 V
		9.3	10	10.4	mV	V_{ISET} = 2.3 V
Start-Up Current Limit	$V_{SENSECL}$	29.4	30	30.4	mV	V_{ISTART} = 1.2 V; STRT_UP_IOUT_LIM = Code 0x0F
		24.4	25	25.4	mV	V_{ISTART} = 1 V, or V_{ISTART} > 1.65 V
		19.4	20	20.4	mV	V_{ISTART} = 0.8 V
		14.4	15	15.4	mV	V_{ISTART} = 0.6 V
		4.4	5	5.4	mV	V_{ISTART} = 0.2 V
Minimum $V_{SENSECL}$ Clamp	V_{CLAMP}	1.9	2.4	2.9	mV	V_{ISTART} = 0 V or V_{ISET} =2.7 V or STRT_UP_IOUT_LIM = 0x00
Circuit Breaker Offset	V_{CBOS}	0.9	1.1	1.31	mV	Circuit breaker trip voltage, V_{CB} = $V_{SENSECL}$ − V_{CBOS}
SEVERE OVERCURRENT (SOC)						
Voltage Threshold	$V_{SENSEOC}$	43	45	47	mV	V_{ISET} < 1 V; OC_TRIP_SELECT = 11 (1.5×)
		58	60	62	mV	V_{ISET} < 1 V; OC_TRIP_SELECT = 10 (2×, default at power-up)
		88	90	92	mV	V_{ISET} < 1 V; OC_TRIP_SELECT = 01 (3×)
		118	120	122	mV	V_{ISET} < 1 V; OC_TRIP_SELECT = 00 (4×)
Glitch Filter Duration		80		280	ns	$V_{\Delta SENSE}$ step = 40 mV to 48 mV; OC_FILT_SELECT = 00
		500		880	ns	$V_{\Delta SENSE}$ step = 40 mV to 48 mV; OC_FILT_SELECT = 01
		2.2		5.5	µs	$V_{\Delta SENSE}$ step = 40 mV to 48 mV; OC_FILT_SELECT =10
		6.8		10.8	µs	$V_{\Delta SENSE}$ step = 40 mV to 48 mV; OC_FILT_SELECT = 11
Response Time	t_{SOC}					To gate pull-down current active
			330	500	ns	$V_{\Delta SENSE}$ step = 40 mV to 48 mV; OC_FILT_SELECT = 00 (default)
			860	1070	ns	$V_{\Delta SENSE}$ step = 40 mV to 48 mV; OC_FILT_SELECT = 01
			6500	9000	ns	$V_{\Delta SENSE}$ step = 40 mV to 48 mV; OC_FILT_SELECT = 10
			11500	15000	ns	$V_{\Delta SENSE}$ step = 40 mV to 48 mV; OC_FILT_SELECT = 11
ESTART PIN						
Pull-Up Current[4]	$I_{ESTARTUP}$	−88	−100	−113	µA	V_{CC} − V_{OUT} = 100 V; V_{ISTART} >1.65 V; $V_{\Delta SENSE}$ = 25 mV
		−8.4	−10	−11.3	µA	V_{CC} − V_{OUT} = 10 V; V_{ISTART} >1.65 V; $V_{\Delta SENSE}$ = 25 mV
		−0.8	−1	−1.2	µA	V_{CC} − V_{OUT} = 0 V; V_{ISTART} >1.65 V; $V_{\Delta SENSE}$ = 25 mV
Pull-Down Current	$I_{ESTARTDN}$	350	500	680	nA	V_{CC} − V_{OUT} = 0 V
High Threshold	$V_{ESTARTH}$	0.98	1.0	1.02	V	
Low Threshold	$V_{ESTARTL}$	35	50	65	mV	
Glitch Filter	$V_{ESTARTGF}$		10		µs	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
EFAULT						
Pull-Up Current[4]	$I_{EFAULTUP}$	−88	−100	−113	µA	$V_{CC} - V_{OUT}$ = 100 V; V_{ISET} = 0 V; $V_{\Delta SENSE}$ = 30 mV
		−8.4	−10	−11.3	µA	$V_{CC} - V_{OUT}$ = 10 V; V_{ISET} = 0 V; $V_{\Delta SENSE}$ = 30 mV
		−0.8	−1	−1.2	µA	$V_{CC} - V_{OUT}$ = 0 V; V_{ISET} < 1 V; $V_{\Delta SENSE}$ = 30 mV
Pull-Down Current	$I_{EFAULTDN}$	350	500	680	nA	Always present on active pin when pull-up currents are not active
High Threshold	$V_{EFAULTH}$	0.98	1.0	1.02	V	
Low Threshold	$V_{EFAULTL}$	35	50	65	V	
Glitch Filter	$V_{EFAULTGF}$		10		µs	
MCB PIN						Mask severe OC shutdown
Input Current	I_{MCB}			4.4	µA	MCB ≤ 3.6 V (internal 1 MΩ pull-down resistor)
MCB Threshold	V_{MCB_TH}	0.58	0.6	0.62	V	MCB rising
MCB Threshold Hysteresis	V_{MCB_HYST}	10	25	40	mV	
MCB masking window	t_{MCB}					Must exceed V_{MCB_TH} within t_{MCB} of severe over current event
		150			ns	OC_FILT_SELECT = 00
		600			ns	OC_FILT_SELECT = 01
		4.5			µs	OC_FILT_SELECT = 10
		9.0			µs	OC_FILT_SELECT = 11
VOUT PIN						
Input Current		20		200	µA	1 V ≤ VOUT ≤ 80 V
$\overline{\text{FAULT}}$ PIN						
Output Low Voltage	V_{OL_LATCH}			0.4	V	I_{FAULT} = 1 mA
				1.5	V	I_{FAULT} = 5 mA
Leakage Current				100	nA	V_{FAULT} ≤ 2 V; $\overline{\text{FAULT}}$ output high-Z
				1	µA	V_{FAULT} = 20 V; $\overline{\text{FAULT}}$ output high-Z
ENABLE PIN						
Input High Voltage	V_{IH}	1.1			V	
Input Low Voltage	V_{IL}			0.8	V	
Glitch Filter			1		µs	
Leakage Current				100	nA	V_{ENABLE} ≤ 2 V
				1	µA	V_{ENABLE} = 18 V
RND PIN						
Pull-Up Current		−3.6	−4.2	−4.9	µA	V_{RND} = 0.5 V
High Threshold		0.93	1	1.07	V	
Delay Range[5]		0.28		38.9	ms	RND pin not connected
		16.6		2274	ms	C_{RND} = 100 nF
Timeout				3.63	sec	If pin fails to cycle, power-up continues following this timeout
Maximum External Capacitance				220	nF	
$\overline{\text{RESTART}}$ PIN						
Input Voltage High	V_{IH}	1.1			V	
Input Voltage Low	V_{IL}			0.8	V	
Glitch Filter			10		µs	
Internal Pull-Up Current			−16		µA	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
GPIO1/$\overline{\text{ALERT1}}$/CONV AND GPIO2/$\overline{\text{ALERT2}}$ PINS						
Output Low Voltage	V_{OL_GPIO}			0.4	V	I_{GPIO1} = 1 mA
				1.5	V	I_{GPIO1} = 5 mA
Leakage Current	I_{LKG_GPIO}			100	nA	$V_{GPIO1} \leq 2$ V; GPIO output high-Z
				1	µA	V_{GPIO1} = 20 V; GPIO output high-Z
Input High Voltage	V_{GPIOIH}	1.1			V	
Input Low Voltage	V_{GPIOIL}			0.8	V	
Glitch Filter			1		µs	
PWRGD PIN						
Output Low Voltage	V_{OL_PWRGD}			0.4	V	I_{PWRGD} = 1 mA
				1.5	V	I_{PWRGD} = 5 mA
VCC That Guarantees Valid Output		1.9			V	I_{SINK} = 100 µA; V_{OL_PWRGD} = 0.4 V
Leakage Current				100	nA	$V_{PWRGD} \leq 2$ V; PWRGD output high-Z
				1	µA	V_{PWRGD} = 20 V; PWRGD output high-Z
PWGIN PIN						
Input Current	I_{PWGIN}			50	nA	PWGIN ≤ 3.6 V
PWGIN Threshold	V_{PWGIN_TH}	0.99	1.0	1.01	V	PWGIN falling
PWGIN Threshold Hysteresis	V_{PWGIN_HYST}	45	60	75	mV	
Glitch Filter			2		µs	Asserting and deasserting of PWRGD pin
ADC						
Conversion Time						Includes time for power multiplication
			144	160	µs	One sample of I_{OUT}; from command received to valid data in register
			78	87	µs	One sample of V_{IN}; from command received to valid data in register
			78	87	µs	One sample of V_{OUT}; from command received to valid data in register
ADR0/ADR1 PINS						
Address Set to 00		0		0.8	V	Connect to GND
Input Current for Address Set to 00		−40	−22		µA	V_{ADRx} = 0 V to 0.8 V
Address Set to 01		135	150	165	kΩ	Resistor to GND
Address Set to 10		−1		+1	µA	No connect state; maximum leakage current allowed
Address Set to 11		2			V	Connect to VCAP or alternative supply within ratings
Input Current for Address Set to 11			3	10	µA	V_{ADRx} = 2.0 V to VCAP; must not exceed the maximum allowable current draw from VCAP
TEMP± PINS						External transistor is 2N3904
Operating Range		−55		+150	°C	Limited by external diode
Accuracy			±1	±7	°C	$T_A = T_{DIODE}$ = −40°C to +125°C
Resolution			0.25		°C	LSB size
Low Level Output Current Source[6]			5		µA	
Medium Level Output Current Source[6]			30		µA	
High Level Output Current Source[6]			105		µA	
Maximum Series Resistance for External Diode[6]	R_{STEMP}			100	Ω	For <±0.5°C additional error, C_P = 0 pF
Maximum Parallel Capacitance for External Diode[6]	C_{PTEMP}			1	nF	R_{STEMP} = 0 Ω

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL BUS DIGITAL INPUTS (SDAI/SDAO, SCL)						
Input High Voltage	V_{IH}	1.1			V	
Input Low Voltage	V_{IL}			0.8	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4 mA
Input Leakage	I_{LEAK_PIN}	−10		+10	µA	
		−5		+5	µA	Device is not powered
Nominal Bus Voltage	V_{DD}	2.7		5.5	V	3 V to 5 V ± 10%
Capacitive Load per Bus Segment	C_{BUS}			400	pF	
Capacitance for SDAI, SDAO, or SCL Pin	C_{PIN}		5		pF	
Input Glitch Filter, t_{SP}	t_{SP}	0		50	ns	

[1] Tolerances included in the total sense voltage tolerances.
[2] V_{CLREF} is the active current-limit reference. $V_{CLREF} = V_{SENSECL} \times AV_{CSAMP}$, where $V_{SENSECL}$ is the current limit at the SENSE± pins.
[3] Maximum voltage on the gate with respect to VOUT is always clamped to ≤14 V.
[4] Pull-up current is (VCC − VOUT − V_{TH})/R, where V_{TH} is approximately 1 V and R = 1 MΩ (±10%).
[5] Guaranteed by design, but not production tested.
[6] Sampled during initial release to ensure compliance, but not subject to production testing.

POWER MONITORING ACCURACY SPECIFICATIONS

V_{CC} = 16 V to 80 V, $V_{CC} \geq V_{SENSE+}$, V_{SENSE+} = 16 V to 80 V, $V_{\Delta SENSE} = (V_{SENSE+} - V_{SENSE-})$, T_J = −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT SENSE ABSOLUTE ERROR					128-sample averaging (unless otherwise noted)
			±1.2	%	$V_{\Delta SENSE}$ = 30 mV
			±0.85	%	$V_{\Delta SENSE}$ = 30 mV, T_J = 25°C to 85°C
			±1.5	%	$V_{\Delta SENSE}$ = 25 mV
			±1.0	%	$V_{\Delta SENSE}$ = 25 mV, T_J = 25°C to 85°C
			±1.8	%	$V_{\Delta SENSE}$ = 20 mV
			±1.25	%	$V_{\Delta SENSE}$ = 20 mV, T_J = 25°C to 85°C
			±1.85	%	$V_{\Delta SENSE}$ = 20 mV, 16-sample averaging
			±1.9	%	$V_{\Delta SENSE}$ = 20 mV, 1-sample averaging
			±2.4	%	$V_{\Delta SENSE}$ = 15 mV
			±1.7	%	$V_{\Delta SENSE}$ = 15 mV, T_J = 25°C to 85°C
			±3.6	%	$V_{\Delta SENSE}$ = 10 mV
			±2.6	%	$V_{\Delta SENSE}$ = 10 mV, T_J = 25°C to 85°C
			±7	%	$V_{\Delta SENSE}$ = 5 mV
			±5	%	$V_{\Delta SENSE}$ = 5 mV, T_J = 25°C to 85°C
			±14.1	%	$V_{\Delta SENSE}$ = 2.5 mV
			±10	%	$V_{\Delta SENSE}$ = 2.5 mV, T_J = 25°C to 85°C
SENSE+/VOUT ABSOLUTE ERROR			±0.4	%	V_{SENSE+}/V_{OUT} = 40 V to 80 V
POWER ABSOLUTE ERROR			±1.9	%	$V_{\Delta SENSE}$ = 20 mV, V_{CC} = 54 V
			±1.3	%	$V_{\Delta SENSE}$ = 20 mV, V_{CC} = 54 V, T_J = 25°C to 85°C

SERIAL BUS TIMING CHARACTERISTICS

Table 3.

Parameter	Description	Min	Typ	Max	Unit	Test Conditions/Comments
f_{SCLK}	Clock frequency			400	kHz	
t_{BUF}	Bus free time	1.3			µs	
$t_{HD;STA}$	Start hold time	0.6			µs	
$t_{SU;STA}$	Start setup time	0.6			µs	
$t_{SU;STO}$	Stop setup time	0.6			µs	
$t_{HD;DAT}$	SDAO/SDAI hold time	300		900	ns	
$t_{SU;DAT}$	SDAO/SDAI setup time	100			ns	
t_{LOW}	SCL low time	1.3			µs	
t_{HIGH}	SCL high time	0.6			µs	
t_R[1]	SCL, SDAO/SDAI rise time	20		300	ns	
t_F	SCL, SDAO/SDAI fall time	20		300	ns	

[1] $t_R = (V_{IL(MAX)} - 0.15)$ to $(2.1 + 0.15)$ and $t_F = 0.9\ V_{DD}$ to $(V_{IL(MAX)} - 0.15)$; where $V_{IH3V3} = 2.1$ V, and $V_{DD} = 3.3$ V.

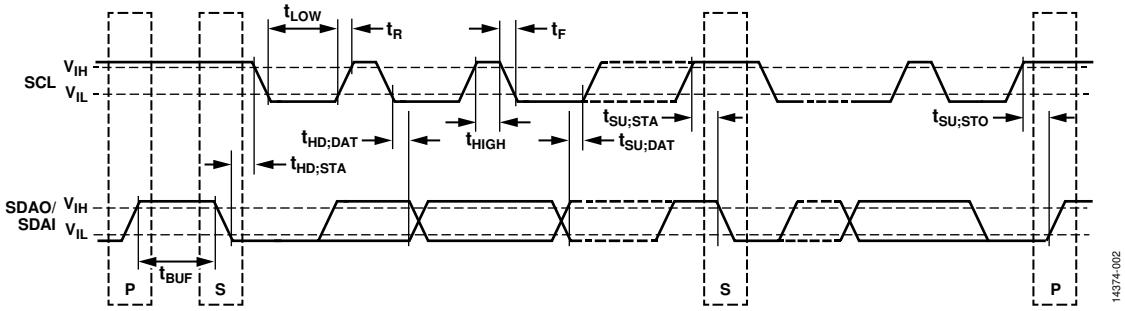


Figure 2. Serial Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VCC, SENSE± to GND	−0.3 V to +120 V
$V_{\Delta SENSE}$ (SENSE+ − SENSE−)	−1 V to +1 V
VOUT to GND	−5 V to +120 V
VCP to GND	−0.3 V to (VOUT + 12 V) or (VCC + 15 V), whichever is lower
GATE (Internal Supply Only)[1] to GND	(VOUT − 0.3 V) to (VCP + 0.3 V)
DVDT to GND	(VOUT − 0.3 V) to (GATE + 0.3 V)
UVH, UVL, OV, MCB to GND	−0.3 V to +6.5 V
ISTART, ISET, VCAP to GND	−0.3 V to +4 V
ESTART, EFAULT, TEMP+ to GND	−0.3 V to VCAP + 0.3 V
VREG (Internal Supply Only) to GND	−0.3 V to +5.5 V
$\overline{\text{FAULT}}$, $\overline{\text{RESTART}}$ to GND	−0.3 V to +20 V
PWGIN, SCL, SDAO, SDAI, ADR0, ADR1 to GND	−0.3 V to +6.5 V
RND to GND	−0.3 V to VCAP + 0.3 V
ENABLE, GPIO1/$\overline{\text{ALERT1}}$/CONV, GPIO2/$\overline{\text{ALERT2}}$, PWRGD to GND	−0.3 V to +20 V
TEMP− Pin to GND (Internally Connected to GND)	0 V
Continuous Current into Any Pin	±10 mA
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range (T_J)	−40°C to +125°C
Lead Temperature, Soldering (10 sec)	300°C
Junction Temperature	125°C

[1] The GATE pin has internal clamping circuits to prevent the GATE pin voltage from exceeding the maximum ratings of a MOSFET with a gate to source voltage (V_{GSMAX}) = 20 V and internal process limits. Applying a voltage source to this pin externally may cause irreversible damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

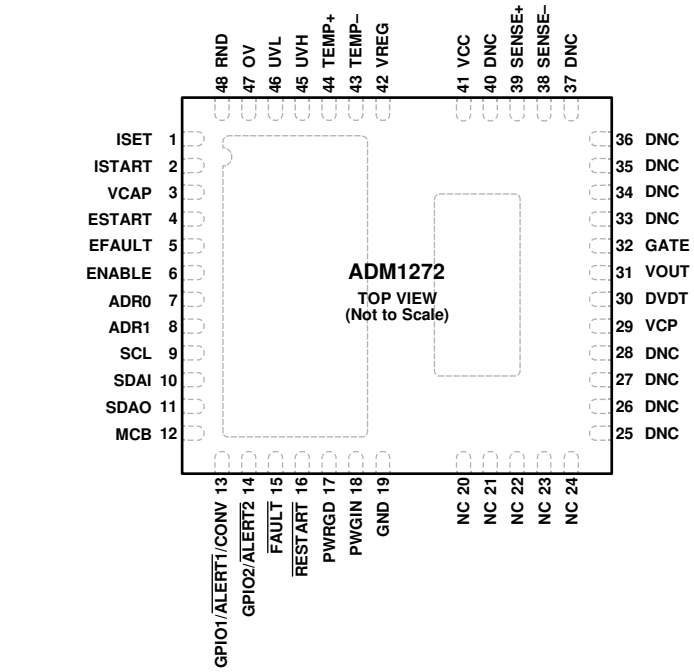
Package Type	θ_{JA}	θ_{JC}	Unit
CP-48-18[1]			
Still Air	50	0.5	°C/W
2 m/sec Air Flow	40	1	°C/W

[1] The thermal resistance values are based on JEDEC 2S2P test conditions.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. THE NC PINS ARE NOT REQUIRED TO BE CONNECTED, BUT DO HAVE INTERNAL CONNECTIONS. THEY SHARE THE SAME ELECTRICAL NODE INTERNALLY TO THE EPVCC PAD AND CAN THEREFORE BE USED AS A THERMAL EXIT ROUTE FROM EPVCC ON THE SAME OUTER LAYER AND SAME ELECTRICAL CONNECTION AS EPVCC.
2. DNC = DO NOT CONNECT. THE DNC PINS MUST NOT BE CONNECTED TO ANY ELECTRICAL SIGNAL, GND, OR SUPPLY VOLTAGE. ANY CONNECT COPPER MUST BE ELECTRICALLY ISOLATED AND APPROPRIATELY SPACED FROM OTHER NODES, WHICH ALLOWS COMPLIANCE WITH IPC-9592 RECOMMENDATIONS FOR 80V.
3. EXPOSED PAD. ALWAYS CONNECT TO GND. THE EXPOSED PAD IS LOCATED ON THE UNDERSIDE OF THE LFCSP PACKAGE AND IS THE LARGER OF THE TWO PADS. SOLDER THE EXPOSED PAD TO THE PCB FOR OPTIMAL THERMAL DISSIPATION.
4. EXPOSED PAD. INTERNALLY CONNECTED TO VCC. THE EXPOSED PAD IS LOCATED ON THE UNDERSIDE OF THE LFCSP PACKAGE AND IS THE SMALLER OF THE TWO PADS. SOLDER THE EXPOSED PAD TO THE PCB FOR OPTIMAL THERMAL DISSIPATION. ALWAYS ELECTRICALLY CONNECT EPVCC TO THE SAME POTENTIAL AS VCC. MOST OF THE DEVICE POWER IS DISSIPATED THROUGH THIS PAD; THEREFORE, CONSIDER A STRONG THERMAL CONNECTION TO AVAILABLE COPPER.

14374-003

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	ISET	Current-Limit Setting. This pin allows the current-limit threshold to be programmed. The default limit of 30 mV is set when this pin is connected directly to 0 V. To achieve a user defined sense voltage, the current limit can be adjusted using a resistor divider from VCAP. An external reference can also be used. The voltage used internally to set the current limit is the voltage between VCAP and ISET. An optional additional resistor from ISET to V_{IN} (or V_{OUT}) can be used to allow the current limit to inversely track V_{IN} (or V_{OUT}), providing an approximate system power limit.
2	ISTART	Start-Up Current limit. This pin allows a separate start-up current limit to be set for power-up modes. When powering up into large capacitive loads, it is desirable to keep the inrush current low and constant to minimize the SOA stress in the MOSFET. The ESTART pin limits the energy when using this mode. The ISTART pin sets the start-up current limit by using a divider from the VCAP pin, $V_{SENSECL} = V_{ISTART}/AV_{CSAMP}$, or if pulled up to VCAP with a 10 kΩ resistor, an internal 1 V threshold is used (25 mV). The start-up current limit is only active prior to PWGDIN being valid. The start-up current limit can also be lowered from the hardware setting over the PMBus with the STRT_UP_IOUT_LIM register. The start-up current limit = $V_{ISTART} \times$ (STRT_UP_IOUT_LIM/16). When using the DVDT pin to set the output voltage ramp, the ISTART pin can also be used as a backup protection feature, but it must be set to a current limit higher than the expected DVDT inrush.
3	VCAP	Internal Regulated 2.7 V Supply. Place a capacitor with a value of 1 µF or greater on this pin to maintain optimal voltage regulation. This pin can be used as a reference to program the ISET pin voltage. To guarantee accuracy specifications, do not load the VCAP pin by more than 100 µA.

Pin No.	Mnemonic	Description
4	ESTART	FET Energy Tracking During Power-Up. This pin approximates the energy in the FET during power-up. The user can place a component network between the ESTART pin and ground that allows the pin voltage to be proportional to the predicted MOSFET junction temperature. If the voltage on the pin exceeds a threshold (1 V), the FET is deemed to be running too close to its SOA and is turned off. This setting assumes lower current limits and greater SOA capability.
5	EFAULT	FET Energy Tracking During Normal Operation. This pin approximates the energy in the FET when faults occur during normal operation. The user can place a component network between the EFAULT pin and ground that allows the pin voltage to be proportional to the predicted MOSFET junction temperature. If the voltage on the pin exceeds a threshold (1 V), the FET is deemed to be running too close to its SOA and is turned off. This setting assumes higher current limits and lesser SOA capability. Considerations must be made if varying ISET with V_{IN}/V_{OUT} when assuming constant current limits.
6	ENABLE	Enable Input. This pin is a digital logic input. This input must be high to allow the ADM1272 hot swap controller to begin a power-up sequence. If this pin is held low, the ADM1272 is prevented from powering up.
7, 8	ADR0, ADR1	PMBus Address. These pins can be tied to GND, tied to VCAP, left floating, or tied low through a resistor for a total of 16 unique PMBus device addresses (see the Device Addressing section).
9	SCL	Serial Clock Pin. SCL is an open-drain input. It requires an external pull-up resistor.
10	SDAI	PMBus Serial Data Input. The serial data is split into an input and an output for easy use with isolators.
11	SDAO	PMBus Serial Data Output. The serial data is split into an input and an output for easy use with isolators.
12	MCB	Mask Circuit Breaker. When the voltage on this pin is greater than the threshold, the SOC shutdown is disabled. The function returns immediately after the voltage returns below this threshold.
13	GPIO1/$\overline{\text{ALERT1}}$/CONV	General-Purpose Digital Input/Output 1 (GPIO1). Alert ($\overline{\text{ALERT1}}$). This pin can be configured to generate an alert signal when one or more fault or warning conditions are detected. Conversion (CONV). This pin can be used as an input signal to control when a power monitor ADC sampling cycle begins. It is also possible to read the state of this pin on the PMBus. This pin defaults to an alert output at power-up. There is no internal pull-up circuit on this pin.
14	GPIO2/$\overline{\text{ALERT2}}$	General-Purpose Digital Input/Output 2 (GPIO2). Alert ($\overline{\text{ALERT2}}$). This pin can be configured to generate an alert signal when one or more fault or warning conditions are detected. It is also possible to read the state of this pin on the PMBus. This pin defaults to an alert output at power-up. There is no internal pull-up circuit.
15	$\overline{\text{FAULT}}$	Fault. This pin asserts low and latches when a fault occurs. The faults that can trigger this pin are an OC fault resulting in the EFAULT/ESTART threshold, an overtemperature fault, or a FET health fault.
16	$\overline{\text{RESTART}}$	Falling Edge Triggered Automatic Restart. The gate remains off for 10 sec by default, and then powers back on. The device has an internal weak pull-up circuit to VCAP. This pin is also used to configure the desired retry scheme. See the Hot Swap Retry section for additional details. The default time for this function is 10 sec. However, this time can be adjusted from 0.1 sec to 25.6 sec by writing to the RESTART_TIME register.
17	PWRGD	Power-Good Signal. This pin indicates that the supply is within tolerance (PWGIN input), no faults are detected, and the ADM1272 hot swap is enabled with the gate fully enhanced.
18	PWGIN	Power-Good Input Threshold. This pin sets the power-good input threshold. The user can set an accurate power-good threshold with a resistor divider from the source of the FET (VOUT). The PWRGD output signal is not asserted until the output voltage is above the threshold set by PWGIN.
19	GND	Ground.
20 to 24	NC	No Connect. The NC pins are not required to be connected, but do have internal connections. They share the same electrical node internally to the EPVCC pad and can therefore be used as a thermal exit route from EPVCC on the same outer layer and same electrical connection as EPVCC.
25 to 28, 33 to 37, 40	DNC	Do Not Connect. The DNC pins must not be connected to any electrical signal, GND, or supply voltage. Any connect copper must be electrically isolated and appropriately spaced from other nodes, which allows compliance with IPC-9592 recommendations for 80 V.

Pin No.	Mnemonic	Description
29	VCP	Internal Charge Pump Voltage Reservoir Capacitor. Connect a capacitor to VOUT to store energy required in the fast gate recovery mode. Ensure that the size of C_{VCP} is at least 10 times that of the parasitic gate capacitance. If C_{VCP} is greater than 500 nF, add additional delays to the initial power-on delay. See the FET Gate Drive section.
30	DVDT	Output Voltage Ramp Rate Setting. The DVDT pin sets a linear output voltage ramp rate. During power-up events, this pin is internally connected to the GATE pin. This internal connection allows the output voltage ramp to be predominately determined by I_{GATEUP} and C_{DVDT}. When the power-up is complete, the DVDT pin is disconnected from the GATE pin and connected to VOUT to prevent impeding the GATE shutdown time. A 20 kΩ resistor must be used in series with the capacitor to limit pin currents during fast transients on VOUT. Use a high voltage capacitor.
31	VOUT	Output Voltage. Connect this pin directly to the source of the MOSFET (output voltage). The GATE pin is referenced from this node and pull-down currents flow through this pin. PCB routing must be sized accordingly to allow all GATE shutdown currents. This pin is also used to read back the output voltage using the internal ADC. It also enables V_{DS} monitoring across the MOSFET to feed back to the SOA protection scheme.
32	GATE	Gate Driver. This pin is the high-side gate drive of an external N channel FET. This pin is driven by the FET drive controller, which uses a charge pump to provide a pull-up current to charge the FET gate pin. The FET drive controller regulates to a maximum load current by regulating the GATE pin. GATE is held to the VOUT pin when the supply is below the UVLO threshold.
38	SENSE−	Negative Current Sense Input. A sense resistor between the SENSE+ pin and the SENSE− pin sets the analog current limit. The hot swap operation of the ADM1272 controls the external FET gate to maintain the sense voltage ($V_{SENSE+} - V_{SENSE-}$). This pin also connects to the FET drain pin.
39	SENSE+	Positive Current Sense Input. This pin connects to the main supply input. A sense resistor between the SENSE+ pin and the SENSE− pin sets the analog current limit. The hot swap operation of the ADM1272 controls the external FET gate to maintain the sense voltage ($V_{SENSE+} - V_{SENSE-}$). This pin also measures the supply input voltage using the ADC.
41	VCC	Positive Supply Input. An undervoltage lockout (UVLO) circuit resets the device when a low supply voltage is detected. GATE is held low when the supply is below UVLO. During normal operation, the voltage on this pin must remain greater than or equal to SENSE+ to ensure that specifications are adhered to. No sequencing is required.
42	VREG	Internal Regulated 5 V Supply. Place a capacitor with a value of 1 µF or greater on this pin to maintain optimal regulation. Do not load this pin externally.
43	TEMP−	Temperature Input GND. Connect this pin directly to the low side of the NPN device.
44	TEMP+	Temperature Input. An external NPN device can be placed close to the MOSFETs and connected back to this pin to report the temperature. The voltage at the TEMP+ pin is measured by the ADC.
45	UVH	Undervoltage Rising Input. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect whether the supply is under the UVH limit.
46	UVL	Undervoltage Falling Input. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect whether the supply is under the UVL limit.
47	OV	Overvoltage Input. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect whether the supply is above the OV limit.
48	RND	Random Delay. A capacitor on this pin sets the minimum and maximum power-up delay time range. With no capacitor on this pin, the system delay is from 0.43 ms to 27.5 ms. With a maximum of 220 nF, the delay can be from 54.3 ms to 3.0 sec. This delay is active only after VCC comes out of UVLO and, therefore, is only present at each power cycle.
	EPGND	Exposed Pad. Always connect to GND. The exposed pad is located on the underside of the LFCSP package and is the larger of the two pads. Solder the exposed pad to the PCB for optimal thermal dissipation.
	EPVCC	Exposed Pad. Internally connected to VCC. The exposed pad is located on the underside of the LFCSP package and is the smaller of the two pads. Solder the exposed pad to the PCB for optimal thermal dissipation. Always electrically connect EPVCC to the same potential as VCC. Most of the device power is dissipated through this pad; therefore, consider a strong thermal connection to available copper.

TYPICAL PERFORMANCE CHARACTERISTICS

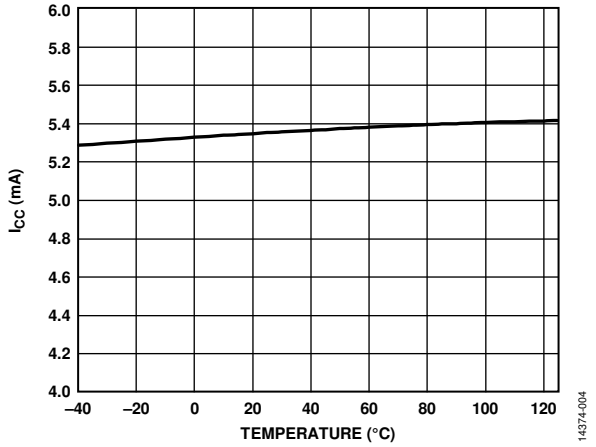


Figure 4. Supply Current (I_{CC}) vs. Temperature

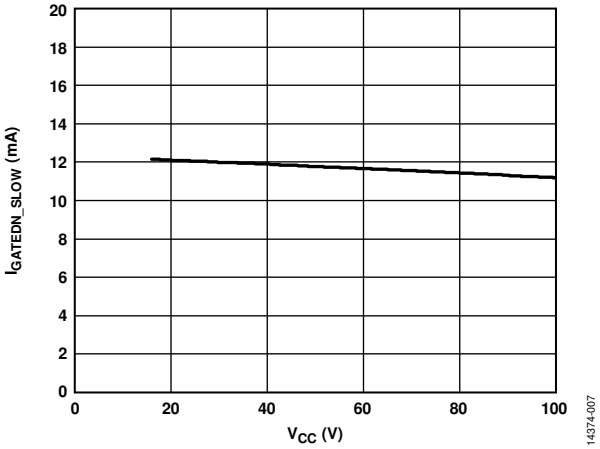


Figure 7. GATE Slow Pull-Down Current (I_{GATEDN_SLOW}) vs. V_{CC}

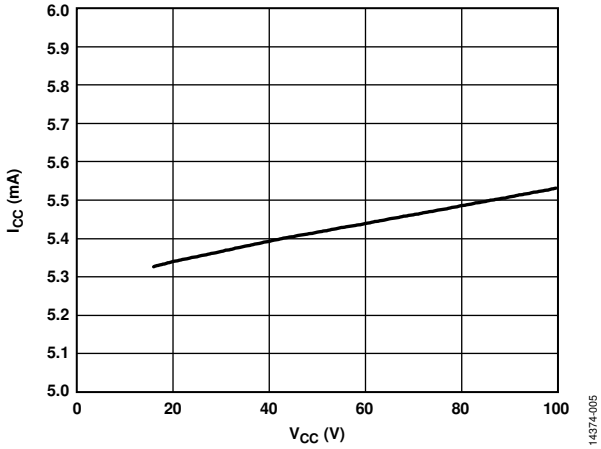


Figure 5. Supply Current (I_{CC}) vs. V_{CC}

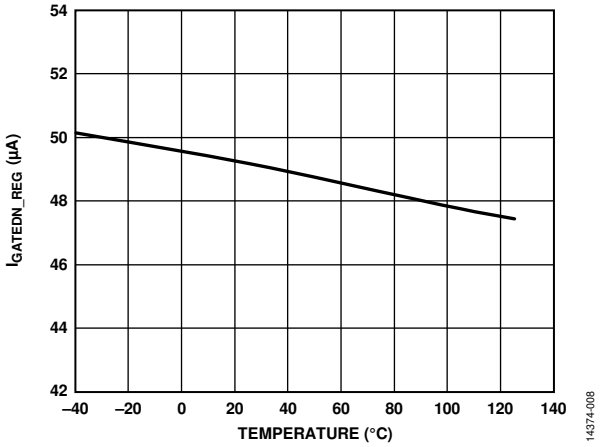


Figure 8. GATE Regulation Pull-Down Current (I_{GATEDN_REG}) vs. Temperature

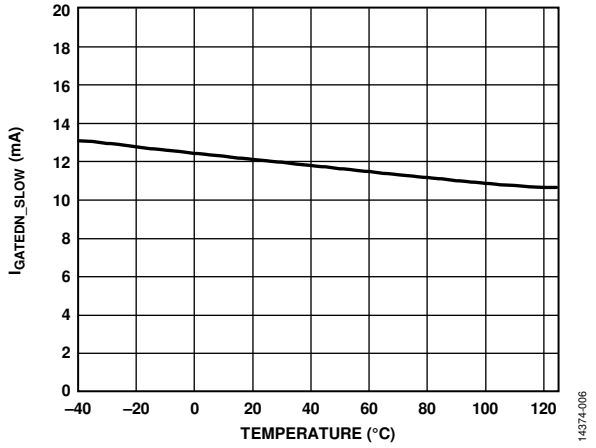


Figure 6. GATE Slow Pull-Down Current (I_{GATEDN_SLOW}) vs. Temperature

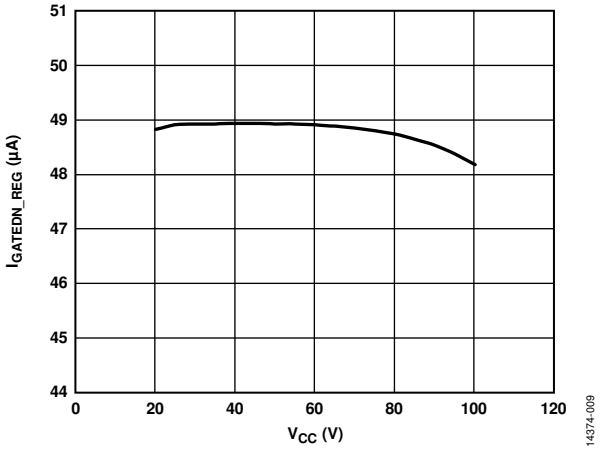


Figure 9. GATE Regulation Pull-Down Current (I_{GATEDN_REG}) vs. V_{CC}

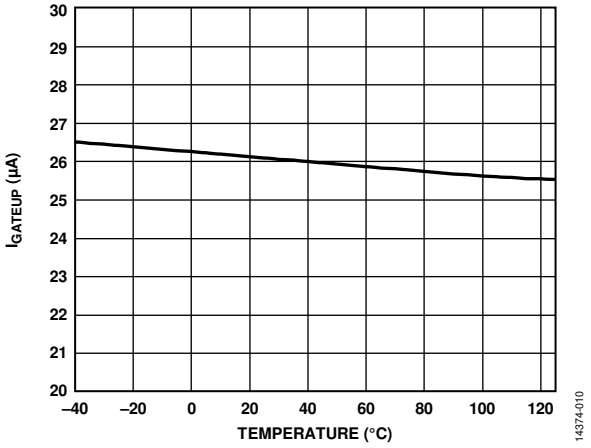


Figure 10. GATE Pull-Up Current (I_{GATEUP}) vs. Temperature

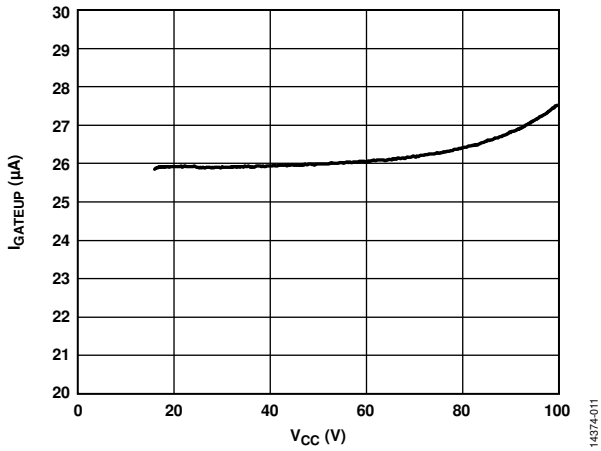


Figure 11. GATE Pull-Up Current (I_{GATEUP}) vs. V_{CC}

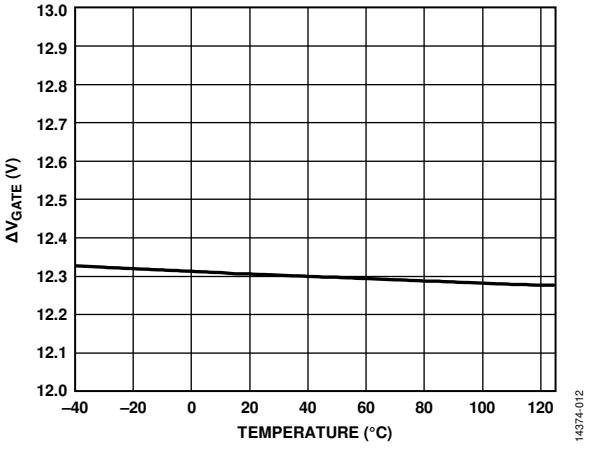


Figure 12. ΔV_{GATE} (5 µA Load) vs. Temperature

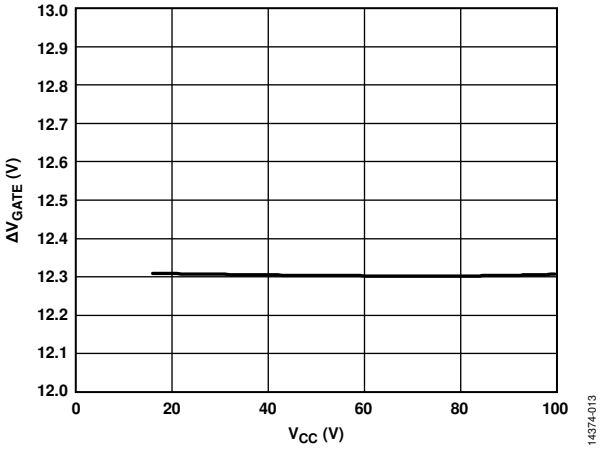


Figure 13. V_{GATE} (5 µA Load) vs. V_{CC}

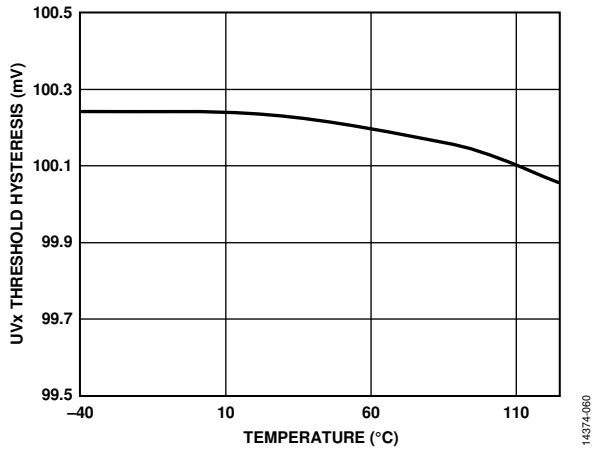


Figure 14. UVx Threshold Hysteresis vs. Temperature

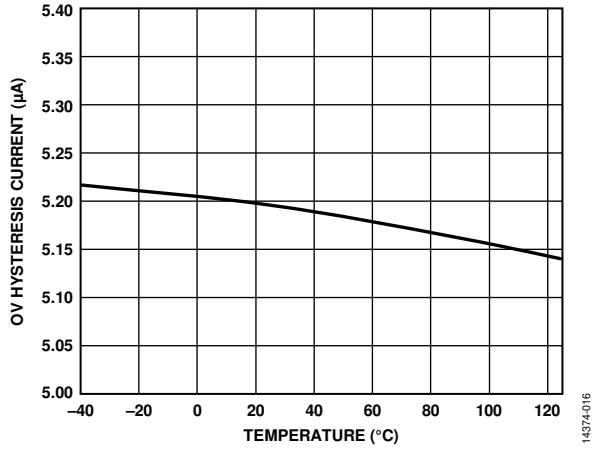


Figure 15. OV Hysteresis Current vs. Temperature

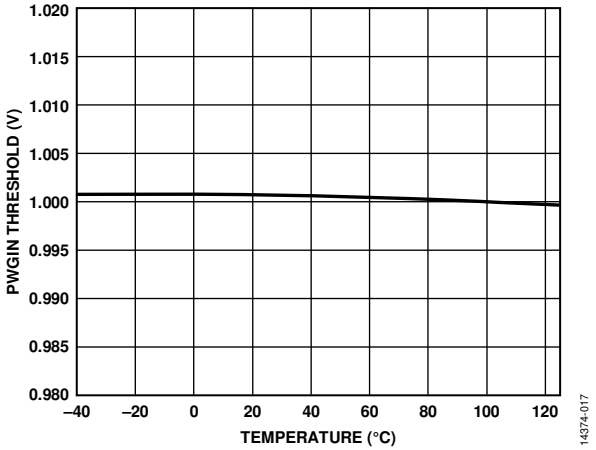


Figure 16. PWGIN Threshold vs. Temperature

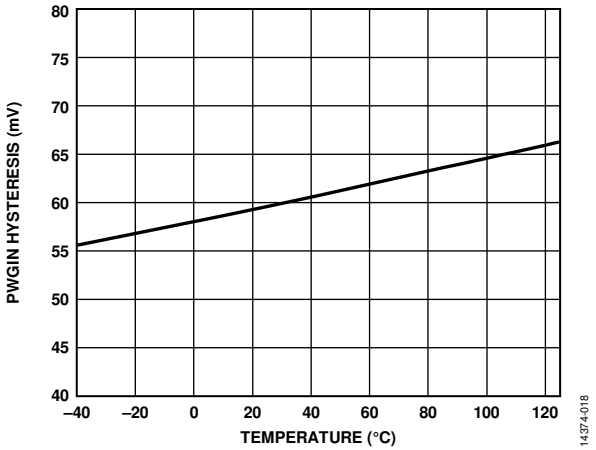


Figure 17. PWGIN Hysteresis vs. Temperature

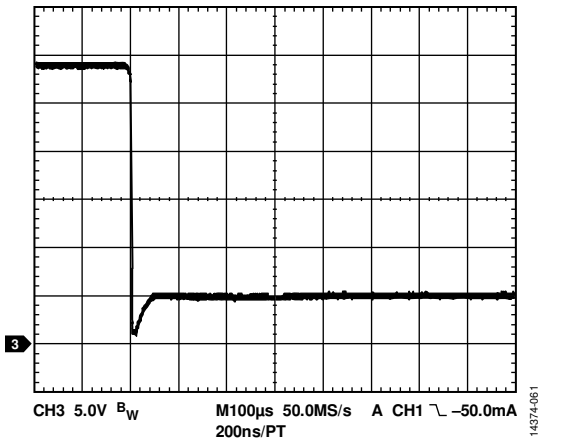


Figure 18. VGATE Response to Severe Overcurrent Event (GATE Fast Pull-Down)

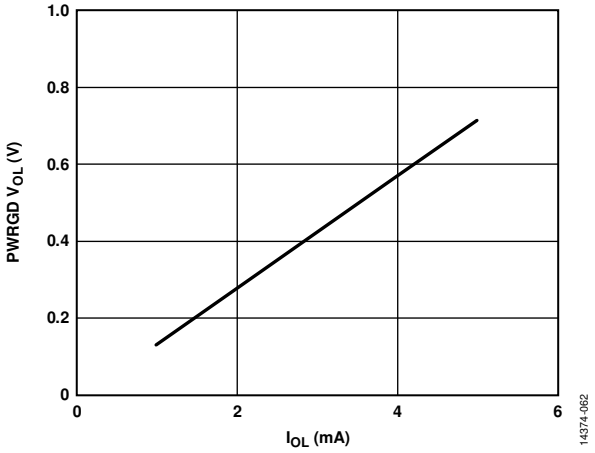


Figure 19. PWRGD V_{OL} vs. I_{OL}

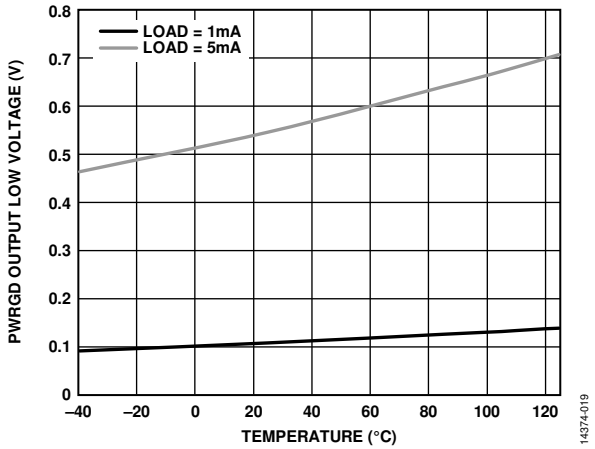


Figure 20. PWRGD Output Low Voltage (V_{OL}) vs. Temperature

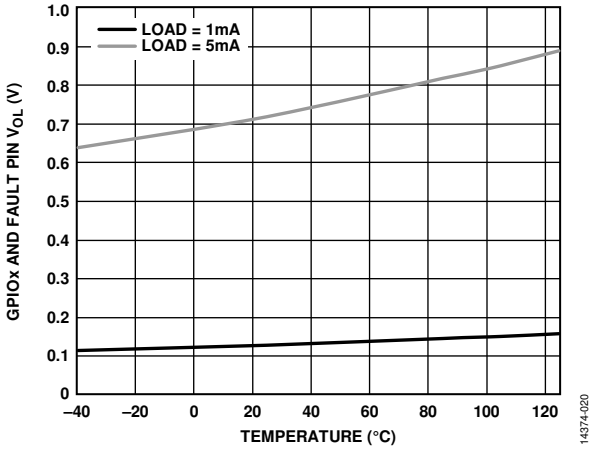


Figure 21. GPIOx and Fault Pin V_{OL} vs. Temperature

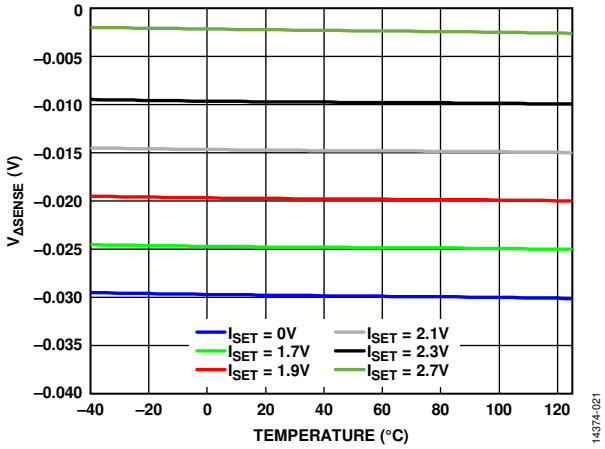


Figure 22. $V_{\Delta SENSE}$ vs. Temperature, V_{ISET} with 1 Ω Sense Resistor

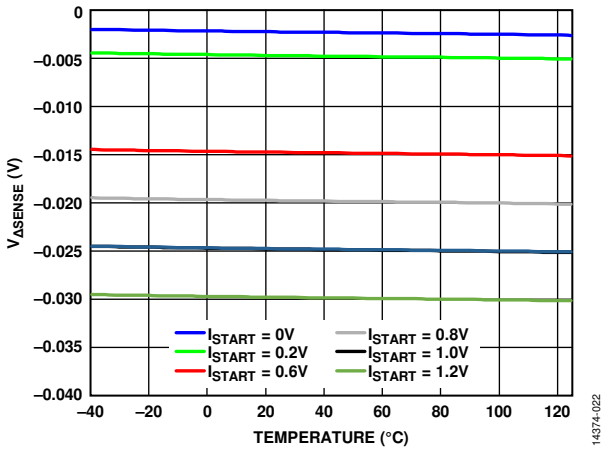


Figure 23. $V_{\Delta SENSE}$ vs. Temperature, V_{ISTART} with 1 Ω Sense Resistor

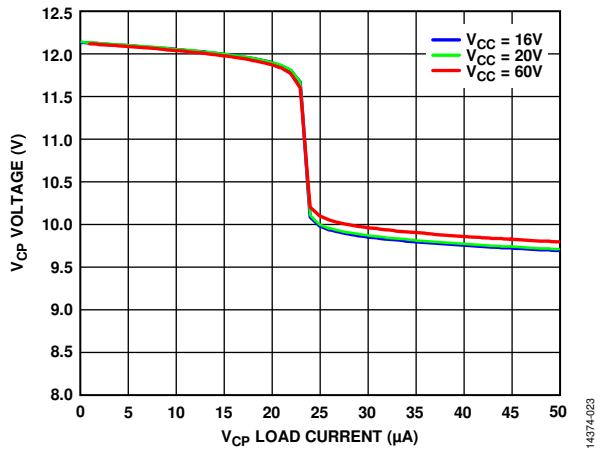


Figure 24 V_{CP} Load Regulation

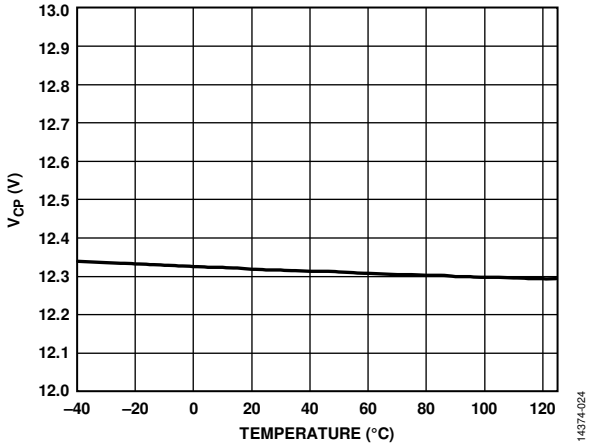


Figure 25. V_{CP} vs. Temperature

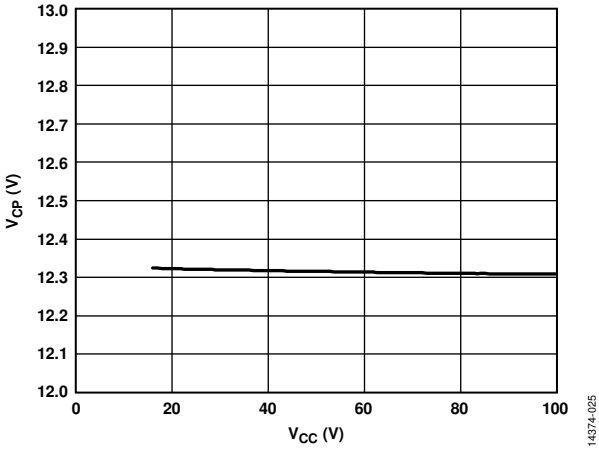


Figure 26. V_{CP} vs. V_{CC}

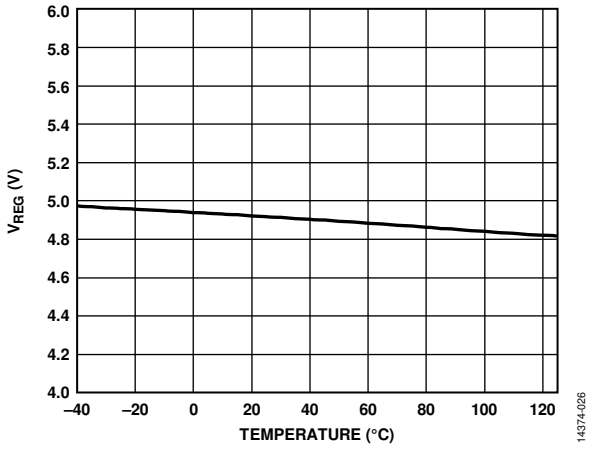


Figure 27. V_{REG} vs. Temperature

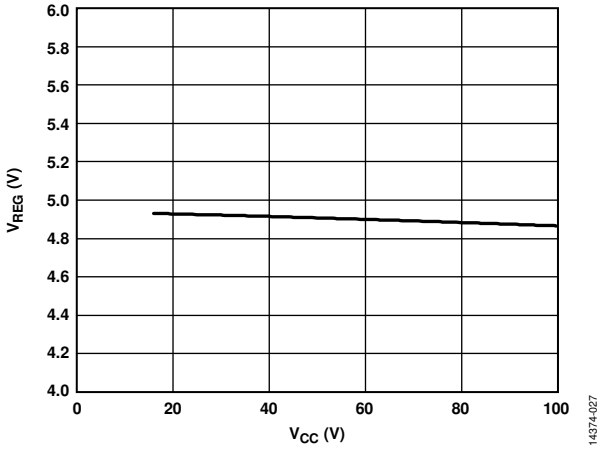


Figure 28. V_{REG} vs. V_{CC}

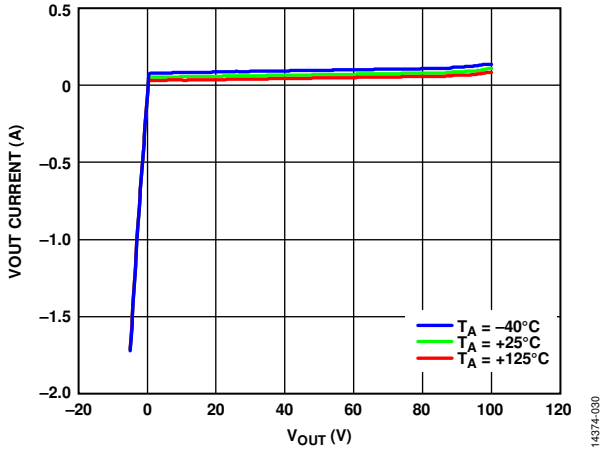


Figure 31. VOUT Current vs. V_{OUT}

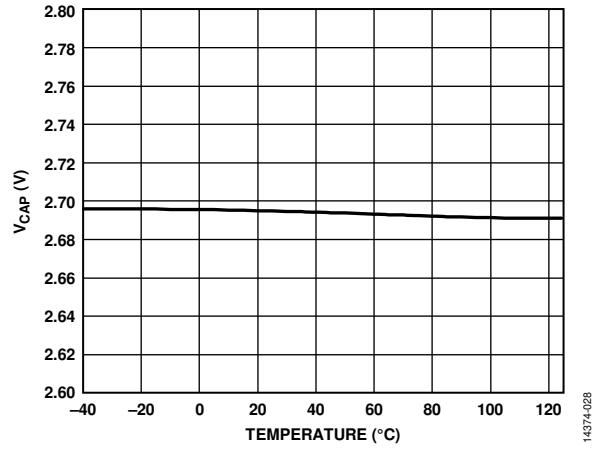


Figure 29. V_{CAP} vs. Temperature

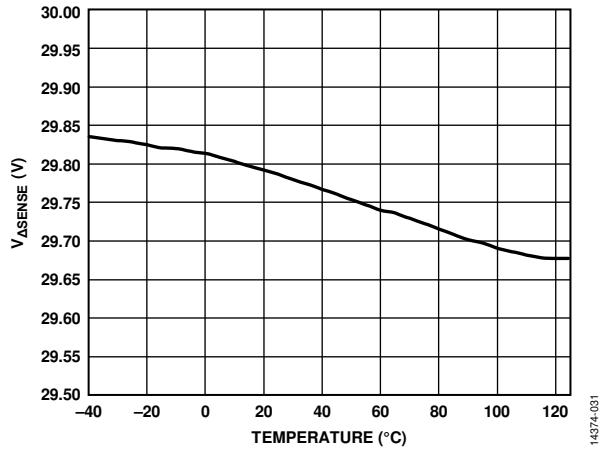


Figure 32. $V_{\Delta SENSE}$ vs. Temperature at ISET = 0

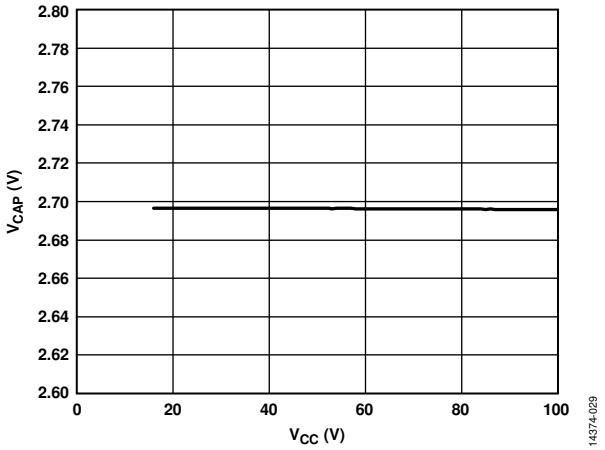


Figure 30. V_{CAP} vs. V_{CC}

THEORY OF OPERATION

When circuit boards are inserted into a live backplane, discharged supply bypass capacitors draw large transient currents from the backplane power bus as they charge. These transient currents can cause permanent damage to connector pins, as well as dips on the backplane supply that can reset other boards in the system.

The ADM1272 is designed to manage the powering on and off of a system in a controlled manner, allowing a board to be removed from, or inserted into, a live backplane by protecting it from excess currents. After power-up is complete, the ADM1272 continues to protect the system from faults. These faults include overcurrent, short circuit, overvoltage, undervoltage, and transient disturbances on the backplane, and some FET fault issues. The ADM1272 is usually placed on a system/board that is removable. However, it also can be placed on the backplane in some cases. The ADM1272 also has the capability of measuring and reporting power and energy telemetry.

POWERING THE ADM1272

A supply voltage from 16 V to 80 V is required to power the ADM1272 via the VCC pin. An internal regulator provides a 5 V rail, which is presented on the VREG pin, to supply the digital section of the ADM1272 (for internal use only), and must be decoupled according to the VREG pin description in Table 6.

The VCC pin provides the majority of the bias current for the device; however, some bias currents are supplied through the SENSE± pins. Both the VCC and SENSE+ pins can be connected to the same voltage node, but in most applications, it is recommended to connect an RC filter to the VCC pin to avoid resets due to very fast transients on the input rail (see Figure 33).

Choose the values of these components such that a time constant is provided that can filter any expected glitches. However, use a resistor that is small enough to keep voltage drops caused by quiescent current to a minimum. Do not place a supply decoupling capacitor on the rail before the FET, unless a series resistor is used to limit the inrush current.

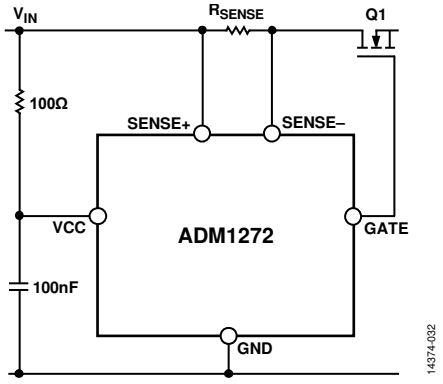


Figure 33. Reinforced Transient Glitch Protection Using an RC Network

UV AND OV

The ADM1272 monitors the supply voltage for UV and OV conditions. The OV pin is connected to the input of an internal voltage comparator, and its voltage level is internally compared with a 1 V voltage reference. The user can program the value of the OV hysteresis by varying the top resistor of the resistor divider on the pin. This impedance in combination with the 5 µA OV hysteresis current (current turned on after OV triggers) sets the OV hysteresis voltage.

$$OV_{RISING} = OV_{THRESHOLD} \times \frac{R_{TOP} + R_{BOTTOM}}{R_{BOTTOM}}$$

$$OV_{FALLING} \approx OV_{RISING} - (R_{TOP} \times 5\ \mu A)$$

The UV detector is split into two separate pins, UVH and UVL. The voltage on the UVH pin is compared internally to a 1 V reference, whereas the UVL pin is compared to a 0.9 V reference. Therefore, if the pins are tied together, the UV hysteresis is 100 mV. The hysteresis can be adjusted by placing a resistor between UVL and UVH.

Figure 1 shows the voltage monitoring input connection. An external resistor network divides the supply voltage for monitoring. An undervoltage event is detected when the voltage connected to the UVL pin falls below 0.9 V, and the gate is shut down using the 10 mA pull-down device. The fault is cleared after the UVH pin rises above 1.0 V.

Similarly, when an overvoltage event occurs and the voltage on the OV pin exceeds 1 V, the gate is shut down using the 10 mA pull-down device.

For the maximum rating on the UVx and OV pins, see Table 4. If transients are expected on the main input line, use external protection circuitry to protect the inputs and to allow these pin voltages to exceed their rating.

HOT SWAP CURRENT SENSE INPUTS

The load current is monitored by measuring the voltage drop across an external sense resistor, R_{SENSE}. An internal current sense amplifier provides a gain of 40 to the voltage drop detected across R_{SENSE}. The result is compared to an internal reference and used by the hot swap control logic to detect when an overcurrent condition occurs.

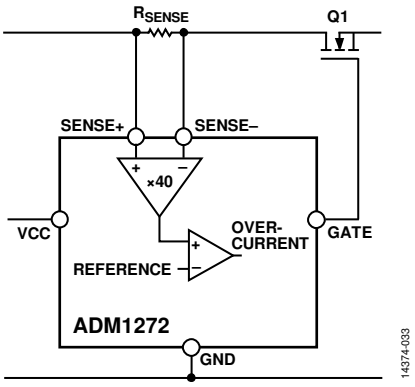


Figure 34. Hot Swap Current Sense Amplifier

The SENSE± inputs can be connected to multiple parallel sense resistors. The way the sense points of these resistors are combined has a significant effect on the accuracy of the voltage drop detected by the ADM1272.

To achieve better accuracy, averaging resistors can be used to sum the voltages from the nodes of each sense resistor, as shown in Figure 35. A typical value for the averaging resistors is 10 Ω, enough to be significantly greater than the trace resistance. The input current to each sense pin is matched to within 5 μA. This matching ensures that the same offset is observed by both sense inputs, reducing differential errors.

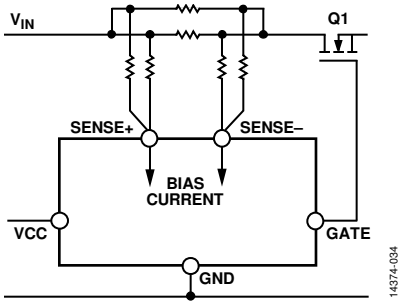


Figure 35. Connection of Multiple Sense Resistors to the SENSE± Pins

CURRENT-LIMIT MODES

The ADM1272 features dual current limits, one for startup (ISTART) and one for normal operation (ISET). At startup, the ISTART pin determines the current limit used during power-up. This dual current limit allows users to program an independent current limit at startup, specific to the conditions of the start-up profile and expectations. After startup is complete, the system switches to the main current limit determined by ISET. The conditions that must be satisfied for this switch to occur are as follows:

- The system is not in current limit.
- (V_{OUT} − V_{IN}) < 2 V.
- The gate voltage is fully enhanced (V_{GS} > 10 V).

The system remains at the normal current limit (ISET) unless there is an interruption triggered by an OV, UV, or manual shutdown (enable, restart, or PMBus command) and this interruption results in V_{DS} > 2 V and inactive PWRGD. If this interruption occurs, the system resets to ISTART and assumes a full system restart. For this reset to happen, a shutdown must be signaled with enough time to allow the gate to disable the FETs and the output to discharge. However, the system remains in ISET current limit following an OC fault to allow a recovery attempt. If the system cannot recover, a latchoff occurs and ISTART assumes control at the next startup.

SETTING THE CURRENT LIMITS (ISET/ISTART)

The current limit is typically determined by selecting a sense resistor to match the current sense voltage limit on the controller for the desired load current. However, as currents become larger, the sense resistor requirements become smaller, and resolution can be difficult to achieve when selecting the appropriate sense resistor or combination thereof. The ADM1272 provides adjustable current sense voltage limits to manage this issue. The device allows the user to program the required current sense voltage limits independently up to 30 mV. The recommended range is 2.5 mV to 30 mV, although tolerances and errors increase as $V_{SENSECL}$ decreases.

In conjunction with the sense resistor, the current-limit reference voltage determines the load current level to which the ADM1272 limits the current during an overcurrent event. This reference voltage is compared to the amplified current sense voltage to determine whether the limit is reached.

The active current-limit reference voltage input to the internal comparator is clamped to a minimum level of 100 mV (that is, $V_{SENSECL}$ = 2.5 mV) to prevent current limits being set too low, which may result in zero current flow across all conditions.

The current limit set by the ISET/ISTART pins is the current at which the ADM1272 tries to regulate when the load requires more current. This current limit, defined by the reference to the current control loop, is the regulation current limit or I_{REG} ($V_{SENSECL}$ at the sense voltage).

Another current-limit threshold just below I_{REG} that alerts the ADM1272 when the current limit is reached and is active, is the circuit breaker current limit or I_{CB} (V_{CB} at sense voltage). V_{CB} can be expressed at the sense pins (in mV) as follows:

$$V_{CB} = V_{SENSECL} - V_{CBOS}$$

where V_{CBOS} is the circuit breaker offset and is listed in Table 1 as 1.1 mV (typical).

ISTART

The ISTART pin sets the start-up current limit in start-up mode using a divider from the VCAP pin, or if pulled up to VCAP with a 10 kΩ resistor, an internal 1 V threshold is used (25 mV).

The VCAP pin has a 2.7 V internal regulated voltage that can be used as a reference to set a voltage at the ISET pin. Assuming that V_{ISET} equals the voltage on the ISET pin, size the resistor divider to set the ISET voltage as follows:

$$V_{ISTART} = V_{SENSECL} \times 40$$

where $V_{SENSECL}$ is the current sense voltage limit.

The default value of 25 mV is achieved by connecting the ISET pin directly to the VCAP pin (or V_{ISTART} > 1.65 V). This connection configures the device to use an internal 1 V reference, which equates to 25 mV at the sense inputs (see Figure 36).

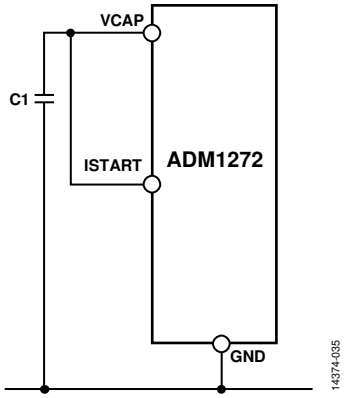


Figure 36. Fixed 25 mV ISTART Current Sense Limit

To program the sense voltage from 10 mV to 30 mV, a resistor divider sets the reference voltage on the ISET pin (see Figure 37).

When using the DVDT pin to set the output voltage ramp, set the ISTART pin high enough to prevent the inrush current from reaching the current limit.

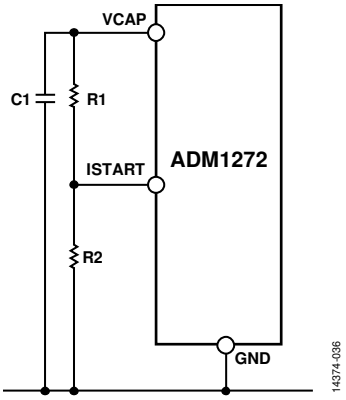


Figure 37. Adjustable 5 mV to 30 mV Current Sense Limit

The start-up current limit can be programmed via the ISTART pin or reduced via the PMBus register, STRT_UP_IOUT_LIM (Register 0xF6). If both are configured, the lowest current limit is selected as the active current limit. The clamp level in both cases is a 2.5 mV $V_{\Delta SENSE}$ current limit.

The start-up current limit PMBus register is set to the maximum value at power-on reset; therefore, the ADM1272 uses the ISTART pin setting by default.

If configuring the start-up current limit with the PMBus register, the start-up current limit is set as a fraction of the effective ISET current limit. There are four register bits so that the start-up current limit can be set from 1/16th to 16/16th of the normal current limit. The effective ISTART voltage can be calculated as

$$V_{ISTART} = (V_{VCAP} - V_{ISET}) \times \left(\frac{STRT\_UP\_IOUT\_LIM + 1}{16} \right)$$

The start-up circuit breaker and current limits can then be calculated from this effective ISTART voltage.

ISET

The ISET pin sets the system current limit during normal operation using a divider from the VCAP pin or pulled down to GND. The ISET pin differs from ISTART in that the resulting current-limit reference voltage is not the voltage presented on the pin, but the difference between VCAP and ISET. This relationship is presented as follows:

$$V_{VCAP} - V_{ISET} = V_{SENSECL} \times 40$$

where $V_{SENSECL}$ is the current sense voltage limit.

This configuration allows a third optional resistor (from ISET to V_{IN}) to be used to allow the current limit to inversely track the input voltage. This feature is useful to avoid overdesigning the system current limit and allows the maximum current demand to output load at low V_{IN}, which results in an unnecessarily high current limit for maximum V_{IN}. The high current limit may even exceed input power limitations.

The default value of 30 mV is achieved by pulling the ISET pin directly to GND (or V_{ISET} < 1.5 V). Although the ISET pin may be at 0 V, the internal buffered ISET voltage does not drop below 1.5 V. This configuration clamps the current-limit reference voltage to 1.2 V ($V_{VCAP} - V_{ISET}$), which equates to 30 mV at the sense inputs (see Figure 38).

For information about the protection of the FET SOA, see the Safe Operating Area Protection (ESTART/EFAULT) section.

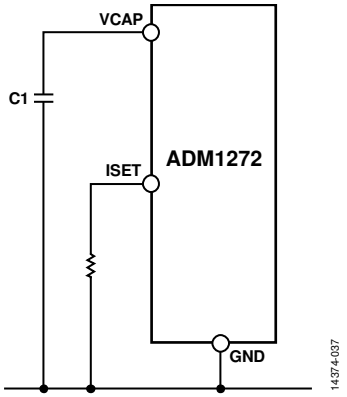


Figure 38. Fixed 30 mV ISET Current Sense Limit

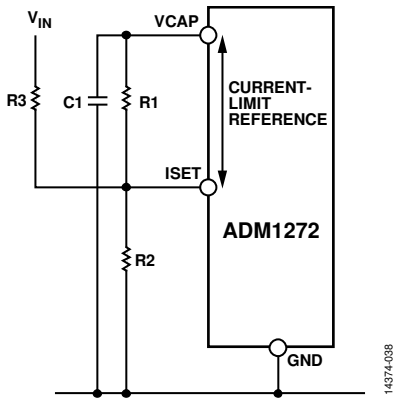


Figure 39. Programming the Variable Current Sense Limit (R3 for Power Limit Setting)

SETTING A LINEAR OUTPUT VOLTAGE RAMP AT POWER-UP (DVDT)

The most common method of power-up in a typical application is to configure a single linear voltage ramp on the output, which allows a constant inrush current into the load capacitance. This method has the advantage of setting slow ramp times, which result in low inrush currents. This method is often required to limit supply inrush demand and to prevent high capacitive loads from stressing the FET SOA.

This design allows a linear monotonic power-up event without the restrictions of the system current limit or fault timer. A power-up ramp is set such that the inrush is low enough not to reach the active circuit breaker current limit, which allows the power-up to continue without any closed-loop interaction but still uses the active current limit to protect against fault conditions. A capacitor on the DVDT pin sets the dv/dt ramp rate of the output voltage. However, the parasitic FET gate capacitances also contribute to the total gate capacitance and must be considered.

The DVDT pin is internally connected to the GATE pin only during start-up mode. When the startup is complete, the DVDT pin is disconnected from the GATE pin and connected internally to VOUT. This configuration prevents unnecessary capacitive loading of GATE, which can slow shutdown responses to faults and impede recovery from transient conditions. The DVDT pin is reconnected to GATE prior to any subsequent start-up events.

To ensure that the inrush current does not approach or exceed the active current-limit level, the output voltage ramp can be set by selecting the appropriate value for C_{DVDT}, as follows:

$$C_{DVDT} = (I_{GATEUP}/I_{INRUSH}) \times C_{LOAD}$$

where:
C_{DVDT} is the total gate capacitance (including FET parasitics).
I_{GATEUP} is the specified gate pull-up current.
C_{LOAD} is the load capacitance.

Add margin and tolerance as necessary to ensure a robust design. Subtract any parasitic gate drain capacitance, C_{GD}, of the MOSFETs from the total to determine the additional external capacitance required.

Next, the power-up ramp time can be approximated by

$$t_{RAMP} = (V_{IN} \times C_{LOAD})/I_{INRUSH} = (V_{IN} \times C_{DVDT})/I_{GATEUP}$$

Check the SOA of the MOSFET for conditions and the duration of this power-up ramp. For more information about protection of the FET SOA during start-up faults, see the information about the protection of the FET SOA, see the Safe Operating Area Protection (ESTART/EFAULT) section.

The diagram in Figure 40 shows a typical hot swap power-up with a DVDT capacitor configured for a linear output voltage ramp.

The ISTART current limit can also be used to provide a constant current instead of using the DVDT pin. However, if linear output voltage ramps are preferred, use of the DVDT function is recommended with an ISTART level above any expected inrush current profiles as protection. Loads can often require dynamic currents, which may result in nonlinear profiles when using a constant current control at startup. In addition, if very low current limits are required (in comparison to the main current limit), using a closed-loop system may result in wide tolerance and/or current limits below the recommended range of V_{SENSE}.

When configuring with the ISTART pin, calculate the circuit breaker (CB) level using the following equation:

$$Start\text{–}Up\ CB = \frac{\left(\frac{V_{ISTART}}{40} - 1.1\,\text{mV}\right)}{R_{SENSE}}$$

To prevent the start-up current limit from being triggered during a normal slew rate controlled power-up, set the circuit breaker level above the maximum expected inrush current.

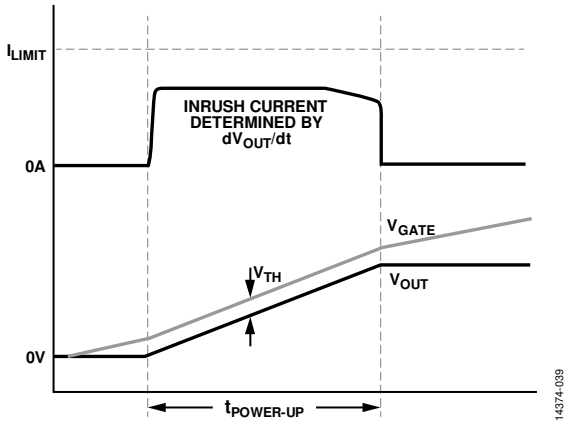


Figure 40. Linear Voltage Ramp Power-Up

SAFE OPERATING AREA PROTECTION (ESTART/EFAULT)

The ADM1272 features an FET protection scheme that offers increased flexibility for managing various system conditions while still protecting the FET from SOA stress.

Traditional timer schemes uses a single fault timer to protect the FET when regulating current or when current limits are exceeded. This approach requires the timers to be set to worst case conditions like short circuits, which limits the robustness of the solution to various system conditions/faults.

For short circuits, the SOA requires the setting of a short timer because the FET V_{DS} is very high. However, for a load fault that results in only a few volts across the FET V_{DS}, because the timer is optimized for worst case conditions, the timer setting remains very short. If a transient fault occurs, resulting in a momentary active current limit but only a few volts of V_{DS}, the system is likely to shut down quickly even though the FET SOA is not exceeded because V_{DS} is low and can operate longer. This condition is problematic during common scenarios such as input line steps and disturbances.

To accommodate these conditions and ensure there are no unnecessary shutdowns, the ADM1272 monitors and uses the FET V_{DS} to optimize how long the FET is allowed to remain in regulation. The ESTART and EFAULT pins control this regulation time for start-up mode and normal mode, respectively. Each pin programs an independent setting for each mode of operation to allow SOA protection to be optimized for its respective current limit. As the system transitions from one mode to another, the ADM1272 retains any potential recent SOA stress history by copying the same voltage from the ESTART pin to the EFAULT pin at transitions and vice versa.

The assumption is that, although there is a significant level of V_{DS} across the FET, its drain current, I_D, is being held constant (at the limit); thus, the FET power is proportional to V_{DS}. The SOA curve of the FET indicates the amount the FET can dissipate, for a given time, before the junction temperature reaches its maximum and SOA is breached. A current source (I_{VDS}) equivalent to 1 µA per 1 V V_{DS} is sourced from EFAULT/ESTART. Through analysis and manipulations of the SOA curves, for a given fixed current, an RC configuration from EFAULT/ESTART to GND can provide a solution to ensure the voltage on the pin reaches 1 V before the SOA is exceeded. This configuration presents a profile on the EFAULT/ESTART pin that is representative of the FET junction temperature. Upon reaching 1 V, the device deems the FET to be at the SOA limit and latches off. This solution results in fault on times that are proportional to V_{DS} and allows low V_{DS} faults to recover without latching off, while ensuring high V_{DS} faults are latched off immediately.

Although the EFAULT and ESTART pins provide the same function for their respective operation mode, there is one subtle difference: the ESTART pin enables I_{VDS} only when the current exceeds I_{CB}, whereas the EFAULT I_{VDS} is solely dependent on V_{DS}.

A pull-down current of 500 nA discharges the RC network, which allows a single capacitor on each pin to be used at the expense of being able to use less of the SOA. When the current control loop is near regulation, this 500 nA pull-down current is disabled and a 1 µA pull-up current enabled. The 1 µA current ensures that the EFAULT and ESTART pins run current even if there is a very small V_{DS}, thus allowing the system to power down if this condition lasts for an extended period. If conditions prevent the pins from reaching 1 V while at a low V_{DS} (where the SOA may indicate dc), there is an internal 100 ms limit, after which the system returns a fault and latches off. This backup limit prevents overheating in a steady state in the MOSFET. The 100 ms timer runs when V_{GS} is <10 V and the current is in regulation.

FET GATE DRIVE

The ADM1272 is designed to control a high-side gate drive of an external N channel FET. The GATE pin is driven by the FET drive controller, which uses a charge pump to provide a pull-up current to charge the FET gate pin. The FET drive controller regulates to a maximum load current by regulating the GATE pin. GATE is held to the VOUT pin when the supply is below the UVLO limit.

The GATE pin features a G_M amplifier output that sources and sinks the GATE node to regulate the current. When a shutdown is requested, the GATE pin uses a 10 mA pull-down device to disable the FET and this pull-down device remains active when the FET is disabled.

The charge pump used on the GATE pin is capable of driving V_{GS} to >10 V, but it is clamped to less than 14 V above VOUT. These clamps ensure that the maximum V_{GS} rating of the FET is not exceeded.

FAST RESPONSE TO SEVERE OVERCURRENT

The ADM1272 features a separate high bandwidth current sense amplifier that detects a severe overcurrent indicative of a short-circuit condition. A fast response time allows the ADM1272 to handle events of this type that may otherwise cause catastrophic damage if not detected and prevented quickly. The fast response circuit ensures that the ADM1272 can detect an overcurrent event at approximately 150% to 400% (default 200%) of the normal current limit set by the ISET pin, and can respond to and control the current within 1 µs in most cases.

There are four severe overcurrent threshold options and four severe overcurrent glitch filter options selectable via the PMBus registers as follows:

- Thresholds: 150%, 200%, 300%, 400%
- Glitch filters: 500 ns, 1 µs, 5 µs, 10 µs

The GATE pin of the ADM1272 is pulled down with ~1.5 A for a maximum duration of 10 µs. Following a severe OC shutdown, by default, the device attempts to regain control of the FET one time. To expedite recovery after sudden shutdown events, a gate boost circuit is enabled to bring the gate voltage back to the FET

V_{TH} threshold within ~50 µs. After the current sense amplifier detects 2 mV at the sense pins, this circuit is disabled and the normal gate drive resumes.

MCB

The MCB pin (mask circuit breaker) is designed to mask the severe overcurrent circuit, when enabled. If the voltage on this pin exceeds the threshold, the severe OC detector is disabled for the duration, which disables the large GATE pull-down circuit while the pin is high. All other protection features remain intact.

RND

The RND pin allows the user to insert a random delay into the start-up routing, which allows staggered distribution of power-up on multiple systems, when commanded simultaneously. Allow this pin to float when not in use. There is a maximum timeout feature of 3 sec to prevent faulty capacitors from impeding a startup.

Table 7. Typical Delay Time with External Capacitor

RND Capacitor	Minimum Time	Maximum Time
None (~10 pF)	0.43 ms	27.5 ms
4.7 nF	1.58 ms	101 ms
10 nF	2.88 ms	184 ms
22 nF	5.82 ms	372 ms
47 nF	11.9 ms	764 ms
100 nF	24.9 ms	1.59 sec
220 nF	54.3 ms	3.0 sec[1, 2]

[1] The discharge time is fixed; capacitors larger than 220 nF may not be fully discharged during the discharge cycle. Therefore, the delay time is not proportional to the capacitance for capacitors larger than this value.
[2] Limited by internal timeout of 3 sec to prevent faulty capacitors on the RND pin from impeding a startup.

VOLTAGE TRANSIENTS

System backplanes are subject to transients. Transients commonly occur following a fast shutdown on a system running high currents. The source inductance results in a fast dv/dt on the input and the load inductance may result in a negative voltage transient at VOUT. It is critical to use appropriately rated TVS diodes on the input and Schottky diodes on the output. The ADM1272 can tolerate 120 V at the input pins and −5 V at the VOUT pin.

SURGE AND TRANSIENT RECOVERY

Surges, line steps, and backplane disturbances are sometimes unavoidable in a system chassis backplane. Usually such events result in a fast dv/dt on the input supply, which in turn causes a sudden inrush current demand on the positive edge. This sudden inrush current is almost identical to a current spike seen during an output fault condition and is therefore always difficult to differentiate and manage without resulting in a system reset.

The ADM1272 uses a number of features designed to address this issue. Many existing solutions rely on masking the severe overcurrent feature and allowing the inrush current to pass. The ADM1272 features an MCB pin for just that function. However, using the MCB pin is not the preferred course of action because it often results in very high currents flowing uninterrupted in the system, which can lead to other issues.

The primary features to address such power line disturbances are as follows:

- Fast recovery allows the inrush current to trigger the severe overcurrent and shuts down the FET quickly to limit the high peak currents from flowing in the system. However, after shutdown, recover the current control quickly so that the output load capacitors do not discharge with the load demand. This recovery is achieved via a gate drive boost circuit designed to deliver extra charge into GATE until the FET is reenabled.
- Isolated DVDT capacitor that controls the gate ramp voltage is disconnected during this recovery, allowing the FET to recover faster.
- No current foldback. If the load is demanding full current during this event, the current limit cannot be reduced without impeding recovery. Instead, the FET on time is managed to ensure SOA protection.
- EFAULT function. This feature replaces the typical timer function. It can be optimized to allow the FET to remain on for longer with lower V_{DS} faults, which is typical in these scenarios.

The combination of these features allows the ADM1272 to maintain the output voltage and prevent system resets during these transients events, while still protecting the MOSFETs.

POWER GOOD

The power-good (PWRGD) output indicates whether the output voltage is above a user defined threshold and can, therefore, be considered good. A resistor divider on the PWGIN pin sets an accurate power-good threshold on the output voltage.

The PWRGD pin is an open-drain output that pulls low when the voltage at the PWGIN pin is lower than 1.0 V (power bad). When the voltage at the PWGIN pin is above this threshold plus a fixed hysteresis of 60 mV, the output power is considered to be good.

However, PWRGD asserts only when the following conditions are met:

- PWGIN is above the rising threshold voltage.
- Hot swap is enabled, that is, the ENABLE pin is high and the UVx and OV pins are within range.
- There is no active fault condition, that is, the $\overline{\text{FAULT}}$ pin is cleared following any fault condition.
- The MOSFET is fully enhanced (V_{GS} > 10 V).

After these conditions are met, the open-drain pull-down current is disabled, allowing PWRGD to be pulled high. PWRGD is guaranteed to be in a valid state for VCC ≥ 1 V. An external pull-up circuit is required.