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ANALOG DEVICES

Hot-Swap Controller and Digital Power Monitor with PMBus Interface

Data Sheet **ADM1275**

FEATURES

- **Controls supply voltages from 2 V to 20 V**
- **370 ns response time to short circuit**
- **Resistor-programmable 5 mV to 25 mV current limit**
- **±1% accurate, 12-bit ADC for current, V_{IN}/V_{OUT} readback**
- **Charge-pumped gate drive for multiple external N-channel FETs**
- **High gate drive voltage to ensure lowest R_{DSON}**
- **Foldback for tighter FET SOA protection**
- **Automatic retry or latch-off on current fault**
- **Programmable current limit timer for SOA**
- **Programmable, multifunction GPOs**
- **Power-good status output**
- **Analog UV and OV protection**
- **ENABLE pin (ADM1275-3 only)**
- **Peak detect registers for current and voltage**
- **PMBus fast mode compliant interface**
- **16-lead QSOP and 20-lead QSOP and LFCSP**

APPLICATIONS

- **Power monitoring and control/power budgeting**
- **Central office equipment**
- **Telecommunication and data communication equipment**
- **PCs/servers**

APPLICATIONS DIAGRAM

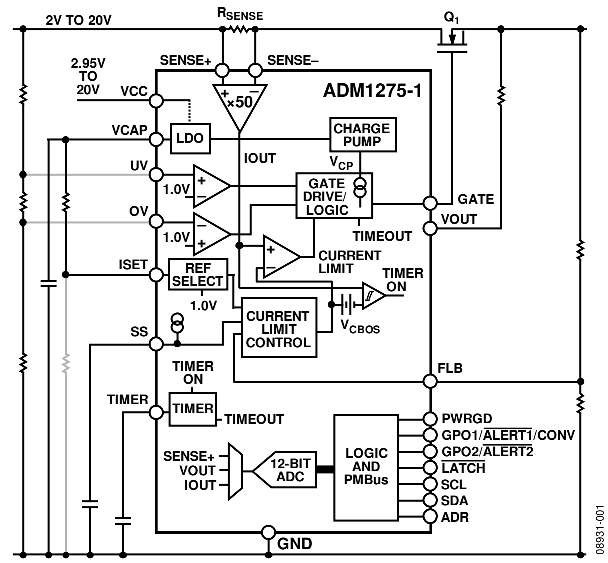

Figure 1.

GENERAL DESCRIPTION

The ADM1275 is a hot-swap controller that allows a circuit board to be removed from or inserted into a live backplane. It also features current and voltage readback via an integrated 12-bit analog-to-digital converter (ADC), accessed using a PMBus™ interface.

The load current is measured using an internal current sense amplifier that measures the voltage across a sense resistor in the power path via the SENSE+ and SENSE– pins. A default limit of 20 mV is set, but this limit can be adjusted, if required, using a resistor divider network from the internal reference voltage to the ISET pin.

The ADM1275 limits the current through the sense resistor by controlling the gate voltage of an external N-channel FET in the power path, via the GATE pin. The sense voltage—and, therefore, the load current—is maintained below the preset maximum. The ADM1275 protects the external FET by limiting the time that the FET remains on while the current is at its maximum value. This current limit time is set by the choice of capacitor connected to the TIMER pin. In addition, a foldback resistor network can be used to actively lower the current limit as the voltage across the FET is increased. This helps to maintain constant power in the FET and allows the safe operating area (SOA) to be adhered to in an effective manner.

In case of a short-circuit event, a fast internal overcurrent detector responds within 370 ns and signals the gate to shut down. A 1500 mA pull-down device ensures a fast FET response. The ADM1275 features overvoltage and undervoltage protection, programmed using external resistor dividers on the UV and OV pins. A PWRGD signal can be used to detect when the output supply is valid, using the FLB pin to monitor the output. GPO pins can be configured as various output signals that can be asserted when a programmed current or voltage level is reached.

The 12-bit ADC can measure the current in the sense resistor, as well as the supply voltage on the SENSE+ pin or the output voltage. A PMBus interface allows a controller to read current and voltage data from the ADC. Measurements can be initiated by a PMBus command. Alternatively, the ADC can run continuously, and the user can read the latest conversion data whenever required. Up to four unique PMBus addresses can be selected, depending on the way that the ADR pin is connected.

The ADM1275-1 and ADM1275-3 are available in a 20-lead QSOP and 20-lead LFCSP and have a LATCH pin that can be configured for automatic retry or latch-off when an overcurrent fault occurs. The ADM1275-2 is available in a 16-lead QSOP with latch-off mode only.

Rev. D **Document Feedback**

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADM1275 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1135: ADC Sampling Information ADM1275/ADM1276/ADM1075

Data Sheet

- ADM1275: Hot Swap Controller and Digital Power Monitor with PMBus Interface Data Sheet

User Guides

- UG-241: Using the Simulation Model for ADI Hotswap Controllers
- UG-263: Evaluating the ADM1275 and ADM1276
- UG-353: Hot Swap and Power Monitor Software
- UG-404: USB-SDP-CABLEZ Serial Interface Board

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADMxxxx Common Run-Time
- Hot Swap Controller Simulation Model Rev. 6
- Hot-Swap & Power Monitoring Evaluation Software

DESIGN RESOURCES

- ADM1275 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADM1275 EngineerZone Discussions.

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SPECIFICATIONS

V_{CC} = 2.95 V to 20 V, $V_{CC} \geq V_{SENSE+}$, V_{SENSE+} = 2 V to 20 V, $V_{SENSE} = (V_{SENSE+} - V_{SENSE-})$ = 0 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
Operating Voltage Range, V_{CC}	2.95		20	V	
Undervoltage Lockout	2.4		2.7	V	V_{CC} rising
Undervoltage Hysteresis		90	120	mV	
Quiescent Current, I_{CC}			5	mA	GATE on and power monitor running
UV PIN					
Input Current, I_{UV}			100	nA	UV ≤ 3.6 V
UV Threshold, UV_{TH}	0.97	1.0	1.03	V	UV falling
UV Threshold Hysteresis, UV_{HYST}	40	50	60	mV	
UV Glitch Filter, UV_{GF}	2		7	µs	50 mV overdrive
UV Propagation Delay, UV_{PD}		5	8	µs	UV low to GATE pull-down active
OV PIN					ADM1275-1 and ADM1275-3
Input Current, I_{OV}			100	nA	OV ≤ 3.6 V
OV Threshold, OV_{TH}	0.97	1.0	1.03	V	OV rising
OV Threshold Hysteresis, OV_{HYST}	50	60	70	mV	
OV Glitch Filter, OV_{GF}	0.5		1.5	µs	50 mV overdrive
OV Propagation Delay, OV_{PD}		1.0	2	µs	OV high to GATE pull-down active
SENSE+ AND SENSE− PINS					
Input Current, I_{SENSEx}			150	µA	Per individual pin; SENSE+, SENSE− = 20 V
Input Imbalance, $I_{\Delta SENSE}$			5	µA	$I_{\Delta SENSE} = (I_{SENSE+}) - (I_{SENSE-})$
VCAP PIN					
Internally Regulated Voltage, V_{VCAP}	2.66	2.7	2.74	V	0 µA ≤ I_{VCAP} ≤ 100 µA; C_{VCAP} = 1 µF
ISET PIN					
Reference Select Threshold, $V_{ISETRSTH}$	1.35	1.5	1.65	V	If $V_{ISET} > V_{ISETRSTH}$, an internal 1 V reference (V_{CLREF}) is used
Internal Reference, V_{CLREF}		1		V	Accuracies included in total sense voltage accuracies
Gain of Current Sense Amplifier, AV_{CSAMP}		50		V/V	Accuracies included in total sense voltage accuracies
Input Current, I_{ISET}			100	nA	$V_{ISET} \leq V_{VCAP}$
GATE PIN					Maximum voltage on the gate is always clamped to ≤31 V
Gate Drive Voltage, ΔV_{GATE}					$\Delta V_{GATE} = V_{GATE} - V_{SENSE+}$
	10	12	14	V	15 V ≥ V_{CC} ≥ 8 V; I_{GATE} ≤ 5 µA
	4.5		13	V	20 V ≥ V_{CC} ≥ 15 V; I_{GATE} ≤ 5 µA
	8		10	V	$V_{SENSE+} = V_{CC}$ = 5 V; I_{GATE} ≤ 5 µA
	4.5		6	V	$V_{SENSE+} = V_{CC}$ = 2.95 V; I_{GATE} ≤ 1 µA
Gate Pull-Up Current, I_{GATEUP}	−20		−30	µA	V_{GATE} = 0 V
Gate Pull-Down Current, I_{GATEDN_REG}	45	60	75	µA	V_{GATE} ≥ 2 V; V_{ISET} = 1.0 V; (SENSE+) − (SENSE−) = 30 mV
Gate Pull-Down Current, I_{GATEDN_SLOW}	5	10	15	mA	V_{GATE} ≥ 2 V
Gate Pull-Down Current, I_{GATEDN_FAST}	750	1500	2000	mA	V_{GATE} ≥ 12 V; V_{CC} ≥ 12 V
Gate Holdoff Resistance		20		Ω	V_{CC} = 0 V
HOT-SWAP SENSE VOLTAGE					
Hot-Swap Sense Voltage Current Limit, $V_{SENSECL}$	19.6	20	20.4	mV	V_{ISET} > 1.65 V; V_{FLB} > 1.12 V; V_{GATE} = (SENSE+) + 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V
Foldback Inactive					V_{GATE} = (SENSE+) + 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V
	24.6	25	25.4	mV	V_{ISET} = 1.25 V; V_{FLB} > 1.395 V
	19.6	20	20.4	mV	V_{ISET} = 1.0 V; V_{FLB} > 1.12 V
	9.6	10	10.4	mV	V_{ISET} = 0.5 V; V_{FLB} > 0.57 V
	4.6	5	5.4	mV	V_{ISET} = 0.25 V; V_{FLB} > 0.295 V
Foldback Active	3.5	4	4.5	mV	V_{FLB} = 0 V; V_{GATE} = (SENSE+) + 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 1 V
	9.6	10	10.4	mV	V_{ISET} > 1.0 V; V_{FLB} = 0.5 V; V_{GATE} = (SENSE+) + 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 1 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Circuit Breaker Offset, V_{CBOS}	0.6	0.88	1.12	mV	Circuit breaker trip voltage, $V_{CB} = V_{SENSECL} - V_{CBOS}$
SEVERE OVERCURRENT					
Voltage Threshold, $V_{SENSEOC}$	40		50	mV	$V_{ISET} = 1.0$ V; $V_{FLB} > 1.1$ V; $V_{SS} \geq 2$ V
	9.5		13.0	mV	$V_{ISET} = 0.25$ V; $V_{FLB} > 1.1$ V; $V_{SS} \geq 2$ V
Short Glitch Filter Duration	90		200	ns	$V_{ISET} > 1.65$ V; V_{SENSE} driven from 18 mV to 52 mV; selectable via PMBus
Long Glitch Filter Duration (Default)	530		900	ns	V_{SENSE} driven from 18 mV to 52 mV
Response Time					
With Short Glitch Filter	180		370	ns	2 mV overdrive maximum severe overcurrent threshold
With Long Glitch Filter	645		1020	ns	
SOFT START (SS PIN)					
SS Pull-Up Current, I_{SS}	−12	−10	−8	μA	$V_{SS} = 0$ V
Default $V_{SENSECL}$ Limit	0.5	1.25	1.8	mV	When V_{SENSE} reaches this level, I_{SS} is enabled, ramping $V_{SENSECL}$; $V_{SS} = 0$ V
SS Pull-Down Current		100		μA	$V_{SS} = 1$ V
TIMER PIN					
Timer Pull-Up Current (POR), $I_{TIMERUPPOR}$	−2	−3	−4	μA	Initial power-on reset; $V_{TIMER} = 0.5$ V
Timer Pull-Up Current (OC Fault), $I_{TIMERUPFLT}$	−57	−60	−63	μA	Overcurrent fault; $0.2\text{ V} \leq V_{TIMER} \leq 1$ V
Timer Pull-Down Current (Retry), $I_{TIMERDNRT}$	1.7	2	2.3	μA	After fault when GATE is off; $V_{TIMER} = 0.5$ V
Timer Retry/OC Fault Current Ratio		3.33	3.8	%	Defines the limits of the autoretry duty cycle
Timer Pull-Down Current (Hold), $I_{TIMERDNHOLD}$		100		μA	Holds TIMER at 0 V when inactive; $V_{TIMER} = 0.5$ V
Timer High Threshold, V_{TIMERH}	0.98	1.0	1.02	V	
Timer Low Threshold, V_{TIMERL}	0.18	0.2	0.22	V	
FOLDBACK (FLB PIN)					
FLB and PWRGD Threshold, V_{FLBTH}	1.08	1.1	1.12	V	FLB rising; $V_{ISET} = 1.0$ V
Input Current, I_{FLB}			100	nA	$V_{FLB} \leq 1.0$ V; $V_{ISET} = 1.25$ V
			100	nA	$V_{VCAP} \leq V_{FLB} \leq 20$ V
Hysteresis Current	1.7		2.3	μA	
Internal Hysteresis Voltage	1.9		3.1	mV	Voltage drop across the internal 1.3 kΩ resistor
Power-Good Glitch Filter, $PWRGD_{GF}$	0.3	0.7	1	μs	50 mV overdrive
Minimum Foldback Clamp		200		mV	Accuracies included in total sense voltage accuracies
VOUT PIN					ADM1275-1 and ADM1275-3
Input Current			20	μA	VOUT = 20 V
$\overline{\text{LATCH}}$ PIN					ADM1275-1 and ADM1275-3
Output Low Voltage, V_{OL_LATCH}			0.4	V	$I_{LATCH} = 1$ mA
			1.5	V	$I_{LATCH} = 5$ mA
Leakage Current			100	nA	$V_{LATCH} \leq 2$ V; $\overline{\text{LATCH}}$ output high-Z
			1	μA	$V_{LATCH} = 20$ V; $\overline{\text{LATCH}}$ output high-Z
GPO1/$\overline{\text{ALERT1}}$/CONV PIN (ADM1275-1 and ADM1275-2), ENABLE PIN (ADM1275-3)					No internal pull-up present on these pins
Output Low Voltage, V_{OL_GPO1}			0.4	V	$I_{GPO1} = 1$ mA
			1.5	V	$I_{GPO1} = 5$ mA
Leakage Current			100	nA	$V_{GPO1} \leq 2$ V; GPO output high-Z
			1	μA	$V_{GPO1} = 20$ V; GPO output high-Z
Input High Voltage, V_{IH}	1.1			V	
Input Low Voltage, V_{IL}			0.8	V	
GPO2/$\overline{\text{ALERT2}}$ PIN					ADM1275-1 and ADM1275-3
Output Low Voltage, V_{OL_GPO2}			0.4	V	$I_{GPO2} = 1$ mA
			1.5	V	$I_{GPO2} = 5$ mA
Leakage Current			100	nA	$V_{GPO2} \leq 2$ V; GPO output high-Z
			1	μA	$V_{GPO2} = 20$ V; GPO output high-Z

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PWRGD PIN					
Output Low Voltage, V_{OL_PWRGD}			0.4	V	I_{PWRGD} = 1 mA
			1.5	V	I_{PWRGD} = 5 mA
VCC That Guarantees Valid Output	1			V	I_{SINK} = 100 µA; V_{OL_PWRGD} = 0.4 V
Leakage Current			100	nA	V_{PWRGD} ≤ 2 V; PWRGD output high-Z
			1	µA	V_{PWRGD} = 20 V; PWRGD output high-Z
CURRENT AND VOLTAGE MONITORING					
Current Sense Absolute Error					25 mV input range; 128 sample averaging (unless otherwise noted)
		±0.2	±0.7	%	V_{SENSE} = 20 mV; V_{SENSE+} = 12 V; T_A = 0°C to 65°C
		±0.08		%	V_{SENSE} = 20 mV; V_{SENSE+} = 12 V; T_A = 25°C
			±1.0	%	V_{SENSE} = 20 mV
		±0.08		%	V_{SENSE} = 20 mV; T_A = 25°C
		±0.2		%	V_{SENSE} = 20 mV; T_A = 0°C to 65°C
			±1.0	%	V_{SENSE} = 20 mV; 16 sample averaging
		±0.08		%	V_{SENSE} = 20 mV; 16 sample averaging; T_A = 25°C
		±0.2		%	V_{SENSE} = 20 mV; 16 sample averaging; T_A = 0°C to 65°C
			±2.8	%	V_{SENSE} = 20 mV; 1 sample averaging
		±0.09		%	V_{SENSE} = 20 mV; 1 sample averaging; T_A = 25°C
		±0.2		%	V_{SENSE} = 20 mV; 1 sample averaging; T_A = 0°C to 65°C
			±0.7	%	V_{SENSE} = 25 mV; V_{SENSE+} = 12 V
		±0.04		%	V_{SENSE} = 25 mV; V_{SENSE+} = 12 V; T_A = 25°C
		±0.15		%	V_{SENSE} = 25 mV; V_{SENSE+} = 12 V; T_A = 0°C to 65°C
			±0.75	%	V_{SENSE} = 20 mV; V_{SENSE+} = 12 V
			±0.8	%	V_{SENSE} = 15 mV; V_{SENSE+} = 12 V
			±1.1	%	V_{SENSE} = 10 mV; V_{SENSE+} = 12 V
			±2.0	%	V_{SENSE} = 5 mV; V_{SENSE+} = 12 V
			±4.3	%	V_{SENSE} = 2.5 mV; V_{SENSE+} = 12 V
SENSE+/VOUT Absolute Error			±1.0	%	Low input range; input voltage ≥ 3 V
			±1.0	%	High input range; input voltage ≥ 10 V
ADC Conversion Time		250	305	µs	1 sample of voltage and current; from command received to valid data in register
		4000	4880	µs	16 samples of voltage and current averaged; from command received to valid data in register
ADR PIN					
Address Set to 00	0		0.8	V	Connect to GND
Input Current for Address 00	−40	−22		µA	V_{ADR} = 0 V to 0.8 V
Address Set to 01	135	150	165	kΩ	Resistor to GND
Address Set to 10	−1		+1	µA	No connect state; maximum leakage current allowed
Address Set to 11	2			V	Connect to VCAP
Input Current for Address 11		3	10	µA	V_{ADR} = 2.0 V to VCAP; must not exceed the maximum allowable current draw from VCAP
SERIAL BUS DIGITAL INPUTS (SDA, SCL)					
Input High Voltage, V_{IH}	1.1			V	
Input Low Voltage, V_{IL}			0.8	V	
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 4 mA
Input Leakage, $I_{LEAK\text{-}PIN}$	−10		+10	µA	
	−5		+5	µA	Device is not powered
Nominal Bus Voltage, V_{DD}	2.7		5.5	V	3 V to 5 V ± 10%
Capacitance for SDA, SCL Pin, C_{PIN}		5		pF	
Input Glitch Filter, t_{SP}	0		50	ns	

SERIAL BUS TIMING CHARACTERISTICS

t_R = ($V_{IL(MAX)}$ − 0.15) to (V_{IH3V3} + 0.15) and t_F = 0.9V_{DD} to ($V_{IL(MAX)}$ − 0.15); where V_{IH3V3} = 2.1 V and V_{DD} = 3.3 V.

Table 2.

Parameter	Description	Min	Typ	Max	Unit	Test Conditions/Comments
f_{SCLK}	Clock frequency			400	kHz	
t_{BUF}	Bus free time	1.3			µs	Following the stop condition of a read transaction
		4.7			µs	Following the stop condition of a write transaction
$t_{HD;STA}$	Start hold time	0.6			µs	
$t_{SU;STA}$	Start setup time	0.6			µs	
$t_{SU;STO}$	Stop setup time	0.6			µs	
$t_{HD;DAT}$	SDA hold time	300		900	ns	
$t_{SU;DAT}$	SDA setup time	100			ns	
t_{LOW}	SCL low time	1.3			µs	
t_{HIGH}	SCL high time	0.6			µs	
t_R	SCL, SDA rise time	20		300	ns	
t_F	SCL, SDA fall time	20		300	ns	

Timing Diagram

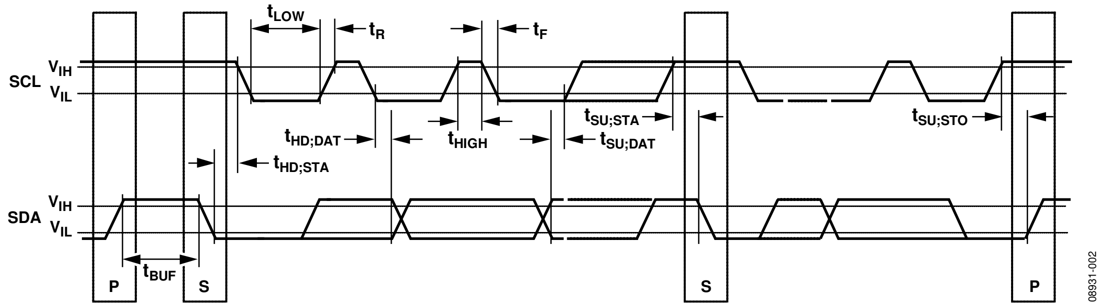

Figure 2. Serial Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VCC Pin	−0.3 V to +25 V
UV Pin	−0.3 V to +4 V
OV Pin	−0.3 V to +4 V
SS Pin	−0.3 V to VCAP + 0.3 V
TIMER Pin	−0.3 V to VCAP + 0.3 V
VCAP Pin	−0.3 V to +4 V
ISET Pin	−0.3 V to VCAP + 0.3 V
$\overline{\text{LATCH}}$ Pin	−0.3 V to +25 V
SCL Pin	−0.3 V to +6.5 V
SDA Pin	−0.3 V to +6.5 V
ADR Pin	−0.3 V to VCAP + 0.3 V
GPO1/$\overline{\text{ALERT1}}$/CONV Pin, ENABLE Pin	−0.3 V to +25 V
GPO2/$\overline{\text{ALERT2}}$ Pin	−0.3 V to +25 V
PWRGD Pin	−0.3 V to +25 V
FLB Pin	−0.3 V to +25 V
VOUT Pin	−0.3 V to +25 V
GATE Pin (Internal Supply Only)[1]	−0.3 V to +36 V
SENSE+ Pin	−0.3 V to +25 V
SENSE− Pin	−0.3 V to +25 V
V_{SENSE} (V_{SENSE+} − V_{SENSE-})	±0.3 V
Continuous Current into Any Pin	±10 mA
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature, Soldering (10 sec)	300°C
Junction Temperature	150°C

[1] The GATE pin has internal clamping circuits to prevent the GATE pin voltage from exceeding the maximum ratings of a MOSFET with V_{GSMAX} = 20 V and internal process limits. Applying a voltage source to this pin externally may cause irreversible damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
16-lead QSOP (RQ-16)	150	°C/W
20-lead QSOP (RQ-20)	126	°C/W
20-lead LFCSP (CP-20-9)	30.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

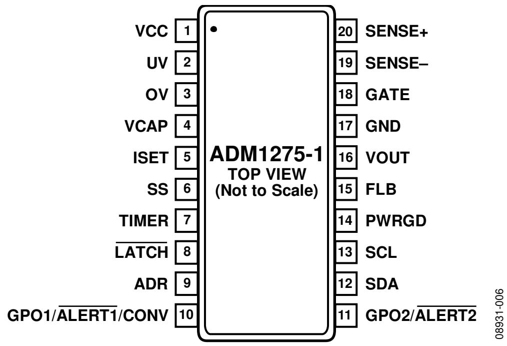

Figure 3. ADM1275-1 Pin Configuration, QSOP

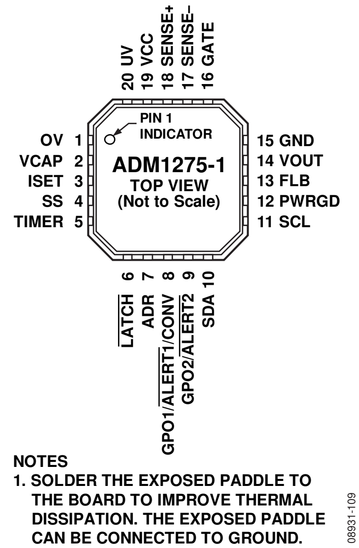

Figure 4. ADM1275-1 Pin Configuration, LFCSP

Table 5. ADM1275-1 Pin Function Descriptions

Pin No.			
QSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	VCC	Positive Supply Input Pin. An undervoltage lockout (UVLO) circuit resets the device when a low supply voltage is detected. GATE is held low when the supply is below UVLO. During normal operation, this pin should remain greater than or equal to SENSE+ to ensure that specifications are adhered to. No sequencing is required.
2	20	UV	Undervoltage Input Pin. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect whether the supply is under the UV limit.
3	1	OV	Overvoltage Input Pin. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect whether the supply is above the OV limit.
4	2	VCAP	Internal Regulated Supply. A capacitor with a value of 1 µF or greater should be placed on this pin to maintain good accuracy. This pin can be used as a reference to program the ISET pin voltage.
5	3	ISET	This pin allows the current limit threshold to be programmed. The default limit is set when this pin is connected directly to VCAP. To achieve a user-defined sense voltage, the current limit can be adjusted using a resistor divider from VCAP. An external reference can also be used.
6	4	SS	Soft Start Pin. A capacitor is used on this pin to set the soft start ramp profile. The voltage on the SS pin controls the current sense voltage limit, which controls the inrush current profile.
7	5	TIMER	Timer Pin. An external capacitor, C_{TIMER}, sets an initial timing cycle delay and a fault delay. The GATE pin is pulled low when the voltage on the TIMER pin exceeds the upper threshold.
8	6	$\overline{\text{LATCH}}$	Signals that the device is latching off after an overcurrent fault. The device can be configured for automatic retry after latch-off by connecting this pin directly back to the UV pin.
9	7	ADR	PMBus Address Pin. This pin can be tied to GND, tied to VCAP, left floating, or tied low through a resistor to set four different PMBus addresses (see the Device Addressing section).
10	8	GPO1/$\overline{\text{ALERT1}}$/CONV	General-Purpose Digital Output (GPO1). Alert ($\overline{\text{ALERT1}}$). This pin can be configured to generate an alert signal when one or more fault or warning conditions are detected. Conversion (CONV). This pin can be used as an input signal to control when a power monitor ADC sampling cycle begins. At power-up, this pin defaults to a high impedance state. There is no internal pull-up on this pin.
11	9	GPO2/$\overline{\text{ALERT2}}$	General-Purpose Digital Output (GPO2). Alert ($\overline{\text{ALERT2}}$). This pin can be configured to generate an alert signal when one or more fault or warning conditions are detected. At power-up, this pin indicates the FET health mode by default. There is no internal pull-up on this pin.

Pin No.		Mnemonic	Description
QSOP	LFCSP		
12	10	SDA	Serial Data Input/Output Pin. Open-drain input/output. Requires an external resistive pull-up.
13	11	SCL	Serial Clock Pin. Open-drain input. Requires an external resistive pull-up.
14	12	PWRGD	Power-Good Signal. Used to indicate that the supply is within tolerance. This signal is based on the voltage present on the FLB pin.
15	13	FLB	Foldback Pin. A foldback resistor divider is placed from the source of the FET to this pin. Foldback is used to reduce the current limit when the source voltage drops. The foldback feature ensures that the power through the FET is not increased beyond the SOA limits.
16	14	VOUT	This pin is used to read back the output voltage using the internal ADC. A 1 kΩ resistor should be inserted in series between the source of a FET and the VOUT pin.
17	15	GND	Chip Ground Pin.
18	16	GATE	Gate Output Pin. This pin is the high-side gate drive of an external N-channel FET. This pin is driven by the FET drive controller, which uses a charge pump to provide a pull-up current to charge the FET gate pin. The FET drive controller regulates to a maximum load current by regulating the GATE pin. GATE is held low when the supply is below UVLO.
19	17	SENSE−	Negative Current Sense Input Pin. A sense resistor between the SENSE+ pin and the SENSE− pin sets the analog current limit. The hot-swap operation of the ADM1275 controls the external FET gate to maintain the sense voltage ($V_{SENSE+} - V_{SENSE-}$). This pin also connects to the FET drain pin.
20	18	SENSE+	Positive Current Sense Input Pin. This pin connects to the main supply input. A sense resistor between the SENSE+ pin and the SENSE− pin sets the analog current limit. The hot-swap operation of the ADM1275 controls the external FET gate to maintain the sense voltage ($V_{SENSE+} - V_{SENSE-}$). This pin is also used to measure the supply input voltage using the ADC.
N/A	EP	EPAD	Exposed Paddle on Underside of LFCSP. Solder the exposed paddle to the board to improve thermal dissipation. The exposed paddle can be connected to ground.

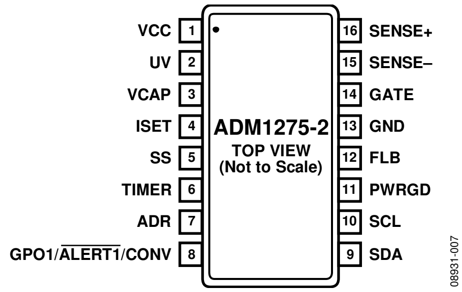

Figure 5. ADM1275-2 Pin Configuration

Table 6. ADM1275-2 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCC	Positive Supply Input Pin. An undervoltage lockout (UVLO) circuit resets the device when a low supply voltage is detected. GATE is held low when the supply is below UVLO. During normal operation, this pin should remain greater than or equal to SENSE+ to ensure that specifications are adhered to. No sequencing is required.
2	UV	Undervoltage Input Pin. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect whether the supply is under the UV limit.
3	VCAP	Internal Regulated Supply. A capacitor with a value of 1 µF or greater should be placed on this pin to maintain good accuracy. This pin can be used as a reference to program the ISET pin voltage.
4	ISET	This pin allows the current limit threshold to be programmed. The default limit is set when this pin is connected directly to VCAP. To achieve a user-defined sense voltage, the current limit can be adjusted using a resistor divider from VCAP. An external reference can also be used.
5	SS	Soft Start Pin. A capacitor is used on this pin to set the soft start ramp profile. The voltage on the SS pin controls the current sense voltage limit, which controls the inrush current profile.
6	TIMER	Timer Pin. An external capacitor, C_{TIMER}, sets an initial timing cycle delay and a fault delay. The GATE pin is pulled low when the voltage on the TIMER pin exceeds the upper threshold.
7	ADR	PMBus Address Pin. This pin can be tied to GND, tied to VCAP, left floating, or tied low through a resistor to set four different PMBus addresses (see the Device Addressing section).
8	GPO1/$\overline{\text{ALERT1}}$/CONV	General-Purpose Digital Output (GPO1). Alert ($\overline{\text{ALERT1}}$). This pin can be configured to generate an alert signal when one or more fault or warning conditions are detected. Conversion (CONV). This pin can be used as an input signal to control when a power monitor ADC sampling cycle begins. At power-up, this pin defaults to a high impedance state. There is no internal pull-up on this pin.
9	SDA	Serial Data Input/Output Pin. Open-drain input/output. Requires an external resistive pull-up.
10	SCL	Serial Clock Pin. Open-drain input. Requires an external resistive pull-up.
11	PWRGD	Power-Good Signal. Used to indicate that the supply is within tolerance. This signal is based on the voltage present on the FLB pin.
12	FLB	Foldback Pin. A foldback resistor divider is placed from the source of the FET to this pin. Foldback is used to reduce the current limit when the source voltage drops. The foldback feature ensures that the power through the FET is not increased beyond the SOA limits.
13	GND	Chip Ground Pin.
14	GATE	Gate Output Pin. This pin is the high-side gate drive of an external N-channel FET. This pin is driven by the FET drive controller, which uses a charge pump to provide a pull-up current to charge the FET gate pin. The FET drive controller regulates to a maximum load current by regulating the GATE pin. GATE is held low when the supply is below UVLO.
15	SENSE–	Negative Current Sense Input Pin. A sense resistor between the SENSE+ pin and the SENSE– pin sets the analog current limit. The hot-swap operation of the ADM1275 controls the external FET gate to maintain the sense voltage ($V_{SENSE+} - V_{SENSE-}$). This pin also connects to the FET drain pin.
16	SENSE+	Positive Current Sense Input Pin. This pin connects to the main supply input. A sense resistor between the SENSE+ pin and the SENSE– pin sets the analog current limit. The hot-swap operation of the ADM1275 controls the external FET gate to maintain the sense voltage ($V_{SENSE+} - V_{SENSE-}$). This pin is also used to measure the supply input voltage using the ADC.

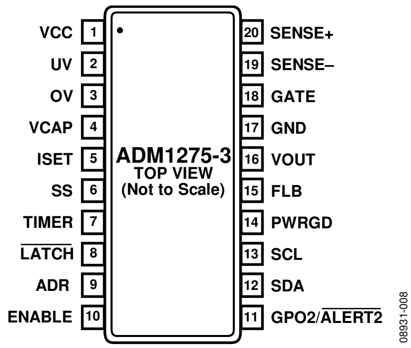

Figure 6. ADM1275-3 Pin Configuration, QSOP

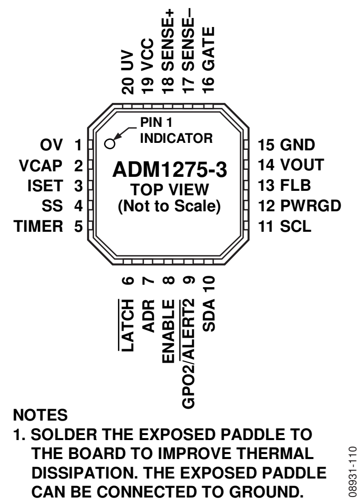

Figure 7. ADM1275-3 Pin Configuration, LFCSP

Table 7. ADM1275-3 Pin Function Descriptions

Pin No.			
QSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	VCC	Positive Supply Input Pin. An undervoltage lockout (UVLO) circuit resets the device when a low supply voltage is detected. GATE is held low when the supply is below UVLO. During normal operation, this pin should remain greater than or equal to SENSE+ to ensure that specifications are adhered to. No sequencing is required.
2	20	UV	Undervoltage Input Pin. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect whether the supply is under the UV limit.
3	1	OV	Overvoltage Input Pin. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect whether the supply is above the OV limit.
4	2	VCAP	Internal Regulated Supply. A capacitor with a value of 1 µF or greater should be placed on this pin to maintain good accuracy. This pin can be used as a reference to program the ISET pin voltage.
5	3	ISET	This pin allows the current limit threshold to be programmed. The default limit is set when this pin is connected directly to VCAP. To achieve a user-defined sense voltage, the current limit can be adjusted using a resistor divider from VCAP. An external reference can also be used.
6	4	SS	Soft Start Pin. A capacitor is used on this pin to set the soft start ramp profile. The voltage on the SS pin controls the current sense voltage limit, which controls the inrush current profile.
7	5	TIMER	Timer Pin. An external capacitor, C_{TIMER}, sets an initial timing cycle delay and a fault delay. The GATE pin is pulled low when the voltage on the TIMER pin exceeds the upper threshold.
8	6	$\overline{\text{LATCH}}$	Signals that the device is latching off after an overcurrent fault. The device can be configured for automatic retry after latch-off by connecting this pin directly back to the UV pin.
9	7	ADR	PMBus Address Pin. This pin can be tied to GND, tied to VCAP, left floating, or tied low through a resistor to set four different PMBus addresses (see the Device Addressing section).
10	8	ENABLE	Digital Logic Input. This input must be high to allow the ADM1275-3 hot-swap controller to begin a power-up sequence. If this pin is held low, the ADM1275-3 is prevented from powering up. There is no internal pull-up on this pin.
11	9	GPO2/$\overline{\text{ALERT2}}$	General-Purpose Digital Output (GPO2). Alert ($\overline{\text{ALERT2}}$). This pin can be configured to generate an alert signal when one or more fault or warning conditions are detected. At power-up, this pin indicates the FET health mode by default. There is no internal pull-up on this pin.
12	10	SDA	Serial Data Input/Output Pin. Open-drain input/output. Requires an external resistive pull-up.
13	11	SCL	Serial Clock Pin. Open-drain input. Requires an external resistive pull-up.
14	12	PWRGD	Power-Good Signal. Used to indicate that the supply is within tolerance. This signal is based on the voltage present on the FLB pin.
15	13	FLB	Foldback Pin. A foldback resistor divider is placed from the source of the FET to this pin. Foldback is used to reduce the current limit when the source voltage drops. The foldback feature ensures that the power through the FET is not increased beyond the SOA limits.

Pin No.			
QSOP	**LFCSP**	**Mnemonic**	**Description**
16	14	VOUT	This pin is used to read back the output voltage using the internal ADC. A 1 kΩ resistor should be inserted in series between the source of a FET and the VOUT pin.
17	15	GND	Chip Ground Pin.
18	16	GATE	Gate Output Pin. This pin is the high-side gate drive of an external N-channel FET. This pin is driven by the FET drive controller, which uses a charge pump to provide a pull-up current to charge the FET gate pin. The FET drive controller regulates to a maximum load current by regulating the GATE pin. GATE is held low when the supply is below UVLO.
19	17	SENSE−	Negative Current Sense Input Pin. A sense resistor between the SENSE+ pin and the SENSE− pin sets the analog current limit. The hot-swap operation of the ADM1275 controls the external FET gate to maintain the sense voltage ($V_{SENSE+} - V_{SENSE-}$). This pin also connects to the FET drain pin.
20	18	SENSE+	Positive Current Sense Input Pin. This pin connects to the main supply input. A sense resistor between the SENSE+ pin and the SENSE− pin sets the analog current limit. The hot-swap operation of the ADM1275 controls the external FET gate to maintain the sense voltage ($V_{SENSE+} - V_{SENSE-}$). This pin is also used to measure the supply input voltage using the ADC.
N/A	EP	EPAD	Exposed Paddle on Underside of LFCSP. Solder the exposed paddle to the board to improve thermal dissipation. The exposed paddle can be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

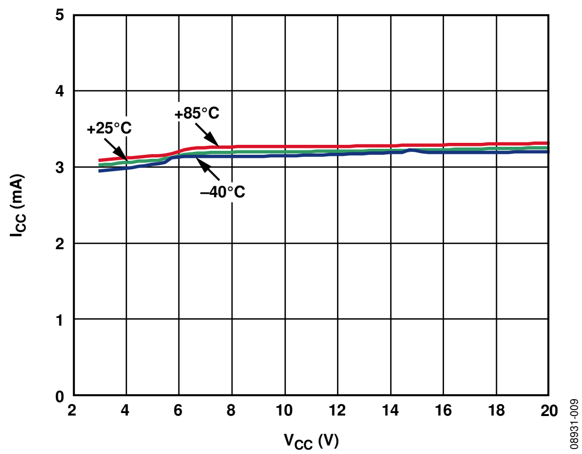

Figure 8. Supply Current (I_{CC}) vs. Supply Voltage (V_{CC})

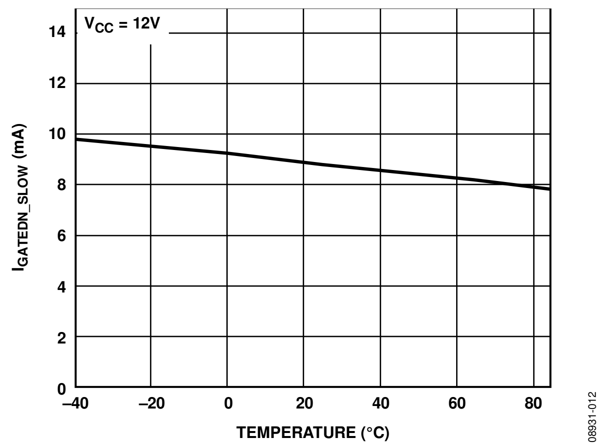

Figure 11. Gate Pull-Down Current (I_{GATEDN_SLOW}) vs. Temperature

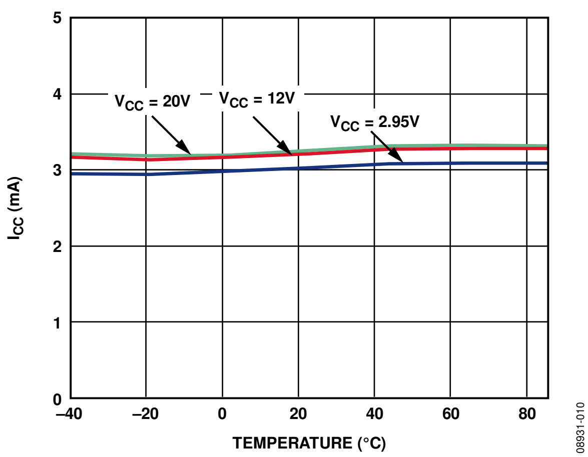

Figure 9. Supply Current (I_{CC}) vs. Temperature

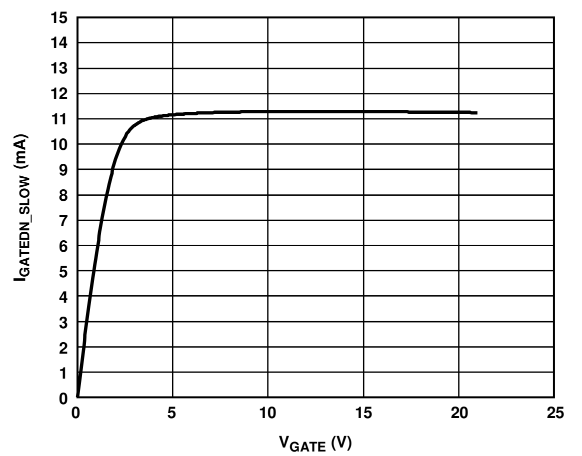

Figure 12. Gate Pull-Down Current (I_{GATEDN_SLOW}) vs. Gate Voltage (V_{GATE})

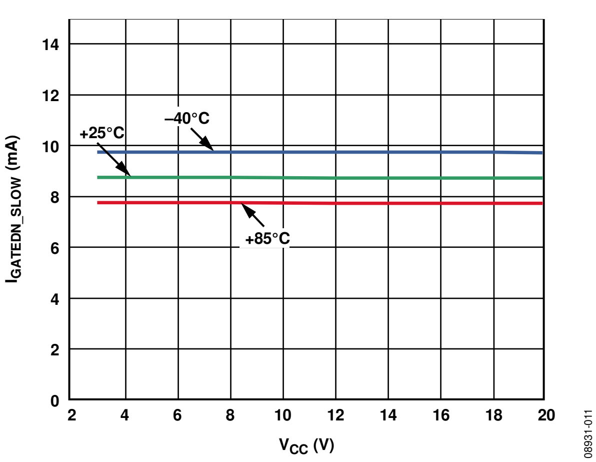

Figure 10. Gate Pull-Down Current (I_{GATEDN_SLOW}) vs. Supply Voltage (V_{CC})

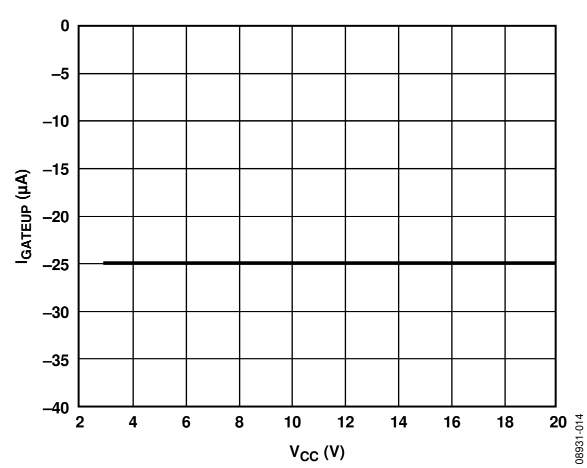

Figure 13. Gate Pull-Up Current (I_{GATEUP}) vs. Supply Voltage (V_{CC})

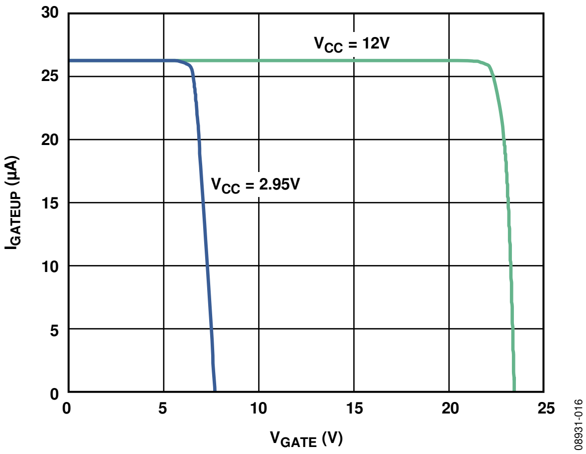

Figure 14. Gate Pull-Up Current (I_{GATEUP}) vs. Gate Voltage (V_{GATE})

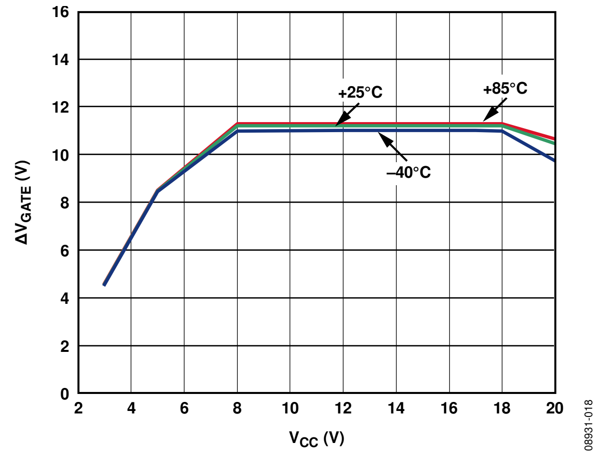

Figure 17. Gate Drive Voltage (ΔV_{GATE}) vs. Supply Voltage (V_{CC}), 5 µA Load

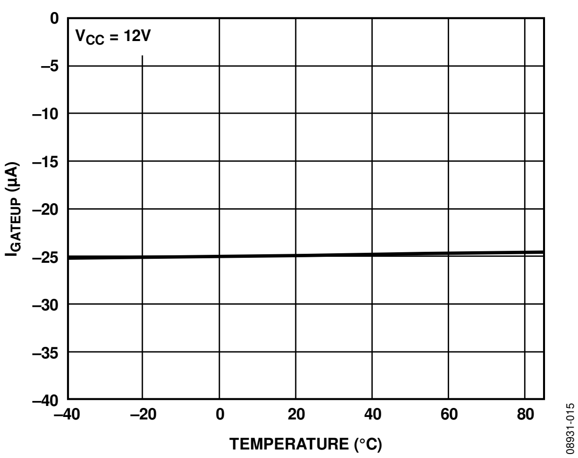

Figure 15. Gate Pull-Up Current (I_{GATEUP}) vs. Temperature

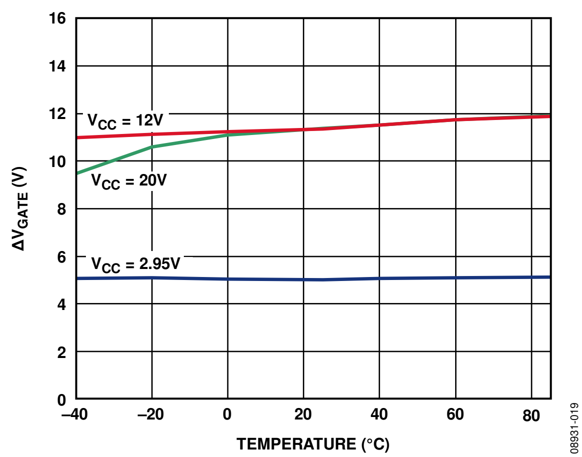

Figure 18. Gate Drive Voltage (ΔV_{GATE}) vs. Temperature, No Load

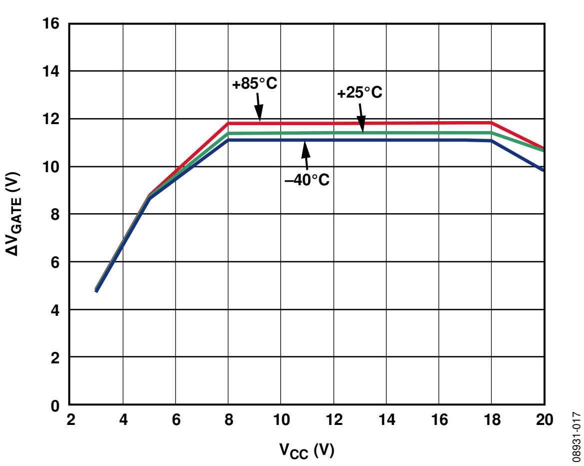

Figure 16. Gate Drive Voltage (ΔV_{GATE}) vs. Supply Voltage (V_{CC}), No Load

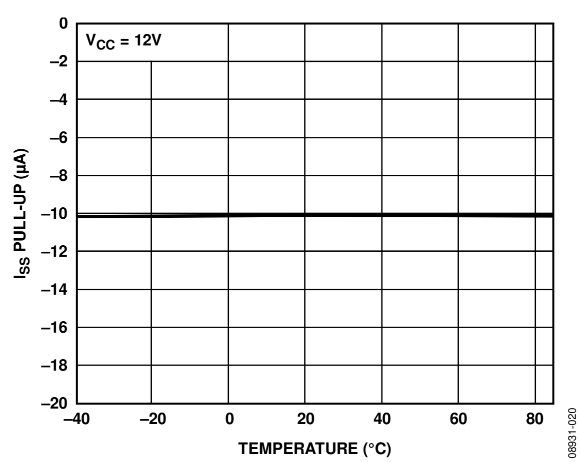

Figure 19. Soft Start Pull-Up Current (I_{SS}) vs. Temperature

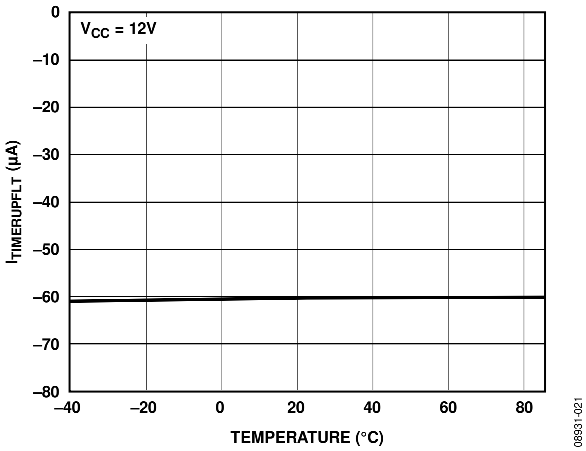

Figure 20. Timer Pull-Up Current, Overcurrent Fault ($I_{TIMERUPFLT}$) vs. Temperature

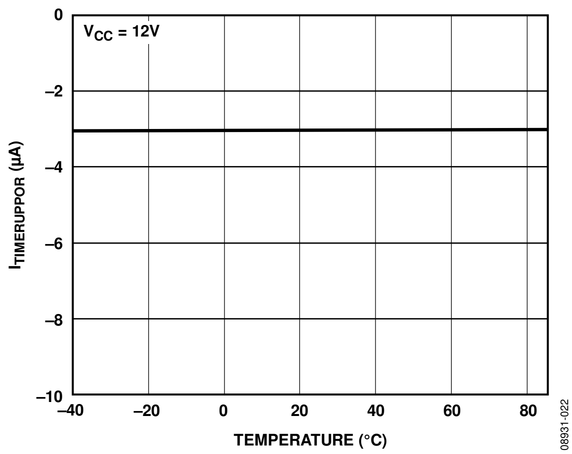

Figure 21. Timer Pull-Up Current, Power-On Reset ($I_{TIMERUPPOR}$) vs. Temperature

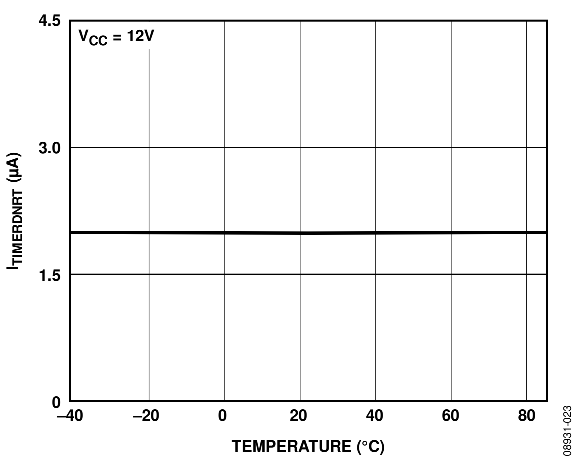

Figure 22. Timer Pull-Down Current, Retry ($I_{TIMERDNRT}$) vs. Temperature

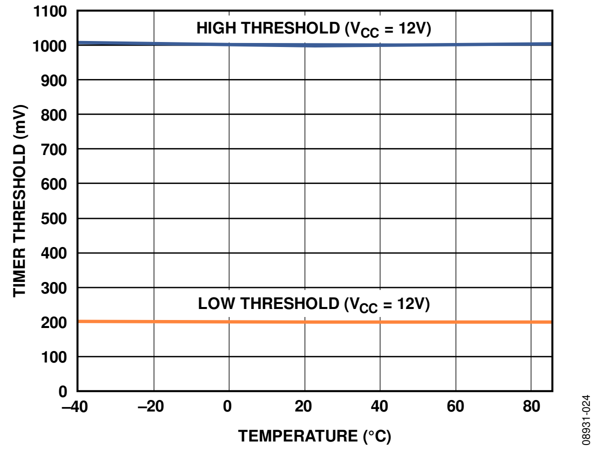

Figure 23. Timer Thresholds vs. Temperature

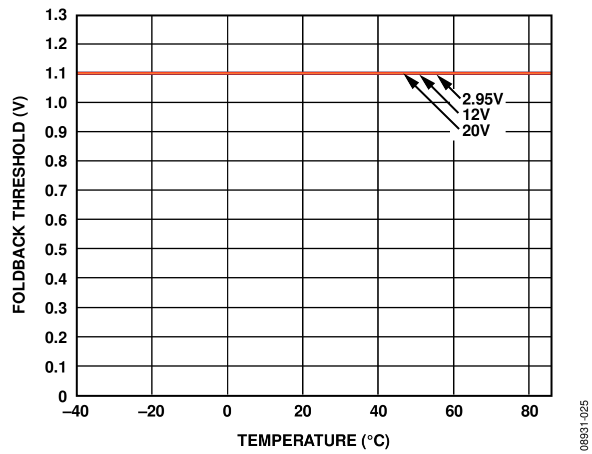

Figure 24. Foldback Threshold vs. Temperature

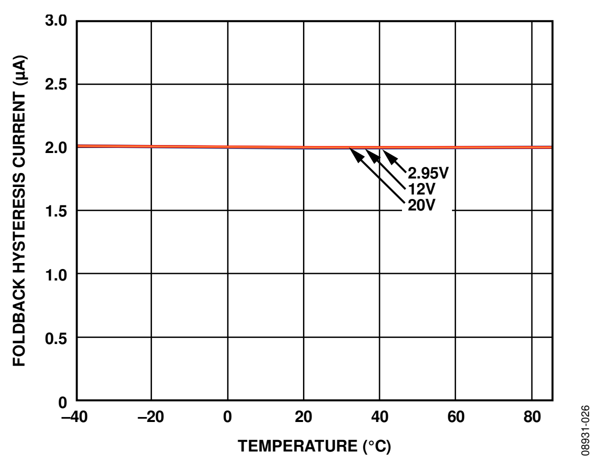

Figure 25. Foldback Hysteresis Current vs. Temperature

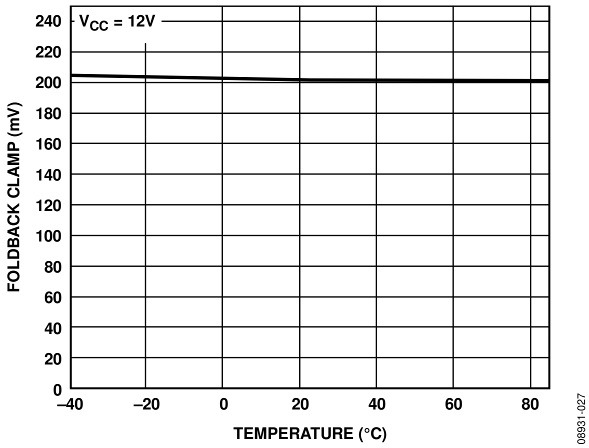

Figure 26. Foldback Clamp vs. Temperature

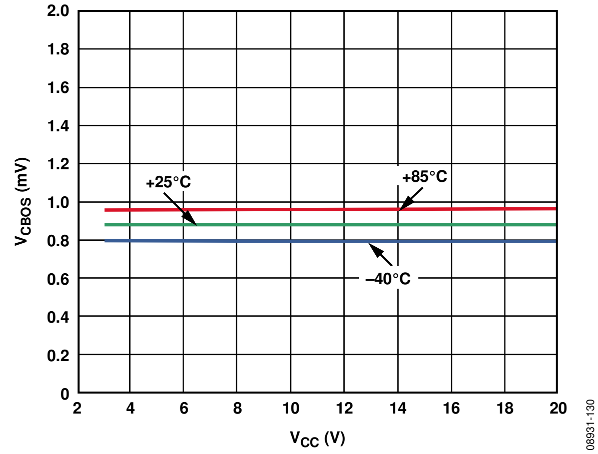

Figure 29. Circuit Breaker Offset (V_{CBOS}) vs. Supply Voltage (V_{CC})

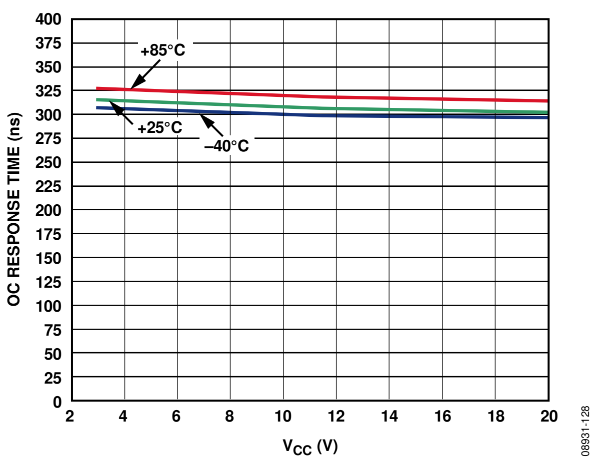

Figure 27. Severe Overcurrent Response Time vs. Supply Voltage (V_{CC}), V_{ISET} = 0.25 V

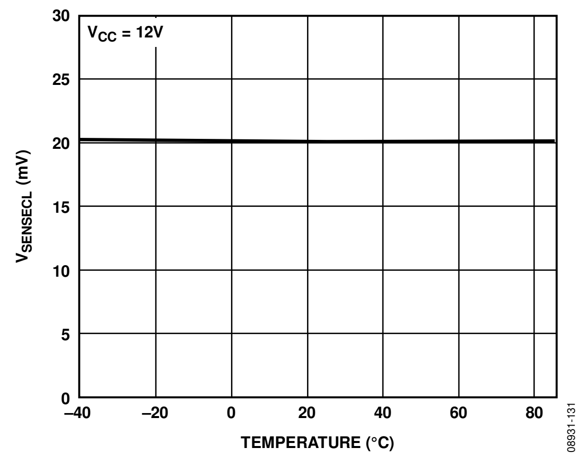

Figure 30. Hot-Swap Sense Voltage Current Limit ($V_{SENSECL}$) vs. Temperature

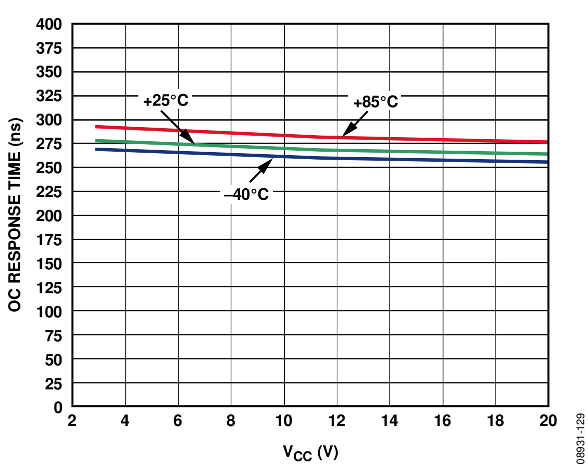

Figure 28. Severe Overcurrent Response Time vs. Supply Voltage (V_{CC}), V_{ISET} = 1 V

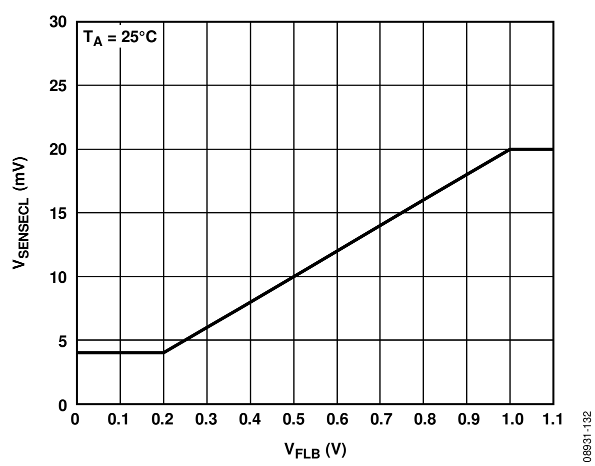

Figure 31. Hot-Swap Sense Voltage Current Limit ($V_{SENSECL}$) vs. Foldback Voltage (V_{FLB})

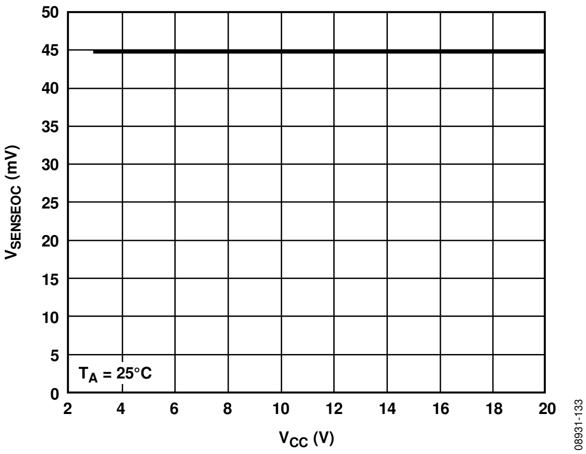

Figure 32. Severe Overcurrent Voltage Threshold ($V_{SENSEOC}$) vs. Supply Voltage (V_{CC}), V_{ISET} = V_{VCAP}

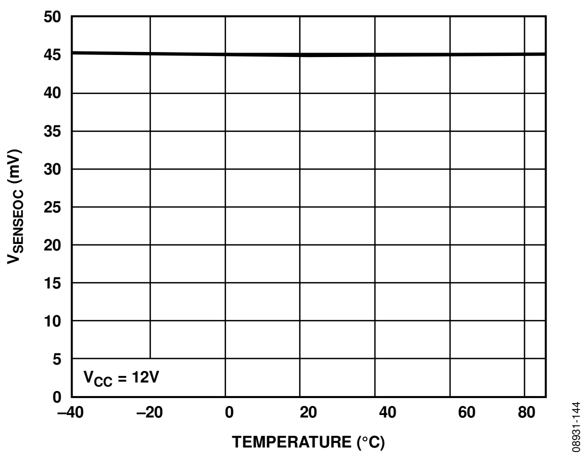

Figure 33. Severe Overcurrent Voltage Threshold ($V_{SENSEOC}$) vs. Temperature, V_{ISET} = V_{VCAP}

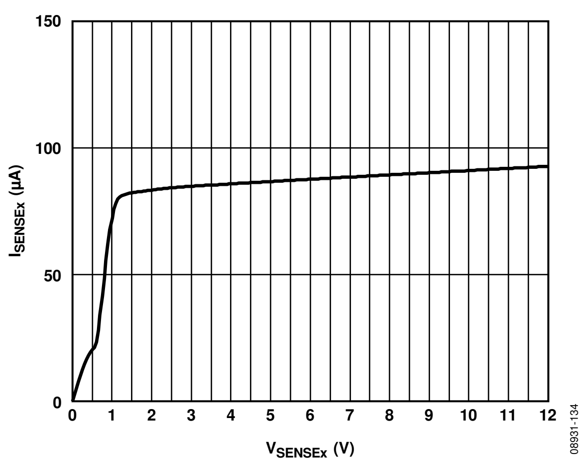

Figure 34. SENSE+/SENSE– Input Current (I_{SENSEx}) vs. Voltage (V_{SENSEx})

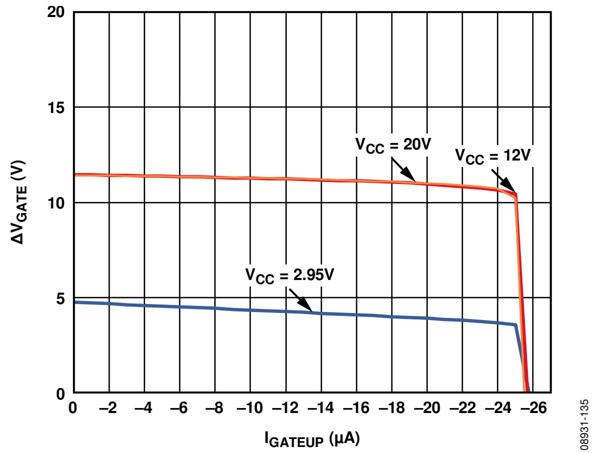

Figure 35. Gate Drive Voltage (ΔV_{GATE}) vs. Gate Pull-Up Current (I_{GATEUP})

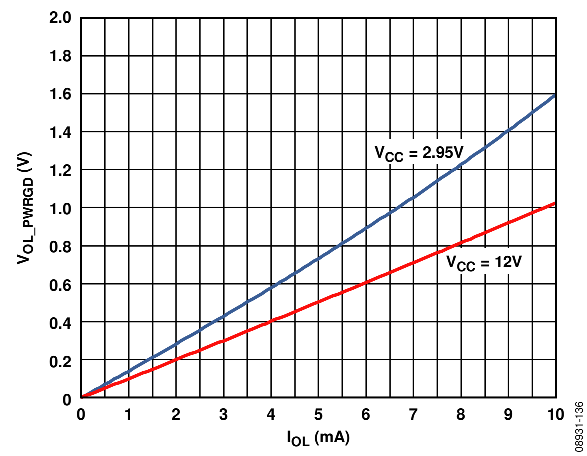

Figure 36. PWRGD Pin, V_{OL_PWRGD} vs. I_{OL}

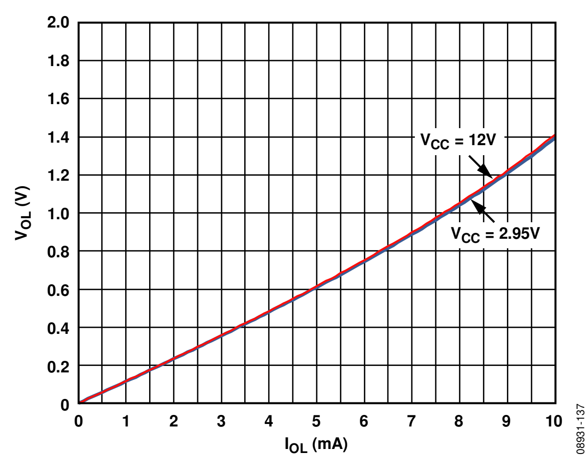

Figure 37. $\overline{\text{LATCH}}$ and GPOx/$\overline{\text{ALERTx}}$ Digital Outputs, V_{OL} vs. I_{OL}

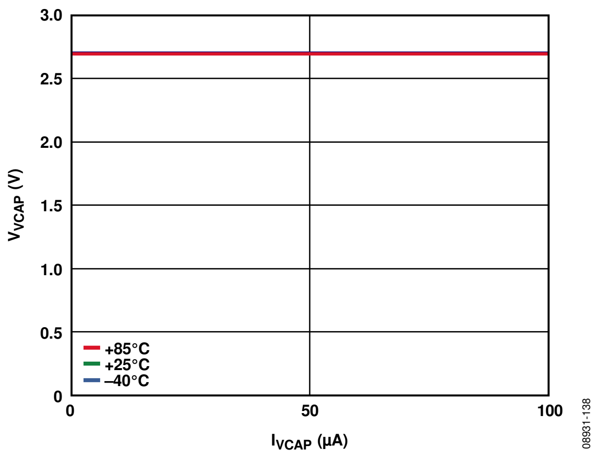

Figure 38. VCAP Voltage (V_{VCAP}) vs. VCAP Load (I_{VCAP})

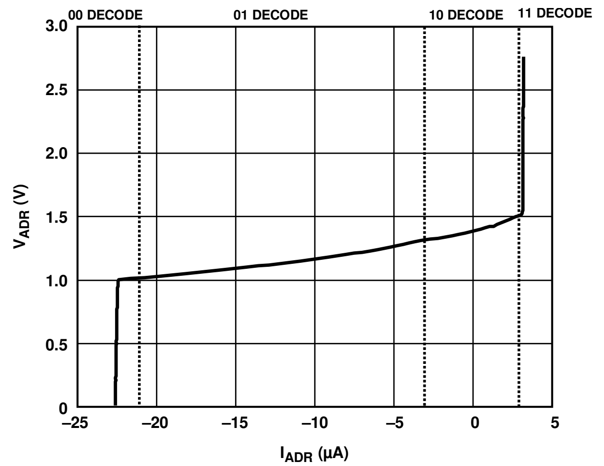

Figure 41. ADR Pin Voltage (V_{ADR}) vs. Current (I_{ADR})

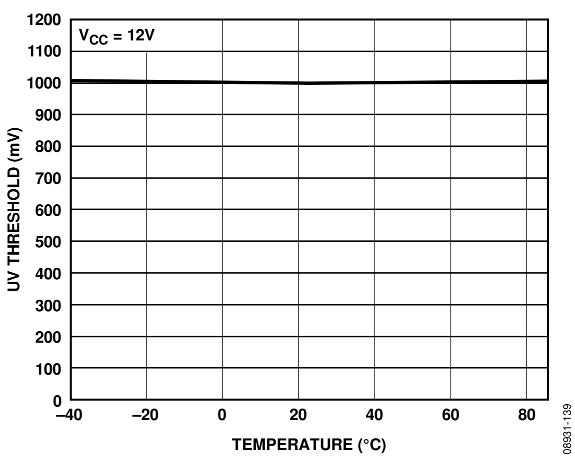

Figure 39. UV Threshold (UV_{TH}) vs. Temperature

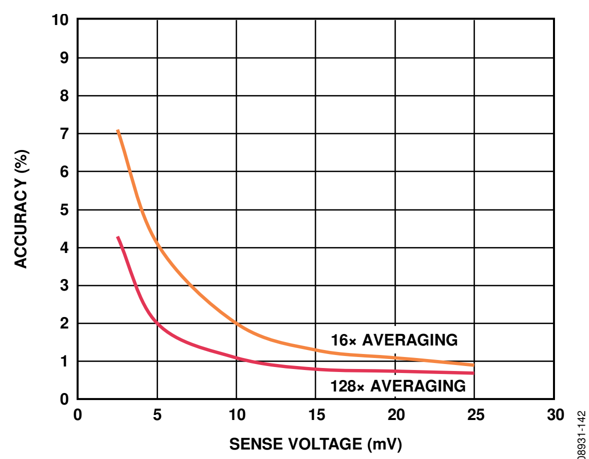

Figure 42. Worst-Case Current Sense Power Monitor Error vs. Current Sense Voltage (V_{SENSE}), 0°C to 65°C, V_{SENSE+} = 12 V

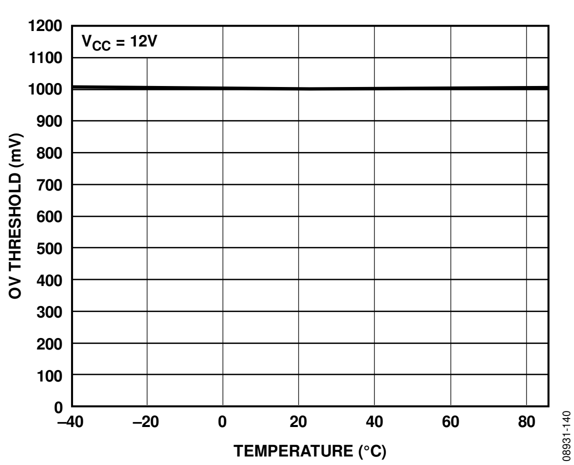

Figure 40. OV Threshold (OV_{TH}) vs. Temperature

FUNCTIONAL BLOCK DIAGRAMS

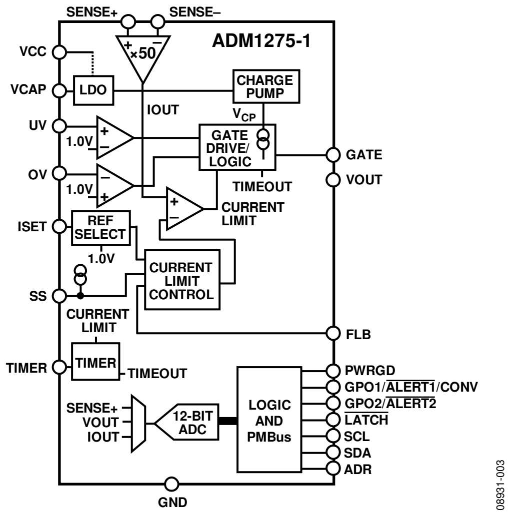

Figure 43. ADM1275-1 Functional Block Diagram

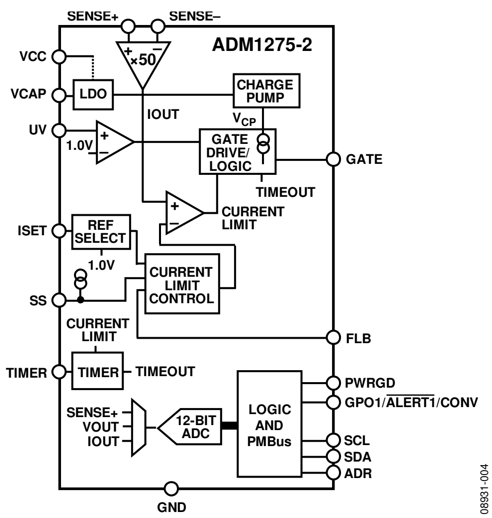

Figure 44. ADM1275-2 Functional Block Diagram

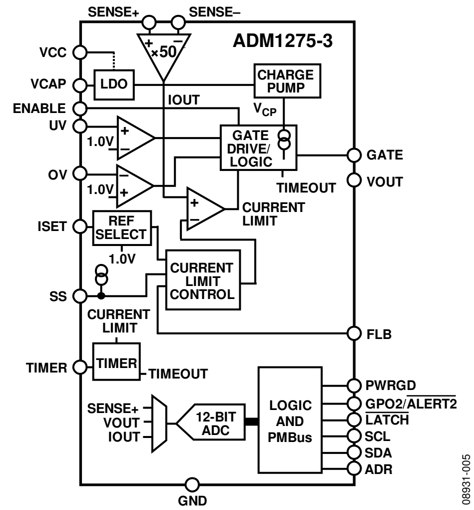

Figure 45. ADM1275-3 Functional Block Diagram

THEORY OF OPERATION

When circuit boards are inserted into a live backplane, discharged supply bypass capacitors draw large transient currents from the backplane power bus as they charge. These transient currents can cause permanent damage to connector pins, as well as dips on the backplane supply that can reset other boards in the system.

The ADM1275 is designed to control the powering on and off of a system in a controlled manner, allowing a board to be removed from, or inserted into, a live backplane by protecting it from excess currents. The ADM1275 can reside on the back-plane or on the removable board.

POWERING THE ADM1275

A supply voltage from 2.95 V to 20 V is required to power the ADM1275 via the VCC pin. The VCC pin provides the majority of the bias current for the device; the remainder of the current needed to control the gate drive and best regulate the V_{GS} voltage is supplied by the SENSE+ pin.

To ensure correct operation of the ADM1275, the voltage on the VCC pin must be greater than or equal to the voltage on the SENSE+ pin. No sequencing of the VCC and SENSE+ rails is necessary. The SENSE+ pin can be as low as 2 V for normal operation provided that a voltage of at least 2.95 V is connected to the VCC pin. In most applications, both the VCC and SENSE+ pins are connected to the same voltage rail, but they are connected via separate traces to prevent accuracy loss in the sense voltage measurement (see Figure 46).

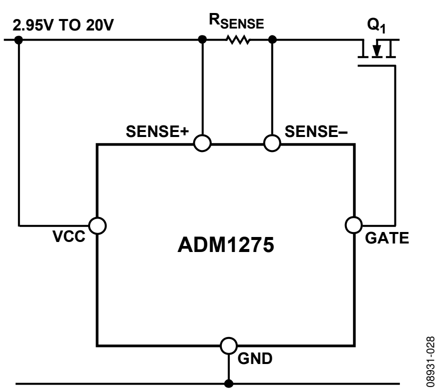

Figure 46. Powering the ADM1275

To protect the ADM1275 from unnecessary resets due to transient supply glitches, an external resistor and capacitor can be added, as shown in Figure 47. The values of these components should be chosen to provide a time constant that can filter any expected glitches. The resistor should, however, be small enough to keep voltage drops due to quiescent current to a minimum. A supply decoupling capacitor should not be placed on the rail before the FET unless a resistor is used to limit the inrush current.

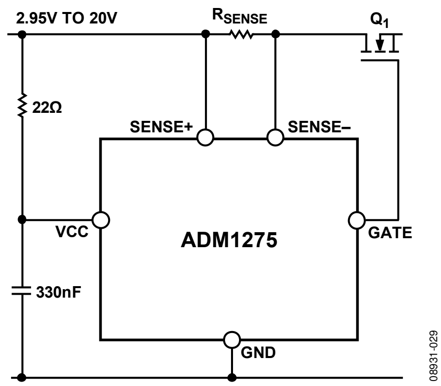

Figure 47. Transient Glitch Protection Using an RC Network

CURRENT SENSE INPUTS

The load current is monitored by measuring the voltage drop across an external sense resistor, R_{SENSE} (see Figure 48). An internal current sense amplifier provides a gain of 50 to the voltage drop detected across R_{SENSE}. The result is compared to an internal reference and used by the hot-swap control logic to detect when an overcurrent condition occurs.

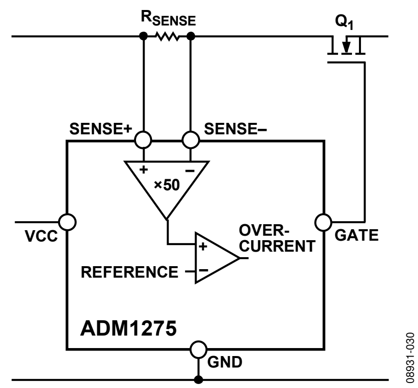

Figure 48. Hot-Swap Current Sense Amplifier

The SENSE inputs may be connected to multiple parallel sense resistors, which can affect the voltage drop detected by the ADM1275. The current flowing through the sense resistors creates an offset, resulting in reduced accuracy.

To achieve better accuracy, averaging resistors sum the current from the nodes of each sense resistor, as shown in Figure 49. The typical value for the averaging resistors is 10 Ω. The value of the averaging resistors is chosen to be much greater than the trace resistance between the sense resistors terminals and the inputs to the ADM1275. This greatly reduces the effects of differences in the trace resistances.

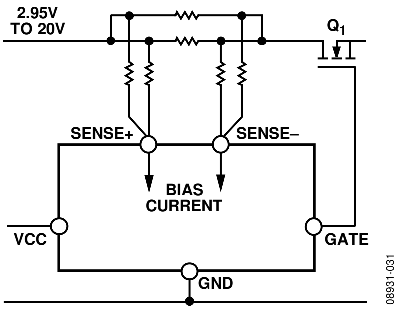

Figure 49. Connection of Multiple Sense Resistors to the SENSE Pins

CURRENT LIMIT REFERENCE

The current limit reference voltage determines the load current level to which the ADM1275 limits the current during an overcurrent event. This reference voltage is compared to the gained-up current sense voltage to determine whether the limit is reached.

An internal current limit reference selector block continuously compares the ISET, soft start, and foldback voltages to determine which voltage is the lowest at any given time; the lowest voltage is used as the current limit reference. This ensures that the programmed current limit, ISET, is used in normal operation, and that the soft start and foldback features reduce the current limit when required during startup and/or fault conditions.

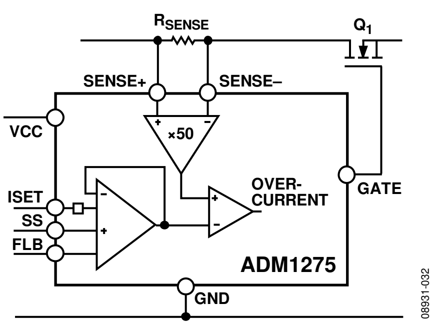

Figure 50. Current Limit Reference Selection

The foldback and soft start voltages vary during different modes of operation and are, therefore, clamped to minimum levels of 200 mV and 100 mV, respectively, to prevent zero current flow due to the current limit being too low. Figure 51 provides an example of how the soft start, foldback, and ISET voltages interact during startup as the ADM1275 is enhancing the FET and charging the load capacitances. Depending on how the soft start and foldback features are configured, the hand-off point can vary to ensure that the FET is operated correctly.

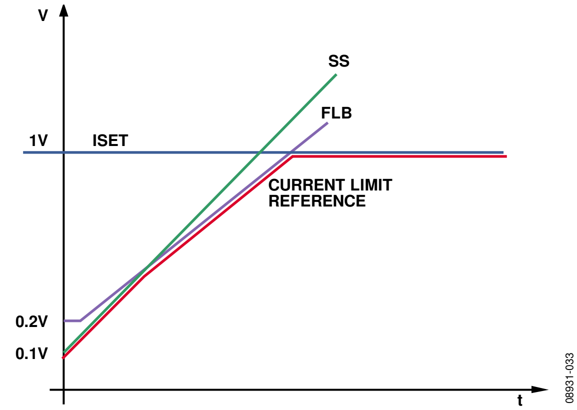

Figure 51. Interaction of Soft Start, Foldback, and ISET Current Limits

SETTING THE CURRENT LIMIT (ISET)

The maximum current limit is partially determined by selecting a sense resistor to match the current sense voltage limit on the controller for the desired load current. However, as currents become larger, the sense resistor requirements become smaller, and resolution can be difficult to achieve when selecting the appropriate sense resistor. The ADM1275 provides an adjustable current sense voltage limit to handle this issue. The device allows the user to program the required current sense voltage limit from 5 mV to 25 mV.

The default value of 20 mV is achieved by connecting the ISET pin directly to the VCAP pin. This configures the device to use an internal 1 V reference, which equates to 20 mV at the sense inputs (see Figure 52).

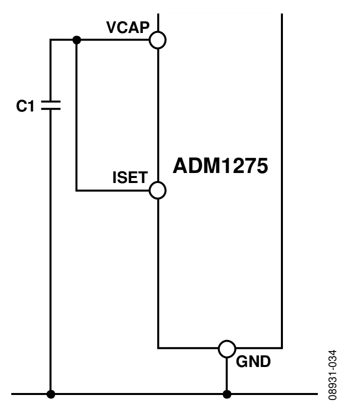

Figure 52. Fixed 20 mV Current Sense Limit

To program the sense voltage from 5 mV to 25 mV, a resistor divider is used to set a reference voltage on the ISET pin (see Figure 53).

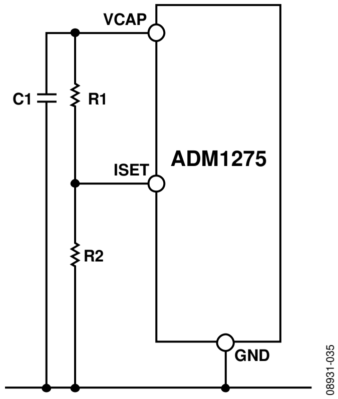

Figure 53. Adjustable 5 mV to 25 mV Current Sense Limit

The VCAP pin has a 2.7 V (±1.5%) internal generated voltage that can be used to set a voltage at the ISET pin. Assuming that V_{ISET} equals the voltage on the ISET pin, the resistor divider should be sized to set the ISET voltage as follows:

$$V_{ISET} = V_{SENSE} \times 50$$

where V_{SENSE} is the current sense voltage limit.

The VCAP rail can also be used as the pull-up supply for setting the I²C address. The VCAP pin should not be used for any other purpose. To guarantee accuracy specifications, care should be taken not to load the VCAP pin by more than 100 µA.

SOFT START

A capacitor connected to the SS pin determines the inrush current profile. Before the FET is enabled, the output voltage of the current limit reference selector block is clamped at 100 mV. This, in turn, holds the hot-swap sense voltage current limit, $V_{SENSECL}$, at approximately 2 mV. When the FET is requested to turn on, the SS pin is held at ground until the voltage between the SENSE+ and SENSE− pins (V_{SENSE}) reaches the circuit breaker voltage, V_{CB}.

$$V_{CB} = V_{SENSECL} - V_{CBOS}$$

where V_{CBOS} is typically 0.88 mV, making V_{CB} = 1.12 mV.

When the load current generates a sense voltage equal to V_{CB}, a 10 µA current source is enabled, which charges the SS capacitor and results in a linear ramping voltage on the SS pin. The current limit reference also ramps up accordingly, allowing the regulated load current to ramp up while avoiding sudden transients during power-up. The SS capacitor value is given by

$$C_{SS} = \frac{I_{SS} \times t}{V_{ISET}}$$

where:
I_{SS} = 10 µA.
t = SS ramp time.

For example, a 10 nF capacitor gives a soft start time of 1 ms.

Note that the SS voltage may intersect with the FLB (foldback) voltage, and the current limit reference may change to follow FLB (see Figure 51). This change has minimal impact on startup because the output voltage rises at a similar rate to the SS voltage.

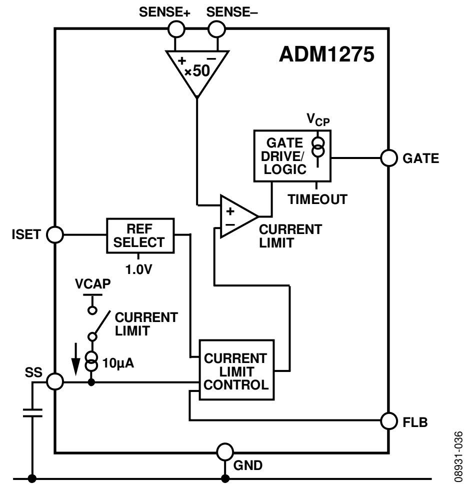

Figure 54. Soft Start

FOLDBACK

Foldback is a method to actively reduce the current limit as the voltage drop across the FET increases. It keeps the power across the FET to a minimum during power-up, overcurrent, or short-circuit events. It also avoids the need to oversize the FET to accommodate worst-case conditions, resulting in board size and cost savings.

The ADM1275 detects the voltage drop across the FET by looking at a resistor-divided version of the output voltage. It is assumed that the supply voltage remains constant and within tolerance. The device therefore relies on the principle that the drain of the FET is at the maximum expected supply voltage, and that the magnitude of the output voltage is relative to that of the V_{DS} of the FET. Using a resistor divider from the output voltage to the FLB pin, a relationship from V_{OUT}, and thus V_{DS}, to V_{FLB} can be derived.

The resistor divider should be designed to output a voltage equal to ISET when V_{OUT} falls below the desired level. This should be well below the working tolerance of the supply rail. As V_{OUT} continues to drop, the current limit reference follows V_{FLB} because it is now the lowest voltage input to the current limit reference selector block. This results in a reduction of the current limit and, therefore, the regulated load current. To prevent complete current flow restriction, a clamp becomes active when the current limit reference reaches 200 mV. The current limit cannot drop below this level.

To suit the SOA characteristics of a particular FET, the required minimum current for this clamp varies from design to design. However, the current limit reference fixes this clamp at 200 mV, which equates to 4 mV at the sense resistor. Therefore, the main ISET voltage can be adjusted to align this clamp to the required percentage current reduction. For example, if ISET equals 0.8 V, the clamp can be set at 25% of the maximum current.

TIMER

The TIMER pin handles several timing functions with an external capacitor, C_{TIMER}. The two comparator thresholds are V_{TIMERL} (0.2 V) and V_{TIMERH} (1 V). There are four timing current sources: a 3 μA pull-up, a 60 μA pull-up, a 2 μA pull-down, and a 100 μA pull-down.

These current and voltage levels, together with the value of C_{TIMER} chosen by the user, determine the initial timing cycle time, the fault current limit time, and the hot-swap retry duty cycle. The TIMER capacitor value is determined using the following equation:

$$C_{TIMER} = (t_{ON} \times 60\ \mu A)/V_{TIMERH}$$

where t_{ON} is the time that the FET is allowed to spend in regulation at the set current limit. The choice of FET is based on matching this time with the SOA requirements of the FET. Foldback can be used to simplify the selection.

When VCC is connected to the backplane supply, the internal supply of the ADM1275 must be charged up. In a very short time, the internal supply is fully charged up and, because the undervoltage lockout (UVLO) voltage is exceeded at VCC, the device comes out of reset. During this first short reset period, the GATE and TIMER pins are both held low.

The ADM1275 then goes through an initial timing cycle. The TIMER pin is pulled high with 3 μA. When the TIMER reaches the V_{TIMERH} threshold (1.0 V), the first portion of the initial timing cycle is complete. The 100 μA current source then pulls down the TIMER pin until it reaches V_{TIMERL} (0.2 V). The initial timing cycle duration is related to C_{TIMER} by the following equation:

$$t_{INITIAL} = \frac{V_{TIMERH} \times C_{TIMER}}{3\ \mu A} + \frac{(V_{TIMERH} - V_{TIMERL}) \times C_{TIMER}}{100\ \mu A}$$

For example, a 100 nF capacitor results in a delay of approximately 34 ms. If the UV and OV inputs indicate that the supply is within the defined window of operation when the initial timing cycle terminates, the device is ready to start a hot-swap operation.

When the voltage across the sense resistor reaches the circuit breaker trip voltage, V_{CB}, the 60 μA timer pull-up current is activated, and the gate begins to regulate the current at the current limit. This initiates a ramp-up on the TIMER pin. If the sense voltage falls below this circuit breaker trip voltage before the TIMER pin reaches V_{TIMERH}, the 60 μA pull-up is disabled and the 2 μA pull-down is enabled.

The circuit breaker trip voltage is not the same as the hot-swap sense voltage current limit. There is a small circuit breaker offset, V_{CBOS}, which means that the timer actually starts a short time before the current reaches the defined current limit.

However, if the overcurrent condition is continuous and the sense voltage remains above the circuit breaker trip voltage, the 60 μA pull-up remains active and the FET remains in regulation.

This allows the TIMER pin to reach V_{TIMERH} and initiate the GATE shutdown. On the ADM1275-1 and ADM1275-3, the $\overline{\text{LATCH}}$ pin is pulled low immediately.

In latch-off mode, the TIMER pin is switched to the 2 μA pull-down when it reaches the V_{TIMERH} threshold. The $\overline{\text{LATCH}}$ pin (ADM1275-1 and ADM1275-3) remains low. While the TIMER pin is being pulled down, the hot-swap controller is kept off and cannot be turned back on.

When the voltage on the TIMER pin goes below the V_{TIMERL} threshold, the hot-swap controller can be reenabled by toggling the UV pin or by using the PMBus OPERATION command to toggle the ON bit from on to off and then on again.

HOT-SWAP RETRY DUTY CYCLE

The ADM1275-1 and ADM1275-3 turn off the FET after an overcurrent fault and then use the capacitor on the TIMER pin to provide a delay before automatically retrying the hot-swap operation. To configure the ADM1275-1 and ADM1275-3 for autoretry mode, the $\overline{\text{LATCH}}$ pin is tied to the UV pin or to the ENABLE pin (ADM1275-3 only). Note that a pull-up is required on the $\overline{\text{LATCH}}$ pin.

When an overcurrent fault occurs, the TIMER capacitor is charged with a 60 μA pull-up current. When the TIMER pin reaches V_{TIMERH}, the GATE pin is pulled down. When the $\overline{\text{LATCH}}$ pin is tied to the UV pin or the ENABLE pin for autoretry mode, the TIMER pin is pulled down with a 2 μA current sink. When the TIMER pin reaches V_{TIMERL} (0.2 V), it automatically restarts the hot-swap operation.

The duty cycle of this automatic retry cycle is set by the ratio of 2 μA/60 μA, which approximates to being on about 4% of the time. The value of the timer capacitor determines the on time of this cycle, which is calculated as follows:

$$t_{ON} = V_{TIMERH} \times (C_{TIMER}/60\ \mu A)$$

$$t_{OFF} = (V_{TIMERH} - V_{TIMERL}) \times (C_{TIMER}/2\ \mu A)$$

A 100 nF TIMER capacitor gives an on time of 1.67 ms and an off time of 40 ms. The device retries indefinitely in this manner and can be disabled manually by holding the UV or ENABLE pin low or by disconnecting the $\overline{\text{LATCH}}$ pin. To prevent thermal stress, an RC network can be used to extend the retry time to any desired level.

FET GATE DRIVE CLAMPS

The charge pump used on the GATE pin is capable of driving the pin to $V_{CC} + (2 \times V_{CC})$, but it is clamped to less than 14 V above the SENSE pins and less than 31 V. These clamps ensure that the maximum V_{GS} rating of the FET is not exceeded.