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Hot Swap Controller and Digital Power and Energy Monitoring with PMBus Interface

Data Sheet **ADM1276**

FEATURES

- Controls supply voltages from 2 V to 20 V
- 370 ns response time to short circuit
- Resistor-programmable 5 mV to 25 mV current limit
- ±1% accurate, 12-bit ADC for current, V_{IN}/V_{OUT} readback
- Charge pumped gate drive for multiple external N-channel FETs
- High gate drive voltage to ensure lowest R_{DSON}
- Foldback for tighter FET SOA protection
- Automatic retry or latch-off on current fault
- Programmable current-limit timer for SOA
- Programmable, multifunction GPO
- Power-good status output
- Analog UV and OV protection
- ENABLE pin
- Reports power and energy consumption over time
- Peak detect registers for current and voltage
- PMBus fast mode compliant interface
- 20-lead LFCSP

APPLICATIONS

- Power monitoring and control/power budgeting
- Central office equipment
- Telecommunication and data communication equipment
- PCs/servers

FUNCTIONAL BLOCK DIAGRAM

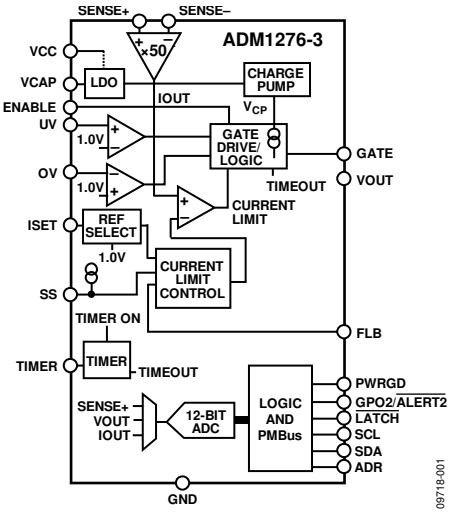

Figure 1.

GENERAL DESCRIPTION

The ADM1276 is a hot swap controller that allows a circuit board to be removed from or inserted into a live backplane. It also features current and voltage readback via an integrated 12-bit analog-to-digital converter (ADC), accessed using a PMBus™ interface.

The load current is measured using an internal current sense amplifier that measures the voltage across a sense resistor in the power path via the SENSE+ and SENSE− pins. A default limit of 20 mV is set, but this limit can be adjusted, if required, using a resistor divider network from the internal reference voltage to the ISET pin.

The ADM1276 limits the current through the sense resistor by controlling the gate voltage of an external N-channel FET in the power path, via the GATE pin. The sense voltage—and, therefore, the load current—is maintained below the preset maximum. The ADM1276 protects the external FET by limiting the time that the FET remains on while the current is at its maximum value. This current-limit time is set by the choice of capacitor connected to the TIMER pin. In addition, a foldback resistor network can be used to actively lower the current limit as the voltage across the FET is increased. This helps to maintain constant power in the FET and allows the safe operating area (SOA) to be adhered to in an effective manner.

In case of a short-circuit event, a fast internal overcurrent detector responds within 370 ns and signals the gate to shut down. A 1500 mA pull-down device ensures a fast FET response. The ADM1276 features overvoltage (OV) and undervoltage (UV) protection, programmed using external resistor dividers on the UV and OV pins. A PWRGD signal can be used to detect when the output supply is valid, using the FLB pin to monitor the output. A GPO pin can be configured as an output signal that can be asserted when a programmed current or voltage level is reached.

The 12-bit ADC can measure the current in the sense resistor, as well as the supply voltage on the SENSE+ pin or the output voltage. A PMBus interface allows a controller to read current and voltage data from the ADC. Measurements can be initiated by a PMBus command. Alternatively, the ADC can run continuously, and the user can read the latest conversion data whenever required. As many as four unique PMBus addresses can be selected, depending on the way that the ADR pin is connected.

The ADM1276 is available in a 20-lead LFCSP with a $\overline{\text{LATCH}}$ pin that can be configured for automatic retry or latch-off when an overcurrent fault occurs.

Rev. C Document Feedback

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ADM1276* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADM1276 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1135: ADC Sampling Information ADM1275/ ADM1276/ADM1075
- AN-1343: Energy Metering on Hot Swap and Power Monitor Devices

Data Sheet

- ADM1276: Hot Swap Controller and Digital Power and Energy Monitoring with PMBus Interface Data Sheet

User Guides

- UG-241: Using the Simulation Model for ADI Hotswap Controllers
- UG-263: Evaluating the ADM1275 and ADM1276
- UG-353: Hot Swap and Power Monitor Software
- UG-404: USB-SDP-CABLEZ Serial Interface Board

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADMxxxx Common Run-Time
- Hot-Swap & Power Monitoring Evaluation Software

DESIGN RESOURCES

- ADM1276 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADM1276 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

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7/11—Rev. 0 to Rev. A

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Added Endnote 1 to Table 2 8
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3/11—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 2.95 V to 20 V, $V_{CC} \geq V_{SENSE+}$, V_{SENSE+} = 2 V to 20 V, $V_{SENSE} = (V_{SENSE+} - V_{SENSE-}) = 0$ V, T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY						
Operating Voltage Range	V_{CC}	2.95		20	V	
Undervoltage Lockout		2.4		2.7	V	V_{CC} rising
Undervoltage Hysteresis			90	120	mV	
Quiescent Current	I_{CC}			5	mA	GATE on and power monitor running
UV PIN						
Input Current	I_{UV}			100	nA	UV ≤ 3.6 V
UV Threshold	UV_{TH}	0.97	1.0	1.03	V	UV falling
UV Threshold Hysteresis	UV_{HYST}	40	50	60	mV	
UV Glitch Filter	UV_{GF}	2		7	µs	50 mV overdrive
UV Propagation Delay	UV_{PD}		5	8	µs	UV low to GATE pull-down active
OV PIN						
Input Current	I_{OV}			100	nA	OV ≤ 3.6 V
OV Threshold	OV_{TH}	0.97	1.0	1.03	V	OV rising
OV Threshold Hysteresis	OV_{HYST}	50	60	70	mV	
OV Glitch Filter	OV_{GF}	0.5		1.5	µs	50 mV overdrive
OV Propagation Delay	OV_{PD}		1.0	2	µs	OV high to GATE pull-down active
SENSE+ AND SENSE− PINS						
Input Current	I_{SENSEx}			150	µA	Per individual pin; SENSE+, SENSE− = 20 V
Input Imbalance	$I_{\Delta SENSE}$			5	µA	$I_{\Delta SENSE} = (I_{SENSE+}) - (I_{SENSE-})$
VCAP PIN						
Internally Regulated Voltage	V_{VCAP}	2.66	2.7	2.74	V	0 µA ≤ I_{VCAP} ≤ 100 µA; C_{VCAP} = 1 µF
ISET PIN						
Reference Select Threshold	$V_{ISETRSTH}$	1.35	1.5	1.65	V	If $V_{ISET} > V_{ISETRSTH}$, an internal 1 V reference (V_{CLREF}) is used
Internal Reference	V_{CLREF}		1		V	Accuracies included in total sense voltage accuracies
Gain of Current Sense Amplifier	AV_{CSAMP}		50		V/V	Accuracies included in total sense voltage accuracies
Input Current	I_{ISET}			100	nA	$V_{ISET} \leq V_{VCAP}$
GATE PIN						Maximum voltage on the gate is always clamped to ≤31 V
Gate Drive Voltage	ΔV_{GATE}					$\Delta V_{GATE} = V_{GATE} - V_{SENSE+}$
		10	12	14	V	15 V ≥ V_{CC} ≥ 8 V; I_{GATE} ≤ 5 µA
		4.5		13	V	20 V ≥ V_{CC} ≥ 15 V; I_{GATE} ≤ 5 µA
		8		10	V	$V_{SENSE+} = V_{CC}$ = 5 V; I_{GATE} ≤ 5 µA
		4.5		6	V	$V_{SENSE+} = V_{CC}$ = 2.95 V; I_{GATE} ≤ 1 µA
Gate Pull-Up Current	I_{GATEUP}	−20		−30	µA	V_{GATE} = 0 V
Gate Pull-Down Current	I_{GATEDN}					
Regulation	I_{GATEDN_REG}	45	60	75	µA	$V_{GATE} \geq 2$ V; V_{ISET} = 1.0 V; (SENSE+) − (SENSE−) = 30 mV
Slow	I_{GATEDN_SLOW}	5	10	15	mA	$V_{GATE} \geq 2$ V
Fast	I_{GATEDN_FAST}	750	1500	2000	mA	$V_{GATE} \geq 12$ V; $V_{CC} \geq 12$ V
Gate Holdoff Resistance			20		Ω	V_{CC} = 0 V
HOT SWAP SENSE VOLTAGE						
Hot Swap Sense Voltage Current Limit	$V_{SENSECL}$	19.6	20	20.4	mV	V_{ISET} > 1.65 V; V_{FLB} > 1.12 V; V_{GATE} = (SENSE+) + 3 V; I_{GATE} = 0 µA; $V_{SS} \geq 2$ V
Foldback Inactive						V_{GATE} = (SENSE+) + 3 V; I_{GATE} = 0 µA; $V_{SS} \geq 2$ V
		24.6	25	25.4	mV	V_{ISET} = 1.25 V; V_{FLB} > 1.395 V
		19.6	20	20.4	mV	V_{ISET} = 1.0 V; V_{FLB} > 1.12 V
		9.6	10	10.4	mV	V_{ISET} = 0.5 V; V_{FLB} > 0.57 V
		4.6	5	5.4	mV	V_{ISET} = 0.25 V; V_{FLB} > 0.295 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Foldback Active		3.5	4	4.5	mV	V_{FLB} = 0 V; V_{GATE} = (SENSE+) + 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 1 V
		9.6	10	10.4	mV	V_{ISET} > 1.0 V; V_{FLB} = 0.5 V; V_{GATE} = (SENSE+) + 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 1 V
Circuit Breaker Offset	V_{CBOS}	0.6	0.88	1.12	mV	Circuit breaker trip voltage, $V_{CB} = V_{SENSECL} - V_{CBOS}$
SEVERE OVERCURRENT						
Voltage Threshold	$V_{SENSEOC}$	40		50	mV	V_{ISET} = 1.0 V; V_{FLB} > 1.1 V; V_{SS} ≥ 2 V
		9.5		13.0	mV	V_{ISET} = 0.25 V; V_{FLB} > 1.1 V; V_{SS} ≥ 2 V
Short Glitch Filter Duration		90		200	ns	V_{ISET} > 1.65 V; V_{SENSE} driven from 18 mV to 52 mV; selectable via PMBus
Long Glitch Filter Duration (Default)		530		900	ns	V_{SENSE} driven from 18 mV to 52 mV
Response Time						
With Short Glitch Filter		180		370	ns	2 mV overdrive maximum severe overcurrent threshold
With Long Glitch Filter		645		1020	ns	
SOFT START (SS PIN)						
SS Pull-Up Current	I_{SS}	−12	−10	−8	µA	V_{SS} = 0 V
Default $V_{SENSECL}$ Limit		0.5	1.25	1.8	mV	When V_{SENSE} reaches this level, I_{SS} is enabled, ramping $V_{SENSECL}$; V_{SS} = 0 V
SS Pull-Down Current			100		µA	V_{SS} = 1 V
TIMER PIN						
Timer Pull-Up Current	$I_{TIMERUP}$					
Power-On Reset(POR)	$I_{TIMERUPPOR}$	−2	−3	−4	µA	Initial power-on reset; V_{TIMER} = 0.5 V
Overcurrent (OC) Fault	$I_{TIMERUPFLT}$	−57	−60	−63	µA	Overcurrent fault; 0.2 V ≤ V_{TIMER} ≤ 1 V
Timer Pull-Down Current						
Retry	$I_{TIMERDNRT}$	1.7	2	2.3	µA	After fault when GATE is off; V_{TIMER} = 0.5 V
Hold	$I_{TIMERDNHOLD}$		100		µA	Holds TIMER at 0 V when inactive; V_{TIMER} = 0.5 V
Timer Retry/OC Fault Current Ratio			3.33	3.8	%	Defines the limits of the autoretry duty cycle
Timer High Threshold	V_{TIMERH}	0.98	1.0	1.02	V	
Timer Low Threshold	V_{TIMERL}	0.18	0.2	0.22	V	
FOLDBACK (FLB PIN)						
FLB and PWRGD Threshold	V_{FLBTH}	1.08	1.1	1.12	V	FLB rising; V_{ISET} = 1.0 V
Input Current	I_{FLB}			100	nA	V_{FLB} ≤ 1.0 V; V_{ISET} = 1.25 V
				100	nA	V_{VCAP} ≤ V_{FLB} ≤ 20 V
Hysteresis Current		1.7		2.3	µA	
Internal Hysteresis Voltage		1.9		3.1	mV	Voltage drop across the internal 1.3 kΩ resistor
Power-Good Glitch Filter	$PWRGD_{GF}$	0.3	0.7	1	µs	50 mV overdrive
Minimum Foldback Clamp			200		mV	Accuracies included in total sense voltage accuracies
VOUT PIN						
Input Current				20	µA	VOUT = 20 V
$\overline{\text{LATCH}}$ PIN						
Output Low Voltage	V_{OL_LATCH}			0.4	V	I_{LATCH} = 1 mA
				1.5	V	I_{LATCH} = 5 mA
Leakage Current				100	nA	V_{LATCH} ≤ 2 V; $\overline{\text{LATCH}}$ output high-Z
				1	µA	V_{LATCH} = 20 V; $\overline{\text{LATCH}}$ output high-Z
ENABLE PIN						No internal pull-up present on this pin
Leakage Current				100	nA	V_{GPO2} ≤ 2 V
				1	µA	V_{GPO2} = 20 V
Input High Voltage	V_{IH}	1.1			V	
Input Low Voltage	V_{IL}			0.8	V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
GPO2/$\overline{\text{ALERT2}}$ PIN						
Output Low Voltage	V_{OL_GPO2}			0.4	V	I_{GPO2} = 1 mA
				1.5	V	I_{GPO2} = 5 mA
Leakage Current				100	nA	$V_{GPO2} \leq 2$ V; GPO output high-Z
				1	µA	V_{GPO2} = 20 V; GPO output high-Z
PWRGD PIN						
Output Low Voltage	V_{OL_PWRGD}			0.4	V	I_{PWRGD} = 1 mA
				1.5	V	I_{PWRGD} = 5 mA
VCC That Guarantees Valid Output		1			V	I_{SINK} = 100 µA; V_{OL_PWRGD} = 0.4 V
Leakage Current				100	nA	$V_{PWRGD} \leq 2$ V; PWRGD output high-Z
				1	µA	V_{PWRGD} = 20 V; PWRGD output high-Z
CURRENT AND VOLTAGE MONITORING						
Current Sense Absolute Error						25 mV input range; 128 sample averaging (unless otherwise noted)
			±0.2	±0.7	%	V_{SENSE} = 20 mV; V_{SENSE+} = 12 V; T_A = 0°C to 65°C
			±0.08		%	V_{SENSE} = 20 mV; V_{SENSE+} = 12 V; T_A = 25°C
				±1.0	%	V_{SENSE} = 20 mV
			±0.08		%	V_{SENSE} = 20 mV; T_A = 25°C
			±0.2		%	V_{SENSE} = 20 mV; T_A = 0°C to 65°C
				±1.0	%	V_{SENSE} = 20 mV; 16 sample averaging
			±0.08		%	V_{SENSE} = 20 mV; 16 sample averaging; T_A = 25°C
			±0.2		%	V_{SENSE} = 20 mV; 16 sample averaging; T_A = 0°C to 65°C
				±2.8	%	V_{SENSE} = 20 mV; 1 sample averaging
			±0.09		%	V_{SENSE} = 20 mV; 1 sample averaging; T_A = 25°C
			±0.2		%	V_{SENSE} = 20 mV; 1 sample averaging; T_A = 0°C to 65°C
				±0.7	%	V_{SENSE} = 25 mV; V_{SENSE+} = 12 V
			±0.04		%	V_{SENSE} = 25 mV; V_{SENSE+} = 12 V; T_A = 25°C
			±0.15		%	V_{SENSE} = 25 mV; V_{SENSE+} = 12 V; T_A = 0°C to 65°C
				±0.75	%	V_{SENSE} = 20 mV; V_{SENSE+} = 12 V
				±0.8	%	V_{SENSE} = 15 mV; V_{SENSE+} = 12 V
				±1.1	%	V_{SENSE} = 10 mV; V_{SENSE+} = 12 V
				±2.0	%	V_{SENSE} = 5 mV; V_{SENSE+} = 12 V
				±4.3	%	V_{SENSE} = 2.5 mV; V_{SENSE+} = 12 V
SENSE+/VOUT Absolute Error				±1.0	%	Low input range; input voltage ≥ 3 V
				±1.0	%	High input range; input voltage ≥ 10 V
ADC Conversion Time						Includes time for power multiplication
			237	280	µs	1 sample of VIN and IOUT; from command received to valid data in register
			360	426	µs	1 sample of VIN, VOUT, and IOUT; from command received to valid data in register
			3753	4233	µs	16 samples of VIN and IOUT averaged; from command received to valid data in register
			5545	6570	µs	16 samples of VIN, VOUT, and IOUT averaged; from command received to valid data in register
Power Multiplication Time			14		µs	
ADR PIN						
Address Set to 00		0		0.8	V	Connect to GND
Input Current for Address 00		−40	−22		µA	V_{ADR} = 0 V to 0.8 V
Address Set to 01		135	150	165	kΩ	Resistor to GND
Address Set to 10		−1		+1	µA	No connect state; maximum leakage current allowed

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Address Set to 11		2			V	Connect to VCAP
Input Current for Address 11			3	10	µA	V_{ADR} = 2.0 V to VCAP; must not exceed the maximum allowable current draw from VCAP
SERIAL BUS DIGITAL INPUTS (SDA, SCL)						
Input High Voltage	V_{IH}	1.1			V	
Input Low Voltage	V_{IL}			0.8	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4 mA
Input Leakage	$I_{LEAK-PIN}$	−10		+10	µA	
		−5		+5	µA	Device is not powered
Nominal Bus Voltage	V_{DD}	2.7		5.5	V	3 V to 5 V ± 10%
Capacitance for SDA, SCL Pins	C_{PIN}		5		pF	
Input Glitch Filter	t_{SP}	0		50	ns	

SERIAL BUS TIMING CHARACTERISTICS

Table 2.

Parameter	Description	Min	Typ	Max	Unit	Test Conditions/Comments
f_{SCLK}	Clock frequency			400	kHz	
t_{BUF}	Bus free time	1.3			µs	Following the stop condition of a read transaction
		4.7			µs	Following the stop condition of a write transaction
$t_{HD;STA}$	Start hold time	0.6			µs	
$t_{SU;STA}$	Start setup time	0.6			µs	
$t_{SU;STO}$	Stop setup time	0.6			µs	
$t_{HD;DAT}$	SDA hold time	300		900	ns	
$t_{SU;DAT}$	SDA setup time	100			ns	
t_{LOW}	SCL low time	1.3			µs	
t_{HIGH}	SCL high time	0.6			µs	
t_R[1]	SCL, SDA rise time	20		300	ns	
t_F	SCL, SDA fall time	20		300	ns	

[1]Note: $t_R = (V_{IL(MAX)} - 0.15)$ to $(V_{IH3V3} + 0.15)$ and $t_F = 0.9\ V_{DD}$ to $(V_{IL(MAX)} - 0.15)$; where V_{IH3V3} = 2.1 V, and V_{DD} = 3.3 V.

Timing Diagram

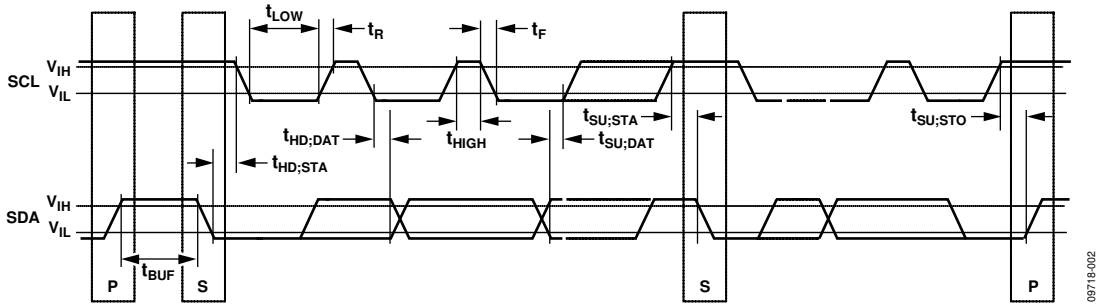

Figure 2. Serial Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VCC Pin	−0.3 V to +25 V
UV Pin	−0.3 V to +4 V
OV Pin	−0.3 V to +4 V
SS Pin	−0.3 V to VCAP + 0.3 V
TIMER Pin	−0.3 V to VCAP + 0.3 V
VCAP Pin	−0.3 V to +4 V
ISET Pin	−0.3 V to VCAP + 0.3 V
$\overline{\text{LATCH}}$ Pin	−0.3 V to +25 V
SCL Pin	−0.3 V to +6.5 V
SDA Pin	−0.3 V to +6.5 V
ADR Pin	−0.3 V to VCAP + 0.3 V
ENABLE Pin	−0.3 V to +25 V
GPO2/$\overline{\text{ALERT2}}$ Pin	−0.3 V to +25 V
PWRGD Pin	−0.3 V to +25 V
FLB Pin	−0.3 V to +25 V
VOUT Pin	−0.3 V to +25 V
GATE Pin (Internal Supply Only)[1]	−0.3 V to +36 V
SENSE+ Pin	−0.3 V to +25 V
SENSE− Pin	−0.3 V to +25 V
V_{SENSE} ($V_{SENSE+} - V_{SENSE-}$)	±0.3 V
Continuous Current into Any Pin	±10 mA
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature, Soldering (10 sec)	300°C
Junction Temperature	150°C

[1] The GATE pin has internal clamping circuits to prevent the GATE pin voltage from exceeding the maximum ratings of a MOSFET with V_{GSMAX} = 20 V and internal process limits. Applying a voltage source to this pin externally may cause irreversible damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
20-lead LFCSP (CP-20-9)	30.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

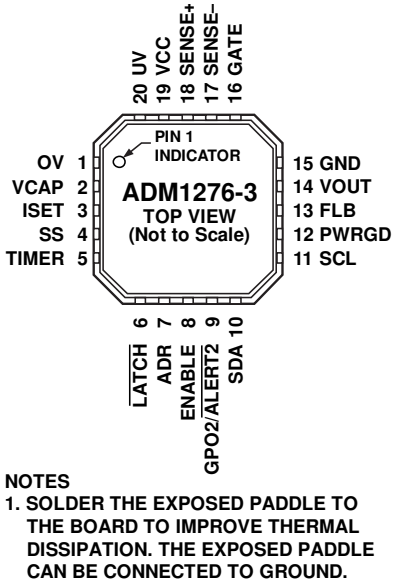

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
19	VCC	Positive Supply Input Pin. An undervoltage lockout (UVLO) circuit resets the device when a low supply voltage is detected. GATE is held low when the supply is below UVLO. During normal operation, this pin should remain greater than or equal to SENSE+ to ensure that specifications are adhered to. No sequencing is required.
20	UV	Undervoltage Input Pin. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect whether the supply is under the UV limit.
1	OV	Overvoltage Input Pin. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect whether the supply is above the OV limit.
2	VCAP	Internal Regulated Supply. Place a capacitor with a value of 1 µF or greater on this pin to maintain good accuracy. This pin can be used as a reference to program the ISET pin voltage.
3	ISET	Current Limit. This pin allows the current-limit threshold to be programmed. The default limit is set when this pin is connected directly to VCAP. To achieve a user defined sense voltage, the current limit can be adjusted using a resistor divider from VCAP. An external reference can also be used.
4	SS	Soft Start Pin. A capacitor is used on this pin to set the soft start ramp profile. The voltage on the SS pin controls the current sense voltage limit, which controls the inrush current profile.
5	TIMER	Timer Pin. An external capacitor, C_{TIMER}, sets an initial timing cycle delay and a fault delay. The GATE pin is pulled low when the voltage on the TIMER pin exceeds the upper threshold.
6	$\overline{\text{LATCH}}$	Latch Pin. This pin signals that the device is latching off after an overcurrent fault. The device can be configured for automatic retry after latch-off by connecting this pin directly to the UV or the ENABLE pin.
7	ADR	PMBus Address Pin. This pin can be tied to GND, tied to VCAP, remain floating, or tied low through a resistor to set four different PMBus addresses (see the Device Addressing section).
8	ENABLE	Enable Pin. This pin is a digital logic input. This input must be high to allow the ADM1276 hot swap controller to begin a power-up sequence. If this pin is held low, the ADM1276 is prevented from powering up. There is no internal pull-up on this pin.
9	GPO2/$\overline{\text{ALERT2}}$	General-Purpose Digital Output/Alert. This is a dual function pin. There is no internal pull-up on this pin. The $\overline{\text{ALERT2}}$ function of this pin can be configured to generate an alert signal when one or more fault or warning conditions are detected. At power-up, $\overline{\text{ALERT2}}$ indicates the FET health mode by default.
10	SDA	Serial Data Input/Output Pin. Open-drain input/output. Requires an external resistive pull-up.
11	SCL	Serial Clock Pin. Open-drain input. Requires an external resistive pull-up.
12	PWRGD	Power-Good Signal. Used to indicate that the supply is within tolerance. This signal is based on the voltage present on the FLB pin.
13	FLB	Foldback Pin. A foldback resistor divider is placed from the source of the FET to this pin. Foldback is used to reduce the current limit when the source voltage drops. The foldback feature ensures that the power through the FET is not increased beyond the SOA limits.

Pin No.	Mnemonic	Description
14	VOUT	Output Voltage. This pin is used to read back the output voltage using the internal ADC. A 1 kΩ resistor should be inserted in series between the source of a FET and the VOUT pin.
15	GND	Ground Pin.
16	GATE	Gate Output Pin. This pin is the high-side gate drive of an external N-channel FET. This pin is driven by the FET drive controller, which uses a charge pump to provide a pull-up current to charge the FET gate pin. The FET drive controller regulates to a maximum load current by regulating the GATE pin. GATE is held low when the supply is below UVLO.
17	SENSE−	Negative Current Sense Input Pin. A sense resistor between the SENSE+ pin and the SENSE− pin sets the analog current limit. The hot swap operation of the ADM1276 controls the external FET gate to maintain the sense voltage ($V_{SENSE+} - V_{SENSE-}$). This pin also connects to the FET drain pin.
18	SENSE+	Positive Current Sense Input Pin. This pin connects to the main supply input. A sense resistor between the SENSE+ pin and the SENSE− pin sets the analog current limit. The hot swap operation of the ADM1276 controls the external FET gate to maintain the sense voltage ($V_{SENSE+} - V_{SENSE-}$). This pin is also used to measure the supply input voltage using the ADC.
N/A[1]	EP	Exposed Pad. The exposed pad is located on the underside of the LFCSP package. Solder the exposed pad to the printed circuit board (PCB) to improve thermal dissipation. The exposed pad can be connected to ground.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

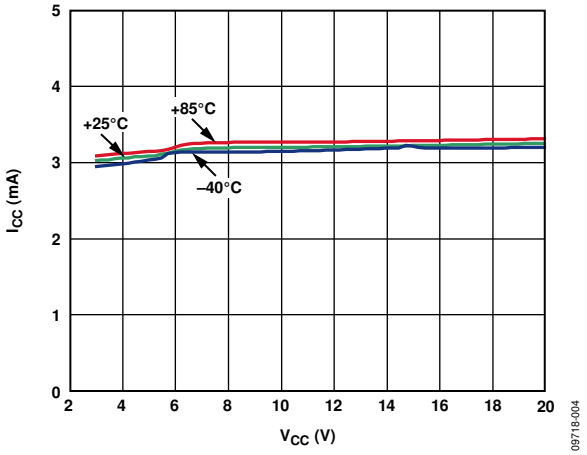

Figure 4. Supply Current (I_{CC}) vs. Supply Voltage (V_{CC})

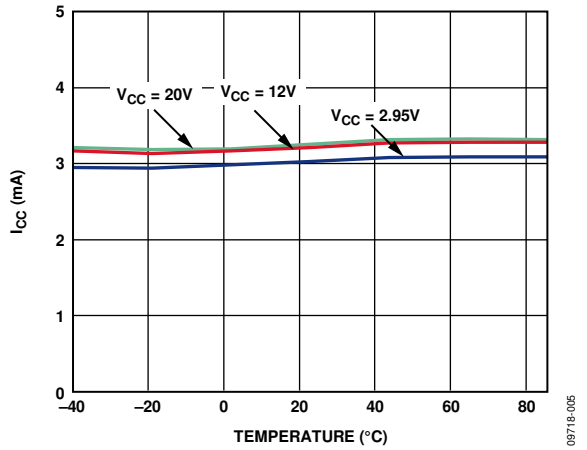

Figure 5. Supply Current (I_{CC}) vs. Temperature

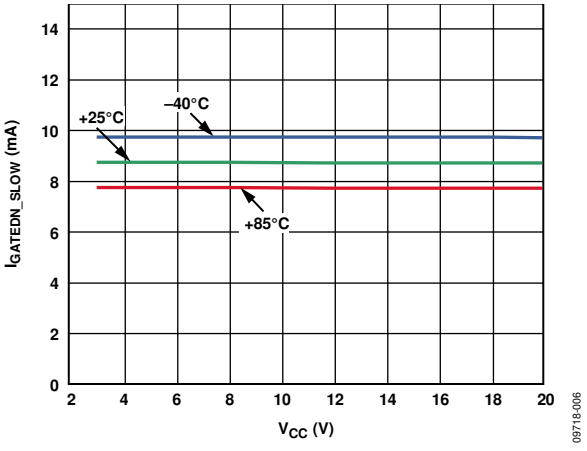

Figure 6. Gate Pull-Down Current (I_{GATEDN_SLOW}) vs. Supply Voltage (V_{CC})

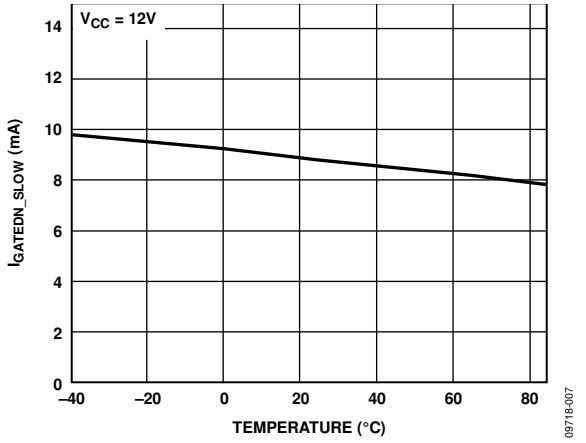

Figure 7. Gate Pull-Down Current (I_{GATEDN_SLOW}) vs. Temperature

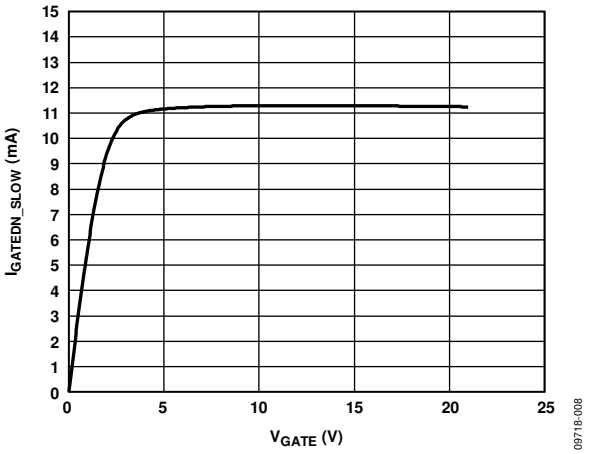

Figure 8. Gate Pull-Down Current (I_{GATEDN_SLOW}) vs. Gate Voltage (V_{GATE})

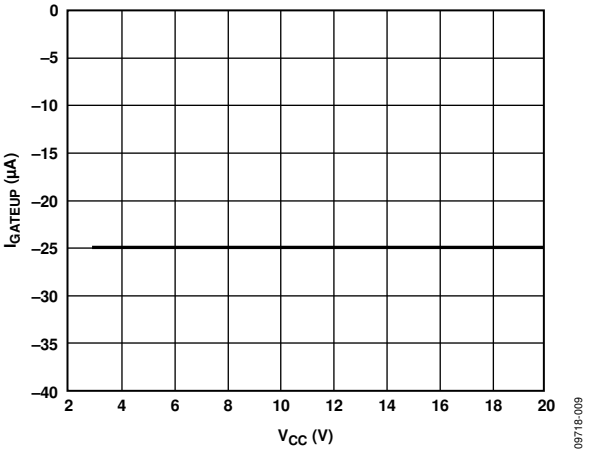

Figure 9. Gate Pull-Up Current (I_{GATEUP}) vs. Supply Voltage (V_{CC})

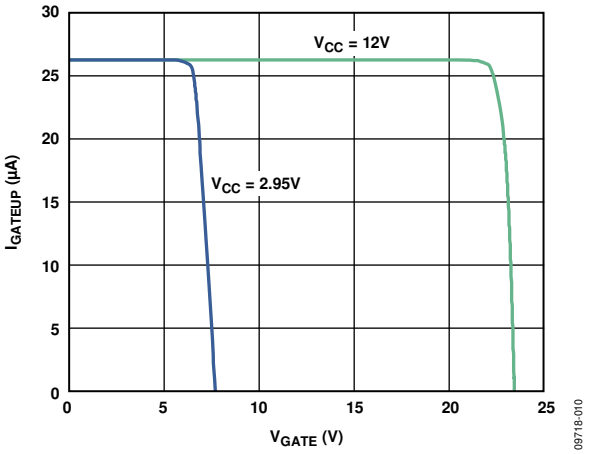

Figure 10. Gate Pull-Up Current (I_{GATEUP}) vs. Gate Voltage (V_{GATE})

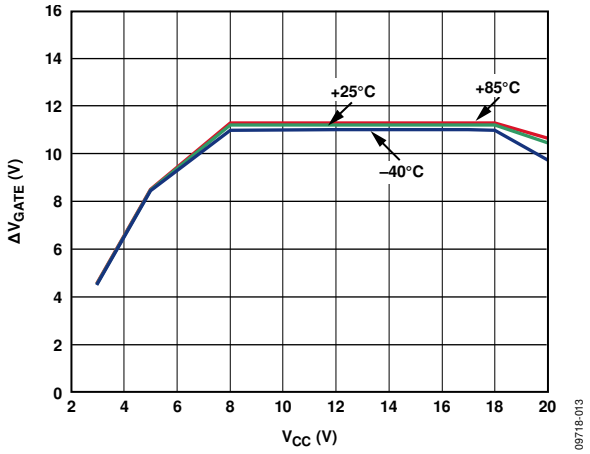

Figure 13. Gate Drive Voltage (ΔV_{GATE}) vs. Supply Voltage (V_{CC}), 5 µA Load

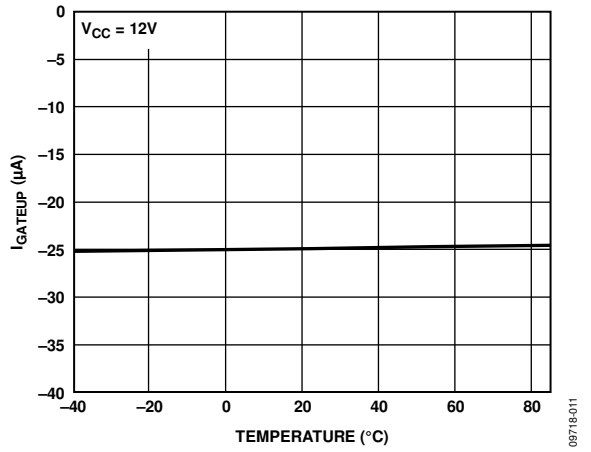

Figure 11. Gate Pull-Up Current (I_{GATEUP}) vs. Temperature

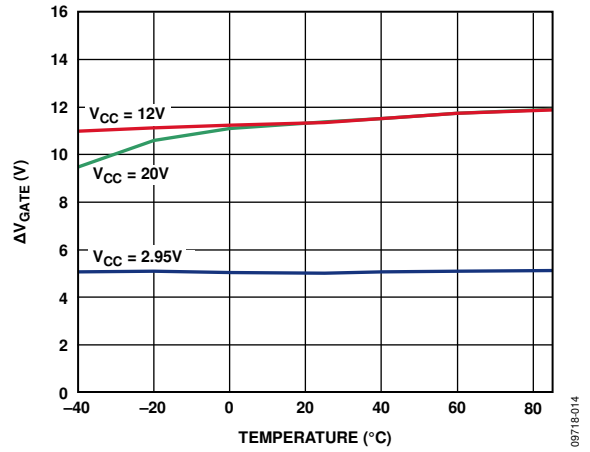

Figure 14. Gate Drive Voltage (ΔV_{GATE}) vs. Temperature, No Load

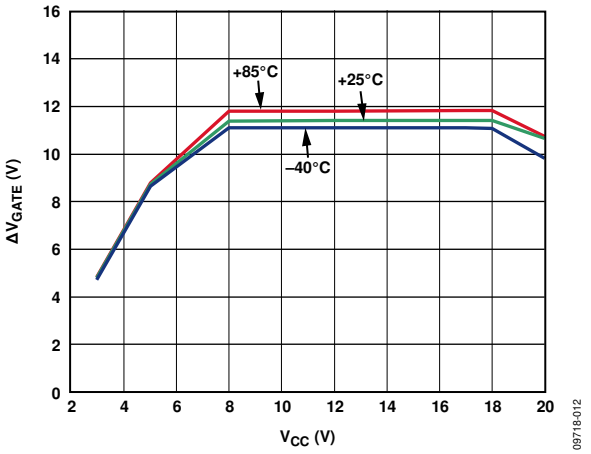

Figure 12. Gate Drive Voltage (ΔV_{GATE}) vs. Supply Voltage (V_{CC}), No Load

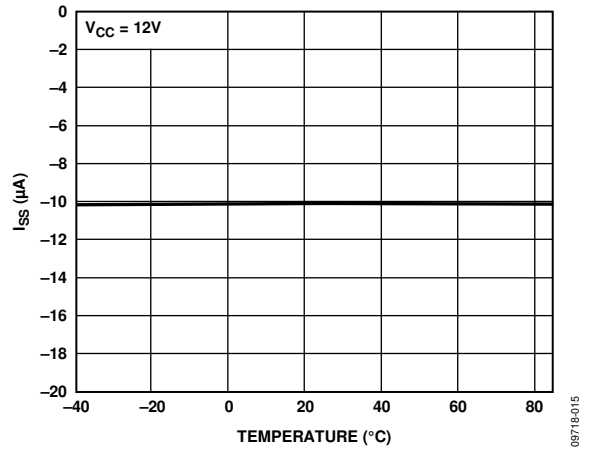

Figure 15. Soft Start Pull-Up Current (I_{SS}) vs. Temperature

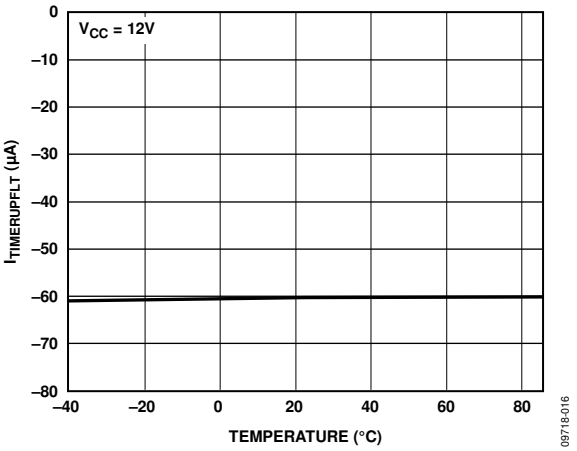

Figure 16. Timer Pull-Up Current, Overcurrent Fault ($I_{TIMERUPFLT}$) vs. Temperature

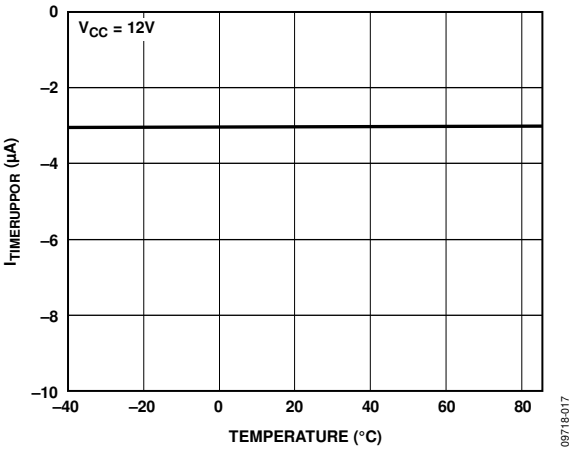

Figure 17. Timer Pull-Up Current, Power-On Reset ($I_{TIMERUPPOR}$) vs. Temperature

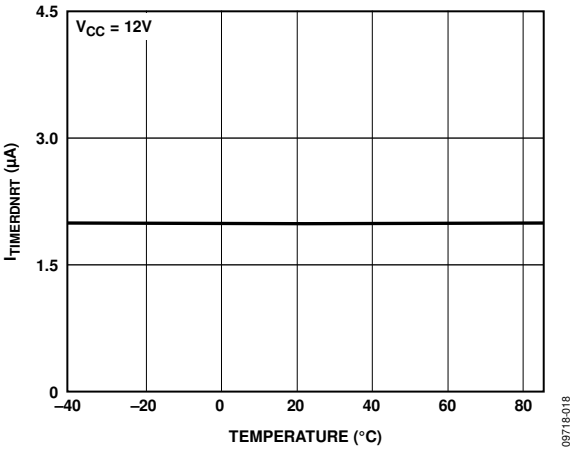

Figure 18. Timer Pull-Down Current, Retry ($I_{TIMERDNRT}$) vs. Temperature

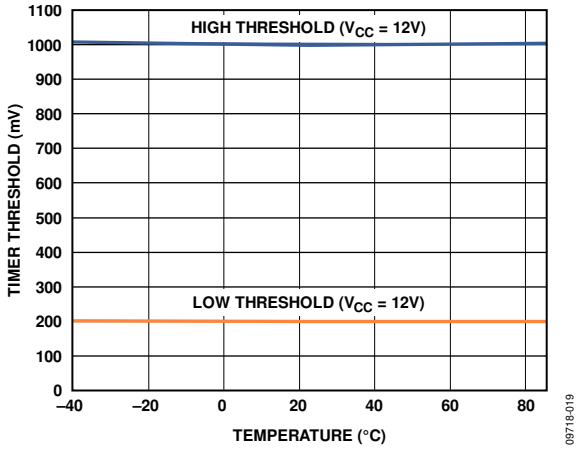

Figure 19. Timer Thresholds vs. Temperature

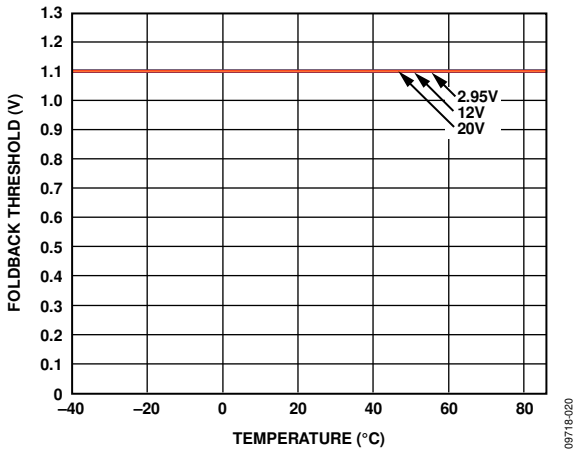

Figure 20. Foldback Threshold vs. Temperature

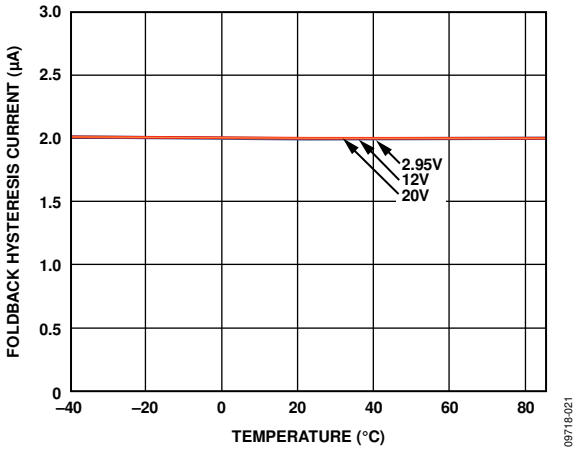

Figure 21. Foldback Hysteresis Current vs. Temperature

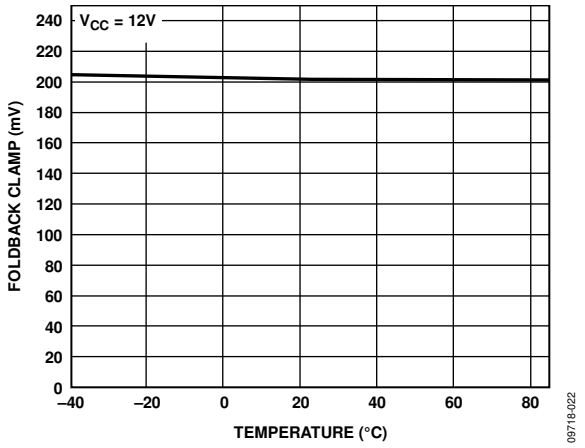

Figure 22. Foldback Clamp vs. Temperature

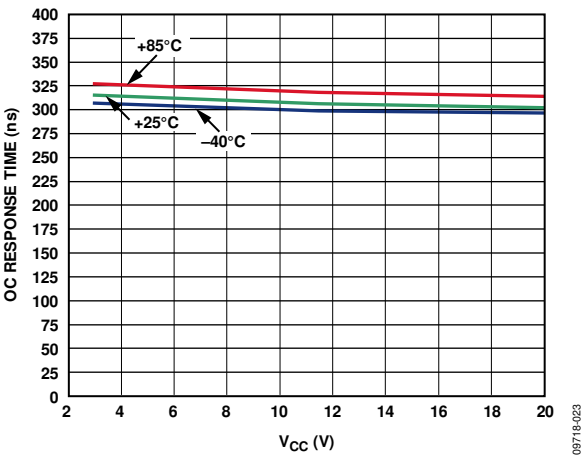

Figure 23. Severe Overcurrent Response Time vs. Supply Voltage (V_{CC}), V_{ISET} = 0.25 V

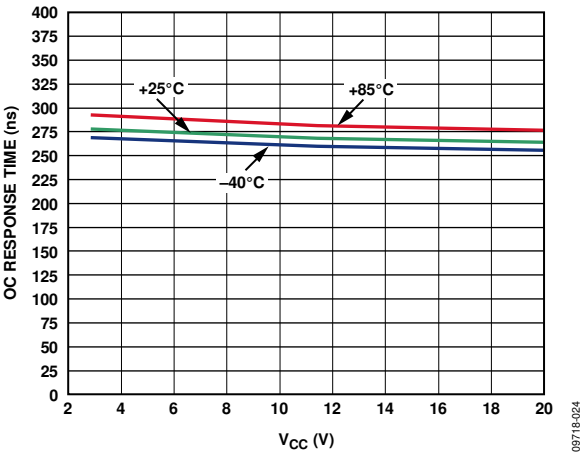

Figure 24. Severe Overcurrent Response Time vs. Supply Voltage (V_{CC}), V_{ISET} = 1 V

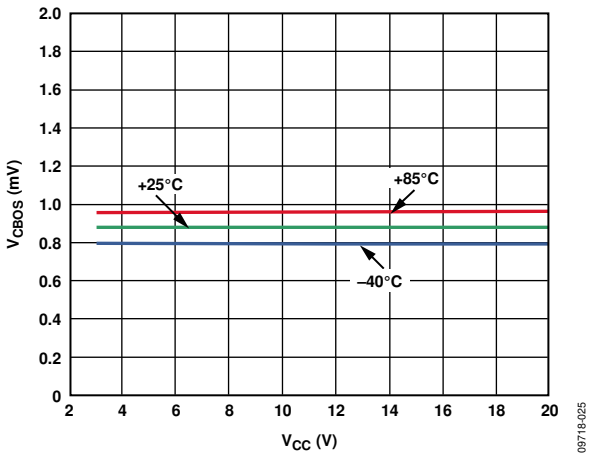

Figure 25. Circuit Breaker Offset (V_{CBOS}) vs. Supply Voltage (V_{CC})

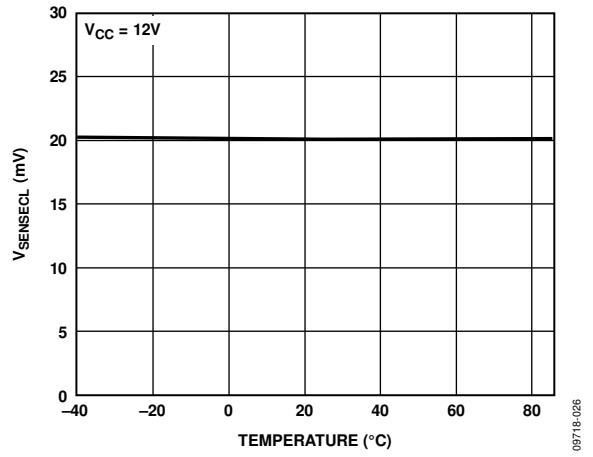

Figure 26. Hot Swap Sense Voltage Current Limit ($V_{SENSECL}$) vs. Temperature

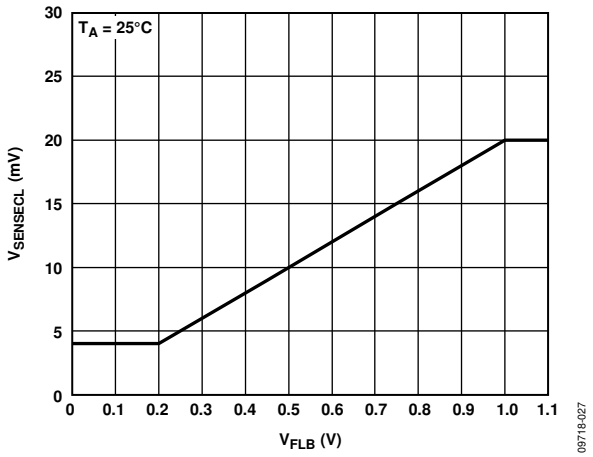

Figure 27. Hot Swap Sense Voltage Current Limit ($V_{SENSECL}$) vs. Foldback Voltage (V_{FLB})

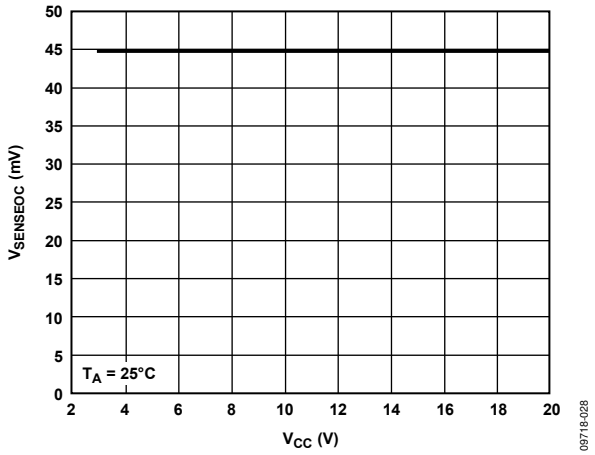

Figure 28. Severe Overcurrent Voltage Threshold ($V_{SENSEOC}$) vs. Supply Voltage (V_{CC}), $V_{ISET} = V_{VCAP}$

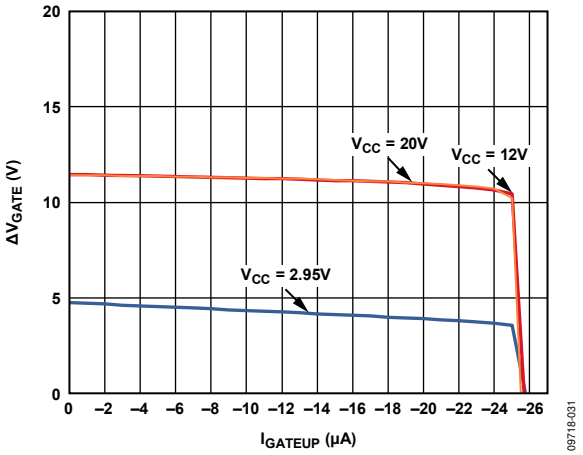

Figure 31. Gate Drive Voltage (ΔV_{GATE}) vs. Gate Pull-Up Current (I_{GATEUP})

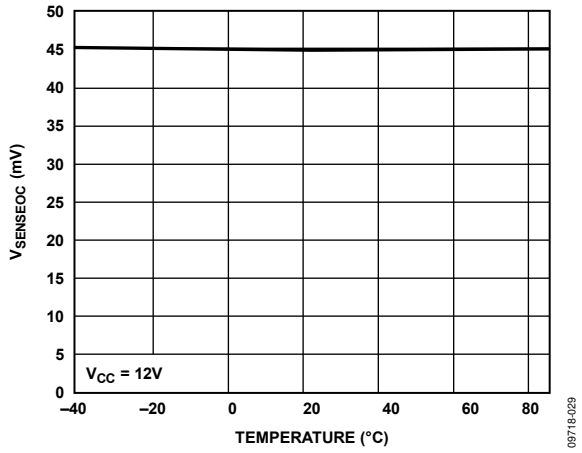

Figure 29. Severe Overcurrent Voltage Threshold ($V_{SENSEOC}$) vs. Temperature, $V_{ISET} = V_{VCAP}$

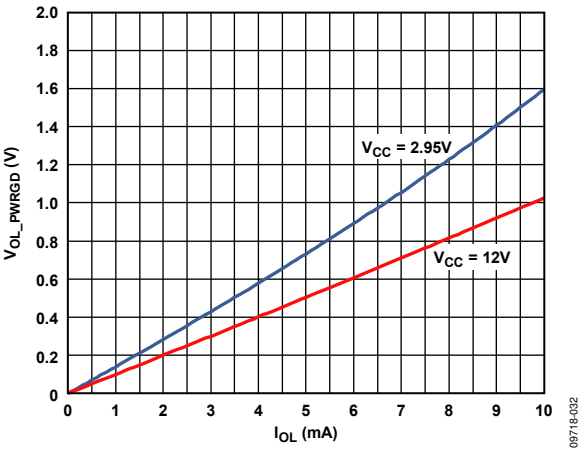

Figure 32. PWRGD Pin, V_{OL} vs. I_{OL}

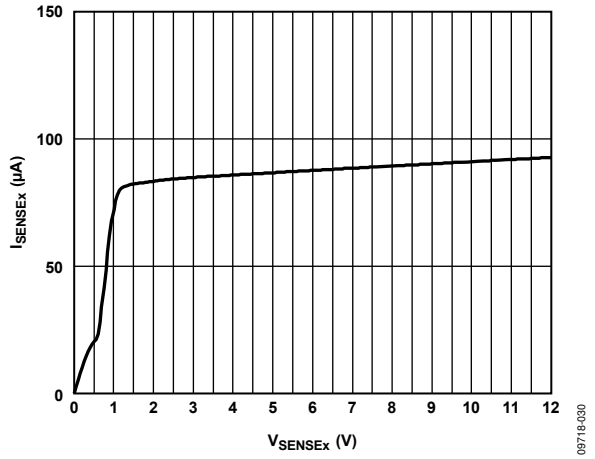

Figure 30. SENSE+/SENSE– Input Current (I_{SENSEx}) vs. Voltage (V_{SENSEx})

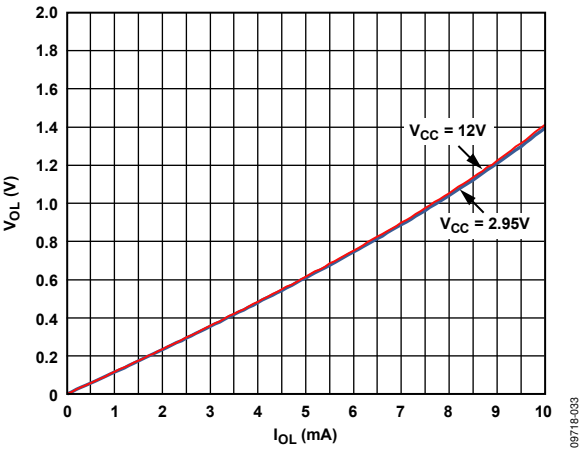

Figure 33. $\overline{LATCH}$ and GPO2/$\overline{ALERT2}$ Digital Outputs, V_{OL} vs. I_{OL}

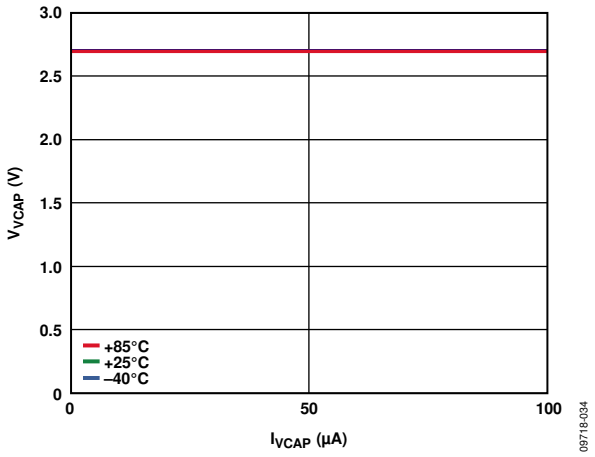

Figure 34. VCAP Voltage (V_{VCAP}) vs. VCAP Load (I_{VCAP})

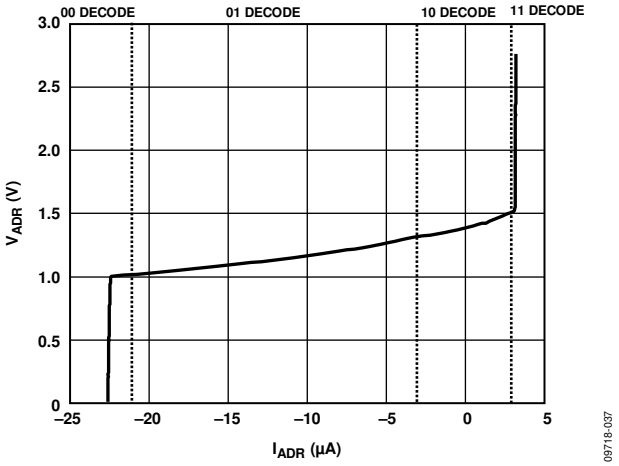

Figure 37. ADR Pin Voltage (V_{ADR}) vs. Current (I_{ADR})

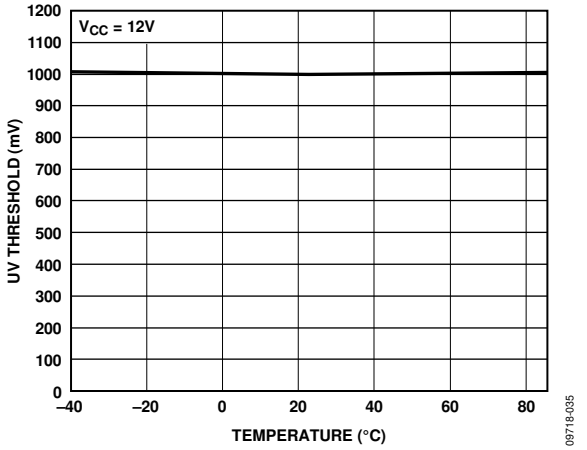

Figure 35. UV Threshold (UV_{TH}) vs. Temperature

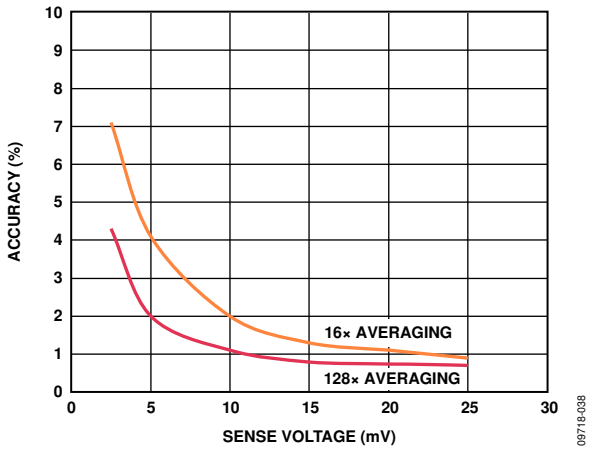

Figure 38. Worst-Case Current Sense Power Monitor Error vs. Current Sense Voltage (V_{SENSE}), 0°C to 65°C, V_{SENSE+} = 12 V

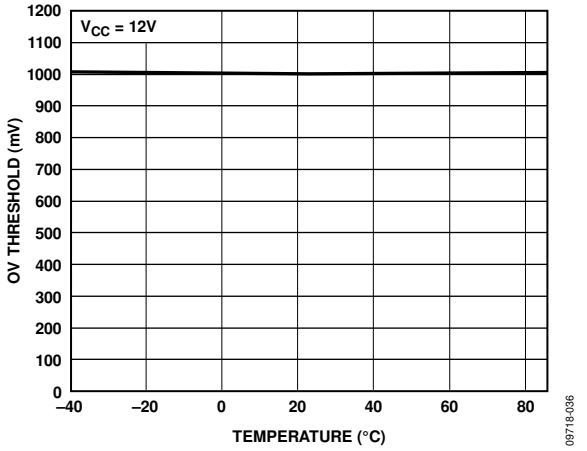

Figure 36. OV Threshold (OV_{TH}) vs. Temperature

TYPICAL APPLICATION CIRCUIT

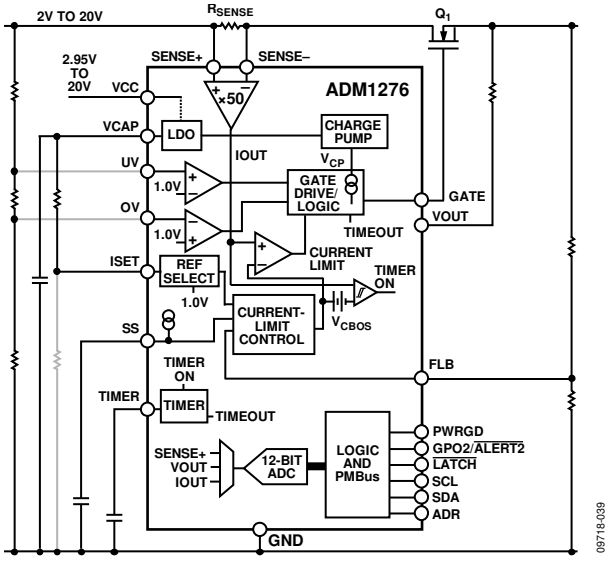

Figure 39. Typical Application Circuit

THEORY OF OPERATION

When circuit boards are inserted into a live backplane, discharged supply bypass capacitors draw large transient currents from the backplane power bus as they charge. These transient currents can cause permanent damage to connector pins, as well as dips on the backplane supply that can reset other boards in the system.

The ADM1276 is designed to control the powering on and off of a system in a controlled manner, allowing a board to be removed from, or inserted into, a live backplane by protecting it from excess currents. The ADM1276 can reside on the backplane or on the removable board.

POWERING THE ADM1276

A supply voltage from 2.95 V to 20 V is required to power the ADM1276 via the VCC pin. The VCC pin provides the majority of the bias current for the device; the remainder of the current needed to control the gate drive and best regulate the V_{GS} voltage is supplied by the SENSE+ pin.

To ensure correct operation of the ADM1276, the voltage on the VCC pin must be greater than or equal to the voltage on the SENSE+ pin. No sequencing of the VCC and SENSE+ rails is necessary. The SENSE+ pin can be as low as 2 V for normal operation provided that a voltage of at least 2.95 V is connected to the VCC pin. In most applications, both the VCC and SENSE+ pins are connected to the same voltage rail, but they are connected via separate traces to prevent accuracy loss in the sense voltage measurement (see Figure 40).

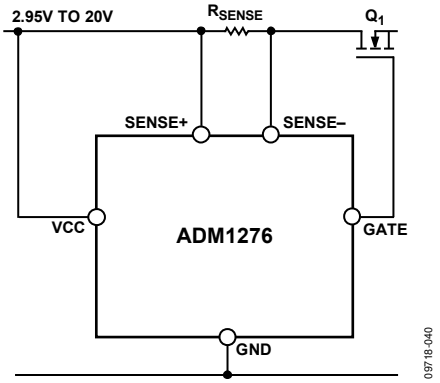

Figure 40. Powering the ADM1276

To protect the ADM1276 from unnecessary resets due to transient supply glitches, an external resistor and capacitor can be added, as shown in Figure 41. Choose the values of these components so as to provide a time constant that can filter any expected glitches. The resistor should, however, be small enough to keep voltage drops due to quiescent current to a minimum. Unless a resistor is used to limit the inrush current, do not place a supply decoupling capacitor on the rail before the FET.

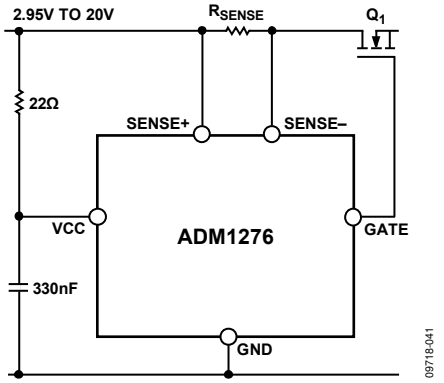

Figure 41. Transient Glitch Protection Using an RC Network

CURRENT SENSE INPUTS

The load current is monitored by measuring the voltage drop across an external sense resistor, R_{SENSE} (see Figure 42). An internal current sense amplifier provides a gain of 50 to the voltage drop detected across R_{SENSE}. The result is compared to an internal reference and used by the hot swap control logic to detect when an overcurrent condition occurs.

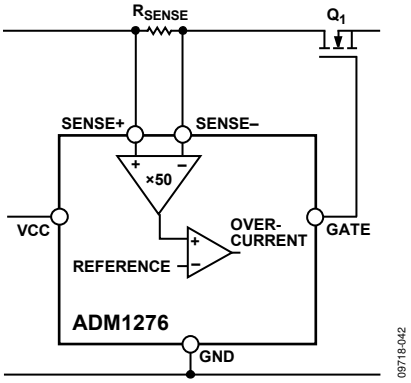

Figure 42. Hot Swap Current Sense Amplifier

The SENSE± inputs may be connected to multiple parallel sense resistors, which can affect the voltage drop detected by the ADM1276. The current flowing through the sense resistors creates an offset, resulting in reduced accuracy.

To achieve better accuracy, the averaging resistors sum the current from the nodes of each sense resistor, as shown in Figure 43. The typical value for the averaging resistors is 10 Ω. The averaging resistors are chosen to balance the input current to both sense pins to within 5 μA. This ensures that the same offset is seen by both sense inputs.

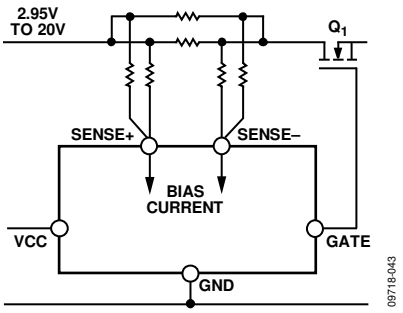

Figure 43. Connection of Multiple Sense Resistors to the SENSE± Pins

CURRENT-LIMIT REFERENCE

The current-limit reference voltage determines the load current level to which the ADM1276 limits the current during an overcurrent event. This reference voltage is compared to the gained-up current sense voltage to determine whether the limit is reached.

An internal current-limit reference selector block continuously compares the ISET, soft start, and foldback voltages to determine which voltage is the lowest at any given time; the lowest voltage is used as the current-limit reference. This ensures that the programmed current limit, ISET, is used in normal operation, and that the soft start and foldback features reduce the current limit when required during startup and/or fault conditions.

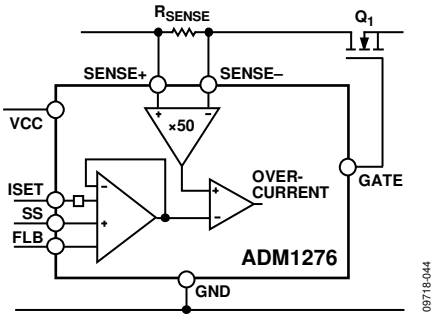

Figure 44. Current-Limit Reference Selection

The foldback and soft start voltages vary during different modes of operation and are, therefore, clamped to minimum levels of 200 mV and 100 mV, respectively, to prevent zero current flow due to the current limit being too low. Figure 45 provides an example of how the soft start, foldback, and ISET voltages interact during startup as the ADM1276 is enhancing the FET and charging the load capacitances. Depending on how the soft start and foldback features are configured, the hand-off point can vary to ensure that the FET is being operated within the correct limits.

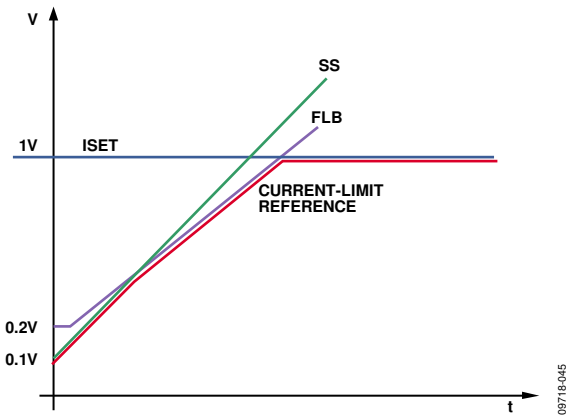

Figure 45. Interaction of Soft Start, Foldback, and ISET Current Limits

SETTING THE CURRENT LIMIT (ISET)

The maximum current limit is partially determined by selecting a sense resistor to match the current sense voltage limit on the controller for the desired load current. However, as currents become larger, the sense resistor requirements become smaller, and resolution can be difficult to achieve when selecting the appropriate sense resistor. The ADM1276 provides an adjustable current sense voltage limit to handle this issue. The device allows the user to program the required current sense voltage limit from 5 mV to 25 mV.

The default value of 20 mV is achieved by connecting the ISET pin directly to the VCAP pin. This configures the device to use an internal 1 V reference, which equates to 20 mV at the sense inputs (see Figure 46).

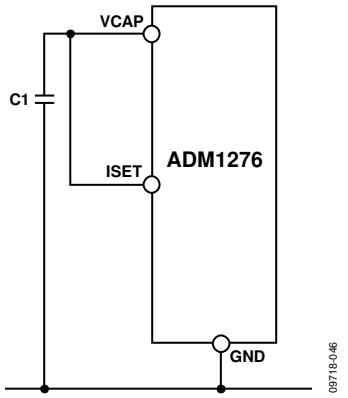

Figure 46. Fixed 20 mV Current Sense Limit

To program the sense voltage from 5 mV to 25 mV, a resistor divider is used to set a reference voltage on the ISET pin (see Figure 47).

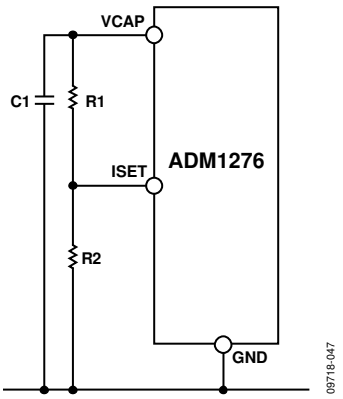

Figure 47. Adjustable 5 mV to 25 mV Current Sense Limit

The VCAP pin has a 2.7 V internal generated voltage that can be used to set a voltage at the ISET pin. Assuming that V_{ISET} equals the voltage on the ISET pin, size the resistor divider to set the ISET voltage as follows:

$$V_{ISET} = V_{SENSE} \times 50$$

where V_{SENSE} is the current sense voltage limit.

The VCAP rail can also be used as the pull-up supply for setting the I²C address. Do not use the VCAP pin for any other purpose. To guarantee accuracy specifications, do not load the VCAP pin by more than 100 µA.

SOFT START

A capacitor connected to the SS pin determines the inrush current profile. Before the FET is enabled, the output voltage of the current-limit reference selector block is clamped at 100 mV. This, in turn, holds the hot swap sense voltage current limit, $V_{SENSECL}$, at approximately 2 mV. When the FET receives a request to turn on, the SS pin is held at ground until the voltage between the SENSE+ and SENSE− pins (V_{SENSE}) reaches the circuit breaker voltage, V_{CB}.

$$V_{CB} = V_{SENSECL} - V_{CBOS}$$

where V_{CBOS} is typically 0.88 mV, making V_{CB} = 1.12 mV.

When the load current generates a sense voltage equal to V_{CB}, a 10 µA current source is enabled, which charges the SS capacitor and results in a linear ramping voltage on the SS pin. The current-limit reference also ramps up accordingly, allowing the regulated load current to ramp up while avoiding sudden transients during power-up. The SS capacitor value is given by

$$C_{SS} = \frac{I_{SS} \times t}{V_{ISET}}$$

where:
I_{SS} = 10 µA.
t = SS ramp time.

For example, a 10 nF capacitor gives a soft start time of 1 ms.

Note that the SS voltage may intersect with the FLB (foldback) voltage, and the current-limit reference may change to follow FLB (see Figure 45). This change has minimal impact on startup because the output voltage rises at a similar rate to the SS voltage.

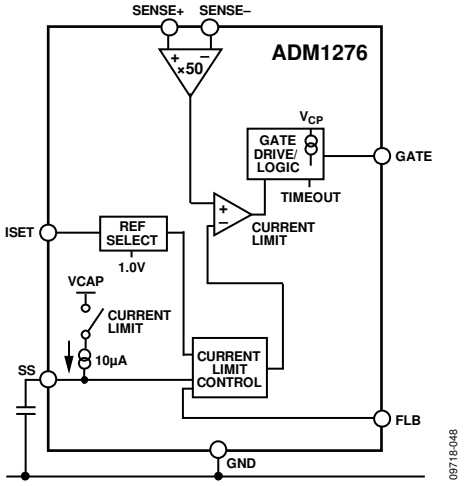

Figure 48. Soft Start

FOLDBACK

Foldback is a method to actively reduce the current limit as the voltage drop across the FET increases. It keeps the power across the FET to a minimum during power-up, overcurrent, or short-circuit events. It also avoids the need to oversize the FET to accommodate worst-case conditions, resulting in board size and cost savings.

The ADM1276 detects the voltage drop across the FET by looking at a resistor divided version of the output voltage. It is assumed that the supply voltage remains constant and within tolerance. The device, therefore, relies on the principle that the drain of the FET is at the maximum expected supply voltage, and that the magnitude of the output voltage is relative to that of the V_{DS} of the FET. Using a resistor divider from the output voltage to the FLB pin, a relationship from V_{OUT}, and thus V_{DS}, to V_{FLB} can be derived.

Design the resistor divider to output a voltage equal to ISET when V_{OUT} falls below the desired level. This should be well below the working tolerance of the supply rail. As V_{OUT} continues to drop, the current-limit reference follows V_{FLB} because it is now the lowest voltage input to the current-limit reference selector block. This results in a reduction of the current limit and, therefore, the regulated load current. To prevent complete current flow restriction, a clamp becomes active when the current-limit reference reaches 200 mV. The current limit cannot drop below this level.

To suit the SOA characteristics of a particular FET, the required minimum current for this clamp varies from design to design. However, the current-limit reference fixes this clamp at 200 mV, which equates to 4 mV at the sense resistor. Therefore, the main ISET voltage can be adjusted to align this clamp to the required percentage current reduction. For example, if ISET equals 0.8 V, the clamp can be set at 25% of the maximum current.

TIMER

The TIMER pin handles several timing functions with an external capacitor, C_{TIMER}. The two comparator thresholds are V_{TIMERL} (0.2 V) and V_{TIMERH} (1 V). There are four timing current sources: a 3 µA pull-up, a 60 µA pull-up, a 2 µA pull-down, and a 100 µA pull-down.

These current and voltage levels, together with the value of C_{TIMER} chosen by the user, determine the initial timing cycle time, the fault current-limit time, and the hot swap retry duty cycle. The TIMER pin capacitor value is determined using the following equation:

$$C_{TIMER} = (t_{ON} \times 60\ \mu A)/V_{TIMERH}$$

where t_{ON} is the time that the FET is allowed to spend in regulation at the set current limit.

The choice of FET is based on matching this time with the SOA requirements of the FET. Foldback can be used to simplify the selection.

When VCC is connected to the backplane supply, the internal supply of the ADM1276 must be charged up. In a very short time, the internal supply is fully charged up and, because the undervoltage lockout (UVLO) voltage is exceeded at VCC, the device emerges from reset. During this first short reset period, the GATE and TIMER pins are both held low.

The ADM1276 then goes through an initial timing cycle. The TIMER pin is pulled high with 3 µA. When the TIMER pin reaches the V_{TIMERH} threshold (1.0 V), the first portion of the initial timing cycle is complete. The 100 µA current source then pulls down the TIMER pin until it reaches V_{TIMERL} (0.2 V). The initial timing cycle duration is related to C_{TIMER} by the following equation:

$$t_{INITIAL} = \frac{V_{TIMERH} \times C_{TIMER}}{3\ \mu A} + \frac{(V_{TIMERH} - V_{TIMERL}) \times C_{TIMER}}{100\ \mu A}$$

For example, a 100 nF capacitor results in a delay of approximately 34 ms. If the UV and OV inputs indicate that the supply is within the defined window of operation when the initial timing cycle terminates, the device is ready to start a hot swap operation.

When the voltage across the sense resistor reaches the circuit breaker trip voltage, V_{CB}, the 60 µA timer pull-up current is activated, and the gate begins to regulate the current at the current limit. This initiates a ramp-up on the TIMER pin. If the sense voltage falls below this circuit breaker trip voltage before the TIMER pin reaches V_{TIMERH}, the 60 µA pull-up is disabled and the 2 µA pull-down is enabled.

The circuit breaker trip voltage is not the same as the hot swap sense voltage current limit. There is a small circuit breaker offset, V_{CBOS}, which means that the timer actually starts a short time before the current reaches the defined current limit.

However, if the overcurrent condition is continuous and the sense voltage remains above the circuit breaker trip voltage, the 60 µA pull-up remains active and the FET remains in regulation.

This allows the TIMER pin to reach V_{TIMERH} and initiate the GATE shutdown. On the ADM1276, the $\overline{LATCH}$ pin is pulled low immediately.

In latch-off mode, the TIMER pin is switched to the 2 µA pull-down when it reaches the V_{TIMERH} threshold. The $\overline{LATCH}$ pin remains low. While the TIMER pin is being pulled down, the hot swap controller remains off and cannot be turned back on.

When the voltage on the TIMER pin goes below the V_{TIMERL} threshold, the hot swap controller can be reenabled by toggling the UV pin or by using the PMBus OPERATION command to toggle the on bit from on to off and then on again.

HOT SWAP RETRY DUTY CYCLE

The ADM1276 turns off the FET after an overcurrent fault and then uses the capacitor on the TIMER pin to provide a delay before automatically retrying the hot swap operation. To configure the ADM1276 for autoretry mode, the $\overline{LATCH}$ pin is tied to either the UV pin or to the ENABLE pin. Note that a pull-up resistor is required on the $\overline{LATCH}$ pin.

When an overcurrent fault occurs, the capacitor on the TIMER pin is charged with a 60 µA pull-up current. When the TIMER pin reaches V_{TIMERH}, the GATE pin is pulled down. When the $\overline{LATCH}$ pin is tied to the UV pin or the ENABLE pin for autoretry mode, the TIMER pin is pulled down with a 2 µA current sink. When the TIMER pin reaches V_{TIMERL} (0.2 V), it automatically restarts the hot swap operation.

The duty cycle of this automatic retry cycle is set by the ratio of 2 µA/60 µA, which approximates to being on about 4% of the time. The value of the timer capacitor determines the on time of this cycle, which is calculated as follows:

$$t_{ON} = V_{TIMERH} \times (C_{TIMER}/60\ \mu A)$$

$$t_{OFF} = (V_{TIMERH} - V_{TIMERL}) \times (C_{TIMER}/2\ \mu A)$$

A 100 nF capacitor on the TIMER pin gives an on time of 1.67 ms and an off time of 40 ms. The device retries indefinitely in this manner and can be disabled manually by holding the UV or ENABLE pin low, or by disconnecting the $\overline{LATCH}$ pin. To prevent thermal stress, an RC network can be used to extend the retry time to any desired level.

FET GATE DRIVE CLAMPS

The charge pump used on the GATE pin is capable of driving the pin to $V_{CC} + (2 \times V_{CC})$, but it is clamped to less than 14 V above the SENSE± pins and less than 31 V. These clamps ensure that the maximum V_{GS} rating of the FET is not exceeded.

FAST RESPONSE TO SEVERE OVERCURRENT

The ADM1276 features a separate high bandwidth current sense amplifier that is used to detect a severe overcurrent that is indicative of a short-circuit condition. A fast response time allows the ADM1276 to handle events of this type that could otherwise cause catastrophic damage if not detected and acted on very quickly. The fast response circuit ensures that the ADM1276 can detect an overcurrent event at approximately 200% to 250% of the normal current limit (ISET) and can respond to and control the current within 1 µs, in most cases.

UNDERVOLTAGE AND OVERVOLTAGE

The ADM1276 monitors the supply voltage for undervoltage (UV) and overvoltage (OV) conditions. The UV and OV pins are connected to the input of an internal voltage comparator, and its voltage level is internally compared with a 1 V voltage reference.

Figure 49 illustrates the voltage monitoring input connections. An external resistor network divides the supply voltage for monitoring. An undervoltage event is detected when the voltage connected to the UV pin falls below 1 V, and the gate is shut down using the 10 mA pull-down device. Similarly, when an overvoltage event occurs and the voltage on the OV pin exceeds 1 V, the gate is shut down using the 10 mA pull-down device.

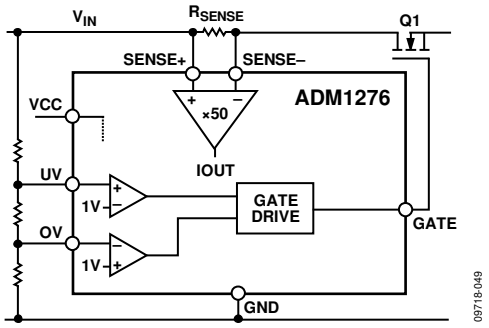

Figure 49. Undervoltage and Overvoltage Supply Monitoring

ENABLE INPUT

The ADM1276 provides a dedicated ENABLE digital input pin. The ENABLE pin allows the ADM1276 to remain off by using a hardware signal, even when the voltage on the UV pin is above 1.0 V and the voltage on the OV pin is less than 1.0 V. Although the UV pin can be used to provide a digital enable signal, using the ENABLE pin for this purpose means that the ability to monitor for undervoltage conditions is not lost.

In addition to the conditions for the UV and OV pins, the ADM1276 ENABLE input pin must be high for the device to begin a power-up sequence.

A similar function can be achieved using the UV pin directly. Alternatively, if the UV divider function is still required, the configuration shown in Figure 50 can be used.

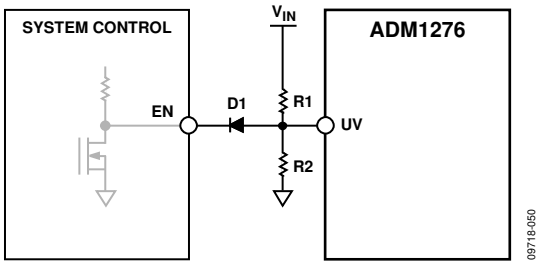

Figure 50. Using the UV Pin as an Enable

Diode D1 prevents the external driver pull-up from affecting the UV threshold. Select Diode D1 using the following criteria:

$$(V_F \times D1) + (V_{OL} \times EN) << 1.0\ \text{V}\ (I_F = V_{IN}/R1)$$

Ensure that the EN sink current does not exceed the specified V_{OL} value. If the open-drain device has no pull-up, the diode is not required.

POWER GOOD

The power good (PWRGD) output can be used to indicate whether the output voltage is above a user-defined threshold and can, therefore, be considered good. The PWRGD output is derived using the FLB resistor network, composed of R1 and R2 (see Figure 51).

The PWRGD pin is an open-drain output that pulls low when the voltage at the FLB pin is lower than 1.1 × V_{ISET} (power bad). When the voltage at the FLB pin is above this threshold (indicating that the output voltage has risen), the open-drain pull-down is disabled, allowing PWRGD to be pulled high. PWRGD is guaranteed to be in a valid state for VCC ≥ 1 V.

Hysteresis on the FLB pin is provided by a 2 µA internal current source that is switched on when the V_{FLB} input voltage exceeds the input threshold. The current source is disconnected when V_{OUT} drops below the foldback threshold voltage minus the hysteresis voltage. Resistor R3 is internal to the ADM1276. The hysteresis voltage at the FLB pin can be varied by adjusting the parallel combination of Resistor R1 and Resistor R2.

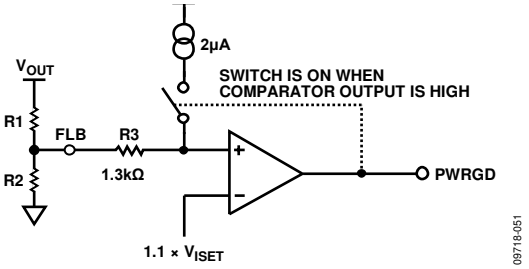

Figure 51. Generation of PWRGD Signal

VOUT MEASUREMENT

The VOUT pin on the ADM1276 can be used to provide an alternate voltage for the power monitor to measure. The user can choose to measure the voltage at the SENSE+ pin or the voltage at the VOUT pin, using either the low or high input voltage range.

If the VOUT pin is to be used to measure the output voltage after the FET, insert a 1 kΩ resistor in series between the source of the FET and the VOUT pin. This resistor provides some separation between the ADM1276 and the FET source during a fault condition; thus, ADM1276 operation is not affected.

FET HEALTH

The ADM1276 provides a method of detecting a shorted pass FET. The FET health status can be used to generate an alert on the GPO2/$\overline{\text{ALERT2}}$ pin. By default at power-up, an alert is generated on the GPO2/$\overline{\text{ALERT2}}$ pin of the ADM1276 when the FET health status indicates that a bad FET is present. FET health is considered bad if all of the following conditions are true:

- The ADM1276 is holding the FET off, for example, during the initial power-on cycle time.
- V_{SENSE} > 2 mV.
- V_{GATE} < ~1 V, that is, less than the FET gate threshold.

POWER MONITOR

The ADM1276 features an integrated ADC that accurately measures the current sense voltage, the input voltage, and (optionally) the output voltage. The measured input voltage and current being delivered to the load are multiplied to give a power value that can be read back. Each power value is also added to an accumulator that can be read back to allow an external device to calculate the energy consumption of the load.

The ADM1276 can report the measured current, input voltage, and the output voltage. The PEAK_IOUT, PEAK_VIN, and PEAK_VOUT commands can be used to read the highest peak current or voltage since the value was last cleared.

An averaging function is provided for voltage and current that allows a number of samples to be averaged by the ADM1276. This function reduces the need for postprocessing of sampled data by the host processor. The number of samples that can be averaged is 2^N, where N is in the range of 0 to 7.

The power monitor current sense amplifier is bipolar and can measure both positive and negative currents. The power monitor amplifier has an input range of ±25 mV.

Two input voltage ranges are available and can be selected using the PMBus interface: 0 V to 6 V (low input range) and 0 V to 20 V (high input range).

The two basic modes of operation for the power monitor are single shot and continuous. In single shot mode, the power monitor samples the input voltage and current a number of times, depending on the averaging value selected by the user. The ADM1276 returns a single value corresponding to the average voltage and current measured. When configured for continuous mode, the power monitor continuously samples voltage and current, making the most recent sample available to be read.

The single shot mode can be triggered in a number of ways. The simplest is by selecting the single shot mode using the PMON_CONFIG command and writing to the convert bit using the PMON_CONTROL command. The convert bit can also be written as part of a PMBus group command. Using a group command allows multiple devices to be written to as part of the same I^2C bus transaction, with all devices executing the command when the stop condition appears on the bus. In this way, several devices can be triggered to sample at the same time.

Each time a current sense and input voltage measurements are taken, a power calculation is performed, multiplying the two measurements together. This can be read from the device using the READ_PIN command, returning the input power.

At the same time, the calculated power value is added to a power accumulator register, that may increment a rollover counter if the value exceeds the maximum accumulator value, and that also increments a power sample counter.

The power accumulator and power sample counter are read using the same READ_EIN command to ensure that the accumulated value and sample count are from the same point in time. The bus host reading the data assigns a timestamp to when the data is read. By calculating the time difference between consecutive uses of READ_EIN, and determining the delta in power consumed, it is possible for the host to determine the total energy consumed over that period.

PMBus INTERFACE

The I²C bus is a common, simple serial bus used by many devices to communicate. It defines the electrical specifications, the bus timing, the physical layer, and some basic protocol rules.

SMBus is based on I²C and aims to provide a more robust and fault tolerant bus. Functions such as bus timeout and packet error checking are added to help achieve this robustness, along with more specific definitions of the bus messages used to read and write data to devices on the bus.

PMBus is layered on top of SMBus and, in turn, on I²C. Using the SMBus defined bus messages, PMBus defines a set of standard commands that can be used to control a device that is part of a power chain.

The ADM1276 command set is based upon the *PMBus™ Power System Management Protocol Specification*, Part I and Part II, Revision 1.2. This version of the standard is intended to provide a common set of commands for communicating with dc-to-dc type devices. However, many of the standard PMBus commands can be mapped directly to the functions of a hot swap controller.

Part I and Part II of the PMBus standard describe the basic commands and how they can be used in a typical PMBus setup. The following sections describe how the PMBus standard and the ADM1276 specific commands are used.

DEVICE ADDRESSING

The ADM1276 is available in one model: the ADM1276-3. The PMBus address is 7 bits in size. The upper 5 bits (MSBs) of the address word are fixed. The base address for the ADM1276 is 01000xx (0x20).

The ADM1276 has a single ADR pin that is used to select one of four possible addresses. The ADR pin connection selects the lowest two bits (LSBs) of the 7-bit address word (see Table 6).

Table 6. PMBus Addresses and ADR Pin Connection

Value of Address LSBs	ADR Pin Connection
00	Connect to GND
01	150 kΩ resistor to GND
10	No connection (floating)
11	Connect to VCAP

SMBus PROTOCOL USAGE

All I²C transactions on the ADM1276 are done using SMBus defined bus protocols. The following SMBus protocols are implemented by the ADM1276:

- Send byte
- Receive byte
- Write byte
- Read byte
- Write word
- Read word
- Block read

PACKET ERROR CHECKING

The ADM1276 PMBus interface supports the use of the packet error checking (PEC) byte that is defined in the SMBus standard. The PEC byte is transmitted by the ADM1276 during a read transaction or sent by the bus host to the ADM1276 during a write transaction. The ADM1276 supports the use of PEC with all the SMBus protocols that it implements.

The use of the PEC byte is optional. The bus host can decide whether to use the PEC byte with the ADM1276 on a message-by-message basis. There is no need to enable or disable PEC in the ADM1276.

The PEC byte is used by the bus host or the ADM1276 to detect errors during a bus transaction, depending on whether the transaction is a read or a write. If the host determines that the PEC byte read during a read transaction is incorrect, it can decide to repeat the read if necessary. If the ADM1276 determines that the PEC byte sent during a write transaction is incorrect, it ignores the command (does not execute it) and sets a status flag.

Within a group command, the host can choose to send or not send a PEC byte as part of the message to the ADM1276.

PARTIAL TRANSACTIONS ON I²C BUS

In the event of a specific sequence of events occurring on the I²C bus, it is possible for the I²C interface on the device to go into a state where it will fail to acknowledge the next I²C transaction directed to it. There are two ways that this behavior can be triggered:

- A partial I²C transaction consisting of a start condition, followed by a single SCL clock pulse and stop condition.
- If the I²C bus master does not follow the 300 ns SDA data hold time when signaling the ACK/NACK bit at the end of a transaction. The device sees this as a single SCL clock partial transaction.

In the event that the device does not acknowledge a transaction, then the I²C interface on the device can be reset by sending a series of up to 16 SCL clock pulses, or performing a dummy transaction to another I²C address on the bus.