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Hot Swap Controller and Digital Power and Energy Monitor with PMBus Interface

Data Sheet **ADM1278**

FEATURES

- ±0.3% accurate, 12-bit ADC for I_{OUT}, V_{IN}, V_{OUT}, and temperature
- 320 ns response time to short circuit
- Shutdown on detection of FET health fault
- Constant power foldback for tighter FET SOA protection
- Remote temperature sensing with programmable warning and shutdown thresholds
- Resistor-programmable 5 mV to 25 mV V_{SENSE} current limit
- Programmable start-up current limit
- 1% accurate UV, OV, and PWRGD thresholds
- Split hot swap and power monitor inputs to allow additional external ADC filtering
- Reports power and energy consumption over time
- Peak detect registers for current, voltage, and power
- PROCHOT power throttling capability
- PMBus fast mode compliant interface
- 5 mm × 5 mm, 32-lead LFCSP

APPLICATIONS

- Servers
- Power monitoring and control/power budgeting
- Telecommunication and data communication equipment

GENERAL DESCRIPTION

The ADM1278 is a hot swap controller that allows a circuit board to be removed from or inserted into a live backplane. It also features current, voltage, power, and temperature readback via an integrated 12-bit analog-to-digital converter (ADC), accessed using a PMBus™ interface. The load current is measured using an internal current sense amplifier that measures the voltage across a sense resistor in the power path via the HS+ and HS− pins. A default current limit of 20 mV is set, but this limit can be adjusted, if required.

The ADM1278 limits the current through the sense resistor by controlling the gate voltage of an external N-channel FET in the power path, via the GATE pin. The sense voltage, and therefore the load current, is maintained below the preset maximum. The ADM1278 protects the external FET by limiting the time that the FET remains on while the current is at its maximum value. This current-limit time is set by the choice of capacitor connected to the TIMER pin. In addition, a constant power foldback scheme is used to control the power dissipation in the MOSFET during power-up and fault conditions. The level of this power, along with the TIMER regulation time, can be set to ensure that the MOSFET remains within safe operating area (SOA) limits.

TYPICAL APPLICATION CIRCUIT

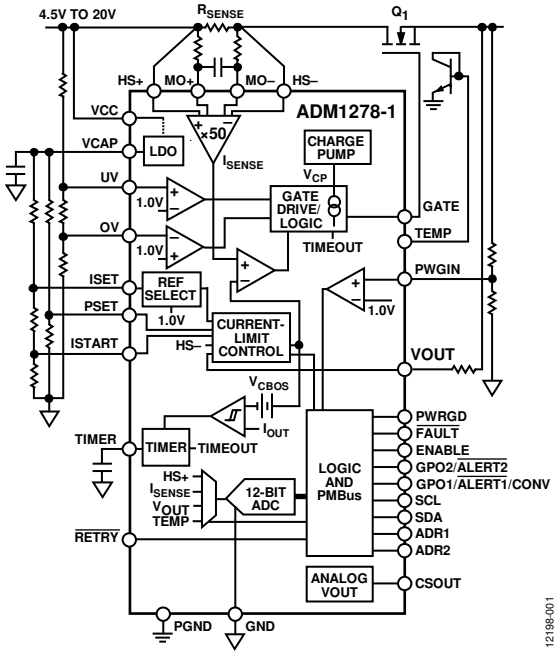

Figure 1.

In case of a short-circuit event, a fast internal overcurrent detector responds within 320 ns and signals the gate to shut down. A 1500 mA pull-down device ensures a fast FET response.

The ADM1278 features overvoltage (OV) and undervoltage (UV) protection, programmed using external resistor dividers on the UV and OV pins. A PWRGD signal can be used to detect when the output supply is valid, using the PWGIN pin to accurately monitor the output.

The ADM1278 is available in a 32-lead LFCSP with a $\overline{\text{RETRY}}$ pin that can be configured for automatic retry or latch-off when an overcurrent fault occurs.

Table 1. Model Options

Model	ADC Accuracy	SPI Interface	Enable Pin[1]
ADM1278-1AA	±0.3%	No	Active high
ADM1278-1A	±0.7%	No	Active high
ADM1278-1B	±1.0%	No	Active high
ADM1278-2A	±0.7%	Yes	Active high
ADM1278-3A	±0.7%	No	Active low

[1] Active high relates to the ENABLE pin, and active low relates to the $\overline{\text{ENABLE}}$ pin.

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADM1278 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1338: ADM1278 Design Guide
- AN-1343: Energy Metering on Hot Swap and Power Monitor Devices

Data Sheet

- ADM1278: Hot Swap Controller and Digital Power and Energy Monitor with PMBus Interface Data Sheet

User Guides

- UG-353: Hot Swap and Power Monitor Software
- UG-601: ADM1278 Evaluation Board User Guide

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADMxxxx Common Run-Time
- Hot-Swap & Power Monitoring Evaluation Software

TOOLS AND SIMULATIONS

- Hot-Swap & Power Monitoring Evaluation Software

DESIGN RESOURCES

- ADM1278 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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View all ADM1278 EngineerZone Discussions.

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Change to Power Cycle Register Section....58

6/14—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 4.5 V to 20 V, $V_{CC} \geq V_{HS+}$ and V_{MO+}, V_{HS+} = 2 V to 20 V, $V_{SENSE\_HS} = (V_{HS+} - V_{HS-}) = 0$ V, T_A = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY						
Operating Voltage Range	V_{CC}	4.5		20	V	
Undervoltage Lockout	UVLO	2.4		2.7	V	V_{CC} rising
Undervoltage Hysteresis			90	120	mV	
Quiescent Current	I_{CC}			5.5	mA	GATE on and power monitor running
UV PIN						
Input Current	I_{UV}			50	nA	UV ≤ 3.6 V
UV Threshold	UV_{TH}					
A Grade and AA Grade		0.99	1.0	1.01	V	UV falling
B Grade Only		0.97	1.0	1.03	V	UV falling
UV Threshold Hysteresis	UV_{HYST}	45	60	75	mV	
UV Glitch Filter	UV_{GF}	2		7	µs	50 mV overdrive
UV Propagation Delay	UV_{PD}		5	8	µs	UV low to GATE pull-down active
OV PIN						
Input Current	I_{OV}			50	nA	OV ≤ 3.6 V
OV Threshold	OV_{TH}					
A Grade and AA Grade		0.99	1.0	1.01	V	OV rising
B Grade Only		0.97	1.0	1.03	V	OV rising
OV Threshold Hysteresis	OV_{HYST}	45	60	75	mV	
OV Glitch Filter	OV_{GF}	1.5		3.5	µs	50 mV overdrive
OV Propagation Delay	OV_{PD}		3.0	4.0	µs	OV high to GATE pull-down active
HS+ AND HS− PINS						
Input Current	I_{SENSEx}			150	µA	Per individual pin; V_{HS+}, V_{HS-} = 20 V
Input Imbalance	$I_{\Delta SENSE}$			5	µA	$I_{\Delta SENSE} = (I_+ - I_-)$
MO+ AND MO− PINS						
Input Current	$I_{MO\pm}$			25	nA	Per individual pin; V_{MO+}, V_{MO-} = 20 V
VCAP PIN						
Internally Regulated Voltage	V_{VCAP}					
A Grade and AA Grade		2.68	2.7	2.72	V	0 µA ≤ I_{VCAP} ≤ 100 µA; C_{VCAP} = 1 µF
B Grade Only		2.66	2.7	2.74	V	0 µA ≤ I_{VCAP} ≤ 100 µA; C_{VCAP} = 1 µF
ISET PIN						
Reference Select Threshold	$V_{ISETRSTH}$	1.35	1.5	1.65	V	If $V_{ISET} > V_{ISETRSTH}$, an internal 1 V reference (V_{CLREF}) is used
Internal Reference	V_{CLREF}		1		V	Accuracies included in total sense voltage accuracies
Gain of Current Sense Amplifier	AV_{CSAMP}		50		V/V	Accuracies included in total sense voltage accuracies
Recommended Maximum Operating Range	V_{ISET}	0.25		1.25	V	5 mV to 25 mV V_{SENSE} current limit
Input Current	I_{ISET}			100	nA	$V_{ISET} \leq V_{VCAP}$
GATE PIN						Maximum voltage on the gate is always clamped to ≤31 V
GATE Drive Voltage	ΔV_{GATE}					$\Delta V_{GATE} = V_{GATE} - V_{OUT}$
		10	12	14	V	20 V ≥ V_{CC} ≥ 8 V; I_{GATE} ≤ 5 µA
		8		10	V	$V_{HS+} = V_{CC}$ = 5 V; I_{GATE} ≤ 5 µA
		7		9	V	$V_{HS+} = V_{CC}$ = 4.5 V; I_{GATE} ≤ 1 µA
GATE Pull-Up Current	I_{GATEUP}	−20		−30	µA	V_{GATE} = 0 V
GATE Pull-Down Current	I_{GATEDN}					
Regulation	I_{GATEDN_REG}	45	60	75	µA	V_{GATE} ≥ 2 V; V_{ISET} = 1.0 V; $(V_{HS+} - V_{HS-})$ = 30 mV
Slow	I_{GATEDN_SLOW}	5	10	15	mA	V_{GATE} ≥ 2 V
Fast	I_{GATEDN_FAST}	750	1500	2250	mA	V_{GATE} ≥ 12 V; V_{CC} ≥ 12 V
GATE Holdoff Resistance			20		Ω	V_{CC} = 0 V, V_{GATE} = 2 V

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
HOT SWAP SENSE VOLTAGE						
Hot Swap Sense Voltage Current Limit	$V_{SENSECL}$					
A Grade and AA Grade		19.75	20	20.25	mV	V_{ISET} > 1.65 V; V_{GATE} = (V_{HS+} + 3 V); I_{GATE} = 0 µA
B Grade Only		19.6	20	20.4	mV	V_{ISET} > 1.65 V; V_{GATE} = (V_{HS+} + 3 V); I_{GATE} = 0 µA
Constant Power Inactive						V_{GATE} = (V_{HS+} + 3 V); I_{GATE} = 0 µA; V_{DS} = (HS−) − V_{OUT}
A Grade and AA Grade		24.75	25	25.25	mV	V_{ISET} = 1.25 V; V_{DS} < 2 V
		19.75	20	20.25	mV	V_{ISET} = 1.0 V; V_{DS} < 2 V
		14.75	15	15.25	mV	V_{ISET} = 0.75 V; V_{DS} < 2 V
B Grade Only		24.6	25	25.4	mV	V_{ISET} = 1.25 V; V_{DS} < 2 V
		19.6	20	20.4	mV	V_{ISET} = 1.0 V; V_{DS} < 2 V
		14.6	15	15.4	mV	V_{ISET} = 0.75 V; V_{DS} < 2V
Constant Power Active						FET power limit = (V_{PSET} × 8)/(50 × R_{SENSE}); constant power active when V_{DS} > (V_{PSET} × 8)/I_{SET}
A Grade and AA Grade		9.25	10	10.75	mV	V_{ISET} > 1.65 V; V_{PSET} = 0.25 V; V_{DS} = 4 V
		4.65	5	5.35	mV	V_{ISET} > 1.65 V; V_{PSET} = 0.25 V; V_{DS} = 8 V
		1.7	2	2.3	mV	V_{ISET} > 1.65 V; V_{PSET} = 0.25 V; V_{DS} = 20 V
B Grade Only		9	10	11	mV	V_{ISET} > 1.65 V; V_{PSET} = 0.25 V; V_{DS} = 4 V
		4.6	5	5.4	mV	V_{ISET} > 1.65 V; V_{PSET} = 0.25 V; V_{DS} = 8 V
		1.4	2	2.6	mV	V_{ISET} > 1.65 V; V_{PSET} = 0.25 V; V_{DS} = 20 V
Start-Up Current Limit	$V_{ISTARTCL}$					
A Grade and AA Grade		4.7	5	5.3	mV	STRT_UP_IOUT_LIM = 3; V_{ISET} > 1.65 V
		3.7	4	4.3	mV	V_{ISTART} = 0.2 V
B Grade Only		4.5	5	5.5	mV	STRT_UP_IOUT_LIM = 3; V_{ISET} > 1.65 V
		3.5	4	4.5	mV	V_{ISTART} = 0.2 V
Start-Up Current-Limit Clamp	$V_{ISTARTCL\_CLAMP}$					
A Grade and AA Grade		1.6	2	2.4	mV	V_{ISTART} = 0 V or STRT_UP_IOUT_LIM = 0
B Grade Only		1.4	2	2.6	mV	V_{ISTART} = 0 V or STRT_UP_IOUT_LIM = 0
Circuit Breaker Offset	V_{CBOS}	0.6	0.88	1.12	mV	Circuit breaker trip voltage, V_{CB} = $V_{SENSECL}$ − V_{CBOS}
SEVERE OVERCURRENT						
Voltage Threshold	$V_{SENSEOC}$					
A Grade and AA Grade		23	25	27	mV	V_{ISET} > 1.65 V; V_{PSET} > 1.1 V; optional select PMBus (125%)
		28	30	32	mV	V_{ISET} > 1.65 V; V_{PSET} > 1.1 V; optional select PMBus (150%)
		38	40	42	mV	V_{ISET} > 1.65 V; V_{PSET} > 1.1 V; optional select PMBus (200%)
		43	45	47	mV	V_{ISET} > 1.65 V; V_{PSET} > 1.1 V; default at power-up (225%)
B Grade Only		20	25	30	mV	V_{ISET} > 1.65 V; V_{PSET} > 1.1 V; optional select PMBus (125%)
		25	30	35	mV	V_{ISET} > 1.65 V; V_{PSET} > 1.1 V; optional select PMBus (150%)
		35	40	45	mV	V_{ISET} > 1.65 V; V_{PSET} > 1.1 V; optional select PMBus (200%)
		40	45	50	mV	V_{ISET} > 1.65 V; V_{PSET} > 1.1 V; default at power-up (225%)
Short Glitch Filter Duration		100		220	ns	V_{SENSE_HS} step = 18 mV to (2 mV above $V_{SENSEOC\_MAX}$)
Long Glitch Filter Duration (Default)		530		900	ns	V_{SENSE_HS} step = 18 mV to (2 mV above $V_{SENSEOC\_MAX}$)
Response Time						
Short Glitch Filter		200		320	ns	V_{SENSE_HS} step = 18 mV to (2 mV above $V_{SENSEOC\_MAX}$)
Long Glitch Filter		630		1000	ns	V_{SENSE_HS} step = 18 mV to (2 mV above $V_{SENSEOC\_MAX}$)
ISTART PIN						
Active Range		0.1		1.25	V	Tie ISTART to VCAP to disable start-up current limit
Gain of Current Sense Amplifier	AV_{CSAMP}		50		V/V	Accuracies included in total sense voltage accuracies
Input Current	I_{ISTART}			100	nA	V_{ISTART} ≤ V_{VCAP}
TIMER PIN						
TIMER Pull-Up Current						
Power-On Reset (POR)	$I_{TIMERUPPOR}$	−2	−3	−4	µA	Initial power-on reset; V_{TIMER} = 0.5 V
Overcurrent (OC) Fault	$I_{TIMERUPFLT}$	−57	−60	−63	µA	Overcurrent fault; 0.2 V ≤ V_{TIMER} ≤ 1 V

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
TIMER Pull-Down Current						
Retry	$I_{TIMERDNRT}$	1.7	2	2.3	µA	After fault when GATE is off; V_{TIMER} = 0.5 V
Hold	$I_{TIMERDNHOLD}$		100		µA	Holds TIMER at 0 V when inactive; V_{TIMER} = 0.5 V
TIMER High Threshold	V_{TIMERH}	0.98	1.0	1.02	V	
TIMER Low Threshold	V_{TIMERL}	0.18	0.2	0.22	V	
TIMER Glitch Filter	$TIMER_{GF}$		10		µs	
Minimum POR Duration			27		ms	Minimum initial insertion delay regardless of C_{TIMER} value
PSET PIN						FET power limit = $(V_{PSET} \times 8)/(50 \times R_{SENSE})$
Reference Select Threshold	$V_{PSETRSTH}$	1.35	1.5	1.65	V	If $V_{PSET} > V_{PSETRSTH}$, constant power is disabled
Gain of Current Sense Amplifier	AV_{CSAMP}		50		V/V	Accuracies included in total sense voltage accuracies
Input Current	I_{PSET}			100	nA	$V_{PSET} \leq V_{VCAP}$
VOUT PIN						
Input Current				40	µA	V_{OUT} = 20 V
$\overline{\text{FAULT}}$ PIN						
Output Low Voltage	V_{OL_LATCH}			0.4	V	I_{FAULT} = 1 mA
				1.5	V	I_{FAULT} = 5 mA
Leakage Current				100	nA	$V_{FAULT} \leq$ 2 V; $\overline{\text{FAULT}}$ output high-Z
				1	µA	V_{FAULT} = 20 V; $\overline{\text{FAULT}}$ output high-Z
ENABLE PIN						
Input High Voltage	V_{IH}	1.1			V	
Input Low Voltage	V_{IL}			0.8	V	
Glitch Filter			1		µs	
$\overline{\text{RETRY}}$ PIN						
Input High Voltage	V_{IH}	1.1			V	Latch off when high; internal pull-up sets this as default
Input Low Voltage	V_{IL}			0.8	V	10 second automatic retry when pin pulled low
Glitch Filter			1		µs	
Internal Pull-Up Current			8		µA	
CSOUT PIN						
CSOUT Gain			350		V/V	CSOUT = $V_{SENSE\_HS} \times 350$; VCC > CSOUT + 2 V
Total Output Error		−1.6		+1.6	%	V_{SENSE_HS} = 20 mV; $I_{CSOUT} \leq$ 1 mA; C_{CSOUT} = 1 nF
		−3.0		+3.0	%	V_{SENSE_HS} = 10 mV; $I_{CSOUT} \leq$ 1 mA; C_{CSOUT} = 1 nF
Output Swing to GND			40		mV	
Current Limiting			5		mA	CSOUT short-circuit current
GPO1/$\overline{\text{ALERT1}}$/CONV PIN						
Output Low Voltage	V_{OL_GPO1}			0.4	V	I_{GPO1} = 1 mA
				1.5	V	I_{GPO1} = 5 mA
Leakage Current				100	nA	$V_{GPO1} \leq$ 2 V; GPO1 output high-Z
				1	µA	V_{GPO1} = 20 V; GPO1 output high-Z
Input High Voltage	V_{IH}	1.1			V	Configured as CONV
Input Low Voltage	V_{IL}			0.8	V	Configured as CONV
Glitch Filter			1		µs	Configured as CONV
GPO2/$\overline{\text{ALERT2}}$ PIN						
Output Low Voltage	V_{OL_GPO2}			0.4	V	I_{GPO2} = 1 mA
				1.5	V	I_{GPO2} = 5 mA
Leakage Current				100	nA	$V_{GPO2} \leq$ 2 V; GPO2 output high-Z
				1	µA	V_{GPO2} = 20 V; GPO2 output high-Z
PWRGD PIN						
Output Low Voltage	V_{OL_PWRGD}			0.4	V	I_{PWRGD} = 1 mA
				1.5	V	I_{PWRGD} = 5 mA
VCC That Guarantees Valid Output		1			V	I_{SINK} = 100 µA; V_{OL_PWRGD} = 0.4 V
Leakage Current				100	nA	$V_{PWRGD} \leq$ 2 V; PWRGD output high-Z
				1	µA	V_{PWRGD} = 20 V; PWRGD output high-Z

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
PWGIN PIN						
Input Current	I_{PWGIN}			50	nA	PWGIN ≤ 3.6 V
PWGIN Threshold	$PWGIN_{TH}$					
A Grade and AA Grade		0.99	1.0	1.01	V	PWGIN falling
B Grade Only		0.97	1.0	1.03	V	PWGIN falling
PWGIN Threshold Hysteresis	$PWGIN_{HYST}$	50	60	70	mV	
Glitch Filter			1		µs	Asserting and deasserting of PWRGD pin
CURRENT AND VOLTAGE MONITORING						See Table 3 for power monitor accuracy specifications
ADC Conversion Time						Includes time for power multiplication
			144	165	µs	One sample of I_{OUT}; from command received to valid data in register
			64	73	µs	One sample of V_{IN}; from command received to valid data in register
			64	73	µs	One sample of V_{OUT}; from command received to valid data in register
ADRx PINS						
Address Set to 00		0		0.8	V	Connect to GND
Input Current for Address Set to 00		−40	−22		µA	V_{ADRx} = 0 V to 0.8 V
Address Set to 01		135	150	165	kΩ	Resistor to GND
Address Set to 10		−1		+1	µA	No connect state; maximum leakage current allowed
Address Set to 11		2			V	Connect to VCAP
Input Current for Address Set to 11			3	10	µA	V_{ADRx} = 2.0 V to VCAP; must not exceed the maximum allowable current draw from VCAP
TEMP PIN						External transistor is 2N3904
Operating Range		−55		+150	°C	Limited by external diode
Accuracy			±1	±10	°C	$T_A = T_{DIODE}$ = −40°C to +85°C
Resolution			0.25		°C	LSB size
Output Current Source[2]						
Low Level			5		µA	
Medium Level			30		µA	
High Level			105		µA	
Maximum Series Resistance for External Diode[2]	R_S			100	Ω	For <±0.5°C additional error, C_P = 0 F
Maximum Parallel Capacitance for External Diode[2]	C_P			1	nF	R_S = 0 Ω
SPI DIGITAL INPUTS ($\overline{SPI\_SS}$, MCLK, MDAT)						Compatible with SPI Mode 0; MDAT is the output data pin; output is high impedance when not transmitting
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4 mA
Leakage Current				1	µA	
Data Rate				1	MHz	
SERIAL BUS DIGITAL INPUTS (SDA, SCL)						
Input High Voltage	V_{IH}	1.1			V	
Input Low Voltage	V_{IL}			0.8	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4 mA
Input Leakage	$I_{LEAK-PIN}$	−10		+10	µA	
		−5		+5	µA	Device is not powered

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Nominal Bus Voltage	V_{DD}	2.7		5.5	V	3 V to 5 V ± 10%
Capacitance for SDA, SCL Pins	C_{PIN}		5		pF	
Input Glitch Filter	t_{SP}	0		50	ns	

[1] Dual function pin names are referenced by the relevant function only (see the Pin Configurations and Function Descriptions section for full pin mnemonics and descriptions).
[2] Sampled during initial release to ensure compliance, but not subject to production testing.

POWER MONITORING ACCURACY SPECIFICATIONS

Table 3.

	AA Grade			A Grade			B Grade				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
CURRENT AND VOLTAGE MONITORING											
Current Sense Absolute Error											V_{CC} = 4.5 V to 15 V; V_{MO+} = 2 V to 15 V, 128-sample averaging (unless otherwise noted)
			±0.25			±0.7			±1.0	%	V_{SENSE_MO} = 25 mV
		±0.04	±0.3		±0.04	±0.7			±1.0	%	V_{SENSE_MO} = 20 mV
			±0.5			±1.0			±1.5	%	V_{SENSE_MO} = 20 mV; 16-sample averaging
			±1.5			±2.8			±4.0	%	V_{SENSE_MO} = 20 mV; one-sample averaging
			±0.3			±0.8			±1.1	%	V_{SENSE_MO} = 15 mV
			±0.4			±1.1			±1.5	%	V_{SENSE_MO} = 10 mV
			±0.75			±2.0			±3.0	%	V_{SENSE_MO} = 5 mV
			±1.6			±4.3			±6.2	%	V_{SENSE_MO} = 2.5 mV
HS+/VOUT Absolute Error			±0.35			±1.0			±1.5	%	V_{HS+}, V_{OUT} = 10 V to 20 V
			±0.5			±1.0			±1.5	%	V_{HS+}, V_{OUT} = 5 V
Power Absolute Error			±0.65			±1.7			±2.5	%	V_{SENSE_MO} = 20 mV, V_{HS+} = 12 V

SERIAL BUS TIMING CHARACTERISTICS

Table 4.

Parameter	Description	Min	Typ	Max	Unit
f_{SCLK}	Clock frequency			400	kHz
t_{BUF}	Bus free time	1.3			µs
$t_{HD;STA}$	Start hold time	0.6			µs
$t_{SU;STA}$	Start setup time	0.6			µs
$t_{SU;STO}$	Stop setup time	0.6			µs
$t_{HD;DAT}$	SDA hold time	300		900	ns
$t_{SU;DAT}$	SDA setup time	100			ns
t_{LOW}	SCL low time	1.3			µs
t_{HIGH}	SCL high time	0.6			µs
t_R[1]	SCL, SDA rise time	20		300	ns
t_F[1]	SCL, SDA fall time	20		300	ns

[1] $t_R = (V_{IL(MAX)} - 0.15)$ to $(V_{IH3V3} + 0.15)$ and $t_F = 0.9\ V_{DD}$ to $(V_{IL(MAX)} - 0.15)$; where V_{IH3V3} = 2.1 V, and V_{DD} = 3.3 V. V_{IH3V3} is the input high voltage when V_{DD} = 3.3 V.

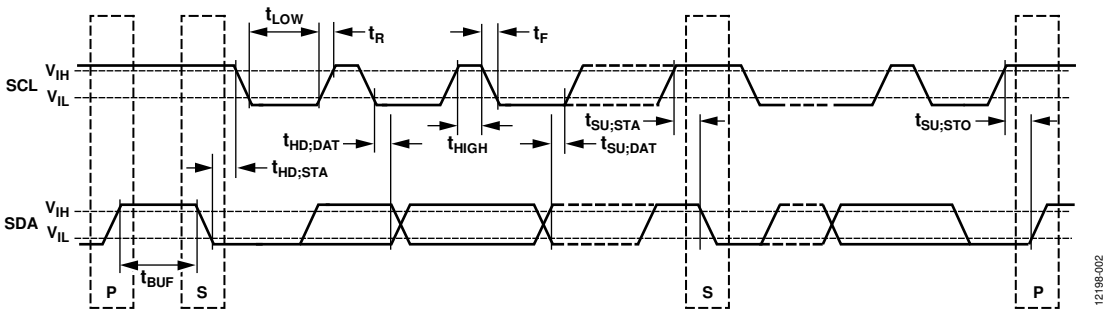


Figure 2. Serial Bus Timing Diagram

SPI TIMING CHARACTERISTICS (ADM1278-2)

Table 5.

Parameter	Description	Min	Typ	Max	Unit	Test Conditions/Comments
t_S[1]	$\overline{\text{SPI\_SS}}$ falling edge to MCLK rising edge setup time	50			ns	
t_{HIGH}[1]	MCLK high time	180			ns	
t_{LOW}[1]	MCLK low time	180			ns	
t_{CLK}[1]	MCLK cycle time	1			µs	
t_H[1]	Hold time between $\overline{\text{SPI\_SS}}$ and MCLK	1			µs	
t_V	Hold time between new data valid and MCLK falling edge	110		260	ns	Track capacitance = 120 pF; I_{OL} = 4 mA
t_{ON}	$\overline{\text{SPI\_SS}}$ falling edge to MDAT active time	130		240	ns	Track capacitance = 120 pF; I_{OL} = 4 mA
t_{OFF}	Bus relinquish time after $\overline{\text{SPI\_SS}}$ rising edge	130		280	ns	Track capacitance = 120 pF; I_{OL} = 4 mA

[1] Guaranteed by design, but not production tested.

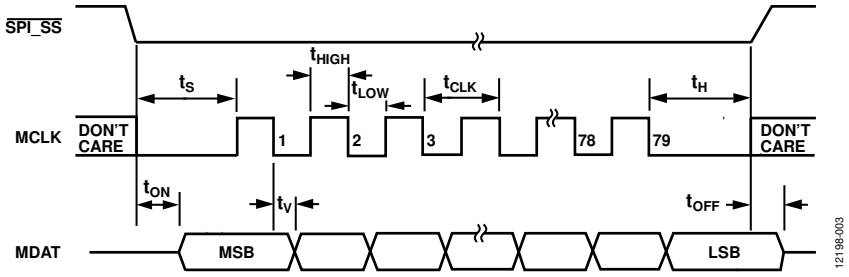


Figure 3. SPI Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
VCC Pin	−0.3 V to +25 V
UV Pin	−0.3 V to +4 V
OV Pin	−0.3 V to +4 V
ISTART Pin	−0.3 V to +4 V
TIMER Pin	−0.3 V to VCAP + 0.3 V
TEMP Pin	−0.3 V to VCAP + 0.3 V
VCAP Pin	−0.3 V to +4 V
ISET Pin	−0.3 V to +4 V
PSET Pin	−0.3 V to +4 V
$\overline{\text{FAULT}}$ Pin	−0.3 V to +25 V
$\overline{\text{RETRY}}$ Pin	−0.3 V to +4 V
PWGIN Pin	−0.3 V to +4 V
SCL Pin	−0.3 V to +6.5 V
SDA Pin	−0.3 V to +6.5 V
$\overline{\text{SPI\_SS}}$ Pin	−0.3 V to +4 V
MCLK Pin	−0.3 V to +4 V
MDAT Pin	−0.3 V to +4 V
ADR1 Pin	−0.3 V to +6.5 V
ADR2 Pin	−0.3 V to +6.5 V
ENABLE Pin	−0.3 V to +25 V
GPO1/$\overline{\text{ALERT1}}$/CONV Pin	−0.3 V to +25 V
GPO2/$\overline{\text{ALERT2}}$ Pin	−0.3 V to +25 V
PWRGD Pin	−0.3 V to +25 V
VOUT Pin	−0.3 V to +25 V
GATE Pin (Internal Supply Only)[1]	−0.3 V to +36 V
HS+ Pin	−0.3 V to +25 V
HS− Pin	−0.3 V to +25 V
MO+ Pin	−0.3 V to +25 V
MO− Pin	−0.3 V to +25 V
PGND	±0.3 V
V_{SENSE_HS} ($V_{HS+} - V_{HS-}$)	±0.3 V
V_{SENSE_MO} ($V_{MO+} - V_{MO-}$)	±0.3 V
CSOUT Short-Circuit Duration	Indefinite
Continuous Current into Any Pin	±10 mA
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature, Soldering (10 sec)	300°C
Junction Temperature	105°C

[1] The GATE pin has internal clamping circuits to prevent the GATE pin voltage from exceeding the maximum ratings of a MOSFET with gain to source voltage, V_{GSMAX} = 20 V, and internal process limits. Applying a voltage source to this pin externally may cause irreversible damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

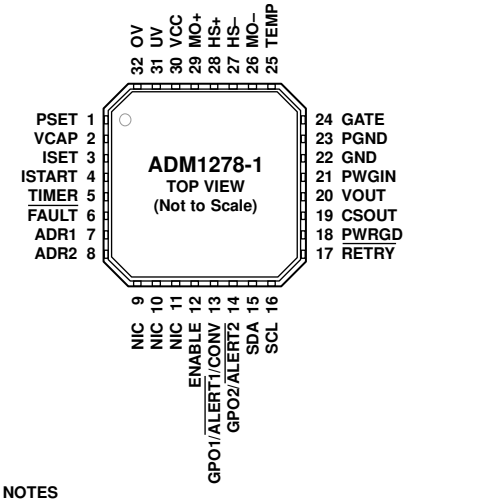
Table 7. Thermal Resistance

Package Type	θ_{JA}	Unit
32-Lead LFCSP (CP-32-13)	32.5	°C/W

ESD CAUTION

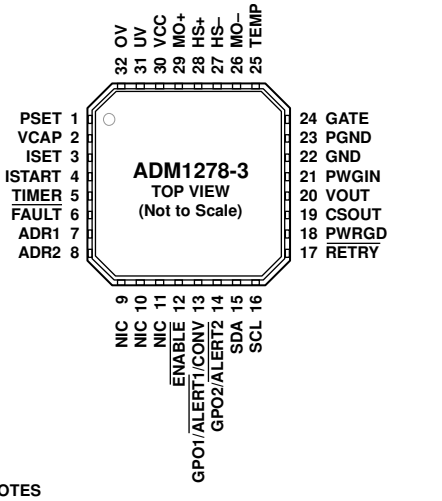
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED.
2. SOLDER THE EXPOSED PAD TO THE BOARD TO IMPROVE THERMAL DISSIPATION. THE EXPOSED PAD CAN BE CONNECTED TO GROUND.

Figure 4. ADM1278-1 Pin Configuration



NOTES
1. NIC = NOT INTERNALLY CONNECTED.
2. SOLDER THE EXPOSED PAD TO THE BOARD TO IMPROVE THERMAL DISSIPATION. THE EXPOSED PAD CAN BE CONNECTED TO GROUND.

Figure 5. ADM1278-3 Pin Configuration

Table 8. ADM1278-1 and ADM1278-3 Pin Function Descriptions

Pin No.	Mnemonic		Description
	ADM1278-1	ADM1278-3	
1	PSET	PSET	Power Limit. This pin allows the constant power limit to be programmed. The current limit is dynamically adjusted to ensure that the maximum power dissipation in the FET never exceeds this limit during any operating condition. The power limit can be adjusted to a user defined value using a resistor divider from VCAP. An external reference can also be used. The FET power is limited to $(V_{PSET} \times 8)/(50 \times R_{SENSE})$.
2	VCAP	VCAP	Internal Regulated Supply. Place a capacitor with a value of 1 µF or greater on this pin to maintain accuracy. This pin can be used as a reference to program the ISET pin voltage.
3	ISET	ISET	Current Limit. This pin allows the current-limit threshold to be programmed. The default limit is set when this pin is connected directly to VCAP. To achieve a user defined sense voltage, the current limit can be adjusted using a resistor divider from VCAP. An external reference can also be used.
4	ISTART	ISTART	Start-Up Current Limit. This pin allows a separate start-up current limit to be set for dv/dt power-up mode. When powering up in dv/dt mode, the current charging the capacitor is constant and is typically much smaller than the normal load current. The ISTART pin sets the start-up current limit in a similar manner as ISET is used to set the normal current limit. The start-up current limit is only active while PWRGD is low. The start-up current limit can also be set over PMBus with the STRT_UP_IOUT_LIM register. Start-up current limit = $V_{ISET} \times$ (STRT_UP_IOUT_LIM/16). The lowest of all the active current limits always takes priority.
5	TIMER	TIMER	Timer. An external capacitor, C_{TIMER}, sets an initial timing cycle delay and a fault delay. The GATE pin is pulled low when the voltage on the TIMER pin exceeds the upper threshold.
6	$\overline{\text{FAULT}}$	$\overline{\text{FAULT}}$	Fault. This pin asserts low and latches after a fault has occurred. The faults that can trigger this pin include an overcurrent fault resulting in the TIMER pin voltage exceeding the upper threshold, an overtemperature fault, and an FET health fault. This is an open-drain output pin.
7, 8	ADR1, ADR2	ADR1, ADR2	PMBus Address. These pins can be tied to GND, tied to VCAP, left floating, or tied low through a resistor for a total of 16 unique PMBus device addresses (see the Device Addressing section).
9, 10, 11	NIC	NIC	Not Internally Connected.

Pin No.	Mnemonic		Description
	ADM1278-1	ADM1278-3	
12	ENABLE	$\overline{\text{ENABLE}}$	Enable. On the ADM1278-1, the ENABLE pin is an active high digital input pin. This input must be high to allow the ADM1278-1 hot swap controller to begin a power-up sequence. If the ENABLE pin is held low, the ADM1278-1 is prevented from initiating a hot swap attempt. On the ADM1278-3, the $\overline{\text{ENABLE}}$ pin is an active low digital input pin. This input must be low to allow the ADM1278-3 hot swap controller to begin a power-up sequence. If the $\overline{\text{ENABLE}}$ pin is held high, the ADM1278-3 is prevented from initiating a hot swap attempt.
13	GPO1/$\overline{\text{ALERT1}}$/CONV	GPO1/$\overline{\text{ALERT1}}$/CONV	General-Purpose Digital Output (GPO1). Alert ($\overline{\text{ALERT1}}$).This pin can be configured to generate an alert signal when one or more fault or warning conditions are detected. Conversion (CONV). This pin can be used as an input signal to control when a power monitor ADC sampling cycle begins. The GPO1/$\overline{\text{ALERT1}}$/CONV pin defaults to an alert output at power-up. This is an open-drain output pin.
14	GPO2/$\overline{\text{ALERT2}}$	GPO2/$\overline{\text{ALERT2}}$	General-Purpose Digital Output (GPO2). Alert ($\overline{\text{ALERT2}}$). This pin can be configured to generate an alert signal when one or more fault or warning conditions are detected. The GPO2/$\overline{\text{ALERT2}}$ pin defaults to an alert output at power-up. This is an open-drain output pin.
15	SDA	SDA	Serial Data Input/Output. Open-drain input/output. Requires an external pull-up resistor. If the I^2C pins, SDA and SCL, are not used, tie them to GND or via a resistor pull-up to VCAP or another supply. This avoids any glitches on the I^2C pins being interpreted as I^2C transactions.
16	SCL	SCL	Serial Clock. Open-drain input. Requires an external pull-up resistor. If the I^2C pins, SDA and SCL, are not used, tie them to GND or via a pull-up resistor to VCAP or another supply. This avoids any glitches on the I^2C pins being interpreted as I^2C transactions.
17	$\overline{\text{RETRY}}$	$\overline{\text{RETRY}}$	Retry. The $\overline{\text{RETRY}}$ pin has an internal pull-up resistor; therefore, it can be left floating to enable the default latch off mode after an overcurrent fault. This pin can be pulled low to enable a 10 second autoretry following an overcurrent fault.
18	PWRGD	PWRGD	Power-Good Signal. This pin indicates that the supply is within tolerance (PWGIN input), no faults have been detected, and the ADM1278-1 hot swap is enabled with the gate fully enhanced. This is an open-drain output pin.
19	CSOUT	CSOUT	Current Sense Output. The V_{SENSE_HS} voltage is amplified to give an output voltage corresponding to the load current.
20	VOUT	VOUT	Output Voltage. VOUT is an input pin and is used to read back the output voltage using the internal ADC. Insert a 1 kΩ resistor in series between the source of a FET and the VOUT pin. This pin is also used along with HS− to calculate the drain to source voltage (V_{DS}) of the FET for constant power foldback operation.
21	PWGIN	PWGIN	Power-Good Input. This pin sets the power-good input threshold. The user can set an accurate power-good threshold with a resistor divider from the source of the FET (VOUT). The PWRGD output signal is not asserted high until the output voltage is above the threshold set by this pin.
22	GND	GND	Ground. This pin is the ground connection for all of the sensitive analog nodes. Take care to isolate this ground connection from the main high current path and any large transients. A good technique for this is to create a ground island around the ADM1278-1 device and the supporting small signal components. Connect this ground island to the main ground plane at a single point as close to the ADM1278-1 GND pin as possible. See the ADM1278 evaluation board (EVAL-ADM1278EBZ) as an example.
23	PGND	PGND	Power Ground. This pin is the ground return path for the strong gate pull-down current. It is also the ground return for the external transistor used for temperature measurements.
24	GATE	GATE	Gate Output. This pin is the high-side gate drive of an external N-channel FET. This pin is driven by the FET drive controller, which uses a charge pump to provide a pull-up current to charge the FET gate pin. The FET drive controller regulates to a maximum load current by regulating the GATE pin. GATE is held low when the supply is below the undervoltage lockout threshold (UVLO).
25	TEMP	TEMP	Temperature Input. An external NPN device can be placed close to the MOSFETs and connected back to the TEMP pin to report temperature. The voltage at the TEMP pin is measured by the internal ADC.

Pin No.	Mnemonic		Description
	ADM1278-1	ADM1278-3	
26	MO−	MO−	Negative Power Monitor Input. A sense resistor between the MO+ pin and the MO− pin sets the sense voltage that is used by the ADC internally to measure load current. Extra filtering can be added between the MO+ and MO− pins if required.
27	HS−	HS−	Negative Current Sense Input. A sense resistor between the HS+ pin and the HS− pin sets the analog current limit. The hot swap operation of the ADM1278-1 controls the external FET gate to maintain the sense voltage ($V_{HS+} - V_{HS-}$).
28	HS+	HS+	Positive Current Sense Input. This pin connects to the main supply input. A sense resistor between the HS+ pin and the HS− pin sets the analog current limit. The hot swap operation of the ADM1278-1 controls the external FET gate to maintain the sense voltage ($V_{HS+} - V_{HS-}$). This pin is also used to measure the supply input voltage using the ADC.
29	MO+	MO+	Positive Power Monitor Input. A sense resistor between the MO+ pin and the MO− pin sets the sense voltage that is used by the ADC internally to measure load current. Extra filtering can be added between the MO+ and MO− pins if required.
30	VCC	VCC	Positive Supply Input. A UVLO circuit resets the device when a low supply voltage is detected. GATE is held low when the supply is below UVLO. During normal operation, it is recommended that this pin be greater than or equal to HS+ and MO+ to ensure that specifications are adhered to. No sequencing is required.
31	UV	UV	Undervoltage Input. An external resistor divider is configured from the input supply to this pin to allow an internal comparator to detect whether the supply is below the UV limit.
32	OV	OV	Overvoltage Input. An external resistor divider is configured from the input supply to this pin to allow an internal comparator to detect whether the supply is above the OV limit.
	EP	EP	Exposed Pad. Solder the exposed pad to the board to improve thermal dissipation. The exposed pad can be connected to ground.

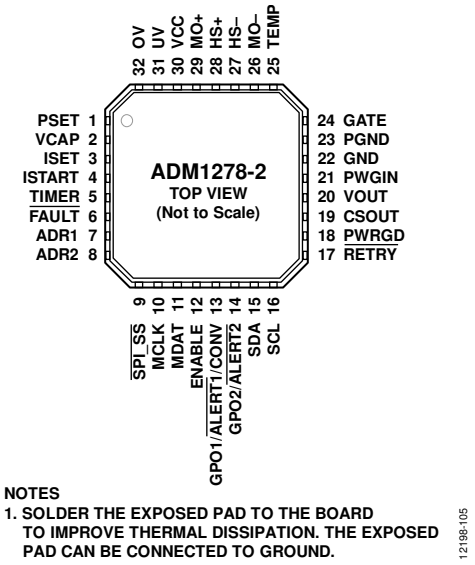


Figure 6. ADM1278-2 Pin Configuration

Table 9. ADM1278-2 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PSET	Power Limit. This pin allows the constant power limit to be programmed. The current limit is dynamically adjusted to ensure that the maximum power dissipation in the FET never exceeds this limit during any operating condition. The power limit can be adjusted to a user defined value using a resistor divider from VCAP. An external reference can also be used. The FET power is limited to $(V_{PSET} \times 8)/(50 \times R_{SENSE})$.
2	VCAP	Internal Regulated Supply. Place a capacitor with a value of 1 µF or greater on this pin to maintain accuracy. This pin can be used as a reference to program the ISET pin voltage.
3	ISET	Current Limit. This pin allows the current-limit threshold to be programmed. The default limit is set when this pin is connected directly to VCAP. To achieve a user defined sense voltage, the current limit can be adjusted using a resistor divider from VCAP. An external reference can also be used.
4	ISTART	Start-Up Current Limit. This pin allows a separate start-up current limit to be set for dv/dt power-up mode. When powering up in dv/dt mode, the current charging the capacitor is constant and is typically much smaller than the normal load current. The ISTART pin sets the start-up current limit in a similar manner as ISET is used to set the normal current limit. The start-up current limit is only active while PWRGD is low. The start-up current limit can also be set over PMBus with the STRT_UP_IOUT_LIM register. Start-up current limit = $V_{ISET} \times$ (STRT_UP_IOUT_LIM/16). The lowest of all the active current limits always takes priority.
5	TIMER	Timer. An external capacitor, C_{TIMER}, sets an initial timing cycle delay and a fault delay. The GATE pin is pulled low when the voltage on the TIMER pin exceeds the upper threshold.
6	$\overline{\text{FAULT}}$	Fault. This pin asserts low and latches after a fault has occurred. The faults that can trigger this pin include an overcurrent fault resulting in the TIMER pin voltage exceeding the upper threshold, an overtemperature fault, and an FET health fault. This is an open-drain output pin.
7, 8	ADR1, ADR2	PMBus Address. These pins can be tied to GND, tied to VCAP, left floating, or tied low through a resistor for a total of 16 unique PMBus device addresses (see the Device Addressing section).
9	$\overline{\text{SPI\_SS}}$	Slave Select. When pulled low, this pin begins to transfer data on the MDAT line.
10	MCLK	Master Clock. The MCLK signal outputs data on the MDAT line. This pin is clocked by an external device.
11	MDAT	Master Data Output. Open-drain output. Requires an external pull-up resistor. The MDAT pin is an output only pin and can be used to stream data from the ADC. There is a fixed format for the current, voltage, and temperature data, and no header information is required. This pin is high impedance when not transmitting data.
12	ENABLE	Enable. This pin is an active high digital input pin. This input must be high to allow the ADM1278-2 hot swap controller to begin a power-up sequence. If this pin is held low, the ADM1278-2 is prevented from initiating a hot swap attempt.

Pin No.	Mnemonic	Description
13	GPO1/$\overline{\text{ALERT1}}$/CONV	General-Purpose Digital Output (GPO1). Alert ($\overline{\text{ALERT1}}$). This pin can be configured to generate an alert signal when one or more fault or warning conditions are detected. Conversion (CONV). This pin can be used as an input signal to control when a power monitor ADC sampling cycle begins. The GPO1/$\overline{\text{ALERT1}}$/CONV pin defaults to an alert output at power-up. This is an open-drain output pin.
14	GPO2/$\overline{\text{ALERT2}}$	General-Purpose Digital Output (GPO2). Alert ($\overline{\text{ALERT2}}$). This pin can be configured to generate an alert signal when one or more fault or warning conditions are detected. The GPO2/$\overline{\text{ALERT2}}$ pin defaults to an alert output at power-up. This is an open-drain output pin.
15	SDA	Serial Data Input/Output. Open-drain input/output. Requires an external pull-up resistor. If the I^2C pins, SDA and SCL, are not used, tie them to GND or via a resistor pull-up to VCAP or another supply. This avoids any glitches on the I^2C pins being interpreted as I^2C transactions.
16	SCL	Serial Clock. Open-drain input. Requires an external pull-up resistor. If the I^2C pins, SDA and SCL, are not used, tie them to GND or via a resistor pull-up to VCAP or another supply. This avoids any glitches on the I^2C pins being interpreted as I^2C transactions.
17	$\overline{\text{RETRY}}$	Retry. The $\overline{\text{RETRY}}$ pin has an internal pull-up resistor; therefore, it can be left floating to enable the default latch off mode after an overcurrent fault. This pin can be pulled low to enable a 10 second autoretry following an overcurrent fault.
18	PWRGD	Power-Good Signal. This pin indicates that the supply is within tolerance (PWGIN input), no faults have been detected, and the ADM1278-2 hot swap is enabled with the gate fully enhanced. This is an open drain output pin.
19	CSOUT	Current Sense Output. The V_{SENSE_HS} voltage is amplified to give an output voltage corresponding to the load current.
20	VOUT	Output Voltage. VOUT is an input pin and is used to read back the output voltage using the internal ADC. Insert a 1 kΩ resistor in series between the source of a FET and the VOUT pin. This pin is also used along with HS− to calculate the drain to source voltage (V_{DS}) of the FET for constant power foldback operation.
21	PWGIN	Power-Good Input. This pin sets the power-good input threshold. The user can set an accurate power-good threshold with a resistor divider from the source of the FET (VOUT). The PWRGD output signal is not asserted high until the output voltage is above the threshold set by this pin.
22	GND	Ground. This pin is the ground connection for all of the sensitive analog nodes. Take care to isolate this ground connection from the main high current path and any large transients. A good technique for this is to create a ground island around the ADM1278-2 device and the supporting small signal components. Connect this ground island to the main ground plane at a single point as close to the ADM1278-2 GND pin as possible. See the ADM1278 evaluation board (EVAL-ADM1278EBZ) as an example.
23	PGND	Power Ground. This is the ground return path for the strong gate pull-down current. It is also the ground return for the external transistor used for temperature measurements.
24	GATE	Gate Output. This pin is the high-side gate drive of an external N-channel FET. This pin is driven by the FET drive controller, which uses a charge pump to provide a pull-up current to charge the FET gate pin. The FET drive controller regulates to a maximum load current by regulating the GATE pin. GATE is held low when the supply is below the UVLO threshold.
25	TEMP	Temperature Input. An external NPN device can be placed close to the MOSFETs and connected back to the TEMP pin to report temperature. The voltage at the TEMP pin is measured by the internal ADC.
26	MO−	Negative Power Monitor Input. A sense resistor between the MO+ pin and the MO− pin sets the sense voltage that is used by the ADC internally to measure load current. Extra filtering can be added between the MO+ and MO− pins if required.
27	HS−	Negative Current Sense Input. A sense resistor between the HS+ pin and the HS− pin sets the analog current limit. The hot swap operation of the ADM1278-2 controls the external FET gate to maintain the sense voltage ($V_{HS+} - V_{HS-}$).
28	HS+	Positive Current Sense Input. This pin connects to the main supply input. A sense resistor between the HS+ pin and the HS− pin sets the analog current limit. The hot swap operation of the ADM1278-2 controls the external FET gate to maintain the sense voltage ($V_{HS+} - V_{HS-}$). This pin is also used to measure the supply input voltage using the ADC.
29	MO+	Positive Power Monitor Input. A sense resistor between the MO+ pin and the MO− pin sets the sense voltage that is used by the ADC internally to measure load current. Extra filtering can be added between the MO+ and MO− pins if required.

Pin No.	Mnemonic	Description
30	VCC	Positive Supply Input. A UVLO circuit resets the device when a low supply voltage is detected. GATE is held low when the supply is below UVLO. During normal operation, it is recommended that this pin be greater than or equal to HS+ and MO+ to ensure that specifications are adhered to. No sequencing is required.
31	UV	Undervoltage Input. An external resistor divider is configured from the input supply to this pin to allow an internal comparator to detect whether the supply is below the UV limit.
32	OV	Overvoltage Input. An external resistor divider is configured from the input supply to this pin to allow an internal comparator to detect whether the supply is above the OV limit.
	EP	Exposed Pad. Solder the exposed pad to the board to improve thermal dissipation. The exposed pad can be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

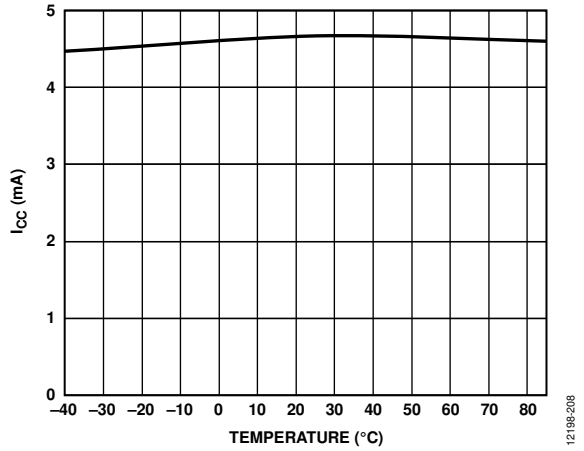


Figure 7. Supply Current (I_{CC}) vs. Temperature

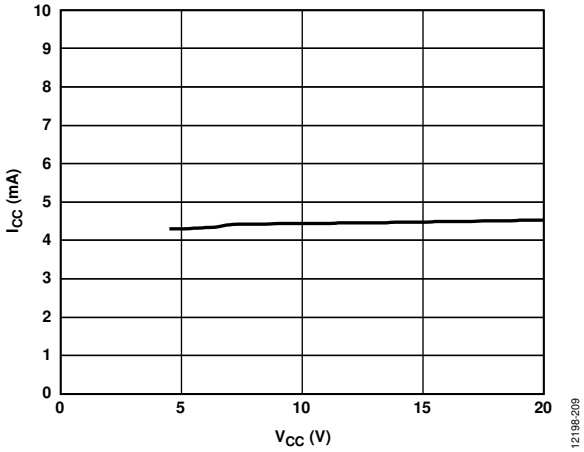


Figure 8. Supply Current (I_{CC}) vs. V_{CC}

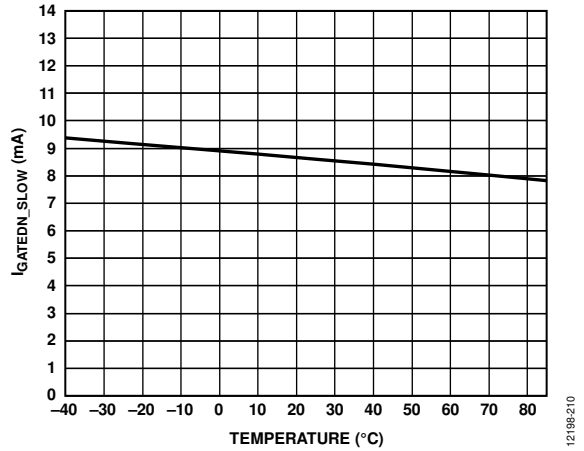


Figure 9. GATE Pull-Down Current (I_{GATEDN_SLOW}) vs. Temperature

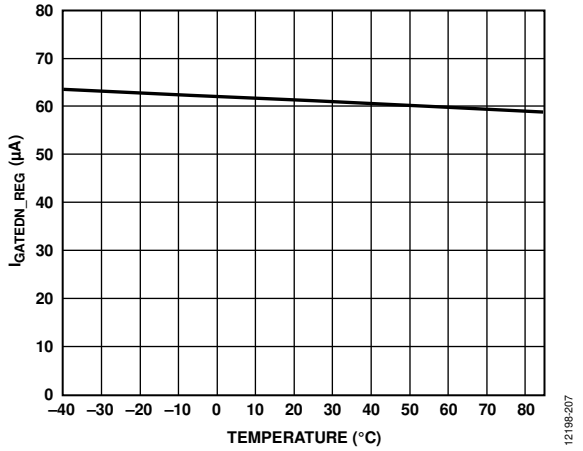


Figure 10. GATE Pull-Down Current (I_{GATEDN_REG}) vs. Temperature

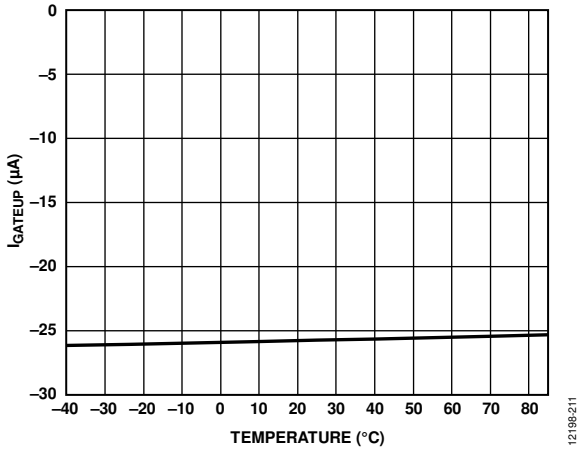


Figure 11. GATE Pull-Up Current (I_{GATEUP}) vs. Temperature

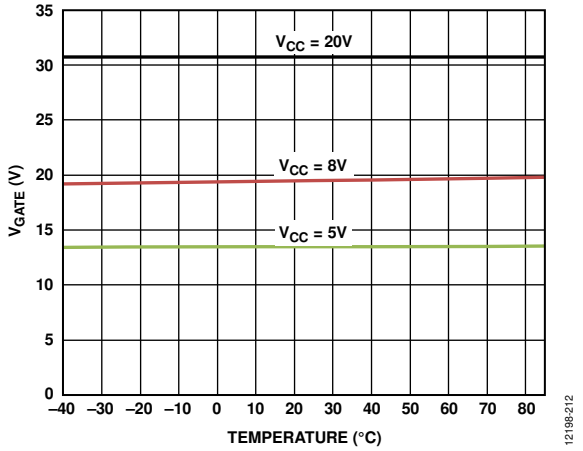


Figure 12. V_{GATE} (5 µA Load) vs. Temperature

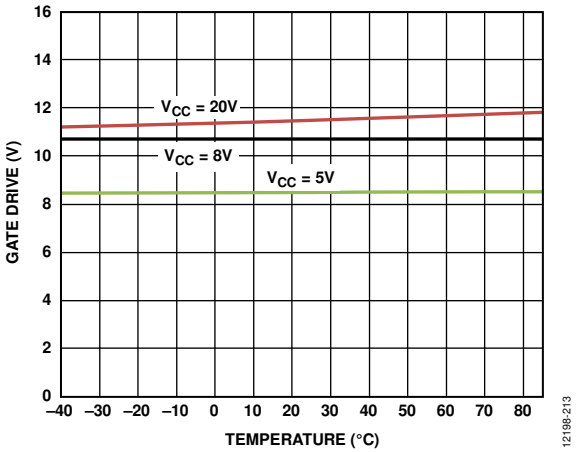


Figure 13. GATE Drive (5 µA Load) vs. Temperature

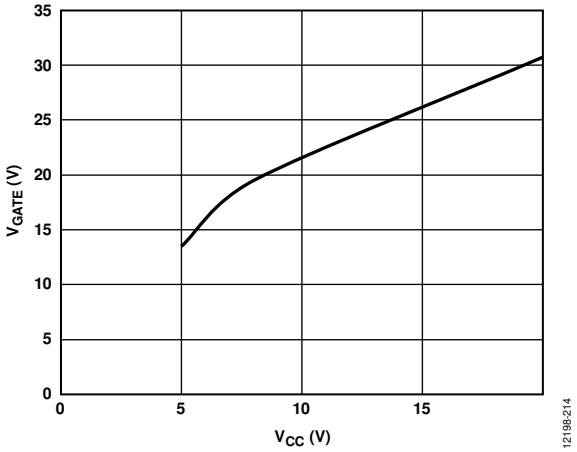


Figure 14. V_{GATE} (5 µA Load) vs. V_{CC}

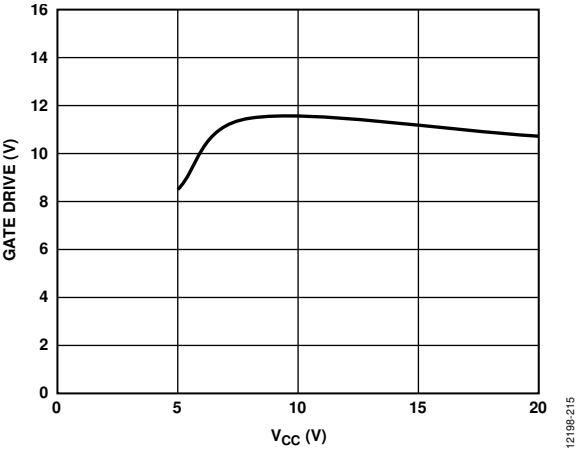


Figure 15. GATE Drive vs. V_{CC}

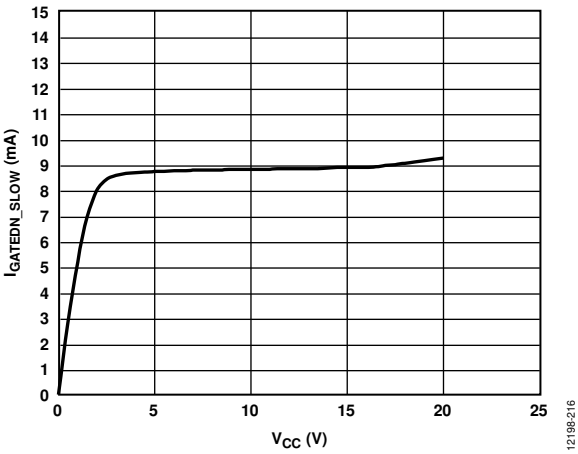


Figure 16. I_{GATEDN_SLOW} vs. V_{CC}

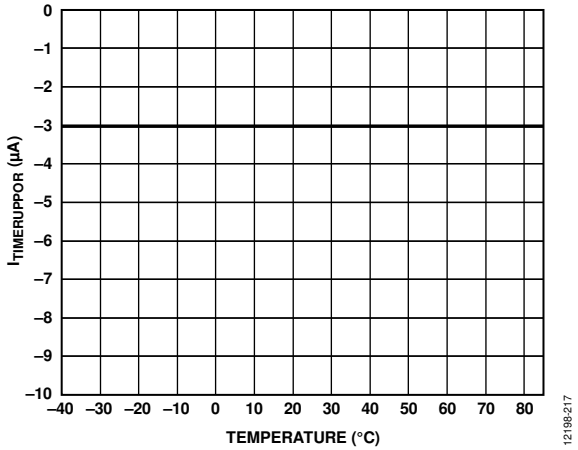


Figure 17. TIMER Pull-Up Current POR ($I_{TIMERUPPOR}$) vs. Temperature

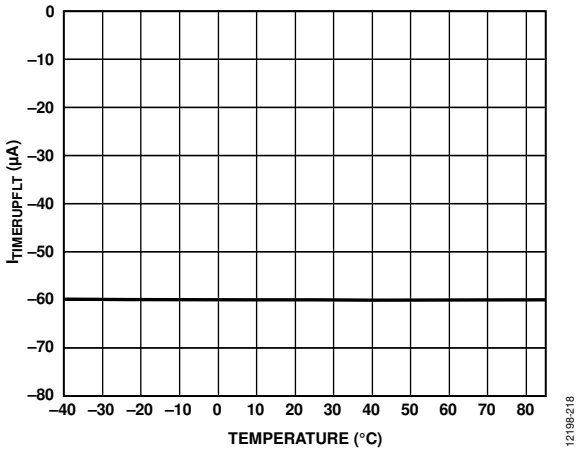


Figure 18. TIMER Pull-Up Current OC Fault ($I_{TIMERUPFLT}$) vs. Temperature

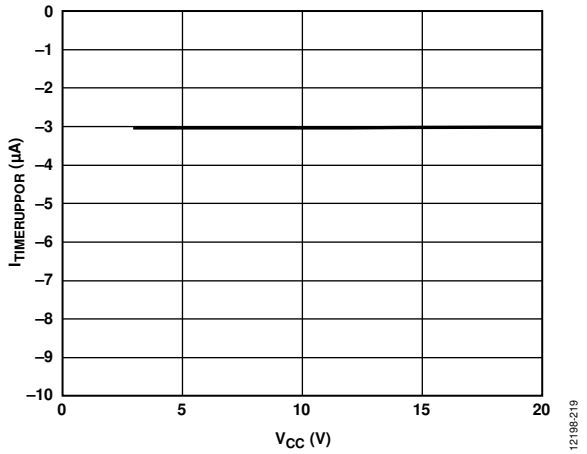


Figure 19. TIMER Pull-Up Current POR ($I_{TIMERUPPOR}$) vs. V_{CC}

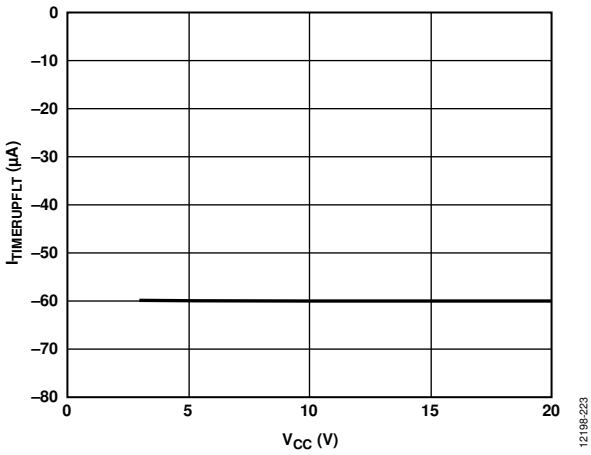


Figure 20. TIMER Pull-Up Current OC Fault ($I_{TIMERUPFLT}$) vs. V_{CC}

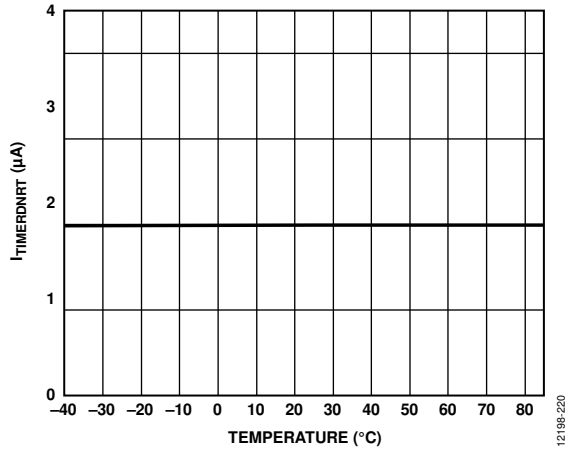


Figure 21. TIMER Pull-Down Current Retry ($I_{TIMERDNRT}$) vs. Temperature

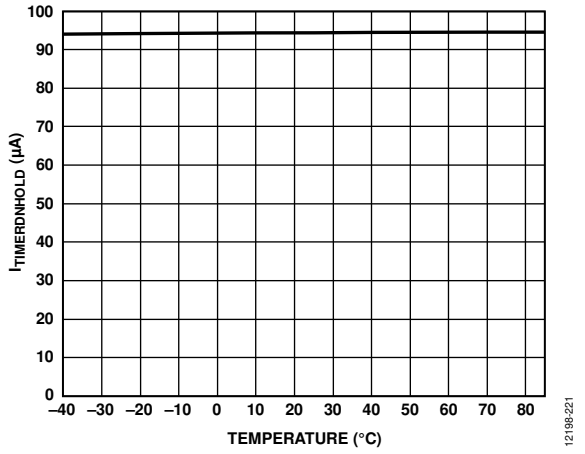


Figure 22. TIMER Pull-Down Current Hold ($I_{TIMERDNHOLD}$) vs. Temperature

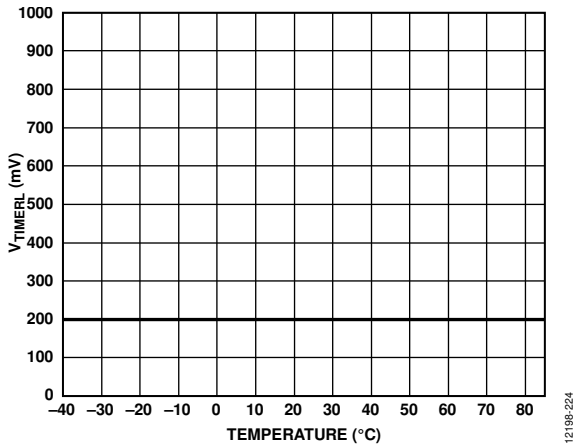


Figure 23. TIMER Low Threshold (V_{TIMERL}) vs. Temperature

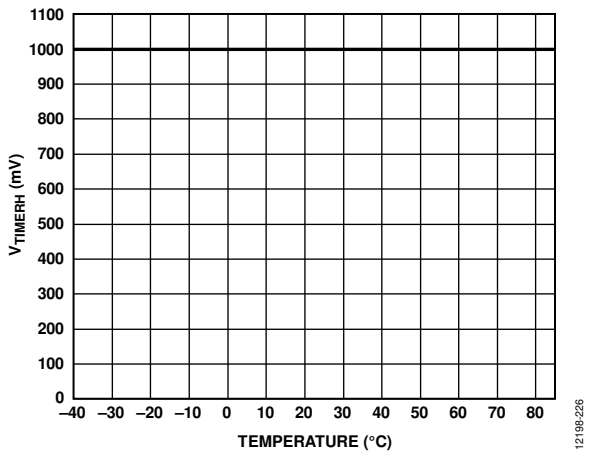


Figure 24. TIMER High Threshold (V_{TIMERH}) vs. Temperature

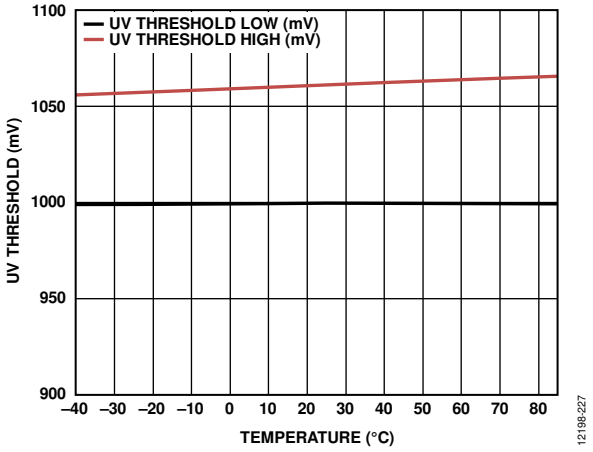


Figure 25. UV Threshold vs. Temperature

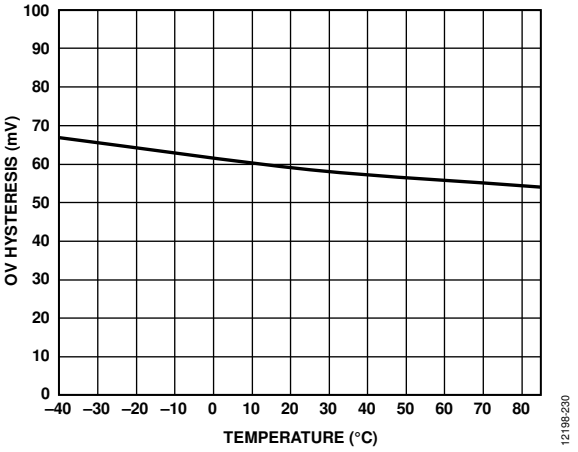


Figure 28. OV Hysteresis vs. Temperature

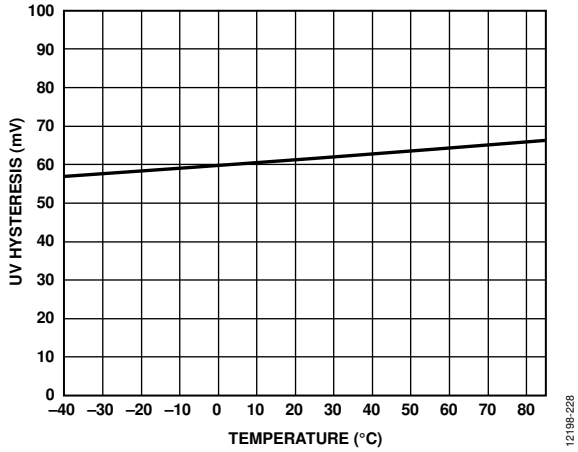


Figure 26. UV Hysteresis vs. Temperature

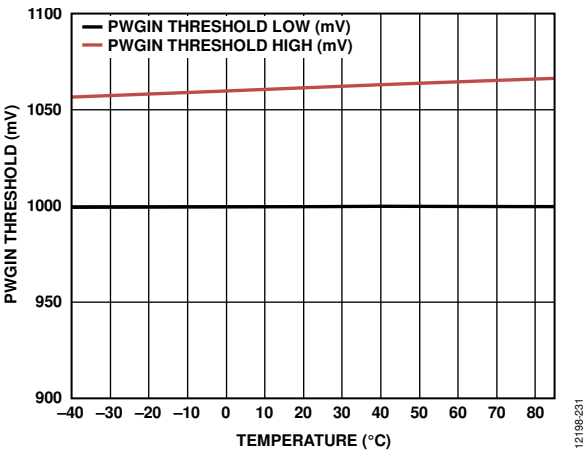


Figure 29. PWGIN Threshold vs. Temperature

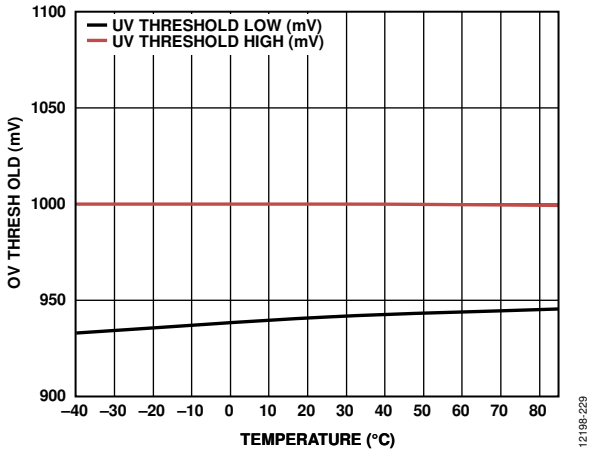


Figure 27. OV Threshold vs. Temperature

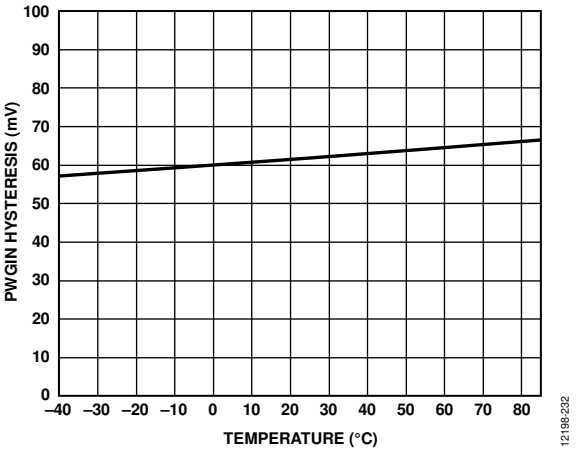


Figure 30. PGIN Hysteresis vs. Temperature

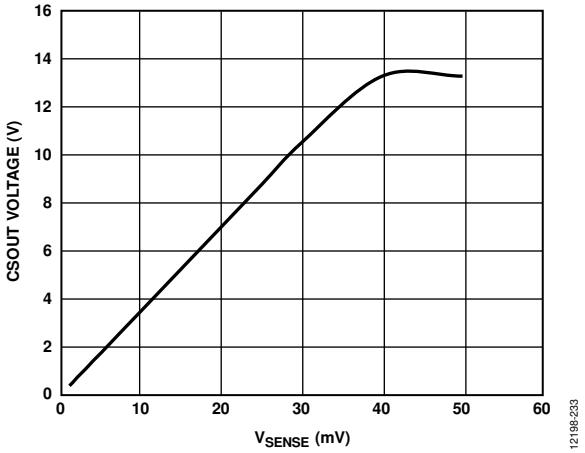


Figure 31. CSOUT Voltage vs. V_{SENSE}

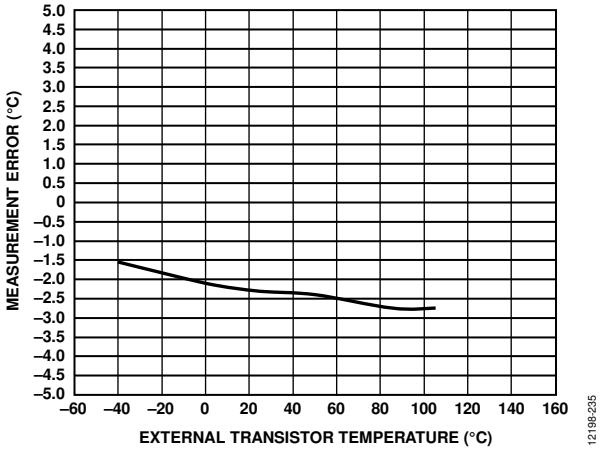


Figure 34. Measurement Error vs. External Transistor Temperature

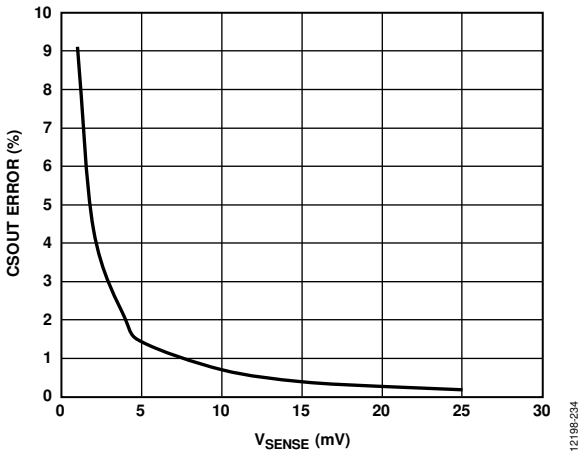


Figure 32. CSOUT Error vs. V_{SENSE}

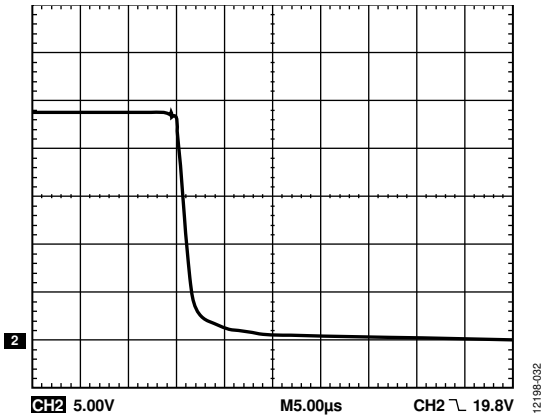


Figure 35. VGATE Response to Severe Overcurrent Event (GATE Fast Pull-Down)

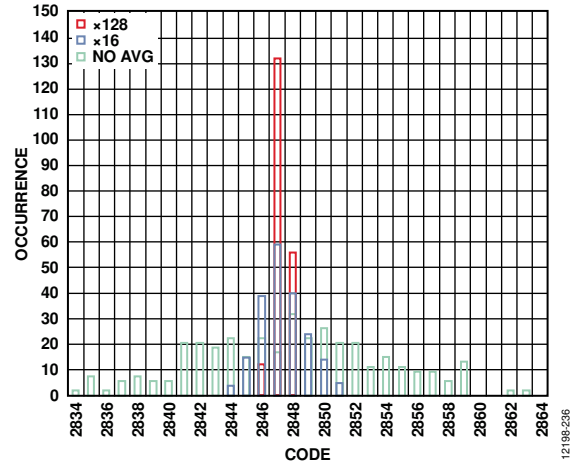


Figure 33. ADC Code Histogram (V_{SENSE} = 10 mV, 200 Measurements)

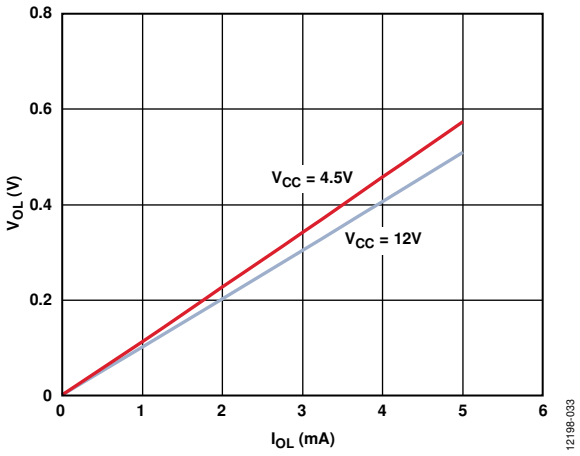


Figure 36. PWGD Pin, V_{OL} vs. I_{OL}

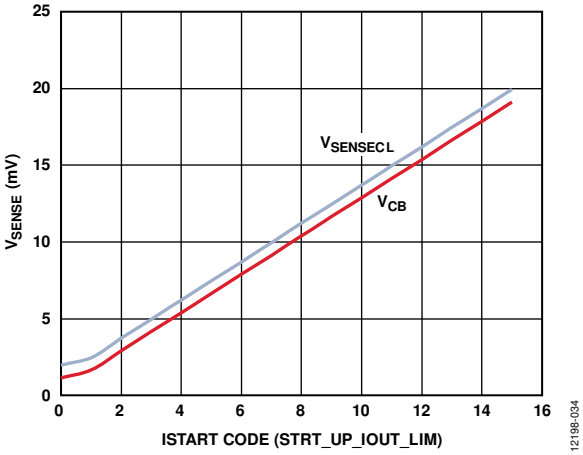


Figure 37. V_{SENSE} vs. ISTART Code (STRT_UP_IOUT_LIM)

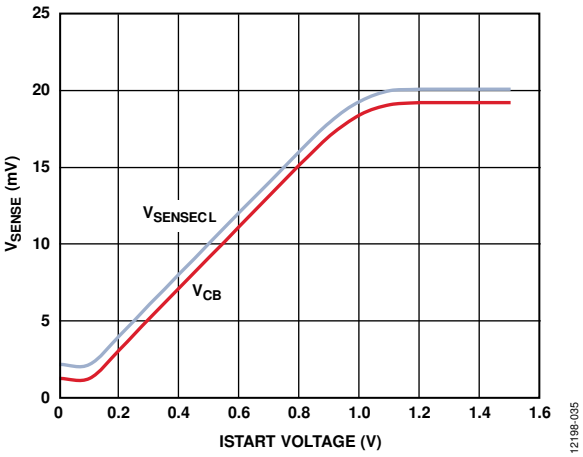


Figure 38. V_{SENSE} vs. ISTART Voltage

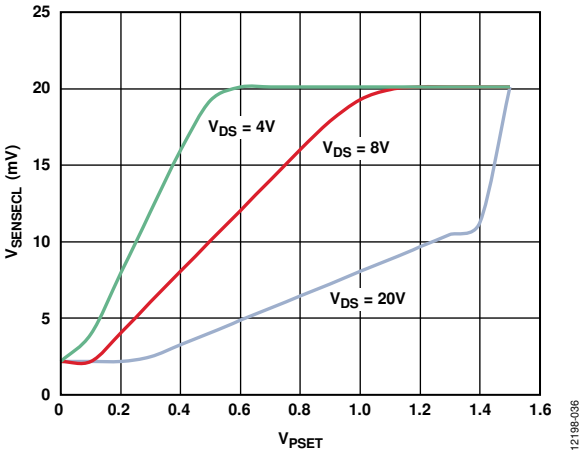


Figure 39. $V_{SENSECL}$ vs. V_{PSET}

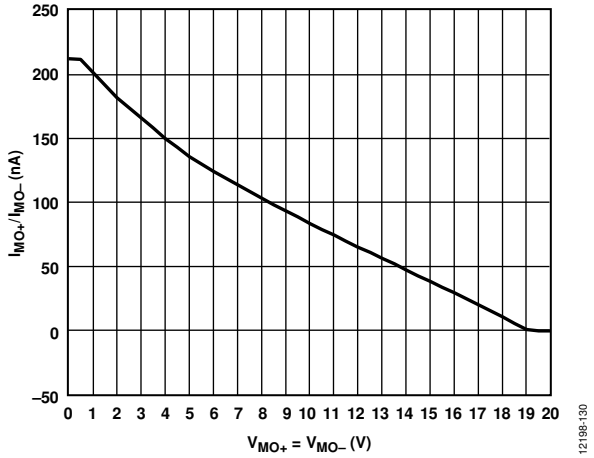


Figure 40. I_{MO+}/I_{MO-} vs. V_{MO+}/V_{MO-} with V_{CC} = 20 V

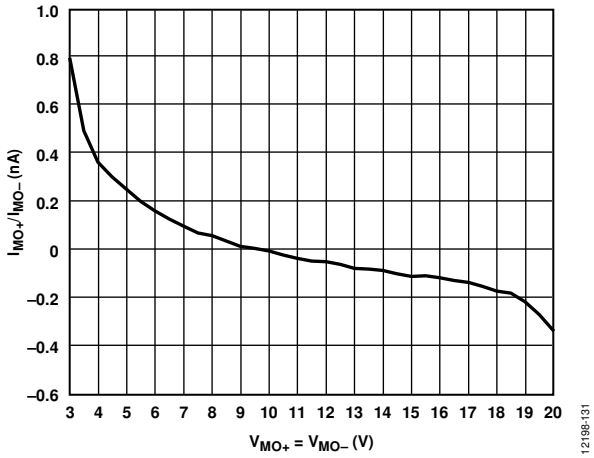


Figure 41. I_{MO+}/I_{MO-} vs. V_{MO+}/V_{MO-} with $V_{CC} = V_{MO+} = V_{MO-}$

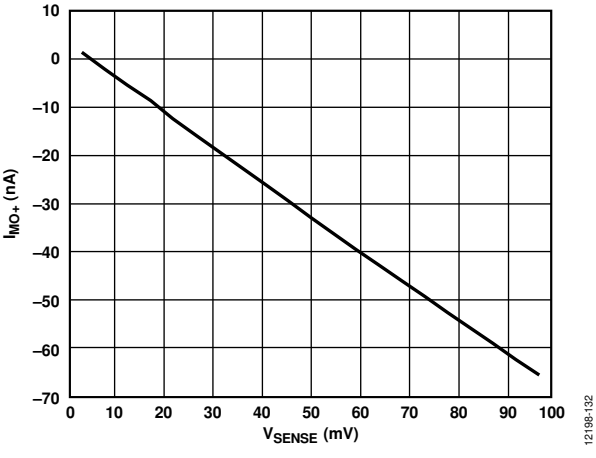


Figure 42. I_{MO+} vs. V_{SENSE} with $V_{CC} = V_{MO+}$ = 20 V

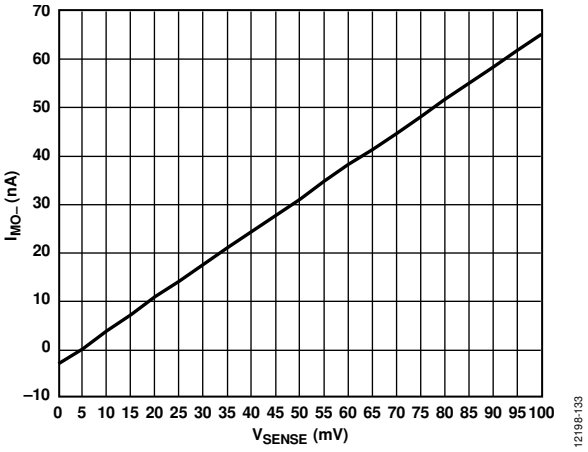


Figure 43. I_{MO-} vs. V_{SENSE} with $V_{CC} = V_{MO+} = 20$ V

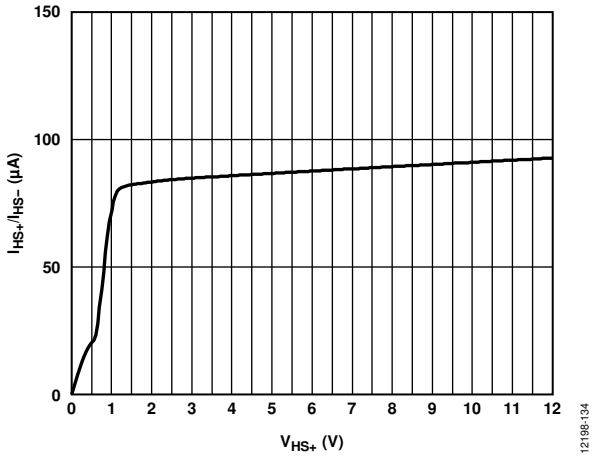


Figure 44. I_{HS+}/I_{HS-} vs. V_{HS+}

THEORY OF OPERATION

When circuit boards are inserted into a live backplane, discharged supply bypass capacitors draw large transient currents from the backplane power bus as they charge. These transient currents can cause permanent damage to connector pins, as well as dips on the backplane supply that can reset other boards in the system.

The ADM1278 is designed to control the powering on and off of a system in a controlled manner, allowing a board to be removed from, or inserted into, a live backplane by protecting it from excess currents. The ADM1278 can reside on the backplane or on the removable board.

POWERING THE ADM1278

A supply voltage from 4.5 V to 20 V is required to power the ADM1278 via the VCC pin. The VCC pin provides the majority of the bias current for the device; the remainder of the current needed to control the gate drive and to best regulate the V_{GS} voltage is supplied by the HS+ pin.

To ensure correct operation of the ADM1278, the voltage on the VCC pin must be greater than or equal to the voltage on the HS+ and MO+ pins. No sequencing of the VCC and HS+ rails is necessary. The HS+ pin can be as low as 2 V for normal operation, provided that a voltage of at least 4.5 V is connected to the VCC pin. In most applications, both the VCC and HS+ pins are connected to the same voltage rail, but they are connected via separate traces to prevent accuracy loss in the sense voltage measurement (see Figure 45).

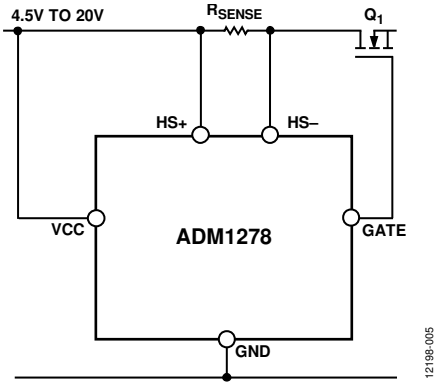


Figure 45. Powering the ADM1278

To protect the ADM1278 from unnecessary resets due to transient supply glitches, an external resistor and capacitor can be added, as shown in Figure 46. Choose the values of these components such that a time constant is provided that can filter any expected glitches. However, use a resistor that is small enough to keep voltage drops caused by quiescent current to a minimum. Unless a resistor is used to limit the inrush current, do not place a supply decoupling capacitor on the rail before the FET.

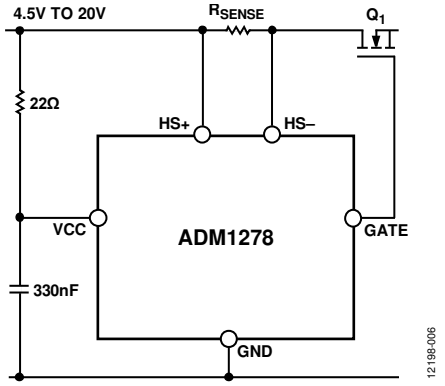


Figure 46. Transient Glitch Protection Using an RC Network

HOT SWAP CURRENT SENSE INPUTS

The load current is monitored by measuring the voltage drop across an external sense resistor, R_{SENSE} (see Figure 47). An internal current sense amplifier provides a gain of 50 to the voltage drop detected across R_{SENSE}. The result is compared to an internal reference and used by the hot swap control logic to detect when an overcurrent condition occurs.

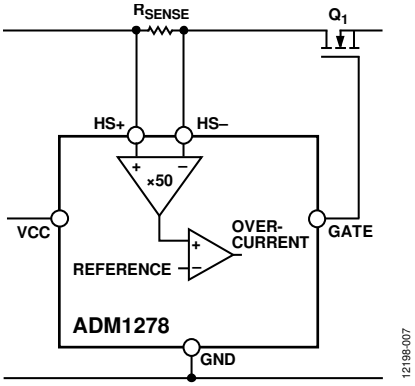


Figure 47. Hot Swap Current Sense Amplifier

The HS± inputs can be connected to multiple parallel sense resistors, which can affect the voltage drop detected by the ADM1278. The current flowing through the sense resistors creates an offset, resulting in reduced accuracy.

To achieve better accuracy, averaging resistors can be used to sum the current from the nodes of each sense resistor, as shown in Figure 48. A typical value for the averaging resistors is 10 Ω. The input current to each sense pin is matched to within 5 µA. This ensures that the same offset is observed by both sense inputs.