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ADM5120P/PX

Network Processor
Version AB

Communications

Never stop thinking

Edition 2005-11-09

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ADM5120P/PX Network Processor
CONFIDENTIAL
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Previous Version:

Page	Subjects (major changes since last revision)
	31-Oct-2005: Updated Registers and deleted reference to 200 MHz support
	12-Nov-2005:Updated Table 7-"MII Management"

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1 Product Overview

The following chapter gives an overview of the ADM5120P/PX.

1.1 Overview

ADM5120P/PX is a high performance, highly integrated, and highly flexible SOC (System-On-Chip) that facilitates the combined functions of a SOHO/SME Gateway, NAT Router, Print Server and VPN Gateway in one package. ADM5120P/PX enables the sharing of IP-based broadband services throughout the home/office using wired computers, entertainment equipment, printers, and other intelligent devices.

The ADM5120P/PX is the environmentally friendly 'green' package version.This is in compliance with Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment

Internally, the ADM5120P/PX ASIC consists of a high performance (227 MIPS) embedded MIPS CPU, an embedded switch engine, a 10/100M PHY, an embedded USB host, and interfaces for UART, SDRAM and Flash. The following diagram illustrates a system configuration that uses the supported functions/facilities of ADM5120P/PX

1.2 Features

The following describes the features of the ADM5120P/PX

1.2.1 ASIC Features

Description of ASIC features:

1.2.1.1 Processor

Processor features:

- MIPS 4Kc CPU
- Embedded cache, 8 Kbyte I-cache, 8 Kbyte D-cache
- Embedded memory management unit (MMU) – 32-entry TLB, organized as 16 entry pairs
- 175 MHz/227 MIPS

1.2.1.2 Networking

Networking features:

- 6 ports
- IEEE 802.3 Fast Ethernet
- 5 auto-MDIX (auto-crossover) twisted paired LAN interfaces, embedded 10/100M PHY
- 1 MII interface
- Flexible WAN port selection
- Embedded switch engine
- Embedded Data-buffer/Address-look-up table
- Look-up table read/write-able
- MAC layer security
- MAC clone solution
- MAC filtering, Bandwidth control
- Class of Services (CoS) with two priority levels
- Shared dynamic data buffer management, embedded SSRAM
- Port grouping VLAN (overlap-able)
- TCP/IP accelerator

1.2.1.3 Memory Interface

Memory features:

- SDRAM
- Two bank support (2 chip select pins)
- Each bank can support -- 1M x 32 up to 32M x 32bit (128M-byte)
- Flash
- NOR Flash boot
- NOR Flash: one banks support (1 chip select pin)
- NOR Flash: support – 1M x 8-bit, up to 1M x 32-bit (4M-byte)

1.2.1.4 System

- UART interface
- 4 GPIO pins
- USB 1.1 host
- Clock source
- 25 MHz crystal for 10/100
- 48 MHz crystal for USB
- 0.18 μ CMOS process
- 1.8 V/3.3 V dual power
- PQFP

1.2.2 Software Features

Description of software features:

- Linux/Nucleus Real-Time OS
- Linux-based and Nucleus-based turn key support
- Telnet
- IEEE 802.3 Ethernet Driver
- RS232 Driver for Console User Interface
- DHCP Server/Client
- PPP over Ethernet (PPPoE)
- Network Address Translation (NAT) for IP Address Mapping/Sharing/Security
- DNS Proxy
- Simple Network Time Protocol (SNTP)
- Firewall
- Web-Based Configuration: WEB and HTTP
- TFTP upload/download

1.2.3 Typical Applications

The typical applications of the ADM5120P/PX are:

- IEEE 802.3 SOHO/SME Gateway
- NAT Router
- Print Server (through USB1.1)

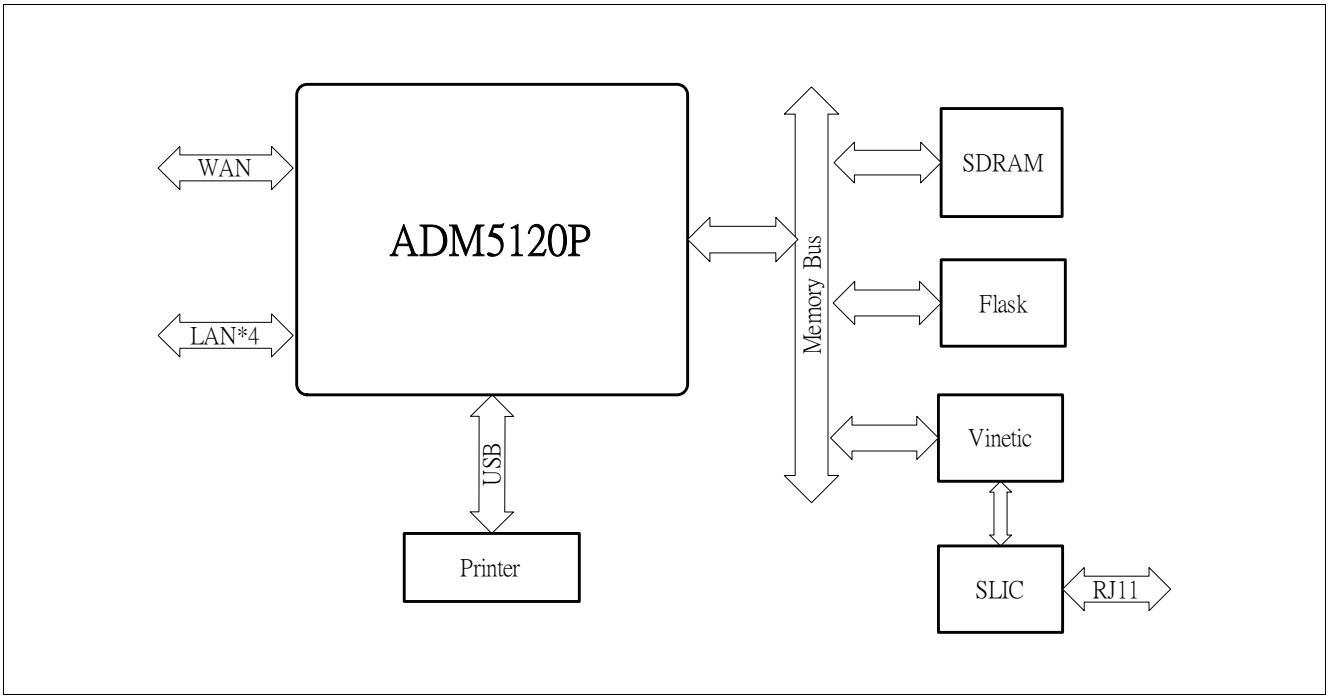

Figure 1 ADM5120P/PX Application

1.3 Conventions

The convention descriptions are described below:

1.3.1 Data Lengths

qword = 64 bits

dword = 32 bits

word = 16 bits

byte = 8 bits

nibble = 4 bits

2 Interface Description

2.1 Pin Description by Function

ADM5120P/PX pins are categorized into one of the following groups:

- **Section 2.1.4, ADM5120P/PX Network Media Connection**
- **Section 2.1.5, Clock for Network**
- **Section 2.1.6, LED**
- **Section 2.1.7, MII Management**
- **Section 2.1.8, Memory Bus**
- **Section 2.1.9, SDRAM Control Signals**
- **Section 2.1.10, UART**
- **Section 2.1.11 JTAG**
- **Section 2.1.12, General Purpose I/O (GPIO)**
- **Section 2.1.13, USB**
- **Section 2.1.14, External CS/INT/Wait**

2.1.1 Section

- **Section 2.1.15, Power and Ground**
- **Section 2.1.16, Regulator Interface**
- **Section 2.1.17, Miscellaneous**

Note: All default settings are 0.

2.1.2 Pin Diagram for P-FQFP-208-10 Package

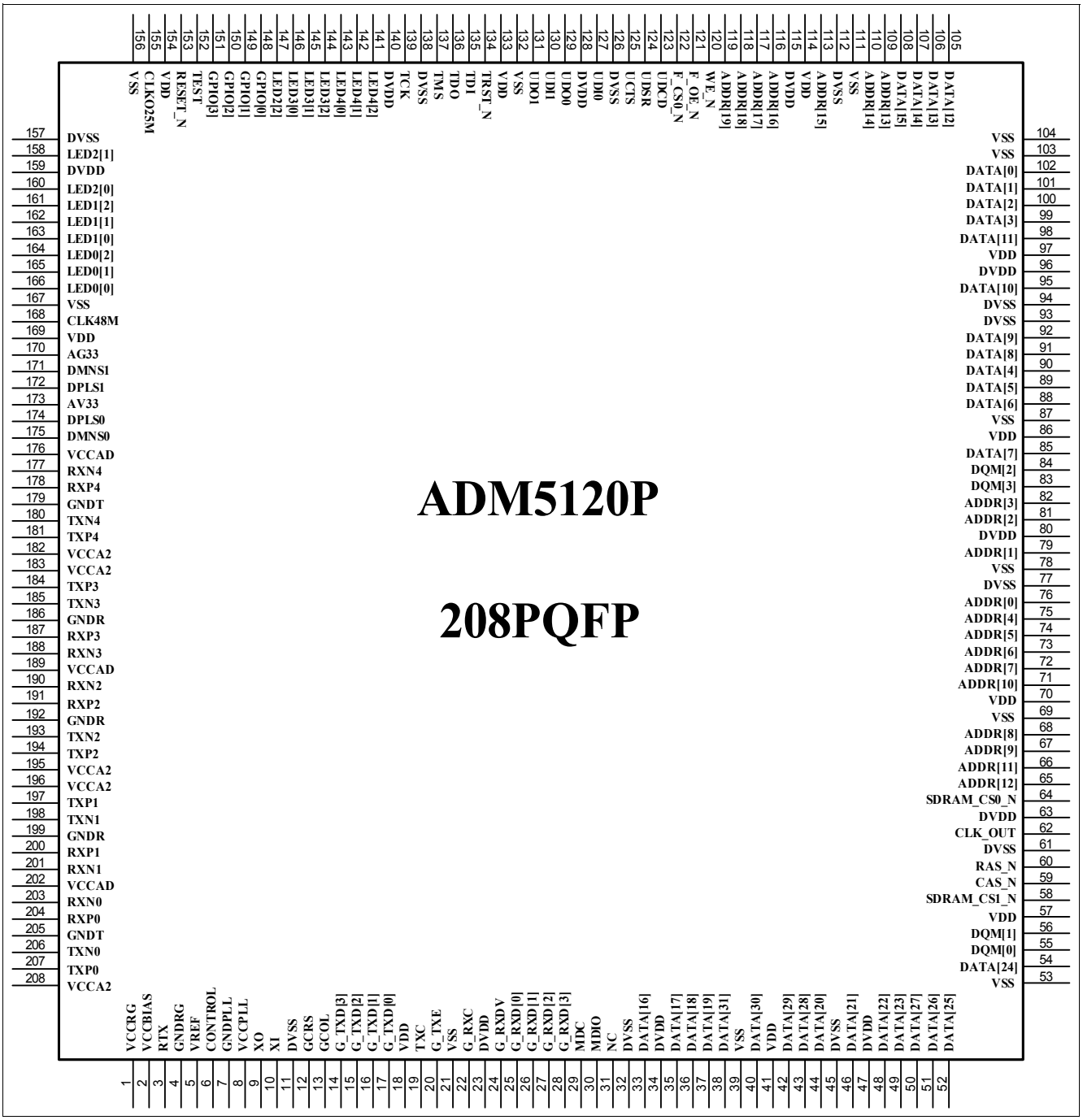

Figure 2 Pin Diagram for P-FQFP-208-10

2.1.3 Abbreviations

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU1	Pull up, 10 kΩ
PD1	Pull down, 10 kΩ
PD2	Pull down, 20 kΩ
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics
A	Analog Differential pair or Analog PAD

2.1.4 ADM5120P/PX Network Media Connection

Table 3 Network Media Connection

Ball No.	Name	Pin Type	Buffer Type	Function
178	RXP4	AI	A	**Receive Pair** Differential data is received on these pins.
187	RXP3			
191	RXP2			
200	RXP1			
204	RXP0			
177	RXN4			
188	RXN3			
190	RXN2			
201	RXN1			
203	RXN0			
181	TXP4	AO	A	**Transmit Pair** Differential data is transmitted on these pins.
184	TXP3			
194	TXP2			
197	TXP1			
207	TXP0			
180	TXN4			
185	TXN3			
193	TXN2			
198	TXN1			
206	TXN0			

2.1.5 Clock for Network

Table 4 Clock for Network

Ball No.	Name	Pin Type	Buffer Type	Function
9	XOI	O	A	**Crystal Clock Output** 25 MHz crystal output
10	XI	I	A	**External Clock Input** 25 MHz crystal input
3	RTX	I	A	**Reference Voltage**

2.1.6 LED

Table 5 LED

Ball No.	Name	Pin Type	Buffer Type	Function
141	LED4_2	O	PD	**LED 4** LED4_2 state, default = 1010, duplex/colLED4_1 state, default = 0101, speedLED4_0 state, default = 1001, link/activity
142	LED4_1			
143	LED4_0			
144	LED3_2	O	PD	**LED 3** LED3_2 state, default = 1010, duplex/colLED3_1 state, default = 0101, speedLED3_0 state, default = 1001, link/activity
145	LED3_1			
146	LED3_0			
147	LED2_2	O	PD	**LED 2** LED2_2 state, default = 1010, duplex/colLED2_1 state, default = 0101, speedLED2_0 state, default = 1001, link/activity
158	LED2_1			
160	LED2_0			
161	LED1_2	O	PD	**LED 1** LED1_2 state, default = 1010, duplex/colLED1_1 state, default = 0101, speedLED1_0 state, default = 1001, link/activity
162	LED1_1			
163	LED1_0			
164	LED0_2	O	PD	**LED 0** LED0_2 state, default = 1010, duplex/colLED0_1 state, default = 0101, speedLED0_0 state, default = 1001, link/activity
165	LED0_1			
166	LED0_0			

*Note: Registers, not hardware pins, control the LED display. There are 3 LEDs per port, and they can be programmed to any state, the programming information can be found in **Table 6** below.*

Table 6 LED Program

Function	State
GPIO_in (or GPIO_disable)	0000
GPIO_output_flash	0001
GPIO_output_1	0010
GPIO_output_0	0011
Link (steady)	0100
Speed (steady)	0101
Duplex (steady)	0110
Activity (flash)	0111
Collision (flash)	1000
Link+activity	1001
Duplex+collision	1010
10 M_link+activity	1011
100 M_link+activity	1100
Reserved	1101

Table 6 LED Program (cont'd)

Function	State
Reserved	1110
Reserved	1111

2.1.7 MII Management

Table 7 MII Management

Ball No.	Name	Pin Type	Buffer Type	Function
29	MDC	O	PP	**Clock Input MDIO** Runs at a 1 MHz frequency clock for MII port auto-negotiation result monitoring.
14	TXD_3	O		**Transmit Data** All internal pull down. 1. The force speed, duplex & flow control can be set by switch control register (B+14) 2. The reverse MII can only be set by switch control register (B+30)
15	TXD_2			
16	TXD_1			
17	TXD_0			
20	TXE	O		**Transmit Enable** Internal pull down.
24	RXDV	I	TTL/PU	**Receive Data Valid** Internal pull up.
28	RXD_3	I	TTL/PU	**Receive Data** Internal pull up.
27	RXD_2			
26	RXD_1			
25	RXD_0			
22	RXC	I	TTL/PD	**Receive Clock** Internal pull down.
19	TXC	I	TTL/PD	**Transmit Clock** Internal pull down.
12	CRS	I	TTL/PD	**Carrier Sense** Internal pull down.
13	COL	I	TTL/PD	**Collision** Internal pull down.
30	MDIO	BI	PD	**Internal Pull Down** Bi-directional serial pin used to write and read from the registers of the device.

2.1.8 Memory Bus

Table 8 Memory Bus

Ball No.	Name	Pin Type	Buffer Type	Function
38	DATA_31	BI	PD	**Data Bus 31-0** Internal pull down. Data bus for SDRAM, flash memory, and external device.
40	DATA_30			
42	DATA_29			
43	DATA_28			
50	DATA_27			
51	DATA_26			
52	DATA_25			
54	DATA_24			
49	DATA_23			
48	DATA_22			
46	DATA_21			
44	DATA_20			
37	DATA_19			
36	DATA_18			
35	DATA_17			
33	DATA_16			
108	DATA_15			
107	DATA_14			
106	DATA_13			
105	DATA_12			
98	DATA_11			
95	DATA_10			
92	DATA_9			
91	DATA_8			
85	DATA_7			
88	DATA_6			
89	DATA_5			
90	DATA_4			
99	DATA_3			
100	DATA_2			
101	DATA_1			
102	DATA_0			

Table 8 Memory Bus (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
119	ADDR_19	O	PD	**Address Bus 19** Address bus for SDRAM, flash memory, and external device. Internal pull down. Pull down = Little Endian. (default)
118	ADDR_18			**Address Bus 18-17** Internal pull down. Can be pulled up and down as following: 00_B boot in 8-bit mode (Flash memory) (default) 01_B boot in 16-bit mode 10_B boot in 32-bit mode 11_B Reserved
117	ADDR_17			
116	ADDR_16			**Address Bus 16-14** Test mode purpose. Normal mode = 000(Default)
113	ADDR_15			
110	ADDR_14			
109	ADDR_13			**Address Bus 13** Default value: 0 0_B PHY separate power on disable 1_B PHY separate power on enable
65	ADDR_12			**Address Bus 12** 0_B BGA package(Default) 1_B 208 PQFP package
66	ADDR_11			**Address Bus 11-5**
71	ADDR_10			
67	ADDR_9			
68	ADDR_8			
72	ADDR_7			
73	ADDR_6			
74	ADDR_5			
75	ADDR_4			**Address Bus 4-3** Can be pulled up and down as following: PLL frequency setting. 00_B 175 MHz (Default) 01_B Reserved $1X_B$ Reserved
82	ADDR_3			
81	ADDR_2			**Address Bus 2** 0_B Enable AutoMDIX 1_B Disable AutoMDIX (Default)
79	ADDR_1			**Address Bus 1** Default value: 0_B 0_B NAND boot disable 1_B NAND boot enable
76	ADDR_0			**Address Bus 0** Default value: 0_B 0_B Normal operation 1_B Simulation mode

2.1.9 SDRAM Control Signals

Table 9 SDRAM Control Signals

Ball No.	Name	Pin Type	Buffer Type	Function
62	CLK_OUT	O	TS	**Clock Out** SDRAM clock, the frequency is set by ADDR_4:3 *Note: 1=pull up, 0=pull down* 00_D 87.5 MHz (Default) 01_D Reserved $1X_B$ Reserved
121	F_OE_N	O	PP	**Output Enable for External Memory** Output enable for external memory banks, active low.
120	WE_N	O	PP	**Write Enable for External Memory** Write Enable for external memory banks and SDRAM.
122	F_CS0_N	O	PP	**Chip Select for External Memory** Chip select for external memory, like flash, bank0, active low.
60	RAS_N	O	PP	**Raw Address Strobe** Raw address strobe, active low.
64	SD_RAM_CS0_N	O	PP	**SDRAM Chip Select 0** SDRAM chip select 0.
59	CAS_N	O	PP	**Column Address Strobe** Column address strobe, active low.
58	SD_RAM_CS1_N	O	PP	**SDRAM Chip Select 1** SDRAM chip select 1.
83	DQM_3	O	PD	**Data Mask Output to SDRAM**
84	DQM_2			
56	DQM_1			
55	DQM_0			

2.1.10 UART

Table 10 UART

Ball No.	Name	Pin Type	Buffer Type	Function
123	UDCD	I	PD	**Data Carrier Detect** UART0 Data carrier detect (modem status input), active low.
124	UDSR			**Data Set Ready** UART0 Data set ready (modem status input), active low.
125	UCTS			**Clear to Send** UART0 clear to send (modem status input), active low.
127	UDI0			**Receive Serial Data Input** UART0 receive serial data input, Internal pull down.
129	UDO0	O		**Transmit Serial Data Output** UART0 transmit serial data output.
130	UDI1	I		**Receive Serial Data Input** UART1 receive serial data input, Internal pull down.
131	UDO1	O		**Transmit Serial Data Output** UART1 transmit serial data output.

2.1.11 JTAG

Table 11 JTAG

Ball No.	Name	Pin Type	Buffer Type	Function
139	TCK	I	PD	**Test Clock** JTAG test clock, Internal pull down.
137	TMS			**Test Mode Select** JTAG test mode select, Internal pull down.
136	TDO	O		**Test Data Out** JTAG test data out.
135	TDI	I		**Test Data In** JTAG test data in, Internal pull down.
134	TRST_N	I	TTL	**Asynchronous Reset** JTAG asynchronous reset (active low).

2.1.12 General Purpose I/O (GPIO)

Table 12 General Purpose I/O (GPIO)

Ball No.	Name	Pin Type	Buffer Type	Function
151	GPIO_3	BI	PD	**BI General Purpose I/O Pin** GPIO_3:0 are internal pull down.
150	GPIO_2			
149	GPIO_1			
148	GPIO_0			

2.1.13 USB

Table 13 USB

Ball No.	Name	Pin Type	Buffer Type	Function
171	DMNS1	BI	A	**Data- of USB Port1** Differential data bus conforming to the USB 1.1.
172	DPLS1			**Data+ of USB Port1** Differential data bus conforming to the USB 1.1.
175	DMNS0			**Data- of USB Port0** Differential data bus conforming to the USB 1.1.
174	DPLS0			**Data+ of USB Port0** Differential data bus conforming to the USB 1.1.
168	CLK48M	I	TTL	**USB Clock Input**

2.1.14 External CS/INT/Wait

Table 14 External CS/INT/Wait

Ball No.	Name	Pin Type	Buffer Type	Function
148	$\overline{\text{WAIT}}$	I	TTL	**WAIT** $\overline{\text{WAIT}}$ is available in switch control register **GPIO_conf2**, bit **CSX0** and **CSX1** and **EW**. When CSX is active and MPMC is programmable then wait_state will time-out, then check the $\overline{\text{WAIT}}$ if high, then complete the access if low, then wait until $\overline{\text{WAIT}}$ goes high.
150	INTX0	I		**External Interrupt Input 0** External interrupt input 0, active high, available if en_csx0_intx0 enable in the switch control register GPIO_config2 (B+BC), bit[4].
149	$\overline{\text{CSX0}}$	O	TS	**External Chip Select 0** External chip select 0, active low, available if en_csx0_intx0 is enabled in the switch control register **GPIO_conf2** bit[4] **CSX0**.
151	$\overline{\text{CSX1}}$	O	TS	**External Chip Select 1** External chip select 1, active low, available if en_csx1_intx1is enabled in the switch control register GPIO_config2 (B+BC), bit[5].

2.1.15 Power and Ground

Table 15 Power and Ground

Ball No.	Name	Pin Type	Buffer Type	Function
18, 41, 57, 70, 86, 97, 114, 133, 154, 169	VDD		A	**Positive Power for Digital Core, 1.8 V**
23, 34, 47, 63, 80, 96, 115, 128, 140, 159	DVDD		A	**Positive Power for I/O, 3.3 V**
182, 183, 195, 196, 208	VDDTS2		A	**Positive Power for Analog Circuitry, 1.8 V**
176, 189, 202	VCCAD		A	**Positive Power for Analog Circuitry, 3.3 V**