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Low Voltage Supervisory Circuits with Watchdog and Manual Reset in 5-Lead SOT-23

Data Sheet

ADM6823/ADM6824/ADM6825

FEATURES

- Precision low voltage monitoring
- 9 reset threshold options: 1.58 V to 4.63 V
- 140 ms (minimum) reset timeout
- Watchdog timer with 1.6 sec timeout
- Manual reset input
- Reset output stages
  - Push-pull active-low
  - Open-drain active-low
  - Push-pull active-high
- Low power consumption: 7 µA
- Guaranteed reset output valid to V_{CC} = 1 V
- Power supply glitch immunity
- Specified from −40°C to +125°C
- 5-lead SOT-23 package

APPLICATIONS

- Microprocessor systems
- Computers
- Controllers
- Intelligent instruments
- Portable equipment

FUNCTIONAL BLOCK DIAGRAM

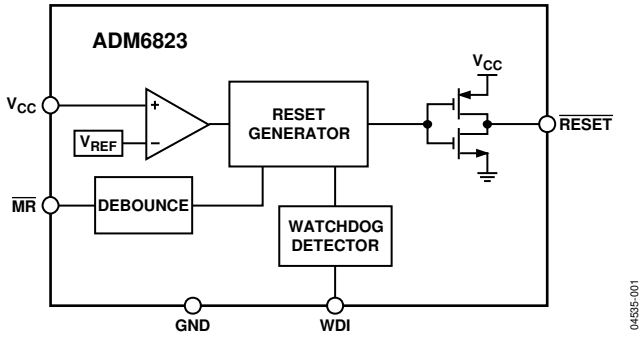

Figure 1.

GENERAL DESCRIPTION

The ADM6823/ADM6824/ADM6825 are supervisory circuits that monitor power supply voltage levels and code execution integrity in microprocessor-based systems. As well as providing power-on reset signals, an on-chip watchdog timer can reset the microprocessor if it fails to strobe within a preset timeout period. A reset signal can also be asserted by means of an external push-button through a manual reset input. The parts feature different combinations of watchdog input and manual reset input and output stage configurations, as shown in Table 1.

Each part is available in nine reset threshold options, ranging from 1.58 V to 4.63 V. The reset and watchdog timeout periods are fixed at 140 ms (minimum) and 1.6 sec (typical), respectively.

The ADM6823/ADM6824/ADM6825 are available in 5-lead SOT-23 packages and typically consume only 7 µA, making them suitable for use in low power, portable applications.

Table 1. Selection Table

Part No.	Watchdog Timer	Manual Reset	Output Stage	
			$\overline{\text{RESET}}$	RESET
ADM6823	Yes	Yes	Push-Pull	
ADM6824	Yes		Push-Pull	Push-Pull
ADM6825		Yes	Push-Pull	Push-Pull

Rev. B

Document Feedback

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Tel: 781.329.4700
Technical Support www.analog.com

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Updated Outline Dimensions ... 11
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9/12—Rev. 0 to Rev. A

Removed ADM6821/ADM6822 (Throughout) ... 1
Updated Outline Dimensions ... 11
Changes to Ordering Guide ... 11
Added Automotive Products Section ... 11

6/05—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 4.5 V to 5.5 V for ADM682xL/ADM682xM; V_{CC} = 2.7 V to 3.6 V for ADM682xT/ADM682xS/ADM682xR; V_{CC} = 2.1 V to 2.75 V for ADM682xZ/ADM682xY; V_{CC} = 1.53 V to 2.0 V for ADM682xW/ADM682xV; T_A = –40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
V_{CC} Operating Voltage Range	1		5.5	V	
Supply Current		10	20	µA	WDI and $\overline{MR}$ unconnected, V_{CC} = 5.5 V
		7	16	µA	WDI and $\overline{MR}$ unconnected, V_{CC} = 3.6 V
RESET THRESHOLD VOLTAGE					
ADM682xL	4.50	4.63	4.75	V	
ADM682xM	4.25	4.38	4.50	V	
ADM682xT	3.00	3.08	3.15	V	
ADM682xS	2.85	2.93	3.00	V	
ADM682xR	2.55	2.63	2.70	V	
ADM682xZ	2.25	2.32	2.38	V	
ADM682xY	2.12	2.19	2.25	V	
ADM682xW	1.62	1.67	1.71	V	
ADM682xV	1.52	1.58	1.62	V	
RESET THRESHOLD TEMPERATURE COEFFICIENT		60		ppm/°C	
RESET THRESHOLD HYSTERESIS		$2 \times V_{TH}$		mV	
V_{CC} TO RESET DELAY		20		µs	$V_{TH} - V_{CC}$ = 100 mV
RESET TIMEOUT PERIOD	140	200	280	ms	
$\overline{RESET}$ OUTPUT VOLTAGE					
V_{OL} (Push-Pull or Open-Drain)			0.3	V	$V_{CC} \geq$ 1 V, I_{SINK} = 50 µA
			0.3	V	$V_{CC} \geq$ 1.2 V, I_{SINK} = 100 µA
			0.3	V	$V_{CC} \geq$ 2.55 V, I_{SINK} = 1.2 mA
			0.4	V	$V_{CC} \geq$ 4.25 V, I_{SINK} = 3.2 mA
V_{OH} (Push-Pull Only)	$0.8 \times V_{CC}$			V	$V_{CC} \geq$ 1.8 V, I_{SOURCE} = 200 µA
	$0.8 \times V_{CC}$			V	$V_{CC} \geq$ 3.15 V, I_{SOURCE} = 500 µA
	$0.8 \times V_{CC}$			V	$V_{CC} \geq$ 4.75 V, I_{SOURCE} = 800 µA
$\overline{RESET}$ OUTPUT LEAKAGE CURRENT (OPEN-DRAIN ONLY)			1	µA	$\overline{RESET}$ not asserted
RESET OUTPUT VOLTAGE (PUSH-PULL ONLY)					
V_{OH}	$0.8 \times V_{CC}$			V	$V_{CC} \geq$ 1 V, I_{SOURCE} = 1 µA
	$0.8 \times V_{CC}$			V	$V_{CC} \geq$ 1.5 V, I_{SOURCE} = 100 µA
	$0.8 \times V_{CC}$			V	$V_{CC} \geq$ 2.55 V, I_{SOURCE} = 500 µA
	$0.8 \times V_{CC}$			V	$V_{CC} \geq$ 4.25 V, I_{SOURCE} = 800 µA
V_{OL}			0.3	V	$V_{CC} \geq$ 1.8 V, I_{SINK} = 500 µA
			0.3	V	$V_{CC} \geq$ 3.15 V, I_{SINK} = 1.2 mA
			0.4	V	$V_{CC} \geq$ 4.75 V, I_{SINK} = 3.2 mA
MANUAL RESET INPUT (ADM6823/ADM6825)					
$\overline{MR}$ Input Threshold					
V_{IL}			$0.3 \times V_{CC}$	V	
V_{IH}	$0.7 \times V_{CC}$			V	
$\overline{MR}$ Input Pulse Width	1			µs	
$\overline{MR}$ Glitch Rejection		100		ns	
$\overline{MR}$ to Reset Delay		200		ns	
$\overline{MR}$ Pull-Up Resistance	25	50	75	kΩ	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
WATCHDOG INPUT (ADM6823/ADM6824)					
Watchdog Timeout Period	1.12	1.6	2.40	sec	
WDI Pulse Width	50			ns	
WDI Input Threshold					
V_{IL}			$0.3 \times V_{CC}$	V	
V_{IH}	$0.7 \times V_{CC}$			V	
WDI Input Current		120	160	µA	$V_{WDI} = V_{CC}$
	−20	−15		µA	$V_{WDI} = 0$

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC}	−0.3 V to +6 V
Output Current (RESET, $\overline{\text{RESET}}$)	20 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
θ_{JA} Thermal Impedance	170°C/W
Soldering Temperature	
Sn/Pb	240°C, 30 sec
RoHS Compliant	260°C, 40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

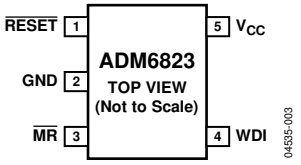


Figure 2. ADM6823 Pin Configuration

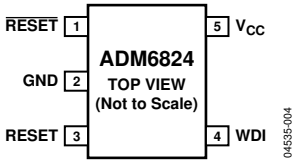


Figure 3. ADM6824 Pin Configuration

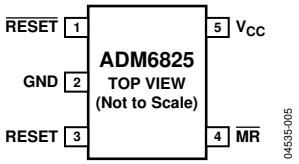


Figure 4. ADM6825 Pin Configuration

Table 4. Pin Function Descriptions

Pin No				
ADM6823	**ADM6824**	**ADM6825**	**Mnemonic**	**Description**
1	1	1	$\overline{\text{RESET}}$	Active-Low Reset Output. Asserted whenever V_{CC} is below the reset threshold, V_{TH}. Push-Pull Output Stage for the ADM6823/ADM6824/ADM6825.
2	2	2	GND	Ground.
3			$\overline{\text{MR}}$	Manual Reset Input. This is an active-low input, which, when forced low for at least 1 µs, generates a reset. It features a 50 kΩ internal pull-up.
	3	3	RESET	Active-High Push-Pull Reset Output.
4	4		WDI	Watchdog Input. Generates a reset if the voltage on the pin remains low or high for the duration of the watchdog timeout. The timer is cleared if a logic transition occurs on this pin or if a reset is generated.
		4	$\overline{\text{MR}}$	Manual Reset Input.
5	5	5	V_{CC}	Power Supply Voltage Being Monitored.

TYPICAL PERFORMANCE CHARACTERISTICS

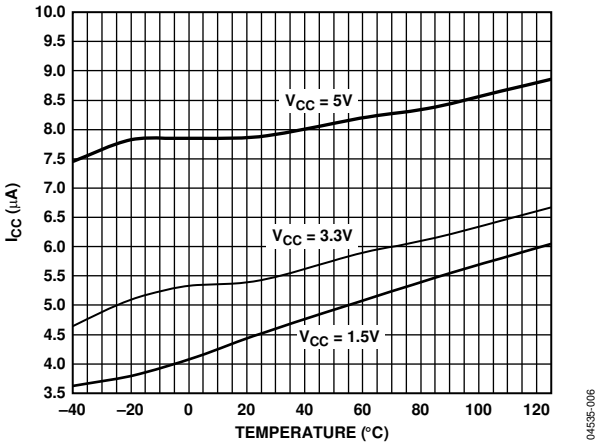


Figure 5. Supply Current vs. Temperature

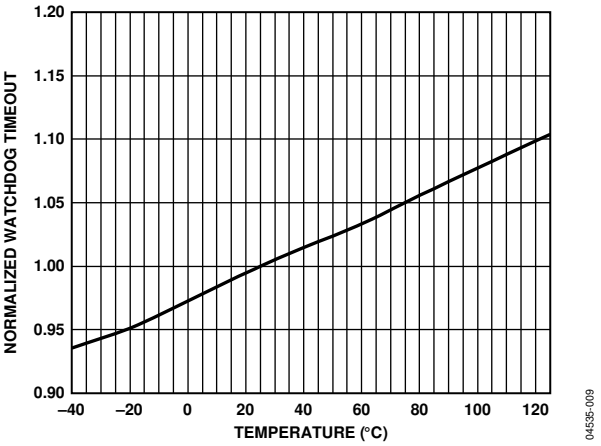


Figure 8. Normalized Watchdog Timeout Period vs. Temperature

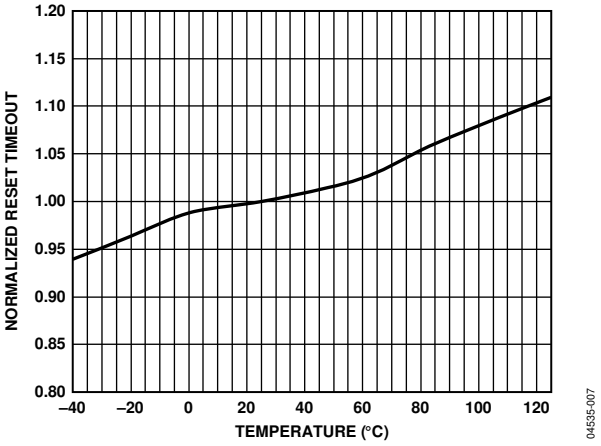


Figure 6. Normalized RESET Timeout Period vs. Temperature

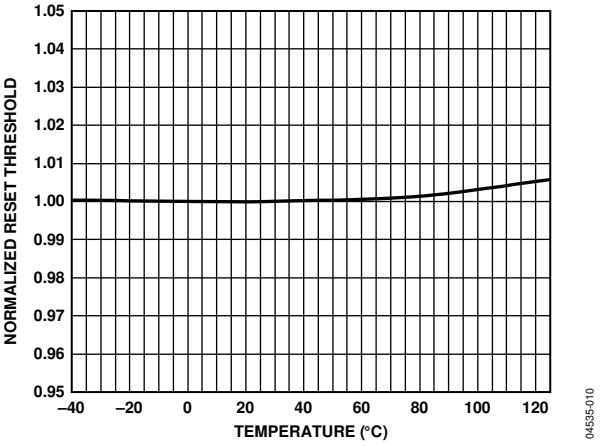


Figure 9. Normalized RESET Threshold vs. Temperature

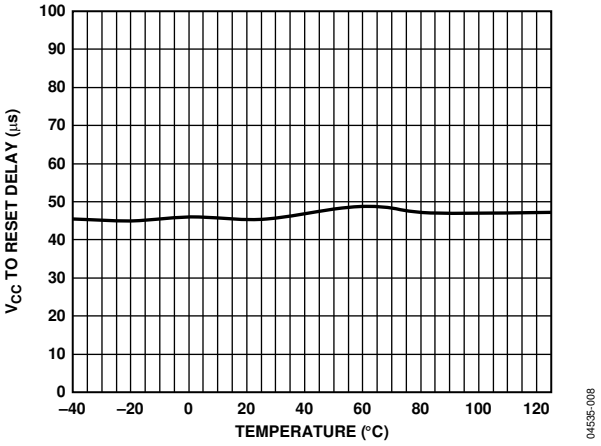


Figure 7. V_{CC} to RESET Output Delay vs. Temperature

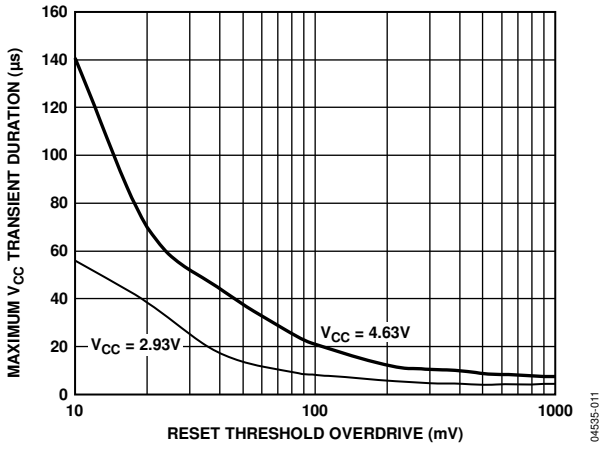


Figure 10. Maximum V_{CC} Transient Duration vs. RESET Threshold Overdrive

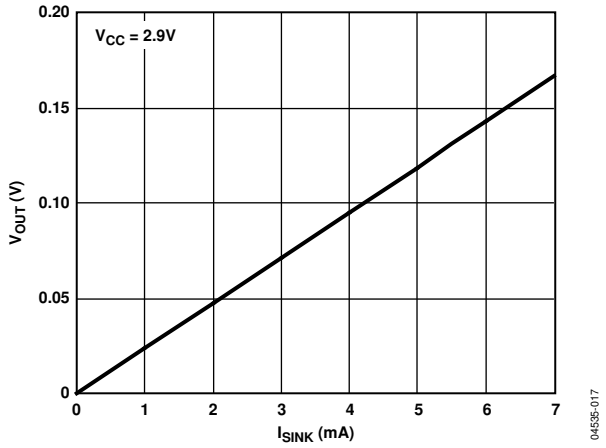


Figure 11. Voltage Output Low vs. I_{SINK}

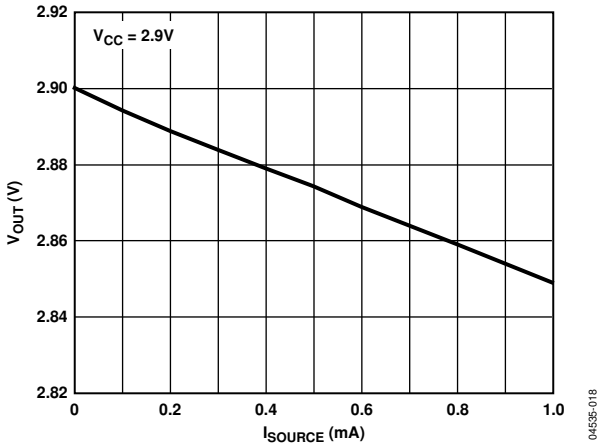


Figure 12. Voltage Output High vs. I_{SOURCE}

THEORY OF OPERATION

The ADM6823/ADM6824/ADM6825 provide microprocessor supply voltage supervision by controlling the microprocessor's reset input. Code execution errors are avoided during power-up, power-down, and brownout conditions by asserting a reset signal when the supply voltage is below a preset threshold. In addition, the ADM6823/ADM6824/ADM6825 allow supply voltage stabilization with a fixed timeout before the reset deasserts after the supply voltage rises above the threshold.

Problems with microprocessor code execution can be monitored and corrected with a watchdog timer (ADM6823/ADM6824). When watchdog strobe instructions are included in microprocessor code, a watchdog timer detects if the microprocessor code breaks down or becomes stuck in an infinite loop. If this happens, the watchdog timer asserts a reset pulse, which restarts the microprocessor in a known state.

If the user detects a problem with the system's operation, a manual reset input is available (ADM6823/ADM6825) to reset the microprocessor by means of an external push-button, for example.

RESET OUTPUT

The ADM6823 features an active-low push-pull output. The ADM6824/ADM6825 feature dual active-low and active-high push-pull reset outputs. For active-low and active-high outputs, the reset signal is guaranteed to be logic low and logic high, respectively, for V_{CC} down to 1 V.

The reset output is asserted when V_{CC} is below the reset threshold (V_{TH}), when $\overline{MR}$ is driven low, or when WDI is not serviced within the watchdog timeout period (t_{WD}). Reset remains asserted for the duration of the reset active timeout period (t_{RP}) after V_{CC} rises above the reset threshold, after $\overline{MR}$ transitions from low to high, or after the watchdog timer times out. Figure 13 shows the reset outputs.

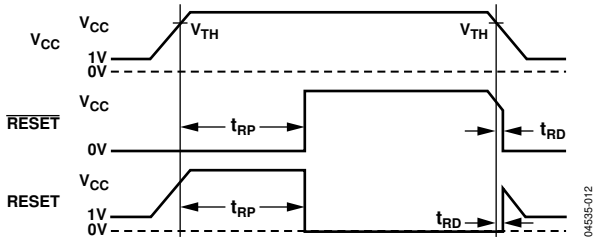


Figure 13. Reset Timing Diagram

MANUAL RESET INPUT

The ADM6823/ADM6825 feature a manual reset input ($\overline{MR}$), which, when driven low, asserts the reset output. When $\overline{MR}$ transitions from low to high, reset remains asserted for the duration of the reset active timeout period before deasserting. The $\overline{MR}$ input has a 50 kΩ internal pull-up so that the input is always high when unconnected. An external push-button switch can be connected between $\overline{MR}$ and ground so that the user can generate a reset. Debounce circuitry is integrated on-chip for this purpose. Noise immunity is provided on the $\overline{MR}$ input, and fast, negative-going transients of up to 100 ns (typical) are ignored. A 0.1 µF capacitor between $\overline{MR}$ and ground provides additional noise immunity.

WATCHDOG INPUT

The ADM6823/ADM6824 feature a watchdog timer, which monitors microprocessor activity. A timer circuit is cleared with every low-to-high or high-to-low logic transition on the watchdog input pin (WDI), which detects pulses as short as 50 ns. If the timer counts through the preset watchdog timeout period (t_{WD}), reset is asserted. The microprocessor is required to toggle the WDI pin to avoid being reset. Failure of the microprocessor to toggle WDI within the timeout period therefore indicates a code execution error, and the reset pulse generated restarts the microprocessor in a known state.

In addition to logic transitions on WDI, the watchdog timer is also cleared by a reset assertion due to an undervoltage condition on V_{CC} or $\overline{MR}$ being pulled low. When reset is asserted, the watchdog timer is cleared and does not begin counting again until reset deassserts. The watchdog timer can be disabled by leaving WDI floating or by three-stating the WDI driver.

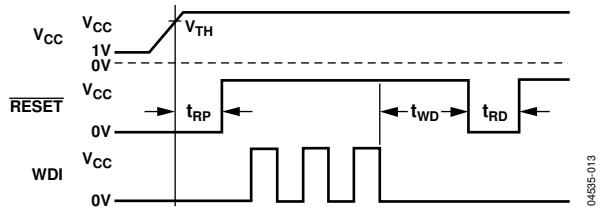


Figure 14. Watchdog Timing Diagram

APPLICATION INFORMATION

WATCHDOG INPUT CURRENT

To minimize watchdog input current (and minimize overall power consumption), leave WDI low for the majority of the watchdog timeout period. When driven high, WDI can draw as much as 160 µA. Pulsing WDI low-high-low at a low duty cycle reduces the effect of the large input current. When WDI is unconnected, a window comparator disconnects the watchdog timer from the reset output circuitry so that reset is not asserted when the watchdog timer times out.

NEGATIVE-GOING V_{CC} TRANSIENTS

To avoid unnecessary resets caused by fast power supply transients, the ADM6823/ADM6824/ADM6825 are equipped with glitch rejection circuitry. The typical performance characteristic in Figure 10 plots V_{CC} transient duration vs. the transient magnitude. The curves show combinations of transient magnitude and duration for which a reset is not generated for the 4.63 V and 2.93 V reset threshold parts. For example, with the 2.93 V threshold, a transient that goes 100 mV below the threshold and lasts 8 µs typically does not cause a reset, but if the transient is any bigger in magnitude or duration, a reset is generated. An optional 0.1 µF bypass capacitor mounted close to V_{CC} provides additional glitch rejection.

ENSURING RESET VALID TO V_{CC} = 0 V

Both active-low and active-high reset outputs are guaranteed to be valid for V_{CC} as low as 1 V. However, by using an external resistor with push-pull configured reset outputs, valid outputs for V_{CC} as low as 0 V are possible. For an active-low reset output, a resistor connected between $\overline{\text{RESET}}$ and ground pulls the output low when it is unable to sink current. For the active-high case, a resistor connected between RESET and V_{CC} pulls the output high when it is unable to source current. A large resistance such as 100 kΩ should be used so that it does not overload the reset output when V_{CC} is above 1 V.

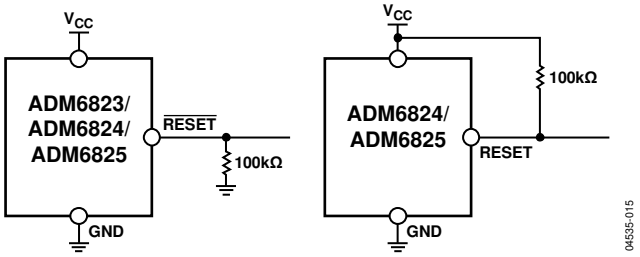


Figure 15. Ensuring Reset Valid to V_{CC} = 0 V

WATCHDOG SOFTWARE CONSIDERATIONS

In implementing the microprocessor's watchdog strobe code, quickly switching WDI low-high and then high-low (minimizing WDI high time) is desirable for current consumption reasons. However, a more effective way of using the watchdog function can be considered.

A low-high-low WDI pulse within a given subroutine prevents the watchdog from timing out. However, if the subroutine becomes stuck in an infinite loop, the watchdog could not detect this because the subroutine continues to toggle WDI. A more effective coding scheme for detecting this error involves using a slightly longer watchdog timeout. In the program that calls the subroutine, WDI is set high. The subroutine sets WDI low when it is called. If the program executes without error, WDI is toggled high and low with every loop of the program. If the subroutine enters an infinite loop, WDI is kept low, the watchdog times out, and the microprocessor is reset.

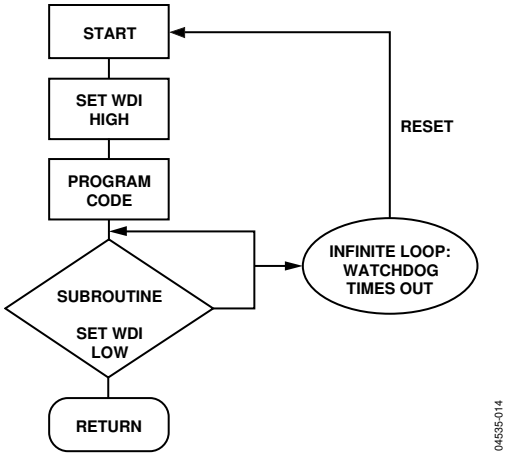


Figure 16. Watchdog Flow Diagram

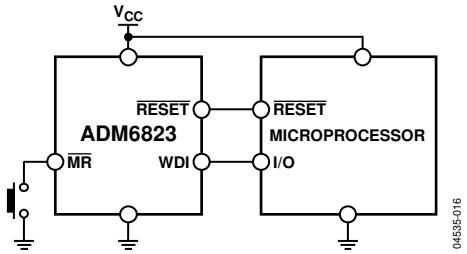
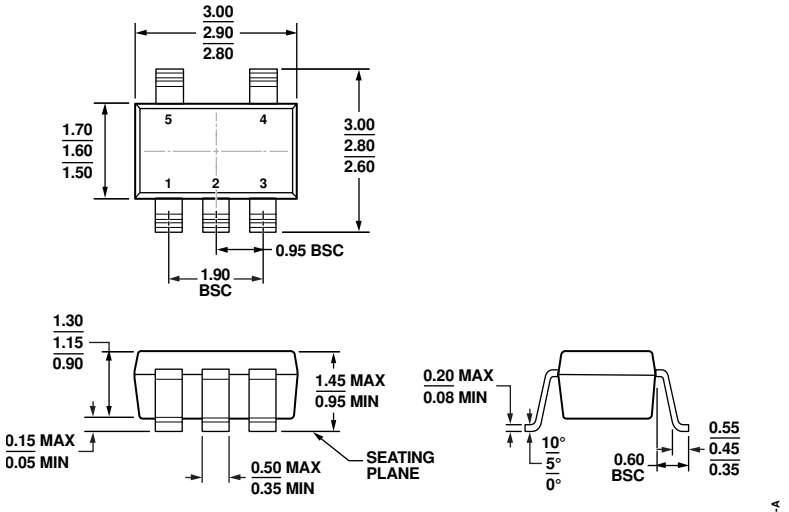


Figure 17. Typical Application Circuit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AA

Figure 18. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters

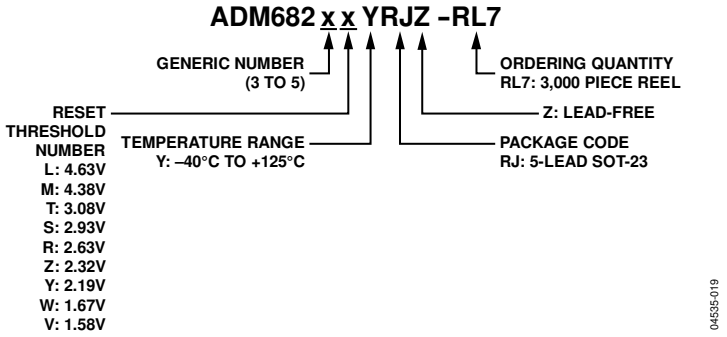


Figure 19. Ordering Code Structure

ORDERING GUIDE

Model[1, 2]	Reset Threshold (V)	Reset Timeout (ms)	Temperature Range	Quantity	Package Description	Package Option	Branding
ADM6823RYRJZ-RL7	2.63	140	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	N0Q
ADM6823SYRJ-R7	2.93	140	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	N0C
ADM6823SYRJZ-RL7	2.93	140	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	N0Q
ADM6823TYRJ-R7	3.08	140	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	N0C
ADM6823TYRJZ-RL7	3.08	140	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	N0Q
ADM6823VYRJZ-RL7	1.58	140	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	N0Q
ADM6823WYRJZ-RL7	1.67	140	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	N0Q
ADM6823ZYRJZ-RL7	2.32	140	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	N0Q
ADM6824TYRJZ-R7	3.08	140	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	N0D
ADM6825TYRJZ-R7	3.08	140	−40°C to +125°C	3k	5-Lead SOT-23	RJ-5	N0E

[1] Z = RoHS Compliant Part.
[2] If ordering nonstandard models, complete the ordering code shown in Figure 19 by inserting the part number and reset threshold suffixes. Contact Sales for availability of nonstandard models.

D04535-0-2/13(B)