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# ADM6918/X

## 18 port 10/100 Mbps Ethernet Switch Controller

ADM6918/X

Communications

Never stop thinking

**Edition 2005-11-08**

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**81669 München, Germany**



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**Revision History: 2005-11-08, Rev 1.01**

**Previous Version:**

| Page/Date | Subjects (major changes since last revision) |
|---|---|
| 2003-11-25 | Rev. 1.0: First release of ADM6918/X |
| 2005-09-09 | Changed to the new Infineon format |
| 2005-09-09 | Rev. 1.0 changed to Rev. 1.01 |
| 2005-11-03 | Minor change. Included Green package information |
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**Trademarks**

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# 1 Product Overview

## 1.1 Overview

The ADM6918/X is a high performance/low cost, eighteen-port 10/100 Mbps Ethernet Switch Controller with all ports supporting 10/100 Mbps full duplex switch function. The ADM6918/X is intended for applications to stand alone the bridge for the low cost ether-switch market. The ADM6918X is the environmentally friendly “green” package version. ADM6918/X can be programmed trunking port active. The trunking port can be connected to server or stacking two switch boxes to enhance the performance.

The ADM6918/X also supports back-pressure in half duplex mode and 802.3x flow control in full duplex mode. When back-pressure is enabled, and there is no receiving buffer available for the incoming packet, the ADM6918/X will force a JAM pattern on the receiving port in half duplex mode and transmit the 802.3x packet back to receiving end in full duplex mode.

An intelligent address recognition algorithm makes ADM6918/X to recognize up to 4096 different MAC addresses and enables filtering and forwarding at full wire speed.

The ADM6918/X has embedded SRAM for the proprietary buffer management. The SRAM is used to store the incoming/outgoing packets. These buffers provide elastic storage for transferring data between low-speed and high-speed segments and buffers are efficiently allocated to improve the efficiency.

## 1.2 Features

- Supports sixteen 10/100M auto-detect Half/Full duplex switch ports with SS-SMII interface and two 10/100M Half/Full duplex port with RMII/MII interface
- Supports up to 4096 MAC addresses table (4-way hashing)
- Supports two queue for QOS (1:2 or 1:4 or 1:8 or 1:16)
- Supports Port-base, 802.1p and IP TOS priority
- Supports store & forward architecture and Performs forwarding and filtering at non-blocking full wire speed
- Supports buffer allocation with 256 bytes each
- Supports aging function and 802.3x flow control for full duplex and back-pressure function for half duplex operation in case buffer is full
- Supports packet length up to 1536 bytes
- Supports Congestion Flow Control
- Broadcast storm filter and Alert LED
- Port-base VLAN and adjustable VLAN to support up to 32 VLAN group
- Serial CPU interface for counter and port status output
- CPU can see-through to access PHY
- Flexible port trunking on fault tolerance and load balance
- Per port 32bits smart counter for Rx/Tx byte/packet count, error count and collision count
- Rate-limit control (64K/128K/256K/512K/1M/4M/10M/20M)
- Per port auto learning enable/disable and if disable, forward non-learned packet to CPU]
- MAC address table accessible (in each entry, reserve one bit for CPU to enable/disable aging out)
- Forward special multicast, BPDU, GMRP, GVRP and IGMP packets to CPU port
- 128 pin QFP package with 3.3 V/1.8V power supply

## 1.3 Package Information

| Product Name | Product Type | Package | Ordering Number |
|---|---|---|---|
| Ethernet Switch Controller | ADM6918/X | P-FQFP-128-1 | Q67801H 70A202[1)] |

1) contact Infineon for the updated ordering information

## 1.4 Data Lengths

- qword: 64-bits
- dword: 32-bits
- word: 16-bits
- byte: 8 bits
- nibble: 4 bits

## 1.5 Block Diagram

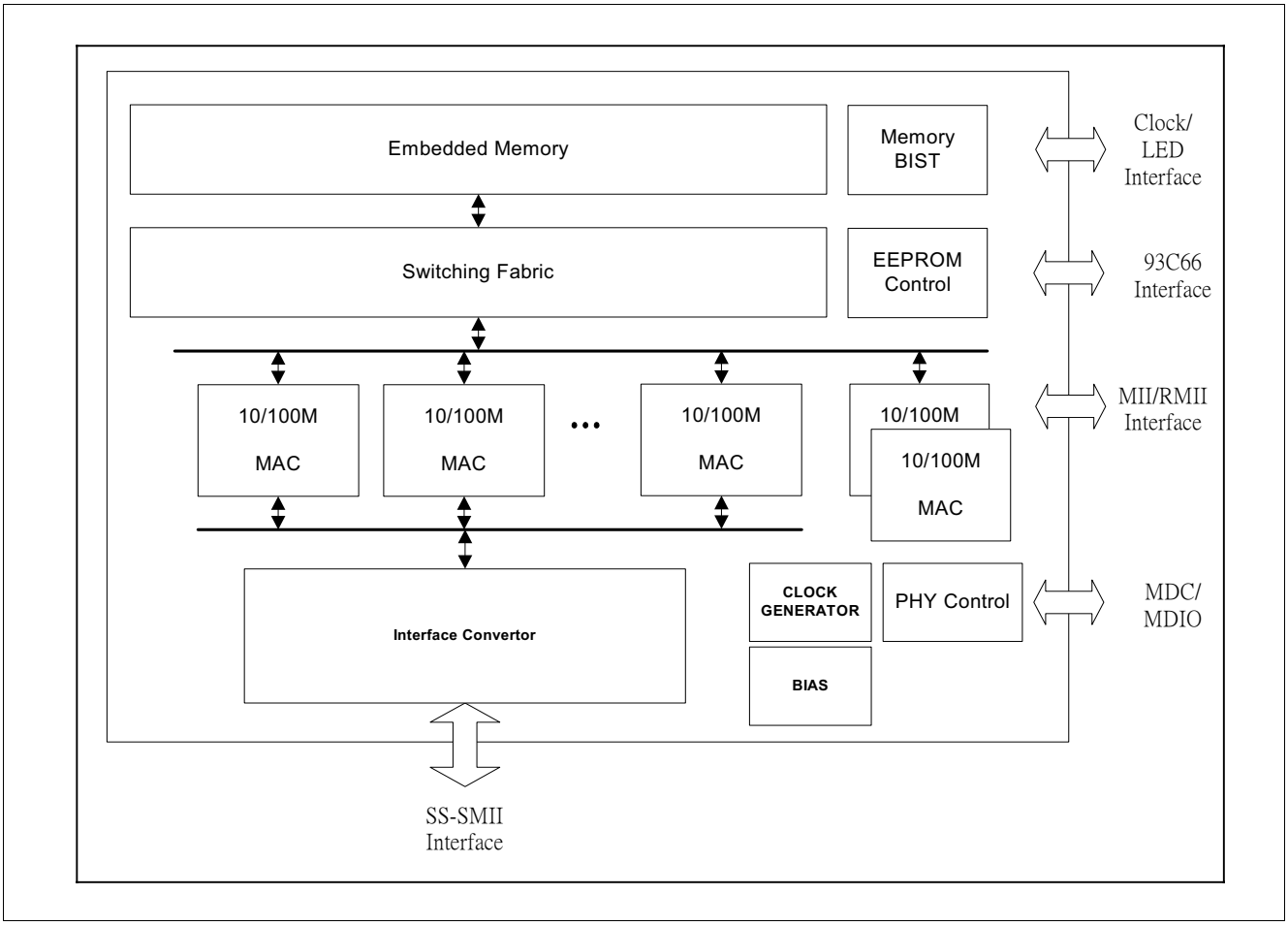


**Figure 1 ADM6918/X Block Diagram**

# 2 Interface Description

## 2.1 Pin Diagram-ADM6918/X (SS-SMII Interface)

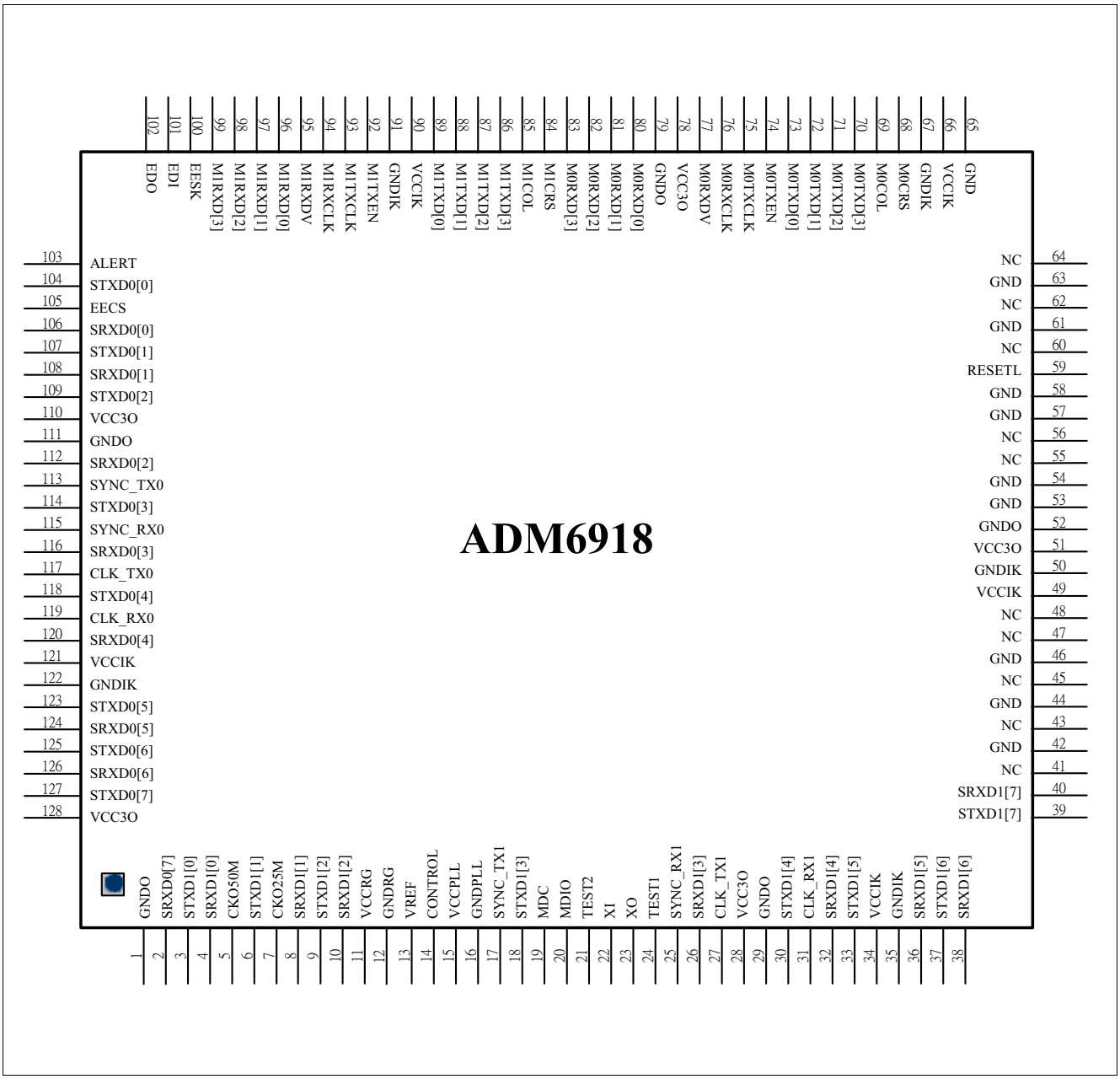


**Figure 2 ADM6918/X Pin Diagram (SS-SMII Interface)**

## 2.2 Abbreviations

Standard abbreviations for I/O tables:

**Table 1 Abbreviations for Pin Type**

| Abbreviations | Description |
|---|---|
| I | Standard input-only pin. Digital levels. |
| O | Output. Digital levels. |
| I/O | I/O is a bidirectional input/output signal. |
| AI | Input. Analog levels. |
| AO | Output. Analog levels. |
| AI/O | Input or Output. Analog levels. |
| PWR | Power |
| GND | Ground |
| MCL | Must be connected to Low (JEDEC Standard) |
| MCH | Must be connected to High (JEDEC Standard) |
| NU | Not Usable (JEDEC Standard) |
| NC | Not Connected (JEDEC Standard) |

**Table 2 Abbreviations for Buffer Type**

| Abbreviations | Description |
|---|---|
| Z | High impedance |
| PU1 | Pull up, 10 kΩ |
| PD1 | Pull down, 10 kΩ |
| PD2 | Pull down, 20 kΩ |
| TS | Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance. |
| OD | Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource. |
| OC | Open Collector |
| PP | Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute). |
| OD/PP | Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute. |
| ST | Schmitt-Trigger characteristics |
| TTL | TTL characteristics |

## 2.3 Pin Description

ADM6918/X pins are categorized into one of the following groups:

- SS-SMII Networking Interface, 60 pins
- MII/RMII Interface, 28 pins
- Power/Ground
- Miscellaneous pins, 16 pins

**Table 3 I/O Signals**

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **SS-SMII Networking Interface, 60 pins** | | | | |
| 106 | SRXD0_0 | I | TTL | **Port 0 to Port 7 SS-SMII Receive Data Bit** The receive data should be synchronous to the rising edge of CLK_RX0. |
| 108 | SRXD0_1 | | | |
| 112 | SRXD0_2 | | | |
| 116 | SRXD0_3 | | | |
| 120 | SRXD0_4 | | | |
| 124 | SRXD0_5 | | | |
| 126 | SRXD0_6 | | | |
| 2 | SRXD0_7 | | | |
| 115 | SYNC_RX0 | I | TTL | **Port 0 to Port 7 SS-SMII Synchronous Signal** This signal is synchronous to the rising edge of CLK_RX0. Active high indicates the byte boundary. |
| 119 | CLK_RX0 | I | TTL | **Reference Receive Clock for Port 0 to Port 7** This signal is 125 MHz input for SS-SMII interface. |
| 104 | STXD0_0 | O | TTL, 8 mA | **Port 0 to Port 7 SS-SMII Transmit Data Bit** The transmit data is synchronous to the rising edge of CLK_TX0. |
| 107 | STXD0_1 | | | |
| 109 | STXD0_2 | | | |
| 114 | STXD0_3 | | | |
| 118 | STXD0_4 | | | |
| 123 | STXD0_5 | | | |
| 125 | STXD0_6 | | | |
| 127 | STXD0_7 | | | |
| 113 | SYNC_TX0 | O | TTL, 8 mA | **Port 0 to Port 7 SS-SMII Synchronous Signal** This signal is synchronous to the rising edge of CLK_TX0. Active high indicates the byte boundary. |
| 117 | CLK_TX0 | O | TTL, 16 mA | **Reference Transmit Clock for Port 0 to Port 7** This signal is 125 MHz output for SS-SMII interface. |
| 4 | SRXD1_0 | I | TTL | **Port 8 to Port 15 SS-SMII Receive Data Bit** The receive data should be synchronous to the rising edge of CLK_RX1. |
| 8 | SRXD1_1 | | | |
| 10 | SRXD1_2 | | | |
| 26 | SRXD1_3 | | | |
| 32 | SRXD1_4 | | | |
| 36 | SRXD1_5 | | | |
| 38 | SRXD1_6 | | | |
| 40 | SRXD1_7 | | | |
| 25 | SYNC_RX1 | I | TTL | **Port 8 to Port 15 SS-SMII Synchronous Signal** This signal is synchronous to the rising edge of CLK_RX1. Active high indicates the byte boundary. |
| 31 | CLK_RX1 | I | TTL | **Reference Receive Clock for Port 8 to Port 15** This signal is 125 MHz input for SS-SMII interface. |

**Table 3 I/O Signals** (cont'd)

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 3 | STXD1_0 | O | TTL, 8 mA | **Port 8 to Port 15 SS-SMII Transmit Data Bit** The transmit data is synchronous to the rising edge of CLK_TX1. |
| 6 | STXD1_1 | | | |
| 9 | STXD1_2 | | | |
| 18 | STXD1_3 | | | |
| 30 | STXD1_4 | | | |
| 33 | STXD1_5 | | | |
| 37 | STXD1_6 | | | |
| 39 | STXD1_7 | | | |
| 17 | SYNC_TX1 | O | TTL, 8 mA | **Port 8 to Port 15 SS-SMII Synchronous Signal** This signal is synchronous to the rising edge of CLK_TX1. Active high indicates the byte boundary. |
| 27 | CLK_TX1 | O | TTL, 16 mA | **Reference Transmit Clock for Port 8 to Port 15** This signal is 125 MHz output for SS-SMII interface. |
| **MII/RMII Interface, 28 pins** | | | | |
| 68 | M0CRS | I | TTL, PD | **MII Port0 Carrier Sense** This pin is internal pull-down. |
| 69 | M0COL | I | TTL, PD | **MII Port0 Collision Input** This pin is internal pull-down. |
| 73 | M0TXD_0 | I/O | TTL, 8 mA, PD | **MII Port 0 Transmit Data Bit[0:3]** Synchronous to the rising edge of M0TXCLK. **RMII Port 0 Transmit Data Bit[0:1]** Synchronous to the rising edge of M0RXCLK. **RMIIMODE[1]**: Value on M0TXD_3 will be latched at the rising edge of RESETL to configure port 25 as RMII mode. **RMIIMODE[0]**: Value on M0TXD[2] will be latched at the rising edge of RESETL to configure port 24 as RMII mode. |
| 72 | M0TXD_1 | | | |
| 71 | M0TXD_2 | | | |
| 70 | M0TXD_3 | | | |
| 74 | M0TXEN | I/O | TTL, 8 mA, PD | **MII/RMII Port 0 Transmit Enable** AGDIS. Value on this pin will be latched at the rising edge of RESETL to set aging disable. |
| 75 | M0TXCLK | I | TTL, PD | **MII Port 0 Transmit Clock Input** This pin is 25 MHz input for MII interface. |
| 76 | M0RXCLK | I | TTL, PD | **MII/RMII Port 0 Receive Clock Input** This pin is 25 MHz input for MII interface and 50 MHz REFCLK input for RMII interface. |
| 77 | M0RXDV | I | TTL, PD | **MII Port 0 Receive Data Valid** **RMII Port 0 Carrier Sense/Receive Data Valid** This pin is internal pull-down. |
| 80 | M0RXD_0 | I | TTL, PD | **MII Port 0 Receive Data Bit[0:3]** **RMII Port 0 Receive Data Bit[0:1]** If in RMII mode, M0RXD_3 used for ext_dup_enable and M0RXD_2 used for ext_dup_full. Internal pull-down. See Sec3.1.27 for details. |
| 81 | M0RXD_1 | | | |
| 82 | M0RXD_2 | | | |
| 83 | M0RXD_3 | | | |
| 84 | M1CRS | I | TTL, PD | **MII Port 1 Carrier Sense** This pin is internal pull-down. |

**Table 3 I/O Signals** (cont'd)

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 85 | M1COL | I | TTL, PD | **MII Port 1 Collision Input**<br>This pin is internal pull-down. |
| 89 | M1TXD_0 | I/O | TTL, 8 mA | **MII Port 1Transmit Data Bit[0:3]**<br>Synchronous to the rising edge of M1TXCLK.<br>**RMII Port 1Transmit Data Bit[0:1]**<br>Synchronous to the rising edge of M1RXCLK.<br>**BPEN**. Value on M1TXD[3] will be latched at the rising edge of RESETL to set Back_pressure enable. Internal pull-up.<br>**FCEN**. Value on M1TXD[2] will be latched at the rising edge of RESETL to set flow control enable. Internal pull-up.<br>**TNKEN**. Value on M1TXD[1] will be latched at the rising edge of RESETL to set trunking enable. Internal pull-up.<br>**IPGLVING**. Value on M1TXD[0] will be latched at the rising edge of RESETL to set shorter IPG. Internal pull-down. |
| 88 | M1TXD_1 | | | |
| 87 | M1TXD_2 | | | |
| 86 | M1TXD_3 | | | |
| 92 | M1TXEN | O | TTL, 8 mA, PU | **MII Port 1 Transmit Enable**<br>ANEN. Value on this pin will be latched at the rising edge of RESETL to set auto_negotiation enable. Internal pull-up. |
| 93 | M1TXCLK | I | TTL, PD | **MII Port1 Transmit Clock Input**<br>This signal is 25 MHz input for MII interface. |
| 94 | M1RXCLK | I | TTL, PD | **MII1 Receive Clock Input**<br>This signal is 25 MHz input for MII interface and 50 MHz REFCLK input for RMII interface. |
| 95 | M1RXDV | I | TTL, PD | **MII/RMII Port 1 Receive Data Valid**<br>This pin is internal pull-down. |
| 96 | M1RXD_0 | I | TTL PD | **MII Port 1 Receive Data Bit[0:3]**<br>**RMII Port 1 Receive Data Bit[0:1]**<br>If in RMII mode, M1RXD_3 used for ext_dup_enable and M1RXD_2 used for ext_dup_full. Internal pull-down. See Sec3.1.27 for details. |
| 97 | M1RXD_1 | | | |
| 98 | M1RXD_2 | | | |
| 99 | M1RXD_3 | | | |
| **Power/Ground** | | | | |
| 12 | GNDRG | Analog GND | – | **Ground for Regulator** |
| 11 | VCCRG | Analog PWR | – | **3.3 V Power Supply for Regulator** |
| 16 | GNDPLL | Analog GND | – | **Ground for PLL** |
| 15 | VCCPLL | Analog PWR | – | **1.8 V Power Supply PLL** |
| 35, 50, 67, 91, 122 | GNDIK | Digital GND | – | **Ground for Core Logic** |
| 34, 49, 66, 90, 121 | VCCIK | Digital PWR | – | **1.8 V Power Supply for Core Logic** |
| 1, 29, 52, 79, 111 | GNDO | Digital GND | – | **Ground for I/O PAD** |

**Table 3 I/O Signals** (cont'd)

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 28, 51, 78, 110, 128 | VCC3O | Digital PWR | – | **3.3 V Power Supply for I/O PAD** |
| **Miscellaneous Pins, 16 pins** | | | | |
| 7 | CK25MO | O | TTL, 16 mA | **25 MHz Clock Output** This pin will drive out 25 MHz. |
| 5 | CK50MO | O | TTL, 16 mA | **50 MHz Clock Output** This pin will drive out 50 MHz. |
| | COL_LED_10M | O | TTL, 16 mA | **COL_LED_10M** This pin shows collision LED for 10M domain (see EEPROM Register 1ch, Bit[9]). |
| 22 | XI | AI | – | **Crystal or OSC 50 MHz Input** This is the clock source of PLL. The PLL will generate 125 MHz for SS-SMII and 50 MHz for RMII and 25 MHz for MII. |
| 23 | XO | AO | – | **Crystal 50 MHz Output** |
| 59 | RESETL | I | TTL, ST | **Reset Signal** An active low signal with minimum 100 ms duration is required. |
| 103 | ALERT | O | TTL, 8 mA | **Alert LED Display** This pin will show the status of power-on-diagnostic and broadcast traffic. |
| | COL_LED_100M | O | TTL, 8 mA | **COL_LED_100M** This pin shows collision LED for 100M domain (see EEPROM Register 1ch, Bit[9]). |
| 21 | TEST_2 | I | TTL, PD | **Industrial Test Pins** These pins are internal pull-down. |
| 24 | TEST_1 | | | |
| 19 | MDC | O | TTL, 16 mA | **Management Data Clock** This pin output 2.2 MHz clock to drive PHY and access corresponding speed and duplex and link status through MDIO. |
| 20 | MDIO | I/O | TTL, 8 mA, PU | **Management Data** This pin is in-out to PHY. When RESETL is low, this pin will be tristate. This pin is internal pull-up. |
| 100 | EESK | I/O | TTL, 4 mA, PU | **EEPROM Serial Clock** This pin is clock source for EEPROM. When RESETL is low, it will be tristate. This pin is internal pull-up. |
| 105 | EECS | I/O | TTL, 4 mA, PD | **EEPROM Chip Select** This pin is chip enable for EEPROM. When RESETL is low, it will be tristate. This pin is internal pull-down. |
| 101 | EDI | I/O | TTL, 4 mA, PU | **EEPROM Serial Data Input** This pin is output for serial data transfer. When RESETL is low, it will be tristate. This pin is internal pull-up. |

**Table 3 I/O Signals** (cont'd)

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 102 | EDO | I | TTL, PU | **EEPROM Serial Data Output**<br>This pin is input for serial data transfer. This pin is internal pull-up. |
| 14 | CONTROL | AO | – | **FET Control Signal**<br>The pin is used to control FET for 3.3 V to 1.8 V regulator. |
| 13 | VREF | AI | – | **Regulator Control Input Signal** |
| 64, 62, 60, 55, 56, 47, 48, 45, 43, 41 | NC | | | **No Connect** |
| 65, 63, 61, 58, 57, 53, 54, 46, 44, 42 | GND | | | **Ground** |

# 3 Function Description

## 3.1 Introduction

The ADM6918/X uses a “store & forward” switching approach for the following reasons:

1. Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require the large elastic buffers, especially bridging between a server on a 100Mbit/s network and clients on a 10 Mbit/s segment.
2. Store & forward switches improve overall network performance by acting as a “network cache”.
3. Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port.

### 3.1.1 Basic Operation

The ADM6918/X receives incoming packets from one of its ports, uses the source address (SA) and VID to update the address table, and then forwards the packet to the output ports determined by the destination address (DA) and VID.

If the DA and VID are not found in the address table, the ADM6918/X treats the packet as a broadcast packet and forwards the packet to the other ports within the same group.

The ADM6918/X automatically learns the port number of attached network devices by examining the SA and VID of all incoming packets. If the SA and VID are not found in the address table, the device adds it to the table.

### 3.1.2 Address Learning

The ADM6918/X provides two ways to create the entry in the address table: dynamic learning and manual learning. A four-way hash algorithm is implemented to allow 4 different addresses to be stored at the same location. Up to 4k entries can be created and all entries are stored in the internal SSRAM. Two parameters, SA and VID, are combined to generate the 10-bit hash key to allow that the same addresses with different port number can exist in the table at the same time.

#### Dynamic Learning

The ADM6918/X searches for SA and VID of an incoming packet in the address table and acts as follows:

If the SA+VID was not found in the address table (a new address), the ADM6918/X waits until the end of the packet (non-error packet) and updates the address table. If the SA+VID was found in the address table, then aging value of each corresponding entry will be reset to 0.

Dynamic learning will be disabled in the following condition:

1. Security violation happened.
2. The packet is a PAUSE frame.
3. The first bit of SA is $1_B$.
4. The packet is an error packet (too long, too short or FCS error).
5. The CPU port leaning function is disabled or enabled but the CPU port instructs the switch not to learn the packet.
6. The port is in the Disabled or Blocking-not-Listening state in the Spanning Tree Protocol.

#### Manual Learning

The ADM6918/X implements the manual learning through the CPU’s help. The CPU can create or remove any entry in the address table. Each entry could be static or pointed to the output port map table. “Static” means the entry will not be aged forever. It is useful in the security function (forward unknown packets to the CPU port or discard) or monitor function (forward monitored address to the specific port). Output port map table is also helpful

in the IGMP function (if the number of the output port is more than one) or the users want to redirect the special packets with reserved DA.

### 3.1.3 Address Aging

The ADM6918/X will periodically (300 ms) remove the non-static address in the address table. This could help to prevent a station leaves the network and occupies a table space for a long time. Aging function can be disabled from the hardware pin.

### 3.1.4 Address Recognition and Packet Forwarding

The ADM6918/X forwards the incoming packets between bridge ports according to the DA and VID as follows:

**Table 4 Address Recognition and Packet Forwarding**

| DA | DA+VID was found in the address table (entry not pointed to the output port map table) | DA+VID was found in the address table (entry pointed to the output port map table) | DA+VID was not found in the address table |
|---|---|---|---|
| Unicast Address | No Security Violation | | |
| | Forward packets to the port determined by the address table. The packet may be dropped because of forwarding group boundary violation. | Forward packets to the ports determined by the output port map table constrained by the forwarding group. | Forward packets to the other ports within the same forwarding group. |
| | Security Violation | | |
| | Drop or forward to CPU | Drop or forward to CPU | Drop or forward to CPU |
| Broadcast Address (All 1'b1) | No Security Violation | | |
| | Forwarding packets to the other ports within the same forwarding group. | Forward packets to the ports determined by the output port map table constrained by the forwarding group. | Forward packets to the other ports within the same forwarding group. |
| | Security Violation | | |
| | Drop or forward to CPU | Drop or forward to CPU | Drop or forward to CPU |
| Reserved Address (01-80-c2-00-00-xx, with the option to forward normally) | No Security Violation | | |
| | Forwarding packets to the other ports within the same forwarding group. | Forward packets to the ports determined by the output port map table constrained by the forwarding group. | Forward packets to the other ports within the same forwarding group. |
| | Security Violation | | |
| | Same as the above | Same as the above | Same as the above |
| Reserved Address (01-80-c2-00-00-xx, with the option to forward to CPU) | No Security Violation | | |
| | Forward the packet to the CPU port. | Forward the packet to the CPU port. | Forward the packet to the CPU port. |
| | Security Violation | | |
| | Same as the above | Same as the above | Same as the above |

**Table 4 Address Recognition and Packet Forwarding** (cont'd)

| DA | DA+VID was found in the address table (entry not pointed to the output port map table) | DA+VID was found in the address table (entry pointed to the output port map table) | DA+VID was not found in the address table |
|---|---|---|---|
| Reserved Address (01-80-c2-00-00-xx, with the option to discard) | No Security Violation | | |
| | Discard the packet. | Discard the packet. | Discard the packet. |
| | Security Violation | | |
| | Same as the above | Same as the above | Same as the above |
| IGMP Packet (Port Enable IGMP) | No Security Violation | | |
| | Forward the packet to the CPU port. | Forward the packet to the CPU port. | Forward the packet to the CPU port. |
| | Security Violation | | |
| | Drop or forward to CPU | Drop or forward to CPU | Drop or forward to CPU |
| IGMP Packet (Port Disable IGMP) | No Security Violation | | |
| | Forward packets to the port determined by the address table. The packet may be dropped because of forwarding group boundary violation. | Forward packets to the ports determined by the output port map table constrained by the forwarding group. | Forward packets according the Multicast Option. |
| | Security Violation | | |
| | Drop or forward to CPU | Drop or forward to CPU | Drop or forward to CPU |
| Others | No Security Violation | | |
| | Forward packets to the port determined by the address table. The packet may be dropped because of forwarding group boundary violation. | Forward packets to the ports determined by the output port map table constrained by the forwarding group. | Forward packets according the Multicast Option. |
| | Security Violation | | |
| | Drop or forward to CPU | Drop or forward to CPU | Drop or forward to CPU |

### 3.1.5 Trunking Port Forwarding

ADM6918/X supports the trunking forwarding and any port could be assigned to the trunking port. When one or more of the members link fail, the ADM6918/X will automatically change the transmitting path from the failed link port to normal link port. Port based load balancing is implemented to distribute the loading.

### 3.1.6 Illegal Frames

The ADM6918/X will discard all illegal frames such as runt packet (less than 64 bytes), oversize packet (greater than 1518 or 1522 bytes) or bad CRC.

### 3.1.7 Back off Algorithm

The ADM6918/X implements the truncated exponential back off algorithm compliant to the 802.3 standard. ADM6918/X will restart the back off algorithm by choosing 0-9 collision count. After 16 consecutive retransmit trials, the ADM6918/X resets the collision counter.

### 3.1.8 Buffers and Queues

The ADM6918/X incorporates 18 transmit queues and receive buffer area for the 18 Ethernet ports. The receive buffers as well as the transmit queues are located within the ADM6918/X along with the switch fabric. The buffers are divided into 640 blocks of 256 bytes each. The queues of each port are managed according to each port's read/write pointer.

Input buffers and output queues are maintained through proprietary patent pending UNIQUE (Universal Queue management) scheme.

### 3.1.9 Half Duplex Flow Control

Back-pressure is supported for half-duplex operation.

When the ADM6918/X cannot allocate a receiving buffer for an incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision.

### 3.1.10 Full Duplex Flow Control

When full duplex port runs out of its receive buffer, a PAUSE command will be issued by ADM6918/X to notice the packet sender to pause transmission. This frame based flow control is totally compliant to IEEE 802.3x. When flow control hardware pin is set to high during power on reset and per port PAUSE is enabled, ADM6918/X will output and accept 802.3x flow control packet.

### 3.1.11 Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The value is 9.6us for 10Mbit/s ETHERNET and 960ns for 100Mbit/s fast Ethernet.

### 3.1.12 Port VLAN or Tag VLAN Support

Two VLAN settings are supported by the ADM6918/X: the port-based VALN or the tag-based VLAN. For the port-based VLAN the ADM6918/X will use the port number as the index to lookup the forwarding table. For the tag-based VLAN, the ADM6918/X will use the VID to lookup the forwarding table. Each port is assigned a Port VID as the Default VID if tag-based VLAN is used. The ADM6918/X will check TAG, remove TAG, insert TAG, and re-calculate CRC if packet is changed.

**Table 5 Packets Received are Untagged**

| Force no Tag | Bypass | Output Port is Tagged or not | Action |
|---|---|---|---|
| Don't Care | No | No | Untag as the original |
| | Yes | No | Untag as the original |
| | No | Yes | Add Tag |
| | Yes | Yes | Untag as the original |

**Table 6 Packets Received are Tagged**

| Force no Tag | Bypass | Output Port is Tagged or not | Action |
|---|---|---|---|
| No | No | No | The Tag is removed. |
| Yes | No | No | Tag as the original. The priority in the TAG header is not checked and VID will not change even if VID is 0 or 1. |

**Table 6 Packets Received are Tagged** (cont'd)

| Force no Tag | Bypass | Output Port is Tagged or not | Action |
|---|---|---|---|
| No | Yes | No | Tag as the original. The priority in the TAG header is checked and if the VID is 0 or 1, it may change to PVID (see EEPROM register $1C_H$, Bit[3]). |
| No | No | Yes | Tag as the original. The priority in the TAG header is checked and if the VID is 0 or 1, it may change to PVID (see EEPROM register 1ch, Bit[3]). |
| No | Yes | Yes | Tag as the original. The priority in the TAG header is checked and if the VID is 0 or 1, it may change to PVID (see EEPROM register 1ch, Bit[3]). |
| Yes | Yes | No | Tag as the original. The priority in the TAG header is not checked. The VID will not change. |
| Yes | No | Yes | The Tag will be added and packet will be double tagged output. The VID will not change. |
| Yes | Yes | Yes | Tag as the original. The priority in the TAG header is not checked. The VID will not change. |

### 3.1.13 Priority Control

The ADM6918/X provides two priority queues on each output port. Five ways could be used to assign a priority to a packet.

1. The priority assigned to each receiving port
2. The priority field in the 802.1Q Tag Header
3. The IPv4 TOS field in the IPv4 Header
4. Priority assigned by the CPU
5. Management packet (high priority assigned)

### 3.1.14 Alert LED Display

Two functions are displayed through the Alert LED.

1. Diagnostic Mode after Power on
   a) After reset or power up, LED keeps on at least 3 second, and processes internal SSRAM self-test.
   b) If test passes, the ADM6918/X turns off LED and goes to the broadcast storm mode.
   c) If SSRAM test fails, the ADM6918/X turns off LED, then keeps on.
2. Broadcast Storm Mode after SSRAM Self-test. Packets with DA = $ffffffffffff_H$will be counted into the storm counter.
   Two thresholds (rising and falling) are used to control the broadcast storm.
   a) Time Scale: 50ms is used. The max packet number in 100BaseT is 7490. The max packet number in 10BaseT is 749.
   b) Port Rising Threshold, see **Table 7**.
   c) Port Falling Threshold, see **Table 8**.

**Table 7 Port Rising Threshold**

| Broadcast Storm Threshold | 00 | 01 | 10 | 11 |
|---|---|---|---|---|
| All 100TX | Disable | 10% | 20% | 40% |
| Not All 100TX | Disable | 1% | 2% | 4% |

**Table 8 Port Falling Threshold**

| Broadcast Storm Threshold | 00 | 01 | 10 | 11 |
|---|---|---|---|---|
| All 100TX | Disable | 5% | 10% | 20% |
| Not All 100TX | Disable | 0.5% | 1% | 2% |

### 3.1.15 Broadcast Storm Filter

If broadcast storming filter is enabled, the broadcast packets (DA = ffff-ffff-ffff$_H$) over the rising threshold within 50 ms will be discarded when the alert LED is turned on.

### 3.1.16 Collision LED Display

Two collision LEDs are supported. (see EEPROM Register 1C$_H$, Bit[9])

1. 100M Collision LED. If collision happens in one of the ports configured 100M, the 100M Collision LED will flash in rate of 2 Hz.
2. 10M Collision LED. If collision happens in one of the ports configured 10M, the 10M Collision LED will flash in rate of 2 Hz.

### 3.1.17 Bandwidth Control

The ADM6918/X allows the user to limit the bandwidth for each input or output port. 64k, 128K, 256k, 512K, 1M, 4M, 10M and 20M are supported.

### 3.1.18 Smart Discard

The ADM6918/X supports a smart mechanism to discard packets early according to their priority to prevent the resource blocked by the low priority. The discard ratio is as follows:

**Table 9 Discard Ratio**

| Discard Mode Utilization | 00 | 01 | 10 | 11 |
|---|---|---|---|---|
| 00 | 0% | 0% | 0% | 0% |
| 01 | 0% | 0% | 25% | 50% |
| 11 | 0% | 25% | 50% | 75% |

### 3.1.19 Security Support

4 level security schemes are supported by the ADM6918/X. All the security violation address will not be automatically learned.

The violated packet could be forwarded to the CPU port for management or discarded. When CPU is not present, ADM6918/X also provides a simple way to lock the first address to prevent illegal address access.

### 3.1.20 Smart Counter Support

Six counters per port are supported by the ADM6918/X.

1. Receive Packet Count
2. Receive Packet Length Count
3. Transmit Packet Count
4. Transmit Packet Length Count
5. The Error Count
6. The Collision Count

### 3.1.21 Length 1536 Mode

The ADM6918/X provides a function to enable the port to receive packets up to 1536 Byte.

### 3.1.22 PHY Management (MDC/MDIO Interface)

The ADM6918/X uses the MDC/MDIO interface to set the PHY status. After the reset or power up, the MDC/MDIO controller will delay about 130 ms to wait for the PHY to ready. The ADM6918/X supports two ways to configure the PHY setting.

1. PHY master. The switch only reads the PHY status (speed, duplex, link, and pause). This mode is useful when users want to configure PHY through the CPU help. The ADM6918/X supports an indirect way (a PHY Control Register) for CPU to access PHYs.
2. PHY slave. The switch uses the EEPROM setting to control the PHY attached (only speed, duplex, link, and pause are supported). After the port setting changed, the ADM6918/X will use the new setting to program the PHY again and update the status. 8 commands are provided in this mode to allow the customer to customize the PHY setting.

*Note: The PHY address attached to port 0 is $00008_H$, the PHY address attached to port 1 is $00009_H$, …, the PHY address attached to port 23 is $0001f_H$, the PHY address attached to port 24 is $00006_H$ and the PHY address attached to port 25 is $00007_H$.*

### 3.1.23 Forward Special Packets to the CPU Port (IGMP and Spanning Tree Support)

ADM6918/X will forward the special packets to the CPU port to provide the management function.

1. DA is 01-80-C2-00-00-00 (BPDU)
2. DA is 01-80-C2-00-00-02 (Slow Protocol)
3. DA is 01-80-C2-00-00-03 (802.1x PAE)
4. DA is 01-80-C2-00-00-04 ~ 01-80-C2-00-00-0f
5. DA is 01-80-C2-00-00-20 (GMRP)
6. DA is 01-80-C2-00-00-21 (GVRP)
7. DA is 01-80-C2-00-00-22 (GVRP)
8. DA is 01-00-5E-xx-xx-xx and protocol field is 2 for IPV4 (IGMP)

### 3.1.24 Special TAG

The ADM6918/X has an ability to insert 4Byte special TAG when packets transmitted to the CPU port or to remove 8Byte additional TAG in the packets when packets are received from the CPU port. The configuration is shown in the CPU Configuration Register. This special function allows the CPU to know the source port which will be used in the IGMP Snooping, Spanning Tree or the Security function. The CPU also could insert additional 8-byte Tag to instruct the switch to handle the packets. The packets format is as follows:

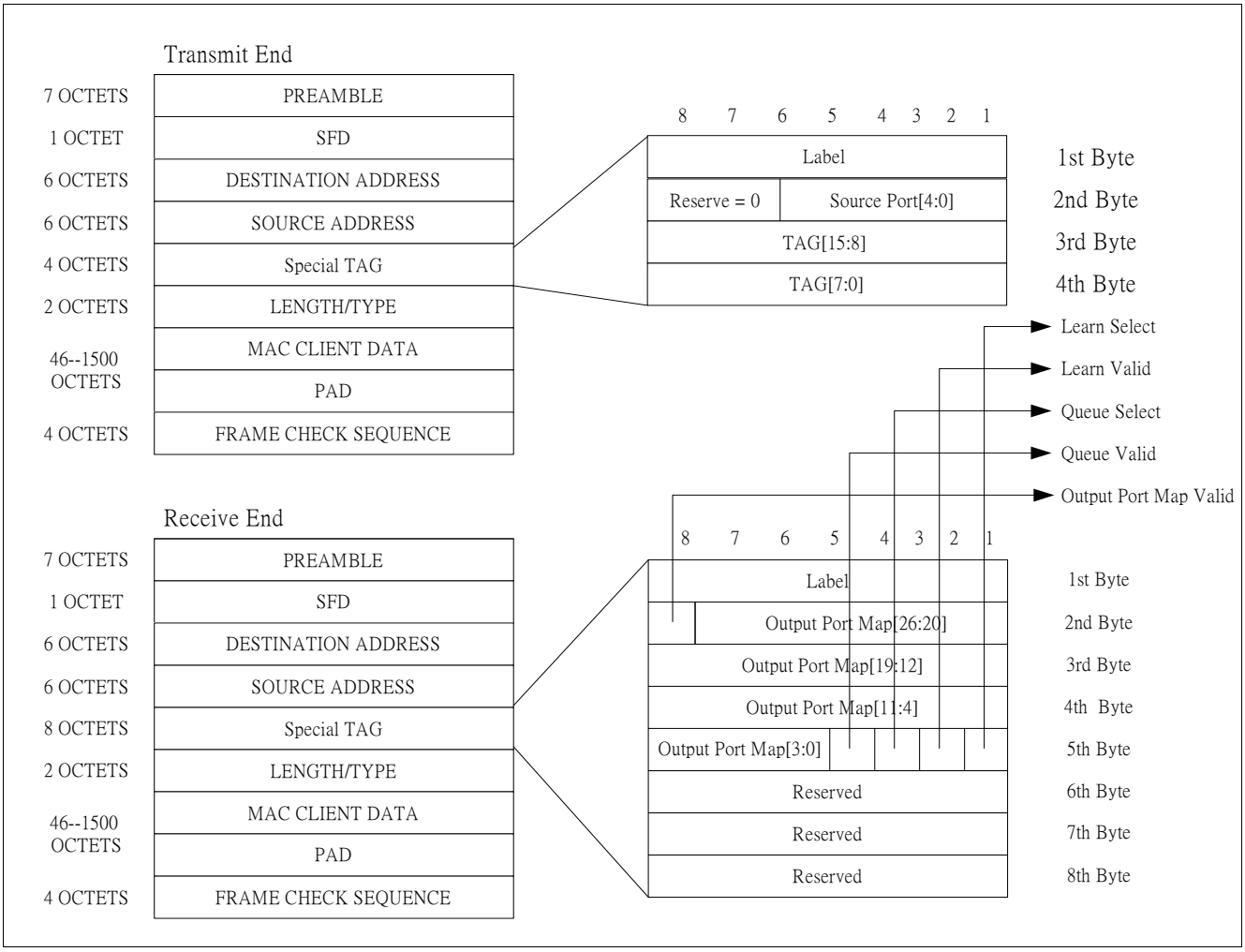


**Figure 3 Packet Format**

**Table 10 Special TAG Fields**

| Configuration | Description | Default |
|---|---|---|
| Label | The field is used for CPU to decide if the special TAG is valid. If the switch finds the Label doesn't equal to the value assigned by the EEPROM, it must receive as the normal mode. This case exists when user wants the switch to insert 4 byte special tag even for Pause packets. | 8b'0 |
| Output Port Map Valid | $1_B$ , The switch is instructed to override the switch operation. It will forward the packets following the Output Port Map field.<br>$0_B$ , The switch will treat the packet as the normal mode. | 1'b0 |