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Ninja C/CX (ADM6992C/CX)

Two Port Bridge Fiber to Fast Ethernet Converter

Communications

Never stop thinking.

Edition 2005-11-25

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2004-05-05	Rev. 1.0, First release of NINJA C (ADM6992C)
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2005-11-25	Rev. 1.01 changed to Rev. 1.02 Minor change. Included Green package information

Trademarks

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1 Product Overview

Features and the block diagram.

1.1 Overview

The NINJA C/CX (ADM6992C/CX) is a single chip integrating two 10/100 Mbps MDIX TX/FX transceivers with a two-port 10/100M Ethernet L2 switch controller. Features include a converter mode to meet demanding applications, such as Fiber-to-Ethernet media converters. The ADM6992CX is the environmentally friendly “green” package version.

The NINJA C/CX (ADM6992C/CX) supports 16 entries of packet classification and marking or filtering for TCP/UDP port numbering, IP protocol ID and Ethernet Type. These can be configured either using the EEPROM or on-the-fly using a small, low-cost micro controller.

On the media side, the NINJA C/CX (ADM6992C/CX)’s 0 and 1 ports support auto-MDIX 10Base-T/100Base-TX and 100Base-FX as specified by the IEEE 802.3 committee through uses of digital circuitry and high speed A/D.

The NINJA C/CX (ADM6992C/CX) also supports a serial management interface (SMI), which is initialized and configured using a small low-cost micro controller. It also provides the port status for remote agent monitoring and a smart counter for reporting port statistics.

1.2 Features

Main features:

- 2-port10/100M switch integrated with a 2-port PHY (10/100TX and 100FX)
- Provides TX<--> FX Converter modes with Link Pass Through (LPT)
- Built-in data buffer 6Kx64bit SRAM
- Up to 1k of Unicast. MAC addresses with a 4-way associative hashing table
- MAC address learning table with aging function
- Supports store & forward frame forwarding, modify cut-through frame forwarding, and fast cut-through frame forwarding.
- Forwarding and filtering at non-blocking full wire speed
- 802.3x flow control for full duplex and back-pressure for half duplex
- Supports Auto-Negotiation
- Supports Auto Cross-Over
- Packet lengths up to 9216 bytes.
- 16 entries of packet classification and marking or filtering for TCP/UDP Port Numbering, IP Protocol ID and Ethernet Type
- Serial Management Interface for low-end CPU
- Hardware bandwidth control support for both ingress/egress traffic
- Provides port status for remote agent monitoring
- Provides smart counters for port statistics reporting
- 64 LQFP packaging with 1.8 V/3.3 V power supply

1.3 Block Diagram

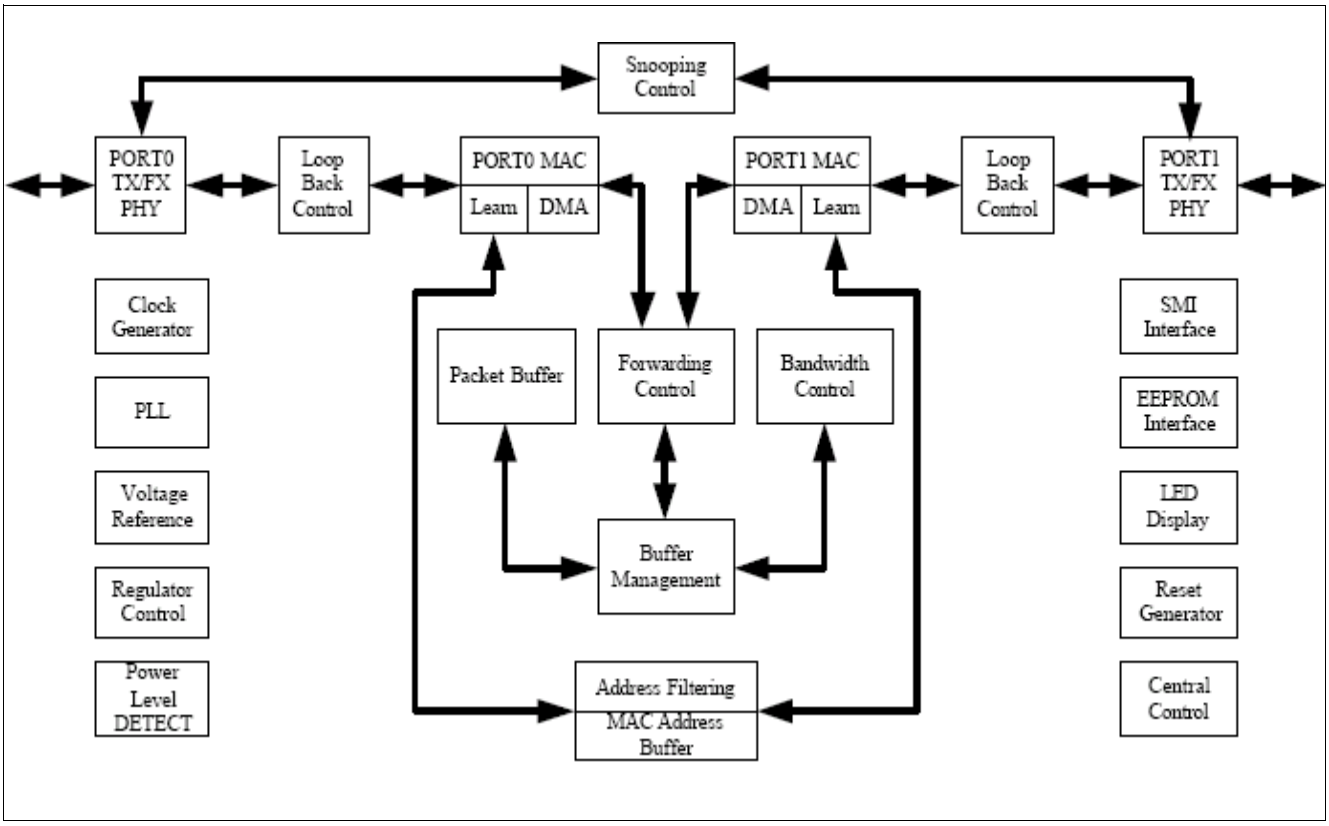

Figure 1 NINJA C/CX (ADM6992C/CX) Block Diagram

1.4 Data Lengths Conventions

Table 1 Data Lengths Conventions

qword	64 bits
dword	32 bits
word	16 bits
byte	8 bits
nibble	4 bits

2 NINJA C/CX Interface Description

This chapter describes Pin Diagram, Pin Type and Buffer Type Abbreviations, and Pin Descriptions.

2.1 Pin Diagram

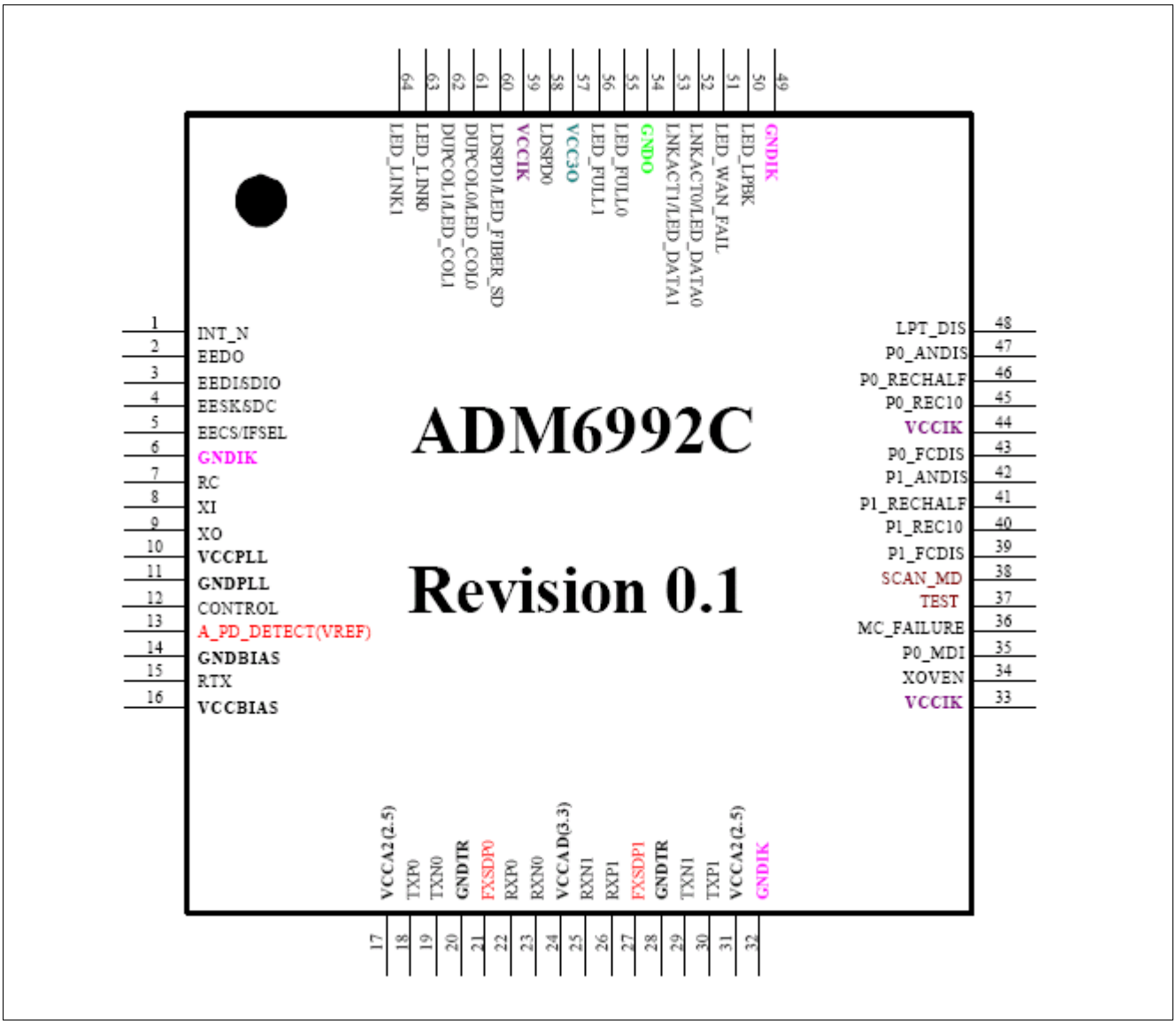

Figure 2 NINJA C/CX (ADM6992C/CX) 64-Pin Assignment

2.2 Pin Type and Buffer Type Abbreviations

Standardized abbreviations:

Table 2 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 3 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU1	Pull up, 10 kΩ
PD1	Pull down, 10 kΩ
PD2	Pull down, 20 kΩ
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

2.3 Pin Descriptions

Interfaces:

- Port 0/1 Twisted Pair Interface, 8 pins
- LED Interface, 12 pins
- EEPROM Interface, 4 pins
- Configuration Interface, 28 pins
- Ground/Power Interface, 27 pins
- Miscellaneous, 14 pins

Note: If not specified, all signals default to digital signals.

Table 4 Port 0/1 Twisted Pair Interface (8 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
18	TXP_0	AI/O		**Twisted Pair Transmit** Output Positive.
30	TXP_1	AI/O		
19	TXN_0	AI/O		**Twisted Pair Transmit** Output Negative.
29	TXN_1	AI/O		
22	RXP_0	AI/O		**Twisted Pair Receive** Input Positive.
26	RXP_1	AI/O		
23	RXN_0	AI/O		**Twisted Pair Receive** Input Negative.
25	RXN_1	AI/O		
21	FXSDP_0	AI		**OMD Signal Detect In**
27	FXSDP_1	AI		

Table 5 LED Interface (12 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
52	LNKACT_0	I/O	TTL, PD, 8mA	**PORT0 Link & Active LED/Link LED.** If LEDMODE_0 is 1, this pin indicates both link status and RX/TX activity. When link status is LINK_UP, LNKACT_0 will be turned on. While PORT0 is receiving/transmitting data, LNKACT_0 will be off for 100ms and then on for 100ms. If LEDMODE[0] is 0, this pin only indicates RX/TX activity.
	LED_DATA_0			
	LEDMODE_0			**LED mode for LINK/ACT LED of PORT0.** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as LEDMODE_0.

Table 5 LED Interface (12 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
53	LNKACT_1	I/O	TTL, PD, 8mA	**PORT1 Link & Active LED/Link LED.** If LEDMODE_2 is 1, this pin indicates both link status and RX/TX activity. When link status is LINK_UP, LNKACT_1 will be turned on. While PORT1 is receiving/transmitting data, LNKACT_1 will be off for 100ms and then on for 100ms. If LEDMODE[2] is 0, this pin only indicates RX/TX activity.
	LED_DATA_1			
	LEDMODE_1			**LED mode for LINK/ACT LED of PORT0 & PORT1.** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as LEDMODE_1. If LEDMODE_1 is 1, DUPCOL[1:0] will display both duplex condition and collision status. If LEDMODE_1 is 0, only collision status will be displayed.
61	DUPCOL_0	I/O	TTL, PD, 8mA	**PORT0 Duplex/Collision LED** If LEDMODE_1 is 1, this pin indicates both duplex condition and collision status. When FULL_DUPLEX, this pin will be turned on for PORT0. When HALF_DUPLEX and no collision occurs, this pin will be turned off. When HALF_DUPLEX and a collision occurs, this pin will be off for 100ms and then on for 100ms. If LEDMODE_1 is 0, this pin indicates collision status. When in HALF_DUPLEX and a collision occurs, this pin will be off for 100ms and turn on for 100ms.
	LED_COL_0			**Collision LED**
	DIS_LEARN			**Disable Address Learning.** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as DIS_LEARN. If DIS_LEARN is 1, MAC address learning will be disabled.
62	DUPCOL_1	I/O	TTL, PU, 8mA	**PORT1 Duplex** If LEDMODE_1 is 1, this pin indicates both duplex condition and collision status. When FULL_DUPLEX, this pin will be turned on for PORT1. When HALF_DUPLEX and no collision occurs, this pin will be turned off. When HALF_DUPLEX and a collision occurs, this pin will be off for 100ms and then on for 100ms. If LEDMODE_1 is 0, this pin indicates collision status. When HALF_DUPLEX and a collision occurs, this pin will be off for 100ms and turn on for 100ms.
	LED_COL_1			**Collision LED**
58	LDSPD_0	I/O	TTL, PD, 8mA	**PORT0 Speed LED** Used to indicate speed status of PORT0. When operating in 100Mbps this pin is turned on, and when operating in 10Mbps this pin is off.
	FXMODE0			**FXMODE0** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as bit 0 of FXMODE.

Table 5 LED Interface (12 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
60	LDSPD_1	I/O	TTL, PD, 8mA	**Speed LED, PORT1** Used to indicate speed status of PORT1. When operating in 100Mbps this pin is turned on, and when operating in 10Mbps this pin is off.
	LED_FIBER_SD			**LED_FIBER_SD.** Used to indicate signal status of PORT1 when NINJA C/CX (ADM6992C/CX) is operating in converter mode.
	LEDMODE2			**LED mode for LINK/ACT LED of PORT1.** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as LEDMODE2. 0_B **TBD**, ACT 1_B **TBD**, LINK/ACT
63	LED_LINK_0	I/O	TTL, PU, 8mA	**PORT0 Link LED** This pin indicates link status. When Port0 link status is LINK_UP, this pin will be turned on.
	FXMODE1			**FXMODE1** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as bit 1 of FXMODE. FXMODE [1:0] Interface 00_B **TBD**, Both Port0 & Port1 are TP port 01_B **TBD**, Port0 is TP port and Port1 is FX port 10_B **TBD**, Port0 is TP port and Port1 is FX port (converter mode) 11_B **TBD**, Both Port0 & Port1 are FX port
64	LED_LINK_1	I/O	TTL, PU, 8mA	**PORT1 Link LED** This pin indicates link status. When Port1 link status is LINK_UP, this pin will be turned on.
	BYPASS_PAUSE			**Bypass frame** which destination address is reserved IEEE MAC address. During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as BYPASS_PAUSE. 0_B **D**, Disable 1_B **E**, Enable
55	LED_FULL_0	I/O	TTL, PU, 8mA	**PORT0 Full Duplex LED** This pin indicates current duplex condition of PORT0. When FULL_DUPLEX, this pin will be turned on. When HALF_DUPLEX this pin will be turned off.
	$\overline{\text{CHIPID\_0}}$			**Chip ID Bit 0.** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as $\overline{\text{CHIPID\_0}}$.

Table 5 LED Interface (12 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
56	LED_FULL_1	I/O	TTL, PU, 8mA	**PORT1 Full Duplex LED** This pin indicates current duplex condition of PORT1. When FULL_DUPLEX, this pin will be turned on. When HALF_DUPLEX this pin will be turned off.
	$\overline{\text{CHIPID\_1}}$			**Chip ID Bit 1** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as $\overline{\text{CHIPID\_1}}$. [$\overline{\text{CHIPID\_1}}$:$\overline{\text{CHIPID\_0}}$] 00_B **TBD**, Master Device 01_B **TBD**, Slave Device $1X_B$ **TBD**, Slave Device
50	LED_LPBK	I/O	TTL, PU, 8mA	**Loop Back Test LED** While performing loop back test this pin is turned on.
	$\overline{\text{CHIPID\_2}}$			**Chip ID Bit 2** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as $\overline{\text{CHIPID\_2}}$.
51	LED_WAN_FAIL	O	TTL, PD, 8mU	**WAN Fail LED** When receiving an OAM frame which has a S2 bit = 1, this pin is turned on.
	$\overline{\text{DISBP}}$			**Disable Back Pressure** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as $\overline{\text{DISBP}}$. 0_B **E**, Enable back-pressure (Default) 1_B **D**, Disable back-pressure

Table 6 EEPROM Interface (4 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
2	EEDO	I	TTL, PU	**EEPROM Data Output** Serial data input from EEPROM. This pin is internal pull-up.
5	EECS/IFSEL	I/O	PD, 4mA	**EEPROM Chip Select** This pin is an active high chip enabled for EEPROM. When RESETL is low, it will be tristate. 0_B **SM**, Select Serial Management Interface 1_B **EE**, Select EEPROM interface

Table 6 EEPROM Interface (4 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
4	EECK/SDC	I/O	TTL, PU, 4mA	**Serial Clock** This pin is the EEPROM clock source. When RESETL is low, it will be tristate. This pin is internal pull-up. If IFSEL is 1, this pin is used as EECK. If IFSEL is 0, this pin is used as SDC.
3	EEDI/SDIO	I/O	TTL, PU, 4mA	**EEPROM Serial Data Input** This pin is the output for serial data transfer. When RESETL is low, it will be tristate. If IFSEL is 1, this pin is used as EEDI. If IFSEL is 0, this pin is used as SDIO.

Table 7 Configuration Interface (28 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
47	P0_ANDIS	I	TTL, PD	**Auto-Negotiation Disable for PORT0** 0_B **E**, Enable 1_B **D**, Disable
46	P0_RECHALF	I	TTL, PD	**Recommend Half Duplex Communication for PORT0** 0_B **F**, Full 1_B **H**, Half
45	P0_REC10	I	TTL, PD	**Recommend 10M for PORT0** 0_B **100**, 100M 1_B **10**, 10M
43	P0_FCDIS	I	TTL, PD	**Flow Control Disable for PORT0** 0_B **E**, Enable 1_B **D**, Disable
42	P1_ANDIS	I	TTL, PD	**Auto-Negotiation Disable for PORT1** 0_B **E**, Enable 1_B **D**, Disable
41	P1_RECHALF	I	TTL, PD	**Recommend Half Duplex Communication for PORT1** 0_B **F**, Full 1_B **H**, Half
40	P1_REC10	I	TTL, PD	**Recommend 10M for PORT1** 0_B **100**, 100M 1_B **10**, 10M
39	P1_FCDIS	I	TTL, PD	**Flow Control Disable for PORT1** 0_B **E**, Enable 1_B **D**, Disable

Table 7 Configuration Interface (28 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
34	XOVEN	I	TTL, PU	**Auto-MDIX Enable.** 0_B **D**, Disable 1_B **E**, Enable
35	P0_MDI	I	TTL, PU	**MDI/MDIX Control for PORT0** This setting will be ignored if enabled Auto-MDIX. 0_B **MDIX**, MDIX 1_B **MDI**, MDI

Table 8 Ground/Power Interface (27 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
20, 28	GNDTR	GND, A		**Ground used by AD receiver/transmitter block.**
17, 31	VCCA2	PWR, A		**1.8 V used for Analogue block**
24	VCCAD	PWR, A		**3.3 V used for TX line driver**
14	GNDBIAS	GND, A		**Ground used by digital substrate**
16	VCCBIAS	PWR, A		**3.3 V used for bios block**
11	GNDPLL	GND, A		**Ground used by PLL**
10	VCCPLL	PWR, A		**1.8 V used for PLL**
6, 32, 49	GNDIK	GND, A		**Ground used by digital core and pre-driver**
33, 44, 59	VCCIK	PWR, D		**1.8 V used for digital core and pre-driver**
54	GNDO	GND, D		**Ground used by digital pad**
57	VCC3O	PWR, D		**3.3 V used for digital pad.**

Table 9 Miscellaneous (14 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
1	$\overline{\text{INT}}$	O	TTL, OD, 4mA	**Interrupt** This pin will be used to interrupt external management device. When EEPROM register 0x5 Bit [15] is 0, this pin is low-active. When EEPROM register 0x5 Bit [15] is 1, this pin is high-active.
12	CONTROL	AO		**FET Control Signal** The pin is used to control FET for 3.3 V to 1.8 V regulator.
15	RTX	A		**TX Resistor**
13	A_PD_DETECT	A		**Analog Reference Voltage**
7	RC	I	TTL, ST	**RC Input for Power On Reset** NINJA C/CX (ADM6992C/CX) sample pin RC as RESETL with the clock input from pin XI.

Table 9 Miscellaneous (14 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
8	XI	AI		**25M Crystal Input** 25M Crystal Input. Variation is limited to +/- 50ppm.
9	XO	AO		**25M Crystal Output** When connected to oscillator, this pin should left unconnected.
37	TEST	I	TTL, PD	**Test pin** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as TEST. Connect to GND at normal application.
38	SCAN_MD	I	TTL, PD	**Scan Mode** For Test Only. Connect to GND at normal application.

3 Function Description

The NINJA C/CX (ADM6992C/CX) integrates two 100Base-X physical layer devices (PHY), two complete 10BaseT modules, a two-port 10/100 switch controller and memory into a single chip for both 10Mbps and 100 Mbps Ethernet switch operation. It also supports 100Base-FX operations through external fiber-optic transceivers. The device is capable of operating in either Full-Duplex or Half-Duplex mode in both 10 Mbps and 100 Mbps operation. Operation modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip auto negotiation logic.

The NINJA C/CX (ADM6992C/CX) consists of four major blocks:

- OAM Engine
- 10/100M PHY Block
- Switch Controller Block
- Built-in 6Kx64 SSRAM

3.1 10/100M PHY Block

The 100Base-X section of the device implements the following functional blocks:

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- 100Base-X physical medium dependent (PMD)

The 10Base-T section of the device implements the following functional blocks:

- 10Base-T physical layer signaling (PLS)
- 10Base-T physical medium attachment (PMA)

The 100Base-X and 10Base-T sections share the following functional blocks:

- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

The interfaces used for the communication between the PHY block and switch core is a MII interface.

An Auto MDIX function is supported. This function can be Enabled/Disabled using the hardware pin. A digital approach for the integrated PHY of the NINJA C/CX (ADM6992C/CX) has been adopted.

3.2 Auto Negotiation and Speed Configuration

3.2.1 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operations supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further details regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The NINJA C/CX (ADM6992C/CX) supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

The auto negotiation function within the NINJA C/CX (ADM6992C/CX) can be controlled either by internal register access or by the use of configuration pins. If disabled, auto negotiation will not occur until software enables bit 12 in MII Register 0. If auto negotiation is enabled, the negotiation process will commence immediately.

When auto negotiation is enabled, the NINJA C/CX (ADM6992C/CX) transmits the abilities programmed into the auto negotiation advertisement register at address 04_H via FLP bursts. Any combination of 10 Mbps, 100 Mbps, half duplex, and full duplex modes may be selected. Auto negotiation controls the exchange of configuration information. Upon successfully auto negotiating, the abilities reported by the link partner are stored in the auto negotiation link partner ability register at address 05_H.

The contents of the “auto negotiation link partner ability register” are used to automatically configure the highest performance protocol between the local and far-end nodes. Software can determine which mode has been configured by auto negotiation, by comparing the contents of register 04_H and 05_H and then selecting the technology whose bit is set in both registers of highest priority relative to the following list:

1. 100Base-TX full duplex (highest priority)
2. 100Base-TX half duplex
3. 10Base-T full duplex
4. 10Base-T half duplex (lowest priority)

The basic mode control register at address 0_H controls the enabling, disabling and restarting of the auto negotiation function. When auto negotiation is disabled, the speed selection bit (bit 13) controls switching between 10 Mbps or 100 Mbps operation, while the duplex mode bit (bit 8) controls switching between full duplex operation and half duplex operation. The speed selection and duplex mode bits have no effect on the mode of operations when the auto negotiation enabled bit (bit 12) is set.

The basic mode status register at address 1_H indicates the set of available abilities for technology types (bit 15 to bit 11), auto negotiation ability (bit 3), and extended register capability (bit 0). These bits are hardwired to indicate the full functionality of the NINJA C/CX (ADM6992C/CX). The BMSR also provides status on:

- Whether auto negotiation is complete (bit 5)
- Whether the Link Partner is advertising that a remote fault has occurred (bit 4)
- Whether a valid link has been established (bit 2)

The auto negotiation advertisement register at address 04_H indicates the auto negotiation abilities to be advertised by the NINJA C/CX (ADM6992C/CX). All available abilities are transmitted by default, but writing to this register or configuring external pins can suppress any ability.

The auto negotiation link partner ability register at address 05_H indicates the abilities of the Link Partner as indicated by auto negotiation communication. The contents of this register are considered valid when the auto negotiation complete bit (bit 5, register address 1_H) is set.

3.2.2 Speed Configuration

The twelve sets of four pins listed in **Table 10** configure the speed capability of each channel of the NINJA C/CX (ADM6992C/CX). The logic states of these pins are latched into the advertisement register (register address 4_H)

for auto negotiation purpose. These pins are also used for evaluating the default value in the base mode control register (register 0_H) according to **Table 10**.

In order to make these pins have the same Read/Write priority as software, they should be programmed to 11111111_B in case a user wishes to update the advertisement register through software.

Table 10 Speed Configuration

Advertise all capability	Advertise single capability	Parallel detect follow IEEE std.	Auto Negoti-ation (Pin & EEPROM)	Speed (Pin & EEPROM)	Duplex (Pin & EEPROM)	Auto Negotiation	Advertise Capability				Parallel Detect Capability			
							10 0F	10 0H	10 F	10 H	10 0F	10 0H	10 F	10 H
1	0	0	1	X	X	1	1	1	1	1	1	0	1	0
1	0	1	1	X	X	1	1	1	1	1	0	1	0	1
1	1	0	1	X	X	1	1	0	0	0	1	0	0	0
1	1	1	1	X	X	1	1	0	0	0	0	1	0	0
0	0	0	1	1	1	1	1	1	1	1	1	0	1	0
0	0	1	1	1	1	1	1	1	1	1	0	1	0	1
0	1	0	1	1	1	1	1	0	0	0	1	0	0	0
0	1	1	1	1	1	1	1	0	0	0	0	1	0	0
0	0	X	1	1	0	1	0	1	0	1	0	1	0	1
0	1	X	1	1	0	1	0	1	0	0	0	1	0	0
0	0	0	1	0	1	1	0	0	1	1	0	0	1	0
0	0	1	1	0	1	1	0	0	1	1	0	0	0	1
0	1	0	1	0	1	1	0	0	1	0	0	0	1	0
0	1	1	1	0	1	1	0	0	1	0	0	0	0	1
0	X	X	1	0	0	1	0	0	0	1	0	0	0	1
X	X	X	0	1	1	0	1	—	—	—	—	—	—	—
X	X	X	0	1	0	0	—	1	—	—	—	—	—	—
X	X	X	0	0	1	0	—	—	1	—	—	—	—	—
X	X	X	0	0	0	0	—	—	—	1	—	—	—	—

3.3 Switch Functional Description

The NINJA C/CX (ADM6992C/CX) supports three types of data forwarding mode, store & forward mode, modified and MII cut-through.

3.3.1 Store & Forward Mode

The NINJA C/CX (ADM6992C/CX) allows switching between different speed media (e.g. 10BaseX and 100BaseX) in store & forward mode. The entire received frame will be stored into its packet buffer. The NINJA C/CX (ADM6992C/CX) checks the length and frame check sequence (FCS) of the received frame to prevent the forwarding of corrupted packets before forwarding to the destination port. A MAC address filtering process can be enabled to filter local traffic to improve overall network performance. The maximum packet length is up to 9216 bytes in this mode. The maximum packet length is defined in Bit [13:0] of EEPROM register 03_H.

3.3.2 Modified Cut-through Mode

The NINJA C/CX (ADM6992C/CX) begins to forward the received packet when it receives the first 64 bytes of the packet. The latency is about 512 bits time width. The NINJA C/CX (ADM6992C/CX) will not forward fragment packets. The MAC address learning & filtering should be disabled in this mode, because the received packets may be corrupted. The maximum packet length is up to 9216 bytes in this mode. The maximum packet length is defined in Bit [13:0] of EEPROM register 03_H.

3.3.3 MII cut-through Mode

The NINJA C/CX (ADM6992C/CX) begins to forward the received packet at the beginning of the received packet. It provides the minimum latency in this mode. The maximum packet length is 9216 bytes if the clock difference between MII receive clock and MII transmit clock is 200Ppm.

3.4 Basic Operations

3.4.1 MAC Address Learning & Filtering

The NINJA C/CX (ADM6992C/CX) adopts 4-way associative hash architecture to store the MAC address table. It can store up to a maximum 1K of MAC addresses.

In store & forward mode, the NINJA C/CX (ADM6992C/CX) receives incoming packets from one of its ports, searches in the Address Table for the Destination MAC Address, and then forwards the packet to the other port, if appropriate. If the destination address is not found in the address table, the NINJA C/CX (ADM6992C/CX) treats the packet as a broadcast packet and forwards the packet to the other ports. If the destination port is the same with the port where the packet received from, the NINJA C/CX (ADM6992C/CX) treats the packet as a local traffic packet and discards it.

3.4.2 Address Learning

The NINJA C/CX (ADM6992C/CX) searches for the Source Address (SA) of an incoming packet in the Address Table and acts as below:

1. The NINJA C/CX (ADM6992C/CX) automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming packets at wire speed
2. If the SA was not found in the Address Table (a new address), the NINJA C/CX (ADM6992C/CX) waits until the end of the packet (non-error packet) and updates the Address Table
3. If the SA was found in the Address Table, then the aging value of each corresponding entry will be reset to 0
4. When the DA is in PAUSE mode, then the learning process will be disabled automatically by the NINJA C/CX (ADM6992C/CX)

3.4.3 Hash Algorithm

The NINJA C/CX (ADM6992C/CX) supports two types of hash algorithms for address learning & filtering. The first is the CRC-CCITT polynomial method. The 48 bits MAC address is reduced to a 16 bits CRC hash value. Bit [7:0] of the CRC are used to index the 1K address table. The CRC-CCITT polynomial is

$$X^{16} + X^{12} + X^5 + 1$$

The second is the direct-map method. The 48-bit MAC address is mapped into a 8 bits address spaced by XOR-method to index the 1K address table.

The hash type can be selected by using bit [15] of EEPROM register 03_H.

3.4.4 Address Recognition and Packet Forwarding

The address learning & filtering process forwards the incoming packets between bridged ports according to the Destination Address (DA) as below.

1. If the DA is a UNICAST address and the address was found in the Address Table, the NINJA C/CX (ADM6992C/CX) will check the port number and act as follows:
   a) If the port number is equal to the port on which the packet was received, the packet is discarded.
   b) If the port number is different from the port on which the packet was received, the packet is forwarded across the bridge.
2. If the DA is a UNICAST address and the address was not found, the NINJA C/CX (ADM6992C/CX) treats it as a multicast packet and forwards it across the bridge.
3. If the DA is a Multicast address, the packet is forwarded across the bridge.
4. If the DA is PAUSE Command (01-80-C2-00-00-01), then this packet will be dropped by the NINJA C/CX (ADM6992C/CX). The NINJA C/CX (ADM6992C/CX) can issue and learn PAUSE commands.
5. The NINJA C/CX (ADM6992C/CX) will forward by default or filter out the packet with DA of (01-80-C2-00-00-00), discard the packet with DA of (01-80-C2-00-00-01), filter out the packet with DA of (01-80-C2-00-00-02 ~ 01-80-C2-00-00-0F), and forward the packet with DA of (01-80-C2-00-00-10 ~ 01-80-C2-00-00-FF) decided by EEPROM Reg. $0E_H$.

3.4.5 Address Aging

Address aging is supported for topology changes such as an address moving from one port to the other. When this happens, the NINJA C/CX (ADM6992C/CX) internally has 300 seconds timer, after which the address will be “aged out” (removed) from the address table. Aging function can enabled/disabled by the user. Normally, disabling the aging function is for security purposes.

3.4.6 Back off Algorithm

The NINJA C/CX (ADM6992C/CX) implements the truncated exponential back off algorithm compliant to the 802.3 CSMA-CD standard. The NINJA C/CX (ADM6992C/CX) will restart the back off algorithm by choosing 0-9 collision counts. The NINJA C/CX (ADM6992C/CX) resets the collision counter after 16 consecutive retransmitting trials.

3.4.7 Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The typical number is 96 bits time. The value is 9.6us for 10Mbps ETHERNET, 960ns for 100Mbps fast ETHERNET, and 96ns for 1000M. The NINJA C/CX (ADM6992C/CX) provides an option of 92 bit-time gaps in the EEPROM to prevent packet loss when Flow Control is turned off and the clock P.P.M. value differs.

3.4.8 Illegal Frames

In store & forward mode, the NINJA C/CX (ADM6992C/CX) will discard all illegal frames such as small packets (less than 64 bytes), oversized packets (greater than the value which is defined in Bit [13:0] of EEPROM register 03_H) and bad CRC. Dribbling packing with good CRC value will accept by NINJA C/CX (ADM6992C/CX).

In modified cut-through mode, the NINJA C/CX (ADM6992C/CX) will forward all received packets except for small packets (less than 64 bytes).

In MII cut-through mode, the NINJA C/CX (ADM6992C/CX) will forward all received packets.

3.4.9 Half Duplex Flow Control

A Back Pressure function is supported for half-duplex operation. When the NINJA C/CX (ADM6992C/CX) cannot allocate a received buffer for an incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision. Back Pressure is disabled by DISBP which is set during RESETL assertion. A proprietary

algorithm is implemented inside the NINJA C/CX (ADM6992C/CX) to prevent the back pressure function causing HUB partition under a heavy traffic environment and reduce the packet lost rate to increase the whole system performance.

3.4.10 Full Duplex Flow Control

When a full duplex port runs out of its received buffer space, a PAUSE packet command will be issued by the NINJA C/CX (ADM6992C/CX) to notify the packet sender to pause transmission. This frame based flow control is totally compliant to IEEE 802.3x. The NINJA C/CX (ADM6992C/CX) can issue or receive pause packets.

3.4.11 Bandwidth Control

NINJA C/CX (ADM6992C/CX) supports hardware-based bandwidth control for both ingress and egress traffics. Ingress and egress rates can be limited independently on a per port base. The NINJA C/CX (ADM6992C/CX) uses 8ms at the scale, and the minimum bandwidth control unit is 4 kbit/s so users can configure the rate equal to K * 4 kbit/s, 1<=K<=25000. The NINJA C/CX (ADM6992C/CX) maintains two counters (input and output) for each port. For example, if users want to limit the rate to 64 kbit/s, they should configure the bandwidth control threshold to 16. For each time unit, the NINJA C/CX (ADM6992C/CX) will add 64 to the counter and decrease the byte length when receiving a packet during this period. When the counter is decreased to zero, we can divide the control behavior into two parts:

1. For the ingress control, the ingress port will not stop receiving packets. If flow control is enabled, Pause packets will be transmitted, if Back Pressure is enabled, Jam packets will be transmitted, and if the above functions are not enabled, the packet will be discarded.
2. For the egress control, the egress port will not transmit any packets. The port receiving packets that are forwarded to the egress port will transmit Pause packets if flow control is enabled, transmit Jam packets if Back Pressure is enabled, and discard packets if all the above functions are not enabled.

3.4.12 Interrupt

With the use of external CPU support, the NINJA C/CX (ADM6992C/CX) can issue an interrupt to the CPU if any event defined in SMI interrupt register 10_H and SMI interrupt mask register 11_H occurs.

3.4.13 Auto TP MDIX function

The normal application in which a Switch connects to a NIC card is by a one-to-one TP cable. If the Switch connects to other devices such as another Switch, it can be done by two ways. The first is to use a Cross Over TP cable and the second way is to use an extra RJ45 connector by internally crossing over the TXP/TXN and RXP/RXN signals. By using the second way, customers can use a one-to-one cable to connect two Switch devices. All these efforts add extra costs and are not a good solution. The NINJA C/CX (ADM6992C/CX) provides an Auto MDIX function, which adjusts the TXP/TXN and RXP/RXN automatically on the correct pins. Users can use one-to-one cabling between the NINJA C/CX (ADM6992C/CX) and other devices either switches or NICs.

3.5 Converter Functional Description

3.5.1 Fault Propagation

The NINJA C/CX (NINJA C/CX (ADM6992C/CX)) Media Converter incorporates a Fault Propagation feature, which allows indirect sensing of a Fiber Link Loss via the 10/100Base-TX UTP connection. Whenever the NINJA C/CX (NINJA C/CX (ADM6992C/CX)) Media Converter detects a Link Loss condition on the Received fiber (Fiber LNK OFF), it disables its UTP link pulse so that a Link Loss condition will be sensed on the UTP port to which the

NINJA C/CX (NINJA C/CX (ADM6992C/CX)) Media Converter is connected. This link loss can then be sensed and reported by a Network Management agent in the remote UTP port's host equipment. This feature will affect the NINJA C/CX (NINJA C/CX (ADM6992C/CX)) UTP LNK LED.

The NINJA C/CX (NINJA C/CX (ADM6992C/CX)) Media Converter also incorporates a Far End Fault feature, which allows the stations on both ends of a pair of fibers to be informed when there is a problem with one of the fibers. Without Far End Fault, it is impossible for a fiber interface to detect a problem that affects only its Transmitting fiber.

When Far End Fault is supported and enabled, a loss of received signal (link) will cause the transmitter to generate a Far End Fault pattern in order to inform the device at the far end of the fiber pair that a fault has occurred. Unless Fiber Link Loss occurs or if the UTP port link fails, the NINJA C/CX (NINJA C/CX (ADM6992C/CX)) Media Converter will also generate a Far End Fault pattern in order to inform the device at the far end of the fiber pair that a fault has occurred.

3.6 Serial Management Interface (SMI) Register Access

The SMI consists of two pins, management data clock (SDC) and management data input/output (SDIO). The NINJA C/CX (ADM6992C/CX) is designed to support an SDC frequency up to 25 MHz. The SDIO line is bi-directional and may be shared with other devices.

The SDIO pin requires a 1.5 K pull-up which, during idle and turnaround periods, will pull SDIO to a logic one state. NINJA C/CX (ADM6992C/CX) requires a single initialization sequence of 35 bits of preamble following power-up/hardware reset. The first 35 bits are preamble consisting of 35 contiguous logic one bits on SDIO and 35 corresponding cycles on SDC. Following preamble is the start-of-frame field indicated by a <01> pattern. The next field signals the operation code (OP): <10> indicates read from management register operation, and <01> indicates write to management register operation. The next field is the management register address. It is 10 bits wide and the most significant bit is transferred first.

Table 11 SMI Read/Write Command Format

Operation	Preamble	SFD	OP	CHIPID[1:0]	Unused	Register Address	TA	Data
Read	35"1"s	01	10	2 bits CHIPID	00	6 bits Address	Z0	32 bits Data Read
Write	35"1"s	01	01	2 bits CHIPID	00	6 bits Address	10	32 bits Data Write

During Read operation, a 2-bit turn around (TA) time spacing between the register address field and data field is provided for the SDIO to avoid contention. Following the turnaround time, a 32-bit data stream is read from or written into the management registers of the NINJA C/CX (ADM6992C/CX).

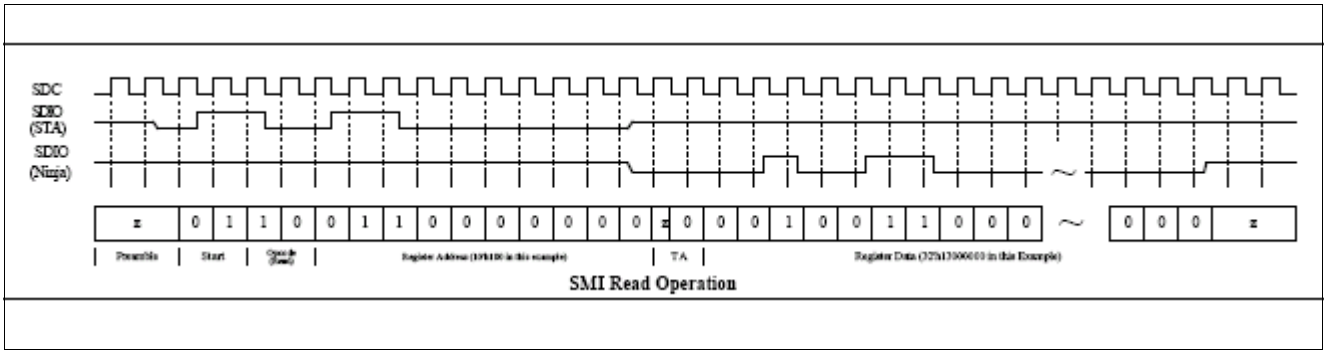

Figure 3 SMI Read Operation