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ADM6993/X

ADM6993/X HDLC to Fast Ethernet Converter

Communications

Never stop thinking.

Edition 2005-11-28

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Previous Version:

Page/Date	Subjects (major changes since last revision)
2003-07-02	Rev. 1.0: First release of ADM6993
2003-10-13	Rev. 1.1: Added sections 4.3&4.4
2005-08-15	Changed to the new Infineo format
2005-09-09	Rev. 1.11: when changed to the new Infineon format
2005-11-28	Minor change. Included Green package information

Trademarks

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1 Product Overview

Features and the block diagram.

1.1 Overview

The ADM6993/X is a single chip integrating two 10/100 Mbps MDIX TX/FX transceivers, a three-port 10/100M Ethernet L2 switch controller, and features converter mode to meet demanding applications, including Fiber-to-Ethernet media converters, 2/3 port Ethernet switches, VoIP gateways, and NAT routers. The ADM6993X is the environmentally friendly “green” package version.

The ADM6993/X supports priority features on Port-Base priority, VLAN TAG priority and IP TOS precedence checking at individual ports. This is done through a small low-cost micro controller to initialize or on-the-fly to configure. The priority of packets can be tagged based on TCP port number for the multi-media application.

The 2nd MAC interface could be selected as TP/FX or MII/RMII/GPSI to connect with bridge devices for different media. The 3rd MAC interface could be selected as MII/RMII/GPSI/HDLC to connect with routing devices, and bridge devices for different media. The dedicated HDLC channel supports rate from 64Kbps to 50Mbps.

On the media side of port0/1, the ADM6993/X supports auto MDIX 10Base-T/100Base-TX and 100Base-FX as specified by the IEEE 802.3 committee through uses of digital circuitry and high speed A/D.

ADM6993/X supports serial management interface (SMI) for a small low-cost micro controller to initialize or configure. It also provides port status for remote agent monitor and smart counter for port statistics.

1.2 Features

Main features:

- 3-port10/100M switch integrated with a 2-port PHY (10/100TX and 100FX) and 3rd MAC port as GPSI/MII/RMII/HDLC.
- Provides TX<-->FX Converter modes with faulted propagation and redundant capability by using of two ADM6993/X.
- Short latency on the converter mode.
- Built-in data buffer 6Kx64bit SRAM.
- Up to 2k MAC Unicast addresses with a 4-way associative hashing table.
- MAC address learning table with aging function.
- Two queues per port for QoS purposes.
- Port-base, 802.1p and TCP/IP ToS priority.
- Store & forward architecture.
- 802.3x flow control for full duplex and back-pressure for half duplex in case the buffer is full.
- Supports Auto-Negotiation.
- Packet lengths up to 1536 bytes.
- Broadcast storming filter.
- Port-base VLAN/tag-base VLAN.
- 16 entries of packet classification and marking or filtering for TCP/UDP Port Numbering, IP Protocol ID and Ethernet Type.
- Serial Management Interface for low-end CPUs.
- Provides port status for remote agent monitoring .
- Provides smart counters for port statistics reporting.
- 128 PQFP packaging with 2.5 V/3.3 V power supply.

1.3 Block Diagram

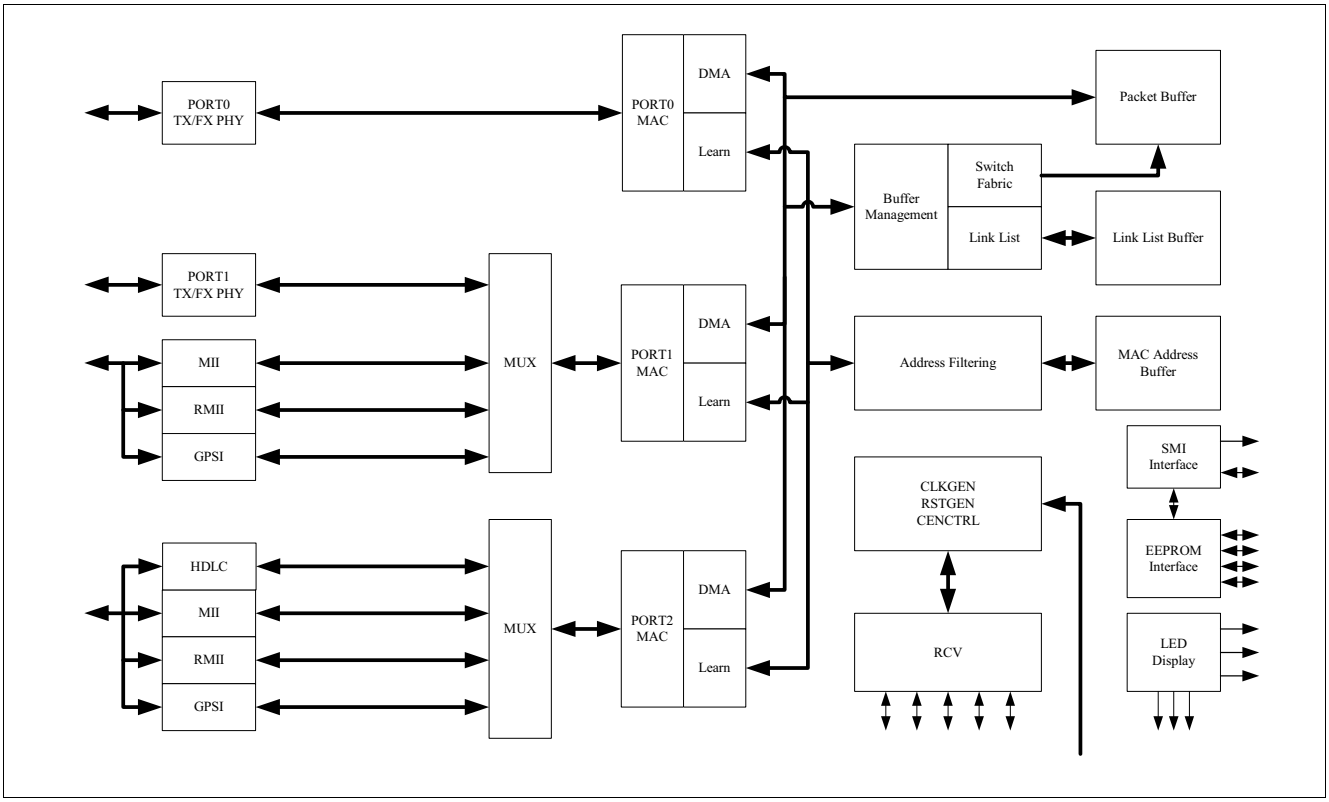

Figure 1 ADM6993/X Block Diagram

1.4 Data Lengths Conventions

Table 1 Data Lengths Conventions

qword	64 bits
dword	32 bits
word	16 bits
byte	8 bits
nibble	4 bits

2 Interface Description

This chapter describes Pin Diagram, Pin Type and Buffer Type Abbreviations, and Pin Descriptions.

2.1 Pin Diagram

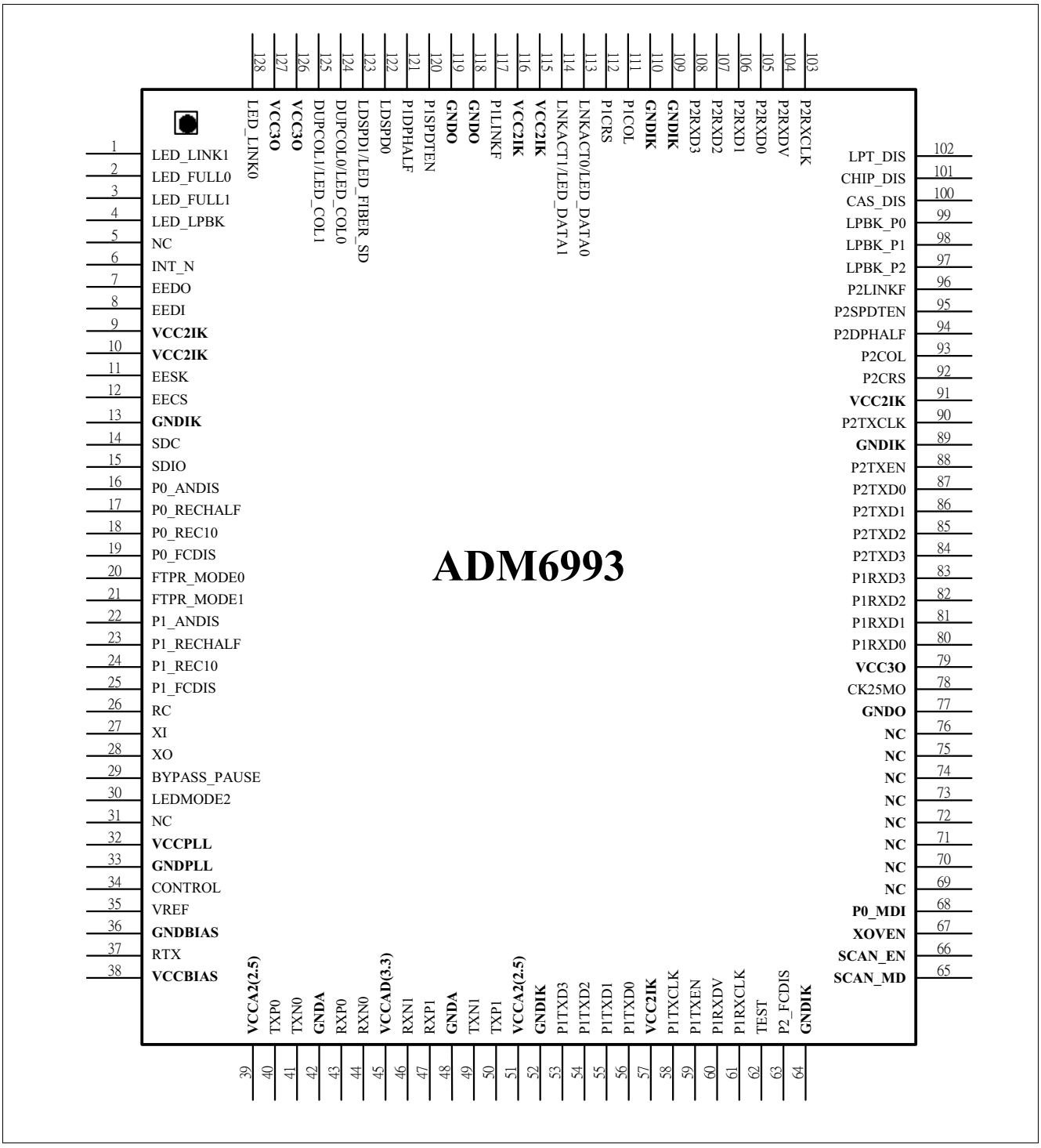

Figure 2 ADM6993/X Pin Assignment

2.2 Pin Type and Buffer Type Abbreviations

Standardized abbreviations:

Table 2 ADM6993/XAbbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 3 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU1	Pull up, 10 k Ω
PD1	Pull down, 10 k Ω
PD2	Pull down, 20 k Ω
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

2.3 Pin Descriptions

ADM6993/X pins are categorized into one of the following groups:

- Port 0/1 Twisted Pair Interface, 8 pins
- Port 2 (MII/RMII/GPSI) Interface, 17 pins
- Port 1 alternative MII Port Interface, 17 pins
- LED Interface, 13 pins
- EEPROM Interface, 4 pins
- Configuration Interface, 28 pins
- Ground/Power Interface, 27 pins
- Miscellaneous, 14 pins

Note: If not specified, all signals default to digital signals.

Table 4 Port 0/1 Twisted Pair Interface (8 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
40	TXP_0	AO		**Twisted Pair Transmit** Output Positive.
50	TXP_1	AO		
41	TXN_0	AO		**Twisted Pair Transmit** Output Negative.
49	TXN_1	AO		
43	RXP_0	AI		**Twisted Pair Receive** Input Positive.
47	RXP_1	AI		
44	RXN_0	AI		**Twisted Pair Receive** Input Negative.
46	RXN_1	AI		

Table 5 Port 2 (MII/RMII/GPSI) Interface (17 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
87	P2TXD0	I/O	TTL, PD, 8mA	**Port 2 MII Transmit Data bit 0** Synchronous to the rising edge of TXCLK.
	FXMODE0			**FXMODE0** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as bit 0 of FXMODE.
86	P2TXD1	I/O	TTL, PD, 8mA	**Port 2 MII Transmit Data bit 1** Synchronous to the rising edge of TXCLK.
	FXMODE1			**FXMODE1** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as bit 1 of FXMODE. FXMODE [1:0] Interface 00_B , Both Port0 & Port1 are TP port 01_B , Port0 is TP port and Port1 is FX port 10_B , Port0 is TP port and Port1 is FX port (converter mode) 11_B , Both Port0 & Port1 are FX port

Table 5 Port 2 (MII/RMII/GPSI) Interface (17 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
85	P2TXD2	I/O	TTL, PD, 8mA	**Port 2 MII Transmit Data bit 2** Synchronous to the rising edge of TXCLK.
	P2BUSMD0			**P2BUSMD0** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as P2BUSMD0.
84	P2TXD3	I/O	PD, 8mA	**Port 2 MII Transmit Data bit 3**
	P2BUSMD1			**P2BUSMD1** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as P2BUSMD1. BUSMD[1:0] Interface 00_B , MII(Default) 01_B , RMII 10_B , GPSI 11_B , HDLC
88	P2TXEN	I/O	PD, 8mA	**Port 2 MII Transmit Enable** Synchronous to the rising edge of TXCLK
	DISBP			**DISBP. Disable Back Pressure** 0_B , Enable back-pressure(Default) 1_B , Disable back-pressure
108	P2RXD_3	I	TTL, PD	**Port 2 MII Receive Data bit 3 ~ 0**
107	P2RXD_2			
106	P2RXD_1			
105	P2RXD_0			
104	P2RXDV	I	TTL, PD	**Port 2 MII Receive Data Valid**
93	P2COL	I	TTL, PD	**Port 2 MII Collision input**
92	P2CRS	I	TTL, PD	**Port 2 MII Carrier Sense**
103	P2RXCLK	I	TTL, PD	**Port 2 MII Receive Clock Input**
90	P2TXCLK	I	TTL, PD	**Port 2 MII Transmit Clock Input**
96	P2LINKF	I	TTL, PU	**P2LINKF** This pin will be used to input the Link Status of Port2 1_B , Link Fail
95	P2SPDTEN	I	TTL, PD	**P2SPDTEN** This pin will be used as Port 2 Speed Status input 1_B , 10M
94	P2DPHALF	I	TTL, PD	**P2DPHALF** This pin will be used as Port 2 Duplex Status input 1_B , Half Duplex

Table 6 Port 1 Alternative MII Port Interface (17 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
56	P1TXD0/CHIPID_0	I/O	TTL, PD, 8mA	**Port 1 MII Transmit Data bit 0/Chip ID Bit 0** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as CHIPID_0.This pin will become P1RXD0 if P1BUSMD[1:0] is 11. Synchronous to the rising edge of TXCLK.
55	P1TXD1/CHIPID_1	I/O	TTL, PD, 8mA	**Port 1 MII Transmit Data bit 1/Chip ID Bit 1** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as CHIPID_1.This pin will become P1RXD1 if P1BUSMD[1:0] is 11. Synchronous to the rising edge of TXCLK.
54	P1TXD2/P1BUSMD0	I/O	TTL, PU, 8mA	**Port 1 MII Transmit Data bit 2/ Port 1 Bus Mode bit 0** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as P1BUSMD0.This pin will become P1RXD2 if P1BUSMD[1:0] is 11. Synchronous to the rising edge of TXCLK. P1BUSMD[1:0] Interface 00_B , MII (Power Down TX Phy) 01_B , RMII (Power Down TX Phy) 10_B , GPSI (Power Down TX Phy) 11_B , TP/FX (default)
53	P1TXD3/P1BUSMD1	I/O	TTL, PU, 8mA	**Port 1 MII Transmit Data bit 3/ Port 1 Bus Mode bit 1** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as P1BUSMD1.This pin will become P1RXD3 if P1BUSMD[1:0] is 11. Synchronous to the rising edge of TXCLK. P1BUSMD[1:0] Interface 00_B , MII (Power Down TX Phy) 01_B , RMII (Power Down TX Phy) 10_B , GPSI (Power Down TX Phy) 11_B , TP/FX (default)
59	P1TXEN	O	TTL, PD, 8mA	**Port 1 MII Transmit Enable** This pin will become P1RXDV if P1BUSMD[1:0] is 11. Synchronous to the rising edge of TXCLK
	IDLE_MODE			**IDEL_MODE** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as HDLC IDLE frame control mode. IDLE_MODE IDLE Pattern 0_B , FF_H(Default) 1_B , $7E_H$

Table 6 Port 1 Alternative MII Port Interface (17 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
83	P1RXD_3	I	TTL, PD	**Port 1 MII Receive Data bit 3 ~ 0** These pins will become P1TXD[3:0] if P1BUSMD[1:0] is 11
82	P1RXD_2			
81	P1RXD_1			
80	P1RXD_0			
60	P1RXDV	I	TTL, PD	**Port 1 MII Receive Data Valid** This pin will become P1TXEN if P1BUSMD[1:0] is 11
111	P1COL	I/O	TTL, PD	**Port 1 MII Collision input** This pin will become P1COL if P1BUSMD[1:0] is 11 and becomes an output pin
112	P1CRS	I/O	TTL, PD	**Port 1 MII Carrier Sense** This pin will become P1CRS if P1BUSMD[1:0] is 11 and becomes an output pin
61	P1RXCLK	I/O	TTL, PD	**Port 1 MII Receive Clock Input** This pin will become P1CRS if P1BUSMD[1:0] is 11 and becomes an output pin
58	P1TXCLK	I/O	TTL, PD	**Port 1 MII Transmit clock Input** This pin will become P1CRS if P1BUSMD[1:0] is 11 and becomes an output pin.
117	P1LINKF	I	TTL, PU	**Port 1 Link Fail Status** This pin will be used to input the Link Status of Port1 if Port1 is not connected to internal PHY 1_B , Link Fail
120	P1SPDTEN	I	TTL, PD	**Port 1 Speed Status** This pin will be used as Port 1 Speed Status input if Port1 is not connected to internal PHY 1_B , 10M
121	P1DPHALF	I	TTL, PD	**Port 1 Duplex Status** This pin will be used as Port 2 Duplex Status input if Port1 is not connected to internal PHY 1_B , Half Duplex

Table 7 LED Interface (13 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
113	LNKACT_0	I/O	TTL PD 8mA	**PORT0 Link & Active LED/Link LED.** If LEDMODE_0 is 1, this pin indicates both link status and RX/TX activity. When link status is LINK_UP, LNKACT_0 will be turned on. While PORT0 is receiving/transmitting data, LNKACT_0 will be off for 100ms and then on for 100ms. If LEDMODE_0 is 0, this pin only indicates RX/TX activity.
	LED_DATA_0			**Port0 LED DATA**
	LEDMODE_0			**LED mode for LINK/ACT LED of PORT0.** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as LEDMODE_0.
114	LNKACT_1	I/O	TTL PD 8mA	**PORT1 Link & Active LED/Link LED.** If LEDMODE_2 is 1, this pin indicates both link status and RX/TX activity. When link status is LINK_UP, LNKACT_1 will be turned on. While PORT1 is receiving/transmitting data, LNKACT_1 will be off for 100ms and then on for 100ms. If LEDMODE_2 is 0, this pin only indicates RX/TX activity.
	LED_DATA_1			**Port1 LED DATA**
	LEDMODE_1			**LED mode DUPLEX/COL LED of PORT0 & PORT1.** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as LEDMODE_1. If LEDMODE_1 is 1, DUPCOL[1:0] will display both duplex condition and collision status. If LEDMODE_1 is 0, only collision status will be displayed.
30	LEDMODE_2	I	TTL PD	**LED mode for LINK/ACT LED of PORT1** 0_B , ACT 1_B , LINK/ACT
124	DUPCOL_0	I/O	TTL PD 8mA	**PORT0 Duplex LED** If LEDMODE_1 is 1, this pin indicates both duplex condition and collision status. When FULL_DUPLEX, this pin will be turned on for PORT0. When HALF_DUPLEX and no collision occurs, this pin will be turned off. When HALF_DUPLEX and a collision occurs, this pin will be off for 100ms and then on for 100ms. If LEDMODE_1 is 0, this pin indicates collision status. When in HALF_DUPLEX and a collision occurs, this pin will be off for 100ms and turn on for 100ms.
	LED_COL_0			**Port0 Collision LED**
	DIS_LEARN			**Disable Address Learning.** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as DIS_LEARN. If DIS_LEARN is 1, MAC address learning will be disabled.

Table 7 LED Interface (13 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
125	DUPCOL_1 /LED_COL_1	I/O	TTL PU 8mA	**PORT1 Duplex** If LEDMODE_1 is 1, this pin indicates both duplex condition and collision status. When FULL_DUPLEX, this pin will be turned on for PORT1. When HALF_DUPLEX and no collision occurs, this pin will be turned off. When HALF_DUPLEX and a collision occurs, this pin will be off for 100ms and then on for 100ms. If LEDMODE_1 is 0, this pin indicates collision status. When HALF_DUPLEX and a collision occurs, this pin will be off for 100ms and turn on for 100ms.
122	LDSPD_0	I/O	TTL PU 8mA	**PORT0 Speed LED** Used to indicate speed status of PORT0. When operating in 100Mbps this pin is turned on, and when operating in 10Mbps this pin is off.
	RDNT_EN			**Enable Redundant Capability** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as RDNT_EN. If RDNT_EN is 0, "REDUNDANT" capability will be disabled. For TS1000 application this pin should have a value of 0.
123	LDSPD_1	I/O	TTL PU 8mA	**PORT1 Speed LED** Used to indicate speed status of PORT1. When operating in 100Mbps this pin is turned on, and when operating in 10Mbps this pin is off.
	LED_FIBER_SD			**LED_FIBER_SD** Used to indicate signal status of PORT1 when ADM6993/X is operating in converter mode.
	SNP_EN			**Enable Snooping Mode** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as SNP_EN. If SNP_EN is 0, "SNOOPING" capability will be disabled.
1	LED_LINK_1	O	TTL 8mA	**PORT[1:0] Link LED** These pins indicate link status. When link status is LINK_UP, these pins will be turned on for relevant port.
128	LED_LINK_0			
3	LED_FULL_1	O	TTL 8mA	**PORT[1:0] Full Duplex LED** These pins indicate current duplex condition of PORT0. When FULL_DUPLEX, these pins will be turned on for relevant port. When HALF_DUPLEX these pins will be turned off for relevant port.
2	LED_FULL_0			
4	LED_LPBK	O	TTL 8mA	**Loop Back Test LED** While performing loop back test this pin is turned on.

Table 8 EEPROM Interface (4 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
7	EEDO	I	TTL PU	**EEPROM Data Output** Serial data input from EEPROM. This pin is internal pull-up.
12	EECS	I/O	PD 4mA	**EEPROM Chip Select** This pin is active high chip enabled for EEPROM. When RESETL is low, it will be tristate.
11	EECK	I/O	TTL PU 4mA	**Serial Clock** This pin is the EEPROM clock source. When RESETL is low, it will be tristate. This pin is internal pull-up.
8	EEDI	I/O	TTL PU 4mA	**EEPROM Serial Data Input** This pin is the output for serial data transfer. When RESETL is low, it will be tristate.

Table 9 Configuration Interface (28 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
16	P0_ANDIS	I	TTL PD	**Auto-Negotiation Disable for PORT0** 0_B **E**, Enable 1_B **D**, Disable
17	P0_RECHALF	I	TTL PD	**Recommend Half Duplex Communication for PORT0** 0_B **F**, Full 1_B **H**, Half
18	P0_REC10	I	TTL PD	**Recommend 10M for PORT0** 0_B **100**, 100M 1_B **10**, 10M
19	P0_FCDIS	I	TTL PD	**Flow Control Disable for PORT0** 0_B **E**, Enable 1_B **D**, Disable
22	P1_ANDIS	I	TTL PD	**Auto-Negotiation Disable for PORT1** 0_B **E**, Enable 1_B **D**, Disable
23	P1_RECHALF	I	TTL PD	**Recommend Half Duplex Communication for PORT1** 0_B **F**, Full 1_B **H**, Half
24	P1_REC10	I	TTL PD	**Recommend 10M for PORT1** 0_B **100**, 100M 1_B **10**, 10M
25	P1_FCDIS	I	TTL PD	**Flow Control Disable for PORT1** 0_B **E**, Enable 1_B **D**, Disable
63	P2_FCDIS	I	TTL PD	**Flow Control Disable for PORT2** 0_B **E**, Enable 1_B **D**, Disable

Table 9 Configuration Interface (28 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
67	XOVEN	I	TTL PD	**Auto-MDIX Enable.** 0_B **D**, Disable 1_B **E**, Enable
68	P0_MDI	I	TTL PU	**MDI/MDIX Control for PORT0** This setting will be ignore if enable Auto-MDIX. 0_B **MDIX**, MDIX 1_B **MDI**, MDI
21, 20	FTPR_MODE[1:0	I	TTL PD	**Fault Propagation Mode** 00_B **R**, Reserved 01_B **Fx**, FX fail -> UTP fail, UTP fail -> FX transmit FEFI 10_B **R**, Reserved 11_B **D**, Disable
99	LPBK_P0	I	TTL PD	**Enable Loop Back Test for PORT0** 0_B **D**, Disable 1_B **E**, Enable
98	LPBK_P1	I	TTL PD	**Enable Loop Back Test for PORT1** 0_B **D**, Disable 1_B **E**, Enable
97	LPBK_P2	I	TTL PD	**Enable Loop Back Test for PORT2** 0_B **D**, Disable 1_B **E**, Enable
101	CHIP_DIS	I	TTL PD	**Chip Disable** 0_B **D**, Disable 1_B **E**, Enable
100	CAS_DIS	O	TTL 4mA	**Disable Cascaded Chip** 0_B **D**, Disable 1_B **E**, Enable
102	LPT_DIS	I	TTL PD	**Link Pass Through Disable** 0_B **E**, Enable 1_B **D**, Disable
29	BYPASS_PAUSE	I	TTL PD	**Bypass Frame** The destination address is reserved IEEE MAC address 0_B **D**, Disable 1_B **E**, Enable

Table 10 Ground/Power Interface (27 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
42, 48	GNDTR	GND, A		**Ground** Used by AD receiver/transmitter block.
39, 51	VCCA2	PWR, A		**2.5 V used for Analogue block**
45	VCCAD	PWR, A		**3.3 V used for TX line driver**

Table 10 Ground/Power Interface (27 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
36	GNDBIAS	GND, A		**Ground used by digital substrate**
38	VCCBIAS	PWR, A		**3.3 V used for bios block**
33	GNDPLL	GND, A		**Ground used by PLL**
32	VCCPLL	PWR, A		**2.5 V used for PLL**
13, 52, 64, 89, 109, 110	GNDIK	GND, D		**Ground used by digital core and pre-driver**
9, 10, 57, 91, 115, 116	VCCIK	PWR, D		**2.5 V used for digital core and pre-driver**
77, 118, 119	GNDO	GND, D		**Ground used by digital pad**
79, 126, 127	VCC3O	PWR, D		**3.3 V used for digital pad.**

Table 11 Miscellaneous (14 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
6	$\overline{\text{INT}}$	O	TTL OD 4mA	**Interrupt** This pin will be used to interrupt external management device. This is a low active and open drain pin.
15	SDIO	I/O	TTL PU 8mA	**Serial Management Data** This pin is in/out to PHY. When RESETL is low, this pin will be tristate.
14	SDC	I	TTL 8mA	**Serial Management Data Clock**
78	CKO25M	O	TTL PU 8mA	**50M output for RMII and 25M Clock output for others**
34	CONTROL	AO		**FET Control Signal** The pin is used to control FET for 3.3 V to 2.5 V regulator.
37	RTX	A		**TX Resistor**
35	VREF	A		**Analog Power Failure Detected**
26	RC	I	TTL ST	**RC Input for Power On Reset** ADM6993/X sample pin RC as RESETL with the clock input from pin XI.
27	XI	AI		**25M Crystal Input** 25M Crystal Input. Variation is limited to +/- 50ppm.

Table 11 Miscellaneous (14 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
28	XO	AO		**25M Crystal Output** When connected to oscillator, this pin should left unconnected.
5, 31, 62, 65, 66, 69, 70, 71, 72, 73, 74, 75, 76	NC			**No Connection**

2.4 Port 2 MII/RMII/GPSI/HDLC Interfaces Comparison

Table 12 Port 2 MII/RMII/GPSI/HDLC Interfaces Comparison

Pin No.	MII	RMII	GPSI	HDLC
87	P2TXD0(O)	P2TXD0(O)	P2TXD0(O)	P2TXD0(O)
86	P2TXD1(O)	P2TXD1(O)		
85	P2TXD2(O)			
84	P2TXD3(O)			
88	P2TXEN(O)	P2TXEN(O)	P2TXE(O)	
No Support	P2TXER(O)			
90	P2TXCLK(I)		P2RXCLK(I)	P2RXCLK(I)
105	P2RXD0(I)	P2RXD0(I)	P2RXD0(I)	P2RXD0(I)
106	P2RXD1(I)	P2RXD1(I)		
107	P2RXD2(I)			
108	P2RXD3(I)			
104	P2RXDV(I)	P2CRS_DV(I)	P2RXE/CRS(I)	
No Support	P2RXER(I)	P2RXER(I)		
93	P2COL(I)		P2COL(I)	
92	P2CRS(I)			
103	P2RXCLK(I)	P2REFCLK(I)	P2RXCLK(I)	P2RXCLK(I)
Port Status				
96	P2LINKF(I)	P2LINKF(I)	P2LINKF(I)	P2LINKF(I)='0'
95	P2SPDTEN(I)	P2SPDTEN(I)	P2SPDTEN(I)	
94	P2DPHALF(I)	P2DPHALF(I)	P2DPHALF(I)	

ADM6993/X doesn't provide MDC/MDIO to access external PHY, but provides PxLINKF, PxSPDTEN, and PxDPHALF to update MAC status from external PHY LINK/SPEED/DUPLEX LED pin.PxLINKF, Input = 1_B means unlink, 0_B means link.PxSPDTEN, Input = 1_B means 10Mbps, 0_B means 100Mbps.PxDPHALF, Input = 1_B means Half Duplex, 0_B means Full Duplex.

3 Function Description

The ADM6993/X integrates a two 100Base-X physical layer device (PHY), two complete 10Base-T modules, a 3-port 10/100 switch controller and memory into a single chip for both 10 Mbps and 100 Mbps Ethernet switch operations. It also supports 100Base-FX operation through external fiber-optic transceivers. The device is capable of operating in either Full-Duplex or Half-Duplex mode in both 10 Mbps and 100 Mbps operations. Operation modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip auto negotiation logic.

The ADM6993/X consists of four major blocks:

- 10/100M PHY Block
- Switch Controller Block
- Built-in 6Kx64 SSRAM

3.1 10/100M PHY Block

The 100Base-X section of the device implements the following functional blocks:

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- 100Base-X physical medium dependent (PMD)

The 10Base-T section of the device implements the following functional blocks:

- 10Base-T physical layer signaling (PLS)
- 10Base-T physical medium attachment (PMA)

The 100Base-X and 10Base-T sections share the following functional blocks:

- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

The interfaces used for the communication between the PHY block and the switch core is a MII interface.

An Auto MDIX function is supported. This function can be Enabled/Disabled by using the hardware pin. A digital approach for the integrated PHY of the ADM6993/X has been adopted.

3.2 Auto Negotiation and Speed Configuration

3.2.1 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operations supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further detail regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The ADM6993/X supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

The auto negotiation function within the ADM6993/X can be controlled either by internal register access or by the use of configuration pins. If disabled, auto negotiation will not occur until software enables bit 12 in MII Register 0. If auto negotiation is enabled, the negotiation process will commence immediately.

When auto negotiation is enabled, the ADM6993/X transmits the abilities programmed into the auto negotiation advertisement register at address 04_H via FLP bursts. Any combination of 10 Mbps, 100 Mbps, half duplex, and full duplex modes may be selected. Auto negotiation controls the exchange of configuration information. Upon successfully auto negotiating, the abilities reported by the link partner are stored in the auto negotiation link partner ability register at address 05_H.

The contents of the “auto negotiation link partner ability register” are used to automatically configure the highest performance protocol between the local and far-end nodes. Software can determine which mode has been configured by auto negotiation, by comparing the contents of register 04_H and 05_H and then selecting the technology whose bit is set in both registers of highest priority relative to the following list:

1. 100Base-TX full duplex (highest priority)
2. 100Base-TX half duplex
3. 10Base-T full duplex
4. 10Base-T half duplex (lowest priority)

The basic mode control register at address 0_H controls the enabling, disabling and restarting of the auto negotiation function. When auto negotiation is disabled, the speed selection bit (bit 13) controls switching between 10 Mbps or 100 Mbps operation, while the duplex mode bit (bit 8) controls switching between full duplex operation and half duplex operation. The speed selection and duplex mode bits have no effect on the mode of operations when the auto negotiation enable bit (bit 12) is set.

The basic mode status register at address 1_H indicates the set of available abilities for technology types (bit 15 to bit 11), auto negotiation ability (bit 3), and extended register capability (bit 0). These bits are hardwired to indicate the full functionality of the ADM6993/X. The BMSR also provides status on:

- Whether auto negotiation is complete (bit 5)
- Whether the Link Partner is advertising that a remote fault has occurred (bit 4)
- Whether a valid link has been established (bit 2)

The auto negotiation advertisement register at address 4_H indicates the auto negotiation abilities to be advertised by the ADM6993/X. All available abilities are transmitted by default, but writing to this register or configuring external pins can suppress any ability.

The auto negotiation link partner ability register at address 05_H indicates the abilities of the Link Partner as indicated by auto negotiation communication. The contents of this register are considered valid when the auto negotiation complete bit (bit 5, register address 1_H) is set.

3.2.2 Speed Configuration

The twelve sets of four pins listed in **Table 13** configure the speed capability of each channel of the ADM6993/X. The logic states of these pins are latched into the advertisement register (register address 4_H) for auto negotiation

purpose. These pins are also used for evaluating the default value in the base mode control register (register 0_H) according to **Table 13**.

In order to make these pins with the same Read/Write priority as software, they should be programmed to 11111111_B in case a user wishes to update the advertisement register through software.

Table 13 Speed Configuration

Advertise all capability	Advertise single capability	Parallel detect follow IEEE std.	Auto Negoti-ation (Pin & EEPROM)	Speed (Pin & EEPROM)	Duplex (Pin & EEPROM)	Auto Negotiation	Advertise Capability				Parallel Detect Capability			
							10 0F	10 0H	10 F	10 H	10 0F	10 0H	10 F	10 H
1	0	0	1	X	X	1	1	1	1	1	1	0	1	0
1	0	1	1	X	X	1	1	1	1	1	0	1	0	1
1	1	0	1	X	X	1	1	0	0	0	1	0	0	0
1	1	1	1	X	X	1	1	0	0	0	0	1	0	0
0	0	0	1	1	1	1	1	1	1	1	1	0	1	0
0	0	1	1	1	1	1	1	1	1	1	0	1	0	1
0	1	0	1	1	1	1	1	0	0	0	1	0	0	0
0	1	1	1	1	1	1	1	0	0	0	0	1	0	0
0	0	X	1	1	0	1	0	1	0	1	0	1	0	1
0	1	X	1	1	0	1	0	1	0	0	0	1	0	0
0	0	0	1	0	1	1	0	0	1	1	0	0	1	0
0	0	1	1	0	1	1	0	0	1	1	0	0	0	1
0	1	0	1	0	1	1	0	0	1	0	0	0	1	0
0	1	1	1	0	1	1	0	0	1	0	0	0	0	1
0	X	X	1	0	0	1	0	0	0	1	0	0	0	1
X	X	X	0	1	1	0	1	—	—	—	—	—	—	—
X	X	X	0	1	0	0	—	1	—	—	—	—	—	—
X	X	X	0	0	1	0	—	—	1	—	—	—	—	—
X	X	X	0	0	0	0	—	—	—	1	—	—	—	—

3.3 Switch Functional Description

The ADM6993/X uses a “store & forward” switching approach for the following reason:

Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require the large elastic buffer especially bridging between a server on a 100Mbps network and clients on a 10Mbps segment.

Store & forward switches improve overall network performance by acting as a “network cache”

Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port.

3.3.1 Basic Operation

The ADM6993/X receives incoming packets from one of its ports, searches in the Address Table for the Destination MAC Address and then forwards the packet to the other port within the same VLAN group, if appropriate. If the destination address is not found in the address table, the ADM6993/X treats the packet as a broadcast packet and forwards the packet to the other ports which in the same VLAN group.

The ADM6993/X automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming packets at wire speed. If the Source Address is not found in the Address Table, the device adds it to the table.

3.3.2 Address Learning

The ADM6993/X uses a hash algorithm to learn the MAC address and can learn up to 2K MAC addresses. Address is stored in the Address Table. The ADM6993/X searches for the Source Address (SA) of an incoming packet in the Address Table and acts as below:

If the SA was not found in the Address Table (a new address), the ADM6993/X waits until the end of the packet (non-error packet) and updates the Address Table. If the SA was found in the Address Table, then aging value of each corresponding entry will be reset to 0.

When the DA is PAUSE command, then the learning process will be disabled automatically by ADM6993/X.

3.3.3 Address Recognition and Packet Forwarding

The ADM6993/X forwards the incoming packets between bridged ports according to the Destination Address (DA) as below. All the packet forwarding will check VLAN first. A forwarding port must be within the same VLAN as the source port.

1. If the DA is an UNICAST address and the address was found in the Address Table, the ADM6993/X will check the port number and acts as follows:
   a) If the port number is equal to the port on which the packet was received, the packet is discarded.
   b) If the port number is different, the packet is forwarded across the bridge.
2. If the DA is an UNICAST address and the address was not found, the ADM6993/X treats it as a multicast packet and forwards across the bridge.
3. If the DA is a Multicast address, the packet is forwarded across the bridge.
4. If the DA is PAUSE Command (01-80-C2-00-00-01), then this packet will be dropped by ADM6993/X. ADM6993/X can issue and learn PAUSE command.
5. ADM6993/X will forward by defaulted or filtering out the packet with DA of (01-80-C2-00-00-00), discarding the packet with DA of (01-80-C2-00-00-01), filtering out the packet with DA of (01-80-C2-00-00-02 ~ 01-80-C2-00-00-0F), and forwarding the packet with DA of (01-80-C2-00-00-10 ~ 01-80-C2-00-00-FF) decided by EEPROM Reg.7_H.

3.3.4 Address Aging

Address aging is supported for topology changes such as an address moving from one port to the other. When this happens, the ADM6993/X internally has a 300 seconds timer will aged out (remove) the address from the address table. Aging function can be enabled/disabled by user. Normally, disabling aging function is for security purpose.

3.3.5 Buffers and Queues

The ADM6993/X incorporates transmitted queues and the receiving buffer area for the three ETHERNET ports. The receiving buffers as well as the transmitted queues are located within the ADM6993/X along with the switch fabric. The buffers are divided into 192 blocks of 256 bytes each. The queues of each port are managed according to each port's read/write pointer.

3.3.6 Back off Algorithm

The ADM6993/X implements the truncated exponential back off algorithm compliant to the IEEE802.3 CSMA/CD standard. ADM6993/X will restart the back off algorithm by choosing 0-9 collision counts. The ADM6993/X resets the collision counter after 16 consecutive retransmit trials.