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An Infineon Technologies Company

ADM6996L

6 port 10/100 Mb/s
Single Chip Ethernet Switch Controller

Data Sheet
Version 1.03

Infineon-ADMtek Co Ltd

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About this Manual
General Release

Intended Audience
Infineon-ADMtek Co Ltd's Customers

Structure

This Data sheet contains 6 chapters

Chapter 1 Product Overview

Chapter 2 Interface Description

Chapter 3 Function Description

Chapter 4. Register Description

Chapter 5. Electrical Specification

Chapter 6. Packaging

Revision History

Date	Version	Change
02 Sep 2003	1.0	1. First release of ADM6996L
07 October 2003	1.01	2. Updated Section 1.1 and 2.2.2
17 November 2003	1.02	3. Updated Section 4.3.12 & 3.4
12 January 2004	1.03	4. Updated Section 5.3.3 - 8
28 April 2004	1.04	Updated Infineon-ADMtek logo

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Chapter 1 Product Overview

1.1 Overview

The ADM6996L is a high performance, low cost, highly integration (Controller, PHY and Memory) five-port 10/100 Mbps TX/FX plus one 10/100 MAC port Ethernet switch controller with all ports supporting 10/100 Mbps Full/Half duplex. The ADM6996L is intended for applications to stand alone bridge for low cost SOHO market such as 5Port, Router application.

ADM6996L provides most advance function such as: **802.1p(Q.O.S.), 802.1q(VLAN), Port MAC address Locking, Management, Port Status, TP Auto-MDIX, 25M Crystal & Extra MII port** function to meet customer request on Switch demand.

The ADM6996L also supports Back Pressure in Half-Duplex mode and 802.3x Flow Control Pause packet in Full-Duplex mode to prevent packet lost when buffer full. When Back Pressure is enabled, and there is no receive buffer available for the incoming packet, the ADM6996L will issue a JAM pattern on the receiving port in Half Duplex mode and transmit the 802.3x Pause packet back to receiving end in Full Duplex mode.

The built-in SRAM used for packet buffer and address learning table is divided into 256 bytes/block to achieve the optimized memory utilization through complicated link list on packets with various lengths.

ADM6996L also supports priority features by Port-Base, VLAN and IP TOS field checking. User can be easy to set as different priority mode in individual port, through a small low-cost micro controller to initialize or on-the-fly to configure. Each output port supports four queues in the way of fixed N: 1 fairness queuing to fit the bandwidth demand on various types of packet such as Voice, Video and data. 802.1Q, Tag/Untag, and up to 16 groups of VLAN also is supported.

An intelligent address recognition algorithm makes ADM6996L to recognize up to 2048 different MAC addresses and enables filtering and forwarding at full wire speed.

Port MAC address Locking function is also supported by ADM6996L to use on Building Internet access to prevent multiple users sharing one port traffic.

1.2 Features

- Supports five 10M/100M auto-detect Half/Full duplex switch ports with **TX/FX** interfaces and one MII/GPSI port.
- Supports 2048 MAC addresses table.
- Supports four queue for QoS
- Supports priority features by Port-Based, 802.1p VLAN & IP TOS of packets.
- Supports Store & Forward architecture and performs forwarding and filtering at non-blocking full wire speed.
- Supports buffer allocation with 256 bytes per block
- Supports Aging function Enable/Disable.
- Supports per port Single/Dual color mode with Power On auto diagnostic.
- Supports 802.3x Flow Control pause packet for Full Duplex in case buffer is full.
- Supports Back Pressure function for Half Duplex operation in case buffer is full.
- Supports packet length up to 1522 bytes.
- Broadcast Storming Filter function.
- Supports 802.1Q VLAN. Up to 16 VLAN groups is implemented by the last four bits of VLAN ID.
- 2bit MAC clone to support multiple WAN application
- Supports TP interface Auto MDIX function for auto TX/RX swap by strapping-pin.
- Easy Management 32bits smart counter for per port RX/TX byte/packet count, error count and collision count.
- Support PHY status output for management system.
- 25M Crystal only for the whole system.
- 128 QFP package with 0.18um technology. 1.8V/3.3V power supply.

1.3 Applications

ADM6996L in 128-pin PQFP:	SOHO 5-port switch
	5-port switch + Router with MII CPU interface.

1.4 Block Diagram

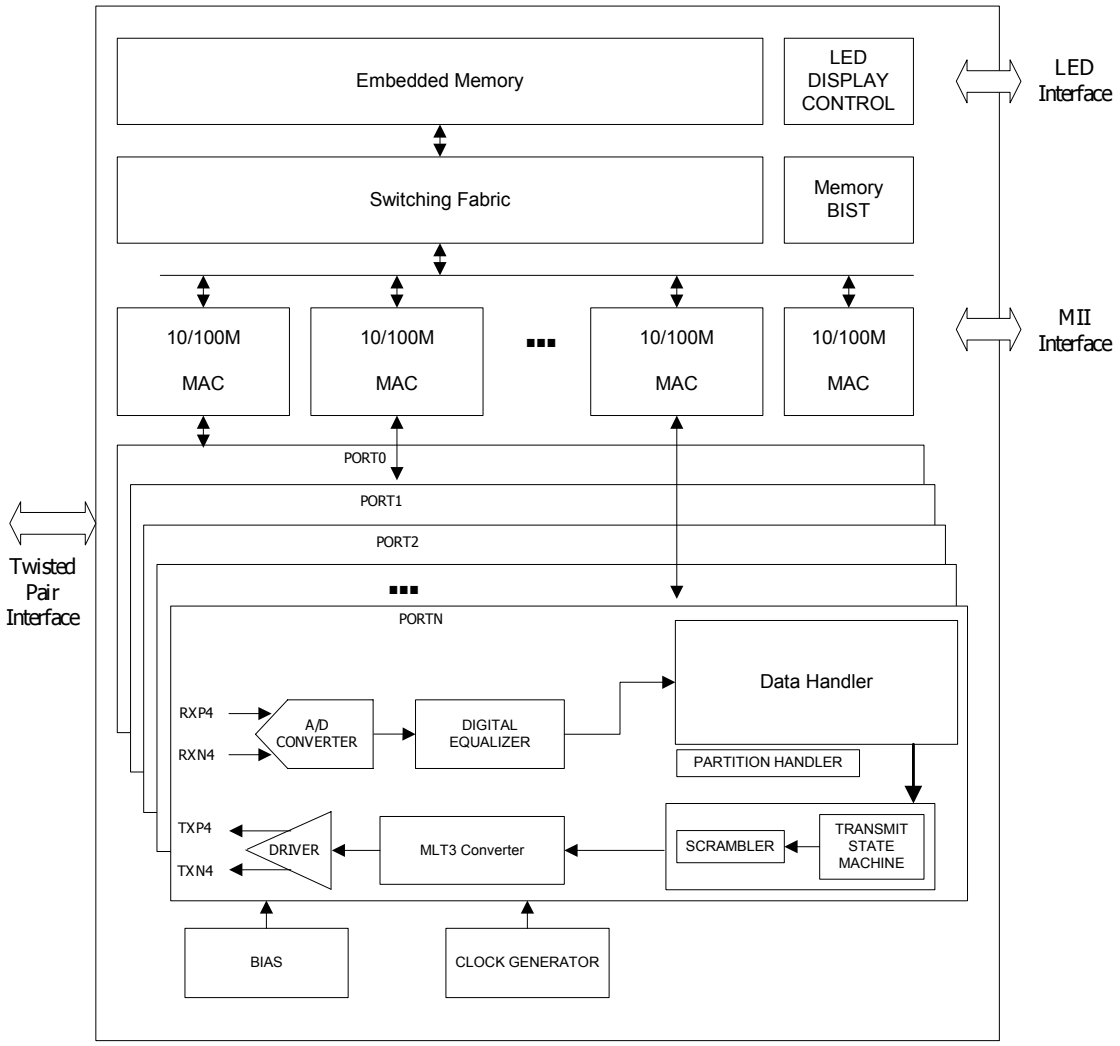

Figure 1-1 ADM6996L Block Diagram

1.5 Abbreviations

BER	Bit Error Rate
CFI	Canonical Format Indicator
COL	Collision
CRC	Cyclic Redundancy Check
CRS	Carrier Sense
CS	Chip Select
DA	Destination Address
DI	Data Input
DO	Data Output
EDI	EEPROM Data Input
EDO	EEPROM Data Output
EECS	EEPROM Chip Select

EESK	EEPROM Clock
ESD	End of Stream Delimiter
FEFI	Far End Fault Indication
FET	Field Effect Transistor
FLP	Fast Link Pulse
GND	Ground
GPSI	General Purpose Serial Interface
IPG	Inter-Packet Gap
LFSR	Linear Feedback Shift Register
MAC	Media Access Controller
MDIX	MDI Crossover
MII	Media Independent Interface
NRZI	Non Return to Zero Inverter
NRZ	Non Return to Zero
PCS	Physical Coding Sub-layer
PHY	Physical Layer
PLL	Phase Lock Loop
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
QoS	Quality of Service
QFP	Quad Flat Package
RST	Reset
RXCLK	Receive Clock
RXD	Receive Data
RXDV	Receive Data Valid
RXER	Receive Data Errors
RXN	Receive Negative (Analog receive differential signal)
RXP	Receive Positive (Analog receive differential signal)
SA	Source Address
SOHO	Small Office Home Office
SSD	Start of Stream Delimiter
SQE	Signal Quality Error
TOS	Type of Service
TP	Twisted Pair
TTL	Transistor Transistor Logic
TXCLK	Transmission Clock
TXD	Transmission Data
TXEN	Transmission Enable
TXN	Transmission Negative
TXP	Transmission Positive

1.6 Conventions

1.6.1 Data Lengths

qword	64-bits
dword	32-bits
word	16-bits
byte	8 bits
nibble	4 bits

1.6.2 Pin Types

Pin Type	Description
I	Input
O	Output
I/O	Bi-directional
OD	Open drain
SCHE	Schmitt Trigger
PD	internal pull-down
PU	internal pull-up

1.6.2 Register Types

Register Type	Description
RO	Read-only
WO	Write-only
RW	Read/Write

Chapter 2 Interface Description

2.1 Pin Diagram

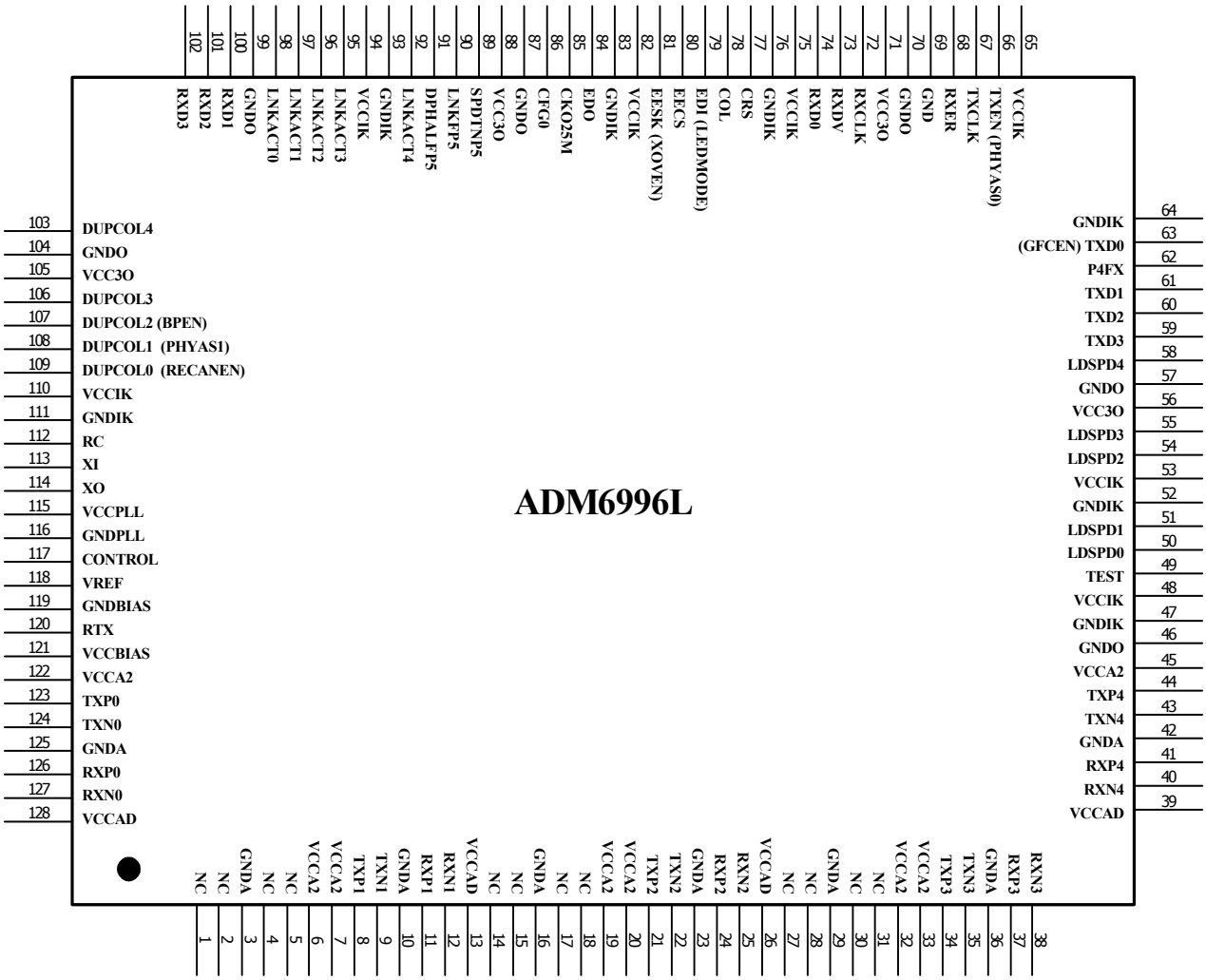

Figure 2-1 5 TP/FX PORT + 1 MII PORT 128 Pin Diagram

2.2 Pin Description by Function

ADM6996L pins are categorized into one of the following groups:

- Section 2.2.1 Twisted Pair Interface
- Section 2.2.2 6th Port (MII) Interfaces
- Section 2.2.3 LED Interface
- Section 2.2.4 EEPROM/Management Interface
- Section 2.2.5 Power/Ground, 48 pins
- Section 2.2.6 MISC

Note:
"Section 1.6.2 Pin Types" can be used for reference.

2.2.1 Twisted Pair Interface

Pin Name	Pin#	Type	Descriptions
RXP[0:4]	126, 11, 24, 37, 41	I/O, Analog	Twisted Pair Receive Input Positive.
RXN[0:4]	127, 12, 25, 38, 40	I/O, Analog	Twisted Pair Receive Input Negative.
TXP[0:4]	123, 8, 21, 34, 44	I/O, Analog	Twisted Pair Transmit Output Positive.
TXN[0:4]	124, 9, 22, 35, 43	I/O, Analog	Twisted Pair Transmit Output Negative.

2.2.2 6th Port (MII) Interfaces

Pin Name	Pin#	Type	Descriptions
TXD[0] Setting GFCEN	63	I/O, 8mA PU	MII transmit data 0 /GPSI TXD Acts as MII transmit data TXD[0]. Synchronous to the rising edge of TXCLK. Setting GFCEN: Global Flow Control Enable. At power-on-reset, latched as Full Duplex Flow control setting "1" to enable flow-control (default), "0" to disable flow-control.
TXD[1] Setting P5GPSI	61	I/O, 8mA PD	MII Transmit Data bit 1 Synchronous to the rising edge of TXCLK. These pins act as MII TXD[1]. Setting P5GPSI: Port 5 GPSI Enable. At power-on-reset, latched as P5 GPSI Enable. "0" to disable port 5 GPSI (default), "1" to enable port 5 GPSI.
TXD[3:2]	59, 60	I/O,	MII Transmit Data bit 3~2

Pin Name	Pin#	Type	Descriptions
		8mA PD	Synchronous to the rising edge of TXCLK. These pins act as MII TXD[3:2].
P4FX	62	I PD	Port4 FX/TX mode select. Internal pull down. 1: Port4 as FX port. 0: Port4 as TX port.
XEN Setting PHYAS0	66	I/O 8mA PD	MII Transmit Enable/GPSI TXEN. Internal pull down. Setting PHYAS0: Chip physical address for multiple chip application on read EEPROM data. Internal pull down. Power on reset value PHYAS0 combines with PHYAS1 PHYAS1 PHYAS0 0 0 Master(93C46) If there is no EEPROM then user must use 93C66 timing to write chip's register. If user put 93C46 with correct Signature then user writes chip register by 93C46 timing. If user put 93C66 then data put in Bank0. User can write chip register by 93C66 timing. User must assert one SK cycle when CS at idle stage when write chip internal register.
RXD[0]	74	I PD	MII port receive data 0 /GPSI RXD These pins act as MII RXD[0]. Synchronous to the rising edge of RXCLK. Internal pull down.
RXD[3:1]	102, 101, 100	I PD	MII port receive data 3~1 These pins act as MII RXD[3:1]. Synchronous to the rising edge of RXCLK. Internal pull down.
RXDV	73	I PD	MII receive data valid. Internal pull down.
RXER	68	I PD	MII Port Receive Error. Internal pull down.
COL	78	I PD	MII Port Collision input /GPSI Collision Input Internal pull down.
CRS	77	I PD	MII Port Carrier Sense /GPSI Carrier Sense Internal pull down.
RXCLK	72	I PD	MII Port Receive Clock Input /GPSI RXCLK
TXCLK	67	I PD	MII Port Transmit clock Input /GPSI TXCLK
DHALFP5	91	I PD	MII Port Hardware Duplex input pin. Low: Full Duplex. High: Half Duplex. Internal pull down.
LNKFP5	90	I PD	MII Port Hardware Link input pin. Low: Link OK. High: Link Off. Internal pull down.
SPDTNP5	89	I PD	MII Port Hardware Speed input pin. Low: 100M. High: 10M. Internal pull down.

2.2.3 LED Interface

Pin Name	Pin#	Type	Descriptions
LNKACT[4:0]	92, 95, 96, 97, 98	O, 8mA	**LINK/Activity LED[4:0].** Active low "1" indicates no link activity on cable "0" indicates link okay on cable, but no activity and signals on idle stage. "Blinking" indicates link activity on cable.
DUPCOL[4:3]	103, 106	O, 8mA	**Duplex/Collision LED[4:3].** Active low "1" for half-duplex and "blinking" for collision indication "0" for full-duplex indication
DUPCOL2 **Setting** BPEN	107	O, 8mA, PU	**Duplex/Collision LED2.** Active low "1" for half-duplex and "blinking" for collision indication "0" for full-duplex indication **Setting** BPEN: At power-on-reset, latched as Back Pressure setting "1" to enable Back-Pressure (defaulted), "0" to disable Back Pressure. At power-on-reset, latched as Back Pressure setting "1" to enable Back-Pressure (defaulted), "0" to disable Back Pressure.
DUPCOL1 **Setting** PHYAS1	108	O, 8mA, PD	**Duplex/Collision LED1.** Active low "1" for half-duplex and "blinking" for collision indication "0" for full-duplex indication **Setting** PHYAS1: Power on Reset latch value combine with TXEN. Internal pull down. Check pin 66.
DUPCOL0 **Setting** ANEN	109	O, 8mA, PU	**Duplex/Collision LED0.** Active low "1" for half-duplex and "blinking" for collision indication "0" for full-duplex indication **Setting** ANEN: On power-on-reset, latched as Auto Negotiation capability for all ports. "1" to enable Auto Negotiation (defaulted by pulled up internally), "0" to disable Auto Negotiation.
LDSPD[4:0]	58, 55, 54, 51, 50	O, 8mA	**Speed LED[4:0].** Used to indicate corresponding port's speed status. "0" for 100Mb/s, "1" for 10Mb/s

2.2.4 EEPROM/Management Interface

Pin Name	Pin#	Type	Descriptions
EDO	84	I, TTL,PU	**EEPROM Data Output.** Serial data input from EEPROM. This pin is internally pull-up.
EECS	80	O, 4mA,PD	**EEPROM Chip Select.** This pin is active high chip enable for EEPROM. When RESETL is low, it will be Tri-state. Internally Pull-down
EECK **Setting** XOVEN	81	I/O, 4mA PD	**Serial Clock**. This pin is clock source for EEPROM. When RESETL is low, it will be tri-state. **Setting** XOVEN: This pin is internal pull-down. On power-on-reset, latched as P4~0 Auto MDIX enable or not. "0" to disable MDIX (defaulted), "1" to enable MDIX. Suggest externally pull up to enable MDIX for all ports.
EDI **Setting** LEDMODE	79	I/O, 4mA PD	**EEPROM Serial Data Input.** This pin is output for serial data transfer. When RESETL is low, it will be tri-state. **Setting** LEDMODE: This pin is internal pull-down. On power-on-reset, latched as Dual Color mode or not. "0" to set Single color mode for LED. "1" to set Dual Color mode for LED.

2.2.5 Power/Ground, 48 pins

Pin Name	Pin#	Type	Descriptions
GNDA	3, 10, 16, 23, 29, 36, 42, 125	I	Ground Used by AD Block.
VCCA2	6, 7, 19, 20, 32, 33, 45, 122	I	1.8V, Power Used by TX Line Driver.
VCCAD	13, 26, 39, 128	I	3.3V, Power Used by AD Block.
GNDBIAS	119	I	Ground Used by Bias Block
VCCBIAS	121	I	3.3V, Power Used by Bias Block.
GNDPLL	116	I	Ground used by PLL
VCCPLL	115	I	1.8V, Power used by PLL
GNDIK	47, 52, 64, 76, 93, 83, 111	I	Ground Used by Digital Core
VCCIK	48, 53, 65, 75, 82, 94, 110	I	1.8V, Power Used by Digital Core
GNDO	46, 57, 70, 87, 99, 104	I	Ground Used by Digital Pad
VCC3O	56, 71, 88, 105	I	3.3V, Power Used by Digital Pad.
GND	69	I	Ground Used by Digital Pad.

2.2.6 MISC

Pin Name	Pin#	Type	Descriptions
CKO25M	85	O, 8mA	**25M Clock Output.**
Control	117	O	FET Control Signal. The pin is used to control FET for 3.3V to 1.8V regulator.
RTX	120	Analog	**TX Resistor.** Add 1.1K %1 resister to GND.
VREF	118	Analog	**Analog Reference Voltage.**
RC	112	I, SCHE	**RC Input for Power On reset.** Reset input pin.
XI	113	I, Analog	**25M Crystal Input.** 25M Crystal Input. Variation is limited to +/- 50ppm.
XO	114	O, Analog	**25M Crystal Output.** When connected to oscillator, this pin should left unconnected.
CFG0	86	I, TTL	Must Connected to GND.
TEST	49	I, TTL	**TEST Value.** At normal application connect to GND.
NC	1, 2, 4,5, 14, 15,17, 18, 27,28,		NC

Chapter 3 Function Description

3.1 Functional Descriptions

The ADM6996L integrates five 100Base-X physical sub-layer (PHY), 100Base-TX physical medium dependent (PMD) transceivers, five complete 10Base-T modules, 6 port 10/100 switch controller and one 10/100 MII/GPSI MAC and memory into a single chip for both 10Mbits/s, 100Mbits/s Ethernet switch operation. It also supports 100Base-FX operation through external fiber-optic transceivers. The device is capable of operating in either Full Duplex mode or Half-Duplex mode in 10Mbits/s and 100Mbits/s. Operational modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip auto negotiation logic.

The ADM6996L consists of three major blocks:

- 10/100M PHY Block
- Switch Controller Block
- Built-in SSRAM

The interfaces used for communication between PHY block and switch core is MII interface.

Auto MDIX function is supported in this block. This function can be Enable/Disable by hardware pin.

3.2 10/100M PHY Block

The 100Base-X section of the device implements the following functional blocks:

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- Twisted-pair transceiver (PMD)
- The 100Base-X and 10Base-T sections share the following functional blocks.
- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

3.3 100Base-X Module

The ADM6996L implements 100Base-X compliant PCS and PMA and 100Base-TX compliant TP-PMD as illustrated in Figure 2. Bypass options for each of the major functional blocks within the 100Base-X PCS provides flexibility for various applications. 100Mbits/s PHY loop back is included for diagnostic purpose.

3.4 100Base-X Receiver

The 100Base-X receiver consists of functional blocks required to recover and condition the 125Mbits/s receive data stream. The ADM6996L implements the 100Base-X receiving state machine diagram as given in ANSI/IEEE Standard 802.3u, Clause 24. The 125Mbits/s receive data stream may originate from the on-chip twisted-pair transceiver in a 100Base-TX application. Alternatively, the receive data stream may be generated by an external optical receiver as in a 100Base-FX application.

The receiver block consists of the following functional sub-blocks:

- A/D Converter
- Adaptive Equalizer and timing recovery module
- NRZI/NRZ and serial/parallel decoder
- De-scrambler
- Symbol alignment block
- Symbol Decoder
- Collision Detect Block
- Carrier sense Block
- Stream decoder block

3.4.1 A/D Converter

High performance A/D converter with 125Mhz sampling rate converts signals received on RXP/RXN pins to 6 bits data streams; besides it possess auto-gain-control capability that will further improve receive performance especially under long cable or harsh detrimental signal integrity. Due to high pass characteristic on transformer, built in base-line-wander correcting circuit will cancel it out and restore its DC level.

3.4.2 Adaptive Equalizer and timing Recovery Module

All digital design is especial immune from noise environments and achieves better correlation between production and system testing. Baud rate Adaptive Equalizer/Timing Recovery compensates line loss induced from twisted pair and tracks far end clock at 125M samples per second. Adaptive Equalizer implemented with Feed forward and Decision Feedback techniques meet the requirement of BER less than 10-12 for transmission on CAT5 twisted pair cable ranging from 0 to 120 meters.

3.4.3 NRZI/NRZ and Serial/Parallel Decoder

The recovered data is converted from NRZI to NRZ. The data is not necessarily aligned to 4B/5B code group’s boundary.

3.4.4 Data De-scrambling

The de-scrambler acquires synchronization with the data stream by recognizing idle bursts of 40 or more bits and locking its deciphering Linear Feedback Shift Register (LFSR) to the state of the scrambling LFSR. Upon achieving synchronization, the incoming data is XORed by the deciphering LFSR and de-scrambled.

In order to maintain synchronization, the de-scrambler continuously monitors the validity of the unscrambled data that it generates. To ensure this, a link state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the de-scrambler the hold timer starts a 722 us countdown. Upon detection of sufficient idle symbols within the 722 us period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given a properly operating network connection with good signal integrity. If the link state monitor does not recognize sufficient unscrambled idle symbols within 722 us period, the de-scrambler will be forced out of the current state of synchronization and reset in order to re-acquire synchronization.

3.4.5 Symbol Alignment

The symbol alignment circuit in the ADM6996L determines code word alignment by recognizing the /J/K delimiter pair. This circuit operates on unaligned data from the de-scrambler. Once the /J/K symbol pair (11000 10001) is detected, subsequent data is aligned on a fixed boundary.

3.4.6 Symbol Decoding

The symbol decoder functions as a look-up table that translates incoming 5B symbols into 4B nibbles as shown in Table 1. The symbol decoder first detects the /J/K symbol pair preceded by idle symbols and replaces the symbol with MAC preamble. All subsequent 5B symbols are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the /T/R symbol pair denoting the end of stream delimiter (ESD). The translated data is presented on the internal RXD[3:0] signal lines with RXD[0] represents the least significant bit of the translated nibble.

3.4.7 Valid Data Signal

The valid data signal (RXDV) indicates that recovered and decoded nibbles are being presented on the internal RXD[3:0] synchronous to receive clock, RXCLK. RXDV is asserted when the first nibble of translated /J/K is ready for transfer over the internal MII. It remains active until either the /T/R delimiter is recognized, link test indicates failure, or no signal is detected. On any of these conditions, RXDV is de-asserted.

3.4.8 Receive Errors

The RXER signal is used to communicate receiver error conditions. While the receiver is in a state of holding RXDV asserted, the RXER will be asserted for each code word that does not map to a valid code-group.

3.4.9 100Base-X Link Monitor

The 100Base-X link monitor function allows the receiver to ensure that reliable data is being received. Without reliable data reception, the link monitor will halt both transmit and receive operations until such time that a valid link is detected.

The ADM6996L performs the link integrity test as outlined in IEEE 100Base-X (Clause 24) link monitor state diagram. The link status is multiplexed with 10Mbits/s link status to form the reportable link status bit in serial management register 1h, and driven to the LNKACT pin.

When persistent signal energy is detected on the network, the logic moves into a Link-Ready state after approximately 500 us, and waits for an enable from the auto negotiation module. When receive, the link-up state is entered, and the transmission and reception logic blocks become active. Should auto negotiation be disabled, the link integrity logic moves immediately to the link-up state after entering the link-ready state.

3.4.10 Carrier Sense

Carrier sense (CRS) for 100Mbits/s operation is asserted upon the detection of two noncontiguous zeros occurring within any 10-bit boundary of the received data stream.

The carrier sense function is independent of symbol alignment. In switch mode, CRS is asserted during either packet transmission or reception. For repeater mode, CRS is asserted only during packet reception. When the idle symbol pair is detected in the received data stream, CRS is de-asserted. In repeater mode, CRS is only asserted due to receive activity. CRS is intended to encapsulate RXDV.

3.4.11 Bad SSD Detection

A bad start of stream delimiter (Bad SSD) is an error condition that occurs in the 100Base-X receiver if carrier is detected (CRS asserted) and a valid /J/K set of code-group (SSD) is not received.

If this condition is detected, then the ADM6996L will assert RXER and present RXD[3:0] = 1110 to the internal MII for the cycles hat correspond to received 5B code-groups until at least two idle code-groups are detected. Once at least two idle code groups are detected, RXER and CRS become de-asserted.

3.4.12 Far-End Fault

Auto negotiation provides a mechanism for transferring information from the Local Station to the link Partner that a remote fault has occurred for 100Base-TX. As auto negotiation is not currently specified for operation over fiber, the far end fault indication function (FEFI) provides this capability for 100Base-FX applications.

A remote fault is an error in the link that one station can detect while the other cannot. An example of this is a disconnected wire at a station's transmitter. This station will be receiving valid data and detect that the link is good via the link integrity monitor, but will not be able to detect that its transmission is not propagating to the other station.

A 100Base-FX station that detects such a remote fault may modify its transmitted idle stream from all ones to a group of 84 ones followed by a single 0. This is referred to as the FEFI idle pattern.

3.5 100Base-TX Transceiver

ADM6996L implements a TP-PMD compliant transceiver for 100Base-TX operation. The differential transmit driver is shared by the 10Base-T and 100Base-TX subsystems. This arrangement results in one device that uses the same external magnetic for both the 10Base-T and the 100Base-TX transmission with simple RC component connections. The individually wave-shaped 10Base-T and 100Base-TX transmit signals are multiplexed in the transmission output driver selection.

3.5.1 Transmit Drivers

The ADM6996L 100Base-TX transmission driver implements MLT-3 translation and wave-shaping functions. The rise/fall time of the output signal is closely controlled to conform to the target range specified in the ANSI TP-PMD standard.

3.5.2 Twisted-Pair Receiver

For 100Base-TX operation, the incoming signal is detected by the on-chip twisted-pair receiver that consists of a differential line receiver, an adaptive equalizer and a base-line wander compensation circuits.

The ADM6996L uses an adaptive equalizer that changes filter frequency response in accordance with cable length. The cable length is estimated based on the incoming signal strength. The equalizer tunes itself automatically for any cable length to compensate for the amplitude and phase distortions incurred from the cable.

3.6 10Base-T Module

The 10Base-T Transceiver Module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loop back, jabber, wave shaper, and link integrity

functions, as defined in the standard. Figure 3 provides an overview for the 10Base-T module.

The ADM6996L 10Base-T module is comprised of the following functional blocks:

- Manchester encoder and decoder
- Collision detector
- Link test function
- Transmit driver and receiver
- Serial and parallel interface
- Jabber and SQE test functions
- Polarity detection and correction

3.6.1 Operation Modes

The ADM6996L 10Base-T module is capable of operating in either half-duplex mode or full-duplex mode. In half-duplex mode, the ADM6996L functions as an IEEE 802.3 compliant transceiver with fully integrated filtering. The COL signal is asserted during collisions or jabber events, and the CRS signal is asserted during transmit and receive. In full duplex mode the ADM6996L can simultaneously transmit and receive data.

3.6.2 Manchester Encoder/Decoder

Data encoding and transmission begins when the transmission enable input (TXEN) goes high and continues as long as the transceiver is in good link state. Transmission ends when the transmission enable input goes low. The last transition occurs at the center of the bit cell if the last bit is a 1, or at the boundary of the bit cell if the last bit is 0.

Decoding is accomplished by a differential input receiver circuit and a phase-locked loop that separate the Manchester-encoded data stream into clock signals and NRZ data. The decoder detects the end of a frame when no more mid bit transitions are detected. Within one and half bit times after the last bit, carrier sense is de-asserted.

3.6.3 Transmit Driver and Receiver

The ADM6996L integrates all the required signal conditioning functions in its 10Base-T block such that external filters are not required. Only one isolation transformer and impedance matching resistors are needed for the 10Base-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmission signal are attenuated properly.

3.6.4 Smart Squelch

The smart squelch circuit is responsible for determining when valid data is present on the differential receive. The ADM6996L implements an intelligent receive squelch on the RXP/RXN differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. The squelch circuitry employs a combination of amplitude

and timing measurements (as specified in the IEEE 802.3 10Base-T standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of the packet is checked by the analog squelch circuit and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150ns. Finally, the signal must exceed the original squelch level within an additional 150ns to ensure that the input waveform will not be rejected.

Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present.

Valid data is considered to be present until the squelch level has not been generated for a time longer than 200 ns, indicating end of packet. Once good data has been detected, the squelch levels are reduced to minimize the effect of noise, causing premature end-of-packet detection. The receive squelch threshold level can be lowered for use in longer cable applications. This is achieved by setting bit 10 of register address 11h.

3.7 Carrier Sense

Carrier Sense (CRS) is asserted due to receive activity once valid data is detected via the smart squelch function. For 10 Mbits/s half duplex operation, CRS is asserted during either packet transmission or reception. For 10 Mbits/s full duplex and repeater mode operations, the CRS is asserted only due to receive activity.

3.8 Jabber Function

The jabber function monitors the ADM6996L output and disables the transmitter if it attempts to transmit a longer than legal sized packet. If TXEN is high for greater than 24ms, the 10Base-T transmitter will be disabled. Once disabled by the jabber function, the transmitter stays disabled for the entire time that the TXEN signal is asserted. This signal has to be de-asserted for approximately 256 ms (The un-jab time) before the jabber function re-enables the transmit outputs. The jabber function can be disabled by programming bit 4 of register address 10h to high.

3.9 Link Test Function

A link pulse is used to check he integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10Base-T twisted-pair transmitter, receiver, and collision detection functions.
The link pulse generator produces pulses as defined in IEEE 802.3 10Base-T standard. Each link pulse is nominally 100ns in duration and is transmitted every 16 ms, in the absence of transmit data.

3.10 Automatic Link Polarity Detection

ADM6996L's 10Base-T transceiver module incorporates an "automatic link polarity detection circuit". The inverted polarity is determined when seven consecutive link pulses of inverted polarity or three consecutive packets are received with inverted end-of-packet pulses. If the input polarity is reversed, the error condition will be automatically corrected and reported in bit 5 of register 10h.

3.11 Clock Synthesizer

The ADM6996L implements a clock synthesizer that generates all the reference clocks needed from a single external frequency source. The clock source must be a TTL level signal at 25 MHz +/- 50ppm

3.12 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further detail regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The ADM6996L supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

Highest priority relative to the following list:

- 100Base-TX full duplex (highest priority)
- 100Base-TX half duplex
- 10Base-T full duplex
- 10Base-T half duplex (lowest priority)

3.13 Memory Block

ADM6996L build in memory is divided as two blocks. One is MAC addressing table and another one is data buffer.

MAC address Learning Table size is 2048 entry with each entry occupy eight bytes length. These eight bytes data include 6 bytes source address, VLAN information, Port information and Aging counter.

Data buffer is divided to 256 bytes/block. ADM6996L buffer management is per port fixed block number and all port share one global buffer. This architecture can get better memory utilization and network balance on different speed and duplex test condition.

Received packet will separate as several 256 bytes/block and chain together. If packet size more than 256 bytes then ADM6996L will chain two or more block to store receiving packet.

3.14 Switch Functional Description

The ADM6996L uses a “store & forward” switching approach for the following reason: Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require the large elastic buffer especially bridging between a server on a 100Mbps network and clients on a 10Mbps segment.

Store & forward switches improve overall network performance by acting as a “network cache”

Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port.

3.15 Basic Operation

The ADM6996L receives incoming packets from one of its ports, searches in the Address Table for the Destination MAC Address and then forwards the packet to the other port within same VLAN group, if appropriate. If the destination address is not found in the address table, the ADM6996L treats the packet as a broadcast packet and forwards the packet to the other ports which in same VLAN group.

The ADM6996L automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming packets at wire speed. If the Source Address is not found in the Address Table, the device adds it to the table.

3.15.1 Address Learning

The ADM6996L uses a hash algorithm to learn the MAC address and can learn up to 2K MAC addresses. Address is stored in the Address Table. The ADM6996L searches for the Source Address (SA) of an incoming packet in the Address Table and acts as below:

If the SA was not found in the Address Table (a new address), the ADM6996L waits until the end of the packet (non-error packet) and updates the Address Table. If the SA was found in the Address Table, then aging value of each corresponding entry will be reset to 0.

When the DA is PAUSE command, then the learning process will be disabled automatically by ADM6996L.