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Data Sheet, Rev. 1.42, Nov. 2005

ADM6999U/UX

9 port 10/100 Mb/s Single Chip Ethernet Switch Controller

Communications

Never stop thinking.

Edition 2005-11-25

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2002-08	Rev. 0.1: First Infineon ADMtek Co Ltd version
2002-09	Rev. 1.0: Remove Preliminary word
2002-12	Rev. 1.1: Modify error word. Add Expansion Port Timing.
2003-04	Rev. 1.2: Modify expansion Port Setup/Hold time. Remove LEDEN pin to NC.
2003-05	Rev. 1.3: A2 version RTX value change to 1K 1%
2004-04	Rev. 1.4: Updated logo to Infineon ADMtek
2005-09	Rev. 1.41: Changed to the new Infineon format
2005-11-25	Rev. 1.41 changed to Rev. 1.42 Minor change. Included Green package information

Trademarks

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1 Introduction

1.1 General Description

The ADM6999U/UX is a high performance, low cost, and highly integration (Controller, PHY and Memory) eight-port 10/100 Mbps TX/FX plus one 1.6G Expansion port Ethernet switch controller with all ports supporting 10/100 Mbps Full/Half duplex switch function. The ADM6999U/UX is intended for applications to stand alone the bridge for low cost 16 Port Switch. The ADM6999UX is the environmentally friendly “green” package version.

ADM6999U/UX provides most advanced functions such as: **802.1p (Q.O.S.ADM6999U/UX), 802.1q (VLAN), Port MAC Address Locking, Management, Port Status, TP Auto-MDIX, 25M Crystal & Extra ninth Port (RMII/MII/GPSI)** functions to meet the customer’s requests on Switch demand.

The built-in 768K SRAM used for the packet buffer and address learning table is divided into 512 bytes/block to achieve the optimized memory utilization through complicated link list on packets with various lengths.

ADM6999U/UX also supports priority features by Port-Base, VLAN and IP TOS field checking. Users can easily set as different priority mode in individual port, through a small low-cost micro controller to initialize or on-the-fly to configure. Each output port supports two queues in the way of fixed N: 1 fairness queuing to fit the bandwidth demand on various types of packet such as Voice, Video and data. 802.1Q, Tag/Untag, and up to 32 groups of VLAN are also supported. ADM6999U/UX learns user define 4 or 5 bits of VLAN ID.

An intelligent address recognition algorithm makes ADM6999U/UX to recognize up to 2048 different MAC addresses and enables filtering and forwarding at full wire speed.

Port MAC address Locking function is also supported by ADM6999U/UX to use on Building Internet access to prevent multiple users share one port traffic.

1.2 Features

Main features:

- Supports eight 10M/100M auto-detect Half/Full duplex switch ports with TX/FX interfaces and one 1.6G Expansion Port.
- Built-in 12Kx64 SRAM.
- Supports 2048 MAC addresses table.
- Supports two queue for Qos.
- Supports priority features by Port-Based, 802.1p VLAN & IP TOS of packets.
- Supports Store & Forward architecture and perform forwarding and filtering at non-blocking full wire speed.
- Supports buffer allocation with 512 bytes per block.
- Supports Aging function Enable/Disable.
- Supports Serial & Scan LED mode with Power On auto diagnostic.
- Supports 802.3x Flow Control pause packet for Full Duplex in case buffer is full.
- Supports Back Pressure function for Half Duplex operation in case buffer is full.
- Supports packet length up to 1522 bytes.
- Broadcast Storming Filter function.
- Supports 802.1Q VLAN. Up to 16/32 VLAN groups is implemented by user define four/five bits of VLAN ID.
- Supports MAC-clone feature.
- Supports TP interface Auto MDIX function for auto TX/RX swap by strapping-pin.
- Easy Management 32bits smart counter for per port RX/TX byte/packet count, error count and collision count.
- Supports PHY status output for management system.
- 25M Crystal only for the whole system.
- 128 QFP package with 0.18um technology. 1.8V/3.3V power supply.

1.3 Applications

ADM6999U/UX in 128-pin PQFP:

- 16-port switch

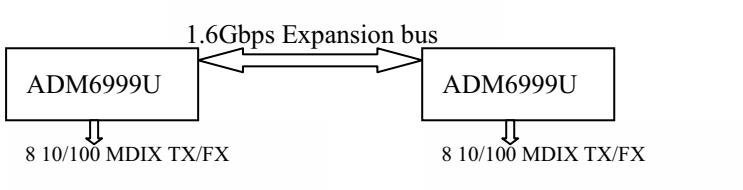

Figure 1 ADM6999U/UX's Application

2 Input and Output Signals

This chapter describes Pin Diagram and Pin Description.

2.1 Pin Diagram

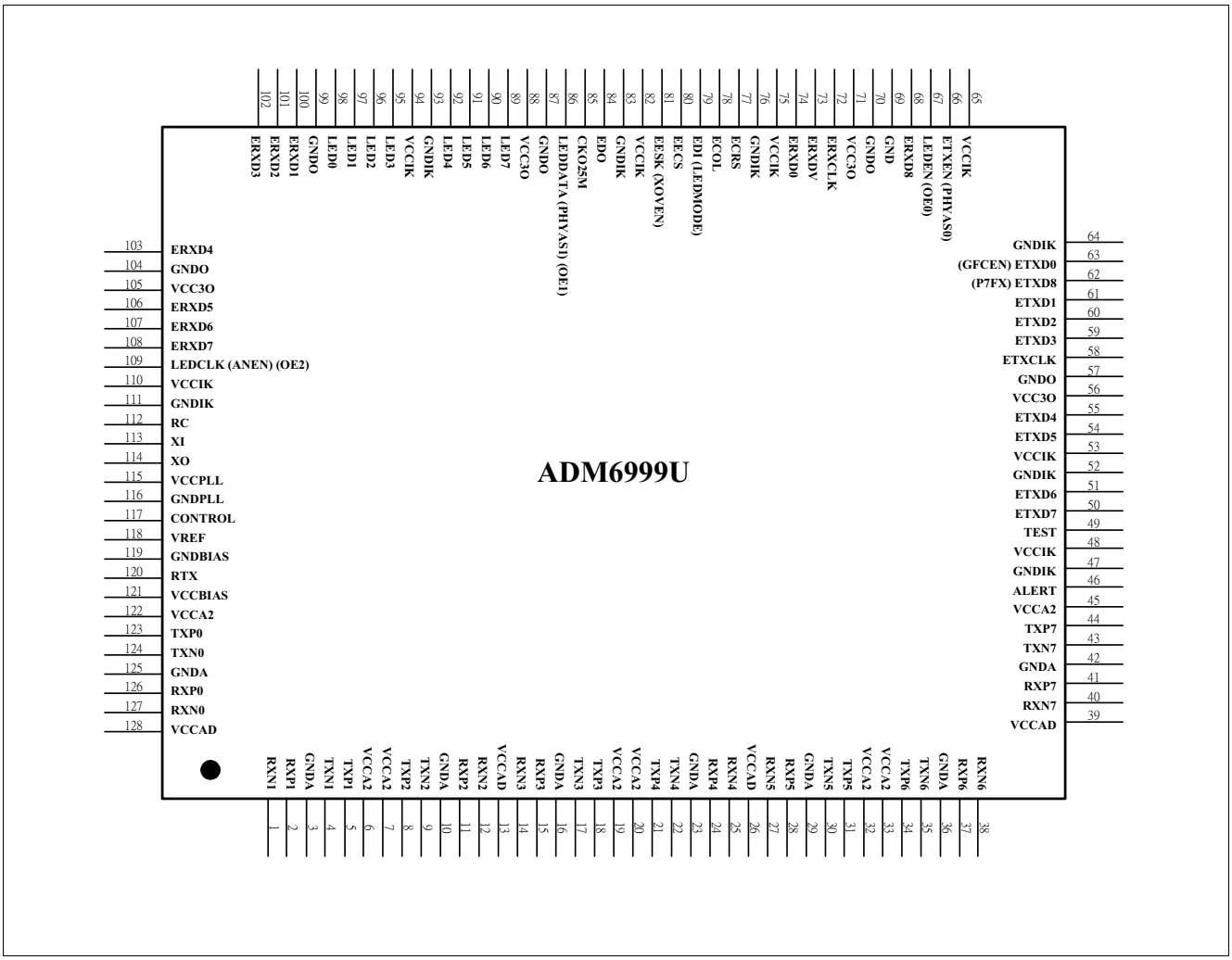

Figure 2 ADM6999U/UX 128 Pin Diagram

2.2 Pin Type and Buffer Type Abbreviations

Standardized abbreviations:

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU1	Pull up, 10 kΩ
PD1	Pull down, 10 kΩ
PD2	Pull down, 20 kΩ
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

2.3 Pin Description

Table 3 ADM6999U/UX 128 Pin Descriptions

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Twisted Pair Interface				
126	RXP0	AI/O		**Twisted Pair Receive Input Positive**
2	RXP1			
11	RXP2			
15	RXP3			
24	RXP4			
28	RXP5			
37	RXP6			
41	RXP7			
127	RXN0	AI/O		**Twisted Pair Receive Input Negative**
1	RXN1			
12	RXN2			
14	RXN3			
25	RXN4			
27	RXN5			
38	RXN6			
40	RXN7			
123	TXP0	AI/O		**Twisted Pair Transmit Output Positive**
5	TXP1			
8	TXP2			
18	TXP3			
21	TXP4			
31	TXP5			
34	TXP6			
44	TXP7			
124	TXN0	AI/O		**Twisted Pair Transmit Output Negative**
4	TXN1			
9	TXN2			
17	TXN3			
22	TXN4			
30	TXN5			
35	TXN6			
43	TXN7			
EBus Interfaces				

Table 3 ADM6999U/UX 128 Pin Descriptions

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
63	ETXD0	I/O	8mA, PU	**EBus Transmit Data 0** Acts as GMII transmit data TXD0. Synchronous to the rising edge of TXCLK. Internally Pull-up. User must add pull high 1K resister to 3.3V on 16 port application.
	GFCEN	I/O	8mA, PU	**Setting GFCEN:Global Flow Control Enable** At power-on-reset, latched as Full Duplex Flow control setting 0_B , Disable flow-control 1_B , Enable flow-control (default)
61	ETXD1	O	8mA	**EBus Transmit Data bit 7~** Synchronous to the rising edge of GTXCLK.
60	ETXD2			
59	ETXD3			
55	ETXD4			
54	ETXD5			
51	ETXD6			
50	ETXD7			
62	P7FX	I/O	8mA, PD	**Setting Port7 FX/TX Mode select** Internal pull down. 0_B , Port7 as TX port 1_B , Port7 as FX port
	ETXD8	I/O	8mA, PD	**EBus Transmit Data 8**
66	ETXEN	I/O	8mA, PD	**EBus Transmit Enable**
	PHYAS0	I/O	8mA, PD	**Setting PHAY0: Chip physical address 0 for multiple chip EEPROM access.** Internal pull down. Power on reset value PHYAS0 combines with PHYAS1(LEDDATA). PHYAD Gigabit PHY Address 00 08_H Master 01 09_H Slave0 1x 18_H Slave1(Not used) For two ADM6999U/UXs as 16port application : Master: ADM6999U/UX will read 93C46/66 EEPROM first Bank.(00_H~27_H). Slave0: ADM6999U/UX will read 93C66 EEPROM second Bank.(40_H~67_H). User must assert one SK cycle when CS is at idle stage and chip internal registers are being writing.

Table 3 ADM6999U/UX 128 Pin Descriptions

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
74	ERXD0	I	PD	**EBUS port receive data 8~0** Synchronous to the rising edge of RXCLK.
100	ERXD1			
101	ERXD2			
102	ERXD3			
103	ERXD4			
106	ERXD5			
107	ERXD6			
108	ERXD7			
68	ERXD8			
73	ERXDV	I	PD	**EBUS receive data valid** Internal pull down.
78	ECOL	I	PD	**EBUS Collision input** Internal pull down.
77	ECRS	I	PD	**EBUS Port Carrier Sense** Internal pull down.
58	ETXCLK	O	16mA	**EBUS 125MHz clock Output**
72	ERXCLK	I		**EBUS Receive Clock Input**
LED Interface, 11 pins				
67	Scan LED OE0	O	8mA	**Scan LED Mode** OE0: Scan LED Control for LINK LED
86	Serial LED LEDDATA	I/O	8mA	**Serial LED Mode** LEDDATA: Serial LED Data
	Scan LED OE1			**Scan LED Mode** OE1: Scan LED Control for Speed LED
	PHYAS1			**Setting PHYAS1: Chip physical address.** See pin 66 define.
109	Serial LED LEDCLK	I/O	8mA, PU	**Serial LED Mode** LEDCLK: Serial LED Clock
	Scan LED OE2			**Scan LED Mode** OE2: Scan LED Control for Duplex LED
	ANEN			**Setting ANEN: On power-on-reset, latched as Auto Negotiation capability for all ports.** 0_B , Disable Auto Negotiation. 1_B , Enable Auto Negotiation (defaulted by pulled up internally)

Table 3 ADM6999U/UX 128 Pin Descriptions

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
98	LED0	I		**Scan LED Data [7:0]**
97	LED1			
96	LED2			
95	LED3			
92	LED4			
91	LED5			
90	LED6			
89	LED7			
92	Dual Color	I		**Setting Dual Color: Serial LED mode only.** Single Color Dual Color Select 0_B , Single Color LED mode 1_B , Dual Color LED mode.
EEPROM/Management Interface				
84	EEDO	I	TTL, PU	**EEPROM Data Output** Serial data input from EEPROM. This pin is internally pull-up.
80	EECS	O	4mA, PD	**EEPROM Chip Select** This pin is active high chip enable for EEPROM. When RC is low, it will be Tristate. This pin is internally pull-down.
81	EECK	I/O	4mA, PD	**Serial Clock** This pin is clock source for EEPROM.
	XOVEN	I/O	4mA, PD	**Setting XOVEN: This pin is internally pull-down.** On power-on-reset, latched as P7~0 Auto MDIX enable or not. Suggest externally pull up to enable Auto MDIX for all ports. 0_B , to disable MDIX (defaulted) 1_B , to enable MDIX
79	EEDI	O	4mA, PD	**EEPROM Serial Data Input** This pin is output for serial data transfer.
	LEDMODE	O	4mA, PD	**Setting** LEDMODE: On power-on-reset, latched as Dual Color mode or not. This pin is internal pull-down. 0_B , to set Single color mode for LED 1_B , to set Dual Color mode for LED
Misc.				
85	CKO25M	O	8mA	**25M Clock Output**
117	Control	O		**FET Control Signal** The pin is used to control FET for 3.3 V to 1.8 V regulator. Add 0.01 µf capacitor to GND.
120	RTX	A		**TX Resistor** Add 1.1K %1(A1), 1K %1 (A2) resister to GND.
118	VREF	A		**Analog Reference Voltage**
112	RC	I	ST	**RC Input for Power On reset** Reset input pin

Table 3 ADM6999U/UX 128 Pin Descriptions

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
113	XI	AI		**25M Crystal Input** 25M Crystal Input. Variation is limited to +/- 50ppm.
114	XO	AO		**25M Crystal Output** When connected to oscillator, this pin should left unconnected.
49	TEST	I	TTL	**TEST Value** At normal application connect to GND.
Chip Configuration				
46	ALERT	O		**Alert LED Display** This pin will show the status of power-on-diagnostic and broadcast traffic.
Power/Ground				
3, 10, 16, 23, 29, 36, 42, 125	GNDA	I		**Ground Used by AD Block**
6, 7, 19, 20, 32, 33, 45, 122	VCCA2	I		**1.8 V, Power Used by TX Line Driver**
13, 26, 39, 128	VCCAD	I		**3.3 V, Power Used by AD Block**
119	GNDBIAS	I		**Ground Used by Bias Block**
121	VCCBIAS	I		**3.3 V, Power Used by Bias Block**
116	GNDPLL	I		**Ground used by PLL**
115	VCCPLL	I		**1.8 V, Power used by PLL**
47, 52, 64, 76, 83, 93, 111	GNDIK	I		**Ground Used by Digital Core**
48, 53, 65, 75, 82, 94, 110	VCCIK	I		**1.8 V, Power Used by Digital Core**
57, 70, 87, 99, 104	GNDO	I		**Ground Used by Digital Pad**
56, 71, 88, 105	VCC3O	I		**3.3 V, Power Used by Digital Pad**
69	GND	I	TTL	**Scan Enable** This pin will be used as the scan enable input for testing. Connect to GND at normal application.

3 Descriptions

This chapter provides Functional Description, 10/100M PHY Block Description, Memory Block Description, Switch Functional Description, EEPROM Content and EEPROM Access Description.

3.1 Functional Description

The ADM6999U/UX integrates eight 100Base-X physical sub-layer (PHY), 100Base-TX physical medium dependent (PMD) transceivers, eight complete 10Base-T modules, 8 port 100/10 switch controller, and one 1.6G Expansion Port and memory into a single chip for both 10Mbits/s, 100Mbits/s Ethernet switch operations. It also supports 100Base-FX operation through external fiber-optic transceivers. The device is capable of operating in either Full Duplex mode or Half-Duplex mode in 10Mbits/s and 100Mbits/s. Operational modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip auto negotiation logic.

The ADM6999U/UX consists of three major blocks:

- 10/100M PHY Block
- Switch Controller Block
- Built-in 12Kx64 SSRAM

3.2 10/100M PHY Block Description

The 100Base-X section of the device implements the following functional blocks:

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- Twisted-pair transceiver (PMD)

The 100Base-X and 10Base-T sections share the following functional blocks:

- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

3.2.1 100Base-X Module

The ADM6999U/UX implements 100Base-X compliant PCS, PMA and 100Base-TX compliant TP-PMD as illustrated in **Figure 3**. Bypass options for each of the major functional blocks within the 100Base-X PCS provide flexibility for various applications. 100Mbits/s PHY loop back is included for diagnostic purpose.

3.2.2 100Base-X Receiver

The 100Base-X receiver consists of functional blocks required to recover and condition the 125Mbits/s received data stream. The ADM6999U/UX implements the 100Base-X receiving state machine diagram as given in ANSI/IEEE Standard 802.3u, Clause 24. The 125Mbits/s received data stream may originate from the on-chip twisted-pair transceiver in a 100Base-TX application. Alternatively, the received data stream may be generated by an external optical receiver as in a 100Base-FX application.

The receiver block consists of the following functional sub-blocks:

- A/D Converter
- Adaptive Equalizer and timing recovery module
- NRZI/NRZ and serial/parallel decoder
- De-scrambler
- Symbol alignment block
- Symbol Decoder
- Collision Detect Block
- Carrier sense Block

- Stream decoder block

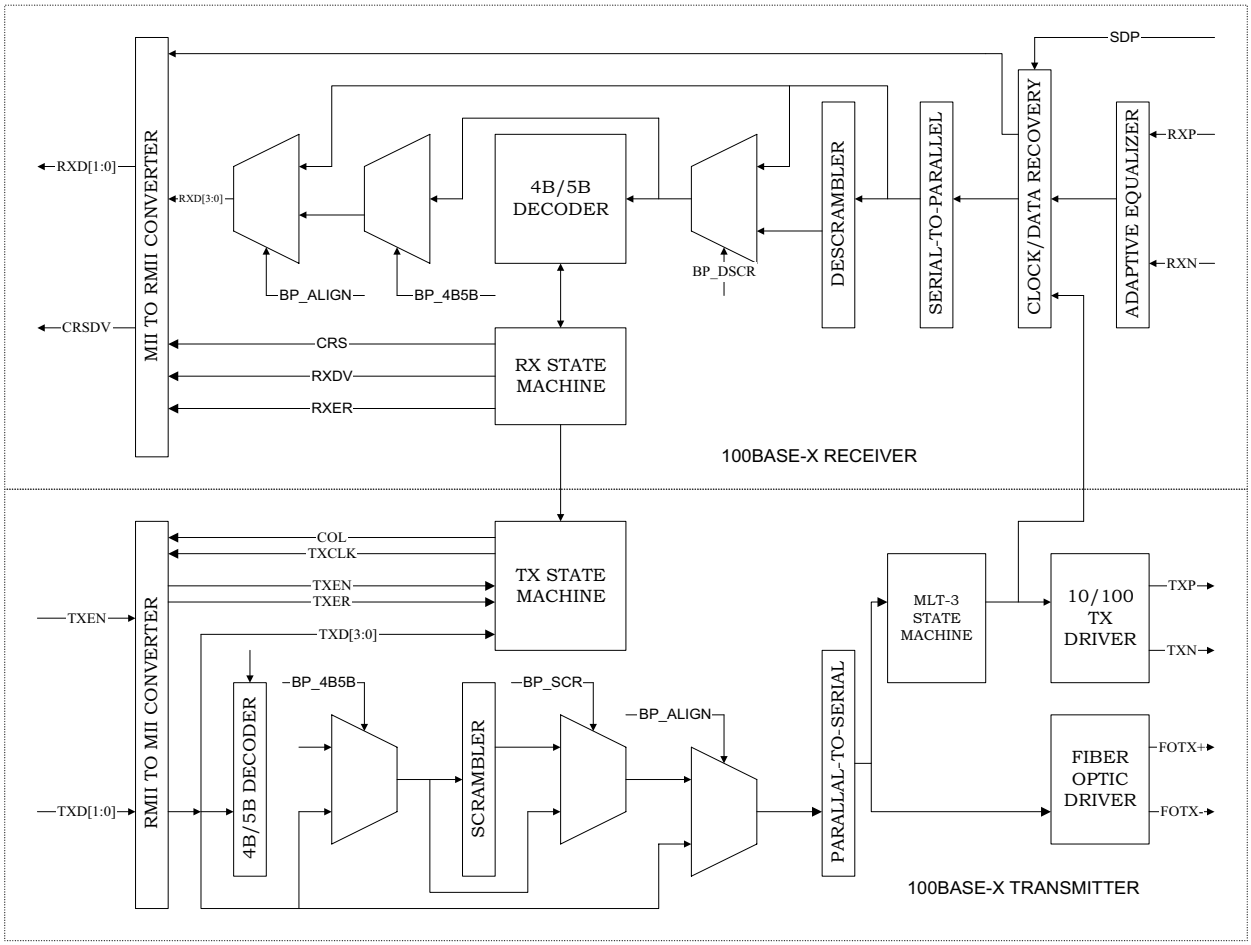

Figure 3 100Base-X Module

3.2.2.1 A/D Converter

High performance A/D converter with 125 MHz sampling rate converts signals received on RXP/RXN pins to 6 bits data streams; besides it possess auto-gain-control capability that will further improve receiving performance especially under long cable or harsh detrimental signal integrity. Due to high pass characteristic on transformer, built in base-line-wander correcting circuit will cancel it out and restore its DC level.

3.2.2.2 Adaptive Equalizer and Timing Recovery Module

All digital design is especial immune from noise environments and achieves better correlation between production and system testing. Baud rate Adaptive Equalizer/Timing Recovery compensates line loss induced from twisted pair and tracks far end clock at 125M samples per second. Adaptive Equalizer implemented with Feed forward and Decision Feedback techniques meet the requirement of BER less than 10-12 for transmission on CAT5 twisted pair cable ranging from 0 to 120 meters.

3.2.2.3 NRZI/NRZ and Serial/Parallel Decoder

The recovered data is converted from NRZI to NRZ. The data is not necessarily aligned to 4B/5B code group's boundary.

3.2.2.4 Data De-scrambling

The de-scrambler acquires synchronization with the data stream by recognizing idle bursts of 40 or more bits and locking its deciphering Linear Feedback Shift Register (LFSR) to the state of the scrambling LFSR. Upon achieving synchronization, the incoming data is XORed by the deciphering LFSR and de-scrambled.

In order to maintain synchronization, the de-scrambler continuously monitors the validity of the unscrambled data that it generates. To ensure this, a link state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the de-scrambler the hold timer starts a 722 us countdown. Upon detection of sufficient idle symbols within the 722 us period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given a properly operating network connection with good signal integrity. If the link state monitor does not recognize sufficient unscrambled idle symbols within 722 us period, the de-scrambler will be forced out of the current state of synchronization and reset in order to re-acquire synchronization.

3.2.2.5 Symbol Alignment

The symbol alignment circuit in the ADM6999U/UX determines code word alignment by recognizing the /J/K delimiter pair. This circuit operates on unaligned data from the de-scrambler. Once the /J/K symbol pair (11000 10001) is detected, subsequent data is aligned on a fixed boundary.

3.2.2.6 Symbol Decoding

The symbol decoder functions as a look-up table that translates incoming 5B symbols into 4B nibbles. The symbol decoder first detects the /J/K symbol pair preceded by idle symbols and replaces the symbol with MAC preamble. All subsequent 5B symbols are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the /T/R symbol pair denoting the end of stream delimiter (ESD). The translated data is presented on the internal RXD[3:0] signal lines with RXD[0] represents the least significant bit of the translated nibble.

3.2.2.7 Valid Data Signal

The valid data signal (RXDV) indicates that recovered and decoded nibbles are being presented on the internal RXD[3:0] synchronous to receive clock, RXCLK. RXDV is asserted when the first nibble of translated /J/K is ready for transfer over the internal MII. It remains active until either the /T/R delimiter is recognized, link test indicates failure, or no signal is detected. On any of these conditions, RXDV is de-asserted.

3.2.2.8 Receive Errors

The RXER signal is used to communicate receiver error conditions. While the receiver is in a state of holding RXDV asserted, the RXER will be asserted for each code word that does not map to a valid code-group.

3.2.2.9 100Base-X Link Monitor

The 100Base-X link monitor function allows the receiver to ensure that reliable data is being received. Without reliable data reception, the link monitor will halt both transmitting and receiving operations until such time that a valid link is detected.

The ADM6999U/UX performs the link integrity test as outlined in IEEE 100Base-X (Clause 24) link monitor state diagram. The link status is multiplexed with 10Mbits/s link status to form the reportable link status bit in serial management register 1_H, and driven to the LNKACT pin.

When persistent signal energy is detected on the network, the logic moves into a Link-Ready state after approximately 500 us, and waits for an enable from the auto negotiation module. When receiving, the link-up state is entered, and the transmission and reception logic blocks become active. Should auto negotiation be disabled, the link integrity logic moves immediately to the link-up state after entering the link-ready state.

3.2.2.10 Carrier Sense

Carrier sense (CRS) for 100Mbits/s operation is asserted upon the detection of two noncontiguous zeros occurring within any 10-bit boundary of the received data stream.

The carrier sense function is independent of symbol alignment. In switch mode, CRS is asserted during either packet transmission or reception. For repeater mode, CRS is asserted only during packet reception. When the idle symbol pair is detected in the received data stream, CRS is de-asserted. In repeater mode, CRS is only asserted due to receive activity. CRS is intended to encapsulate RXDV.

3.2.2.11 Bad SSD Detection

A bad start of stream delimiter (Bad SSD) is an error condition that occurs in the 100Base-X receiver if carrier is detected (CRS asserted) and a valid /J/K set of code-group (SSD) is not received.

If this condition is detected, then the ADM6999U/UX will assert RXER and present RXD[3:0] = 1110 to the internal MII for the cycles hat corresponding to the received 5B code-groups until at least two idle code-groups are detected. Once at least two idle code groups are detected, RXER and CRS become de-asserted.

3.2.2.12 Far-End Fault

Auto negotiation provides a mechanism for transferring information from the Local Station to the link Partner that a remote fault has occurred for 100Base-TX. As auto negotiation is not currently specified for operation over fiber, the far end fault indication function (FEFI) provides this capability for 100Base-FX applications.

A remote fault is an error in the link that one station can detect while the other cannot. An example of this is a disconnected wire at a station's transmitter. This station will be receiving valid data and detect that the link is good via the link integrity monitor, but will not be able to detect that its transmission is not propagating to the other station.

A 100Base-FX station that detects such a remote fault may modify its transmitted idle stream from all ones to a group of 84 ones followed by a single 0. This is referred to as the FEFI idle pattern.

3.2.3 100Base-TX Transceiver

ADM6999U/UX implements a TP-PMD compliant transceiver for 100Base-TX operation. The differential transmitting driver is shared by the 10Base-T and 100Base-TX subsystems. This arrangement results in one device that uses the same external magnetic for both the 10Base-T and the 100Base-TX transmission with simple RC component connections. The individually wave-shaped 10Base-T and 100Base-TX transmitting signals are multiplexed in the transmission output driver selection.

3.2.3.1 Transmit Drivers

The ADM6999U/UX 100Base-TX transmission driver implements MLT-3 translation and wave-shaping functions. The rise/fall time of the output signal is closely controlled to conform to the target range specified in the ANSI TP-PMD standard.

3.2.3.2 Twisted-Pair Receiver

For 100Base-TX operation, the incoming signal is detected by the on-chip twisted-pair receiver that consists of a differential line receiver, an adaptive equalizer and a base-line wander compensation circuits.

The ADM6999U/UX uses an adaptive equalizer that changes filter frequency response in accordance with cable length. The cable length is estimated based on the incoming signal strength. The equalizer tunes itself automatically for any cable length to compensate for the amplitude and phase distortions incurred from the cable.

3.2.4 10Base-T Module

The 10Base-T Transceiver Module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loop back, jabber, wave shaper, and link integrity functions, as defined in the standard.

The ADM6999U/UX 10Base-T module is comprised of the following functional blocks:

- Manchester encoder and decoder
- Collision detector
- Link test function
- Transmit driver and receiver
- Serial and parallel interface
- Jabber and SQE test functions
- Polarity detection and correction

3.2.4.1 Operation Modes

The ADM6999U/UX 10Base-T module is capable of operating in either half-duplex mode or full-duplex mode. In half-duplex mode, the ADM6999U/UX functions as an IEEE 802.3 compliant transceiver with fully integrated filtering. The COL signal is asserted during collisions or jabber events, and the CRS signal is asserted during transmitting and receiving. In full duplex mode the ADM6999U/UX can simultaneously transmit and receive data.

3.2.4.2 Manchester Encoder/Decoder

Data encoding and transmission begin when the transmission enable input (TXEN) goes high and continues as long as the transceiver is in good link state. Transmission ends when the transmission enable input goes low. The last transition occurs at the center of the bit cell if the last bit is a 1, or at the boundary of the bit cell if the last bit is 0.

Decoding is accomplished by a differential input receiver circuit and a phase-locked loop that separate the Manchester-encoded data stream into clock signals and NRZ data. The decoder detects the end of a frame when no more mid bit transitions are detected. Within one and half bit times after the last bit, carrier sense is de-asserted.

3.2.4.3 Transmit Driver and Receiver

The ADM6999U/UX integrates all the required signal conditioning functions in its 10Base-T block such that external filters are not required. Only one isolation transformer and impedance matching resistors are needed for the 10Base-T transmitting and receiving interface. The internal transmitting filtering ensures that all the harmonics in the transmission signal are attenuated properly.

3.2.4.4 Smart Squelch

The smart squelch circuit is responsible for determining when valid data is present on the differential receiption. The ADM6999U/UX implements an intelligent receiving squelch on the RXP/RXN differential inputs to ensure that impulse noise on the receiving inputs will not be mistaken for a valid signal. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10Base-T standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of the packet is checked by the analog squelch circuit and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150ns. Finally, the signal must exceed the original squelch level within an additional 150ns to ensure that the input waveform will not be rejected.

Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present.

Valid data is considered to be present until the squelch level has not been generated for a time longer than 200 ns, indicating end of packet. Once good data has been detected, the squelch levels are reduced to minimize the effect

of noise, causing premature end-of-packet detection. The receiving squelch threshold level can be lowered for use in longer cable applications. This is achieved by setting bit 10 of register address 11_H.

3.2.5 Carrier Sense

Carrier Sense (CRS) is asserted due to receive activity once valid data is detected via the smart squelch function. For 10 Mbits/s half duplex operation, CRS is asserted during either packet transmission or reception. For 10 Mbits/s full duplex and repeater mode operations, the CRS is asserted only due to receive activity.

3.2.6 Jabber Function

The jabber function monitors the ADM6999U/UX output and disables the transmitter if it attempts to transmit a longer than legal sized packet. If TXEN is high for greater than 24ms, the 10Base-T transmitter will be disabled. Once disabled by the jabber function, the transmitter stays disabled for the entire time that the TXEN signal is asserted. This signal has to be de-asserted for approximately 256 ms (The un-jab time) before the jabber function re-enables the transmit outputs. The jabber function can be disabled by programming bit 4 of register address 10_H to high.

3.2.7 Link Test Function

A link pulse is used to check the integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10Base-T twisted-pair transmitter, receiver, and collision detection functions.

The link pulse generator produces pulses as defined in IEEE 802.3 10Base-T standard. Each link pulse is nominally 100ns in duration and is transmitted every 16 ms, in the absence of transmitting data.

3.2.8 Automatic Link Polarity Detection

ADM6999U/UX's 10Base-T transceiver module incorporates an "automatic link polarity detection circuit". The inverted polarity is determined when seven consecutive link pulses of inverted polarity or three consecutive packets are received with inverted end-of-packet pulses. If the input polarity is reversed, the error condition will be automatically corrected and reported in bit 5 of register 10_H.

3.2.9 Clock Synthesizer

The ADM6999U/UX implements a clock synthesizer that generates all the reference clocks needed from a single external frequency source. The clock source must be a TTL level signal at 25 MHz +/- 50ppm

3.2.10 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operations supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further detail regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The ADM6999U/UX supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

Highest priority relative to the following list:

1. 100Base-TX full duplex (highest priority)
2. 100Base-TX half duplex
3. 10Base-T full duplex
4. 10Base-T half duplex (lowest priority)

3.3 Memory Block Description

ADM6999U/UX builds in 768K bits memory inside. Memory buffer is divided as two blocks. One is MAC addressing table and another one is data buffer.

MAC address Learning Table size is 2048 entries with each entry occupying eight bytes length. These eight bytes data include 6 bytes source address, VLAN information, Port information and Aging counter.

Data buffer is divided into 512 bytes/block. ADM6999U/UX buffer management is per port fixed block number and all port share one global buffer. This architecture can get better memory utilization and network balance on different speed and duplex test conditions.

Received packet will separate as several 512 bytes/block and chain together. If packet size more than 512 bytes then ADM6999U/UX will chain two or more blocks to store receiving packet.

3.4 Switch Functional Description

The ADM6999U/UX uses a “store & forward” switching approach for the following reason:

Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require the large elastic buffer especially bridging between a server on a 100Mbps network and clients on a 10Mbps segment.

Store & forward switches improve overall network performance by acting as a “network cache”

Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port.

3.4.1 Basic Operation

The ADM6999U/UX receives incoming packets from one of its ports, searches in the Address Table for the Destination MAC Address and then forwards the packet to the other port within the same VLAN group, if appropriate. If the destination address is not found in the address table, the ADM6999U/UX treats the packet as a broadcast packet and forwards the packet to the other ports which in the same VLAN group.

The ADM6999U/UX automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming packets at wire speed. If the Source Address is not found in the Address Table, the device adds it to the table.

3.4.1.1 Address Learning

The ADM6999U/UX uses a hash algorithm to learn the MAC address and can learn up to 2K MAC addresses. Address is stored in the Address Table. The ADM6999U/UX searches for the Source Address (SA) of an incoming packet in the Address Table and acts as below:

If the SA was not found in the Address Table (a new address), the ADM6999U/UX waits until the end of the packet (non-error packet) and updates the Address Table. If the SA was found in the Address Table, then aging value of each corresponding entry will be reset to 0.

When the DA is PAUSE command, then the learning process will be disabled automatically by ADM6999U/UX.

3.4.1.2 Address Recognition and Packet Forwarding

The ADM6999U/UX forwards the incoming packets between bridged ports according to the Destination Address (DA) as below. All the packet forwarding will check VLAN first. A forwarding port must be within the same VLAN as the source port.

1. If the DA is an UNICAST address and the address was found in the Address Table, the ADM6999U/UX will check the port number and acts as follows:
   a) If the port number is equal to the port on which the packet was received, the packet is discarded.
   b) If the port number is different, the packet is forwarded across the bridge.

2. If the DA is an UNICAST address and the address was not found, the ADM6999U/UX treats it as a multicast packet and forwards across the bridge.
3. If the DA is a Multicast address, the packet is forwarded across the bridge.
4. If the DA is PAUSE Command (01-80-C2-00-00-01), then this packet will be dropped by ADM6999U/UX. ADM6999U/UX can issue and learn PAUSE command.
5. ADM6999U/UX will forward the packet with DA of (01-80-C2-00-00-00), filter out the packet with DA of (01-80-C2-00-00-01), and forward the packet with DA of (01-80-C2-00-00-02 ~ 01-80-C2-00-00-0F)

3.4.1.3 Address Aging

Address aging is supported for topology changes such as an address moving from one port to the other. When this happens, the ADM6999U/UX internally has a 300 seconds timer will aged out (remove) the address from the address table. Aging function can be enabled/disabled by user. Normally, disabling aging function is for security purpose.

3.4.1.4 Back off Algorithm

The ADM6999U/UX implements the truncated exponential back off algorithm compliant to the IEEE802.3 CSMA/CD standard. ADM6999U/UX will restart the back off algorithm by choosing 0-9 collision counts. The ADM6999U/UX resets the collision counter after 16 consecutive retransmit trials.

3.4.1.5 Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The typical number is 96-bits time. The value is 9.6μs for 10Mbps ETHERNET, and 960ns for 100Mbps fast ETHERNET. ADM6999U/UX provides the option of a 92-bit gap in EEPROM to prevent packet lost when Flow Control is turned off and clock P.P.M. value differs.

3.4.1.6 Illegal Frames

The ADM6999U/UX will discard all illegal frames such as runt packet (less than 64 bytes), oversize packet (greater than 1518 or 1522 bytes) and bad CRC. Dribbling packing with good CRC value will accept by ADM6999U/UX. In case of bypass mode enabled, ADM6999U/UX will support tag and untagged packets with size up to 1522 bytes. In case of non-bypass mode, ADM6999U/UX will support tag packets up to 1526bytes, and untagged packets up to 1522bytes.

3.4.1.7 Half Duplex Flow Control

Back Pressure function is supported for half-duplex operation. When the ADM6999U/UX cannot allocate a receiving buffer for an incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision. Back Pressure is enabled by the BPEN set during RESET asserting. An Infineon-ADMtek Co Ltd proprietary algorithm is implemented inside the ADM6999U/UX to prevent back pressure function causing HUB partitioned under heavy traffic environment and reduce the packet lost rate to increase the whole system performance.

3.4.1.8 Full Duplex Flow Control

When full duplex port runs out of its receiving buffer, a PAUSE packet command will be issued by ADM6999U/UX to notice the packet sender to pause transmission. This frame based flow control is totally compliant to IEEE 802.3x. ADM6999U/UX can issue or receive pause packet.

3.4.1.9 Broadcast Storm Filter

If Broadcast Storming filter is enable, the broadcast packets over the rising threshold within 50 ms will be discarded by the threshold setting. See EEPROM Reg.10_H.

Broadcast storm mode after initial:

Time interval: 50 ms

The max. packet number = 7490 in 100Base, 749 in 10Base

Table 4 Port Rising/Falling Threshold

Per Port Rising Threshold				
	00	01	10	11
All 100TX	Disable	10%	20%	40%
Not All 100TX	Disable	1%	2%	4%

Per Port Falling Threshold				
	00	01	10	11
All 100TX	Disable	5%	10%	20%
Not All 100TX	Disable	0.5%	1%	2%

3.4.2 Auto TP MDIX Function

At normal application which Switch connect to NIC card is by one by one TP cable. If Switch connects other device such as another Switch must by two way. First one is Cross Over TP cable. Second way is to use extra RJ45 which crossover internal TX+- and RX+- signal. By second way customers can use one by one cable to connect two Switch devices. All these efforts need extra cost and are not good solutions. ADM6999U/UX provides Auto MDIX function which can adjust TX+- and RX+- at correct pin. Users can use one by one cable between ADM6999U/UX and other device. This function can be Enable/Disable by hardware pin and EEPROM configuration register 01_H~09_H bit 15. If hardware pin set all port at Auto MDIX mode then EEPROM setting is useless. If the hardware pin sets all port at non Auto MDIX mode then EEPROM can set each port this function enable or disable.

3.4.3 Port Locking

Port locking function will provide customers a simple way to limit per port user number to one. If this function is turned on then ADM6999U/UX will lock first MAC address in learning table. After this MAC address locking will never age out except Reset signal. Another MAC address which is not the same as locking one will be dropped. ADM6999U/UX provides one MAC address per port. This function is per port setting. When turning on Port Locking function, recommend customer to turn off aging function. See EEPROM register 12_H bit 0~8.

3.4.4 VLAN Setting & Tag/Untag & Port-base VLAN

ADM6999U/UX supports bypass mode and untagged port as default setting while the chip is power-on. Thus, every packet with or without tag will be forwarding to the destination port without any modification by ADM6999U/UX. Meanwhile port-base VLAN could be enabled according to the PVID value (user define 4bits to map 16 groups written at register 13_H to register 22_H) of the configuration content of each port.

ADM6999U/UX also supports 16 802.1Q VLAN groups. In VLAN four bytes tag include twelve VLAN ID. ADM6999U/UX learns user define four bits of VID. If users need to use this function, two EEPROM registers are needed to be programmed first:

- Port VID number at EEPROM register 01_H~09_H bit 13~10, register 28_H~$2B_H$ and register $2C_H$ bit 7~0: ADM6999U/UX will check coming packet. If coming packet is non VLAN packet then ADM6999U/UX will use PVID as VLAN group reference. ADM6999U/UX will use packet's VLAN value when receiving tagged packet.