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ADM8511/X

USB/Fast Ethernet/HomePNA Controller

Communications

Never stop thinking.

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Previous Version:	
Page/Date	**Subjects (major changes since last revision)**
2000-06	Rev. 0.1: Draft product spec for review
2000-09	Rev. 1.0: Rearrange
2000-10	Rev. 2.0: Add appendix
Page62/ 2000-12	Rev. 2.01: Appendix 5/item 7/item b/item ii/ TXER change to RXER
2000-12	Rev. 2.02: Add max. power consumption P.1 I^2C change to serial
2005-09-12	Rev. 2.03: when changed to the new Infineon format
2005-11-30	Minor change. Included Green package information

Trademarks

Table of Contents

Table of Contents

List of Figures

List of Tables

1 General Description

The ADM8511/X, USB based chip set, provides desktop, notebook and computer peripheral with greater connectivity to ethernet and home network. In the meantime, the ADM8511/X also combines a low power and small package design which is ideal for power and space constrained by the environment. Then, it can reduce the external component BOM cost to a minimum. The ADM8511X is the environmentally friendly “green” package version.

The ADM8511/X device combines a on-chip USB command&EP decoder used for USB interface through SIE (Series Interface Engine), FIFO controller with 24 K SRAM, 64 byte and 2 K byte buffers, 10/100 Mbit/s ethernet physical layer (PHY) and 1M / 10M HomePNA interface 1M8 / 10M8. The 10M HomePNA interface is MII which is the same as the ethernet MAC interface. The ADM8511/X is fully compliant with the IEEE 802.3 u and HomePNA (Home Phoneline Network Alliance) specification reversion 1.0.

The ADM8511/X is capable of providing an easy, universal connectivity to computer peripherals with USB. The transfer rate of USB interface is 12 Mbit/s belonging to a high speed USB device. The ADM8511/X supports all USB commands, 4 endpoints and suspend/resume function.

The ADM8511/X’s LAN PHY supports 100 Base TX (100 Mbit/s mode) and 10 Base T (10 Mbit/s mode) full-duplex operations. It uses the auto-negotiation function to optimize the network traffic and the built-in 24M SRAM for receiving buffer, especially for 100 Mbit/s. Through FIFO controller, data cannot communicate fluently between buffers and external device. To obtain the better signal quality, the PHY provides wave-shaper, filter and adaptive equalizer to reach. By using diagnostic mechanism (loop-back mode), the data correctness will be increased. The Lan PHY supports external transmit/receive transformer turn ratio 1:1. The ADM8511/X chip set can be programmed MAC analysis and it provides MII interface for external PHY, such as 10M8 interface for 1 Mbit/s HomePNA. In the system application, it is essential that the EEPROM loads device ID and vendor ID automatically. So for ADM8511/X, serial interface is applied for EEPROM communication including read/write function. Furthermore, different system status are reported by some LED pins including transfer speed LEDSP (100 Mbit/s or 10 Mbit/s), Link status (LEDL) on network and transfer type LEDFD/COL) full- duplex or half-duplex or collision on network.

ADM8511/X is ideally suited for USB adapter and intelligent networked peripheral design. By fiber media, ADM8511/X can associate with fiber transceiver & PHY through MII interface to network in fiber network. In HomePAN application, ADM8511/X can provide 1M8 interface and 10M8 (MII interface)associated with external 1M&10M Home PHY for 1 Mbit/s & 10 Mbit/s network. ADM8511/X can’t apply only in LAN (Local Area Network) but also in WAN (Wide Area Network), such as xDSL, Cable Modem, and router, etc. In IA (Information Appliance) application, Set-Top box is an example of ADM8511/X application. ADM8511/X also provides serial interface for EEPROM storing default values, e.g. vendor ID, Product ID, etc.(EEPROM Access Program). Specially, ADM8511/X can be tested by test program (MFG) in the less time for mass productions of system board level. This chip provides low power 0.35 μm, 3.3 V/5 V I/Otolerance, and 100 pin LQFP package

In software, ADM8511/X provides a fully software support, NDIS 5 driver, Linux driver, EEPROM burn-in program and MFG program. The NDIS 5 and Linux drivers are windows netware drivers. EEPROM burn-in program is convenient for customers to implement. The MFG program is a powerful tool in mass – production.

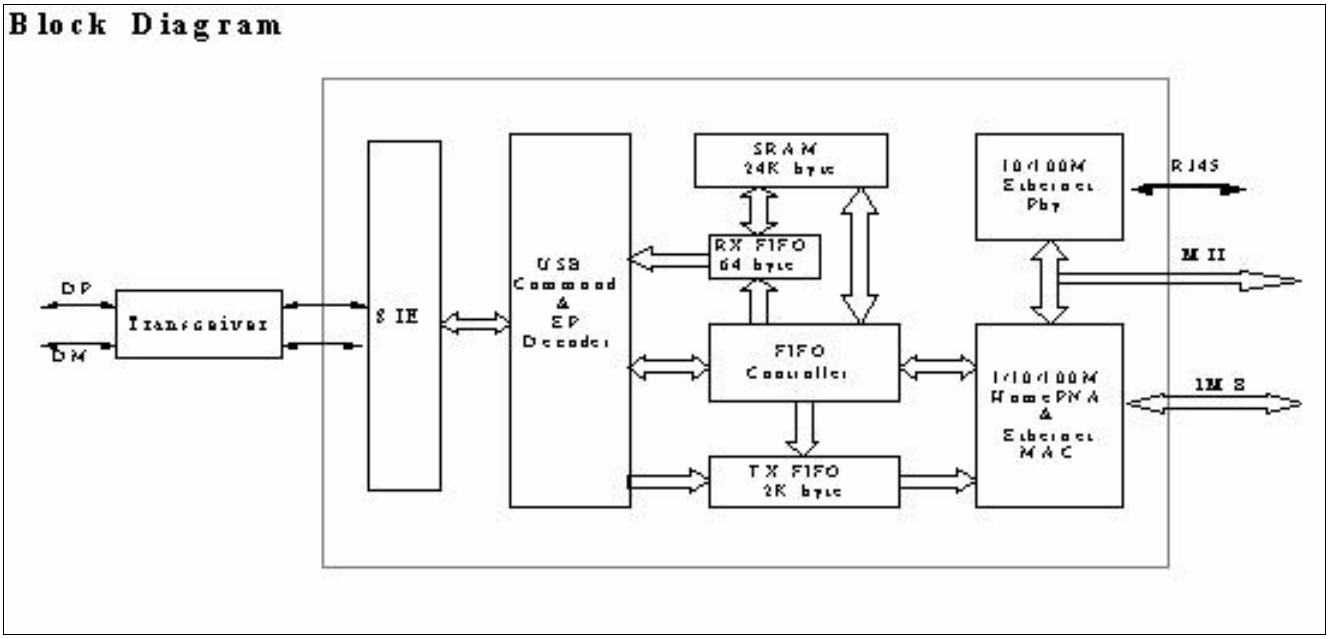

Figure 1 Block Diagram

1.1 Package Information

Product Name	Product Type	Package	Ordering Number
ADM8511/X	ADM8511/X-CC-T-1	P-LQFP-100-1	Q67801H 26A101

1.2 Features

1.2.1 Industry Standard

- IEEE802.3 u 100BASE-TX and IEEE802.3 10BASE-T compliant
- Supports for IEEE 802.3x flow control
- IEEE802.3 u Auto-Negotiation support for 10BASE-T and 100BASE-TX
- USB specification 1.0 and 1.1 compliant

1.2.2 USB I/F

- Full-Speed USB Device
- Supports 1 USB configuration and 1 interface
- Supports all USB standard commands
- Supports two vendor specific commands
- Supports USB Suspend/Resume detection logic
- Supports 4 endpoints: 1 control endpoint with maximum 8-byte packet, 1 bulk IN endpoint with maximum 64-byte packet, 1 bulk OUT endpoint with maximum 64-byte packet and 1 interrupt IN endpoint with maximum 8-byte packet

1.2.3 MAC/Phy

- Integrates the whole physical layer functions of 100BASE-TX and 10BASE-T by using phy address 1
- Be programmed to isolate the internal PHY, the I/F to external PHY could be either IEEE 802.3 MII (10M8 for HomePNA 2.0). Supports configurable threshold for transmitting PAUSE frame
- Supports wakeup frame, link status change and magic packet wake-up
- Provides full-duplex operation on both 100 Mbit/s and 10 Mbit/s Ethernet modes
- Provides Auto-negotiation (NWAY) function of full/half duplex operation for both 10/100 Mbit/s
- Provides transmit wave-shaper, receive filters, and adaptive equalizer
- Provides MLT-3 transceiver with DC restoration for Base-Line Wander compensation
- Provides MAC and Transceiver loop-back modes for diagnostic
- Supports external transmit transformer with turn ratio 1:1
- Supports external receive transformer with turn ratio 1:1

1.2.4 EEPROM I/F

- Provides serial interface for read/write 93C46 EEPROM
- Automatically load device ID, vendor ID from EEPROM after power-on reset

1.2.5 FIFO

- Supports internal 2 Kbytes SRAM for transmission
- Supports external 32 Kbytes SRAM or internal 24 Kbytes synchronous SRAM for receiving.
- Supports “receive 32 packets” or “receive 16 packets” queue in the receive buffer

1.2.6 LED Display

- Provides LED display
- LEDSP: Speed - 100 Mbit/s(on) or 10 Mbit/s(off)
- LEDL: Link (keeps on when link ok) or Active (will be blinking with 10 Hz)
- LEDFD/COL: FD (keeps on when in Full duplex mode) or Collision (will be blinking with 20 Hz when colliding)

1.2.7 Miscellaneous

- Supports 6 GPIO pins
- Provides 100-pin LQFP package
- 3.3 V power supply with 5 V/3.3 V I/O tolerance

1.2.8 LAN Driver Support

- Windows Networks: NDIS 5.0
- Linux

1.2.9 Utility

- EEPROM burn-in program

- MFG testing program

2 Interface Description

2.1 Pin Diagram

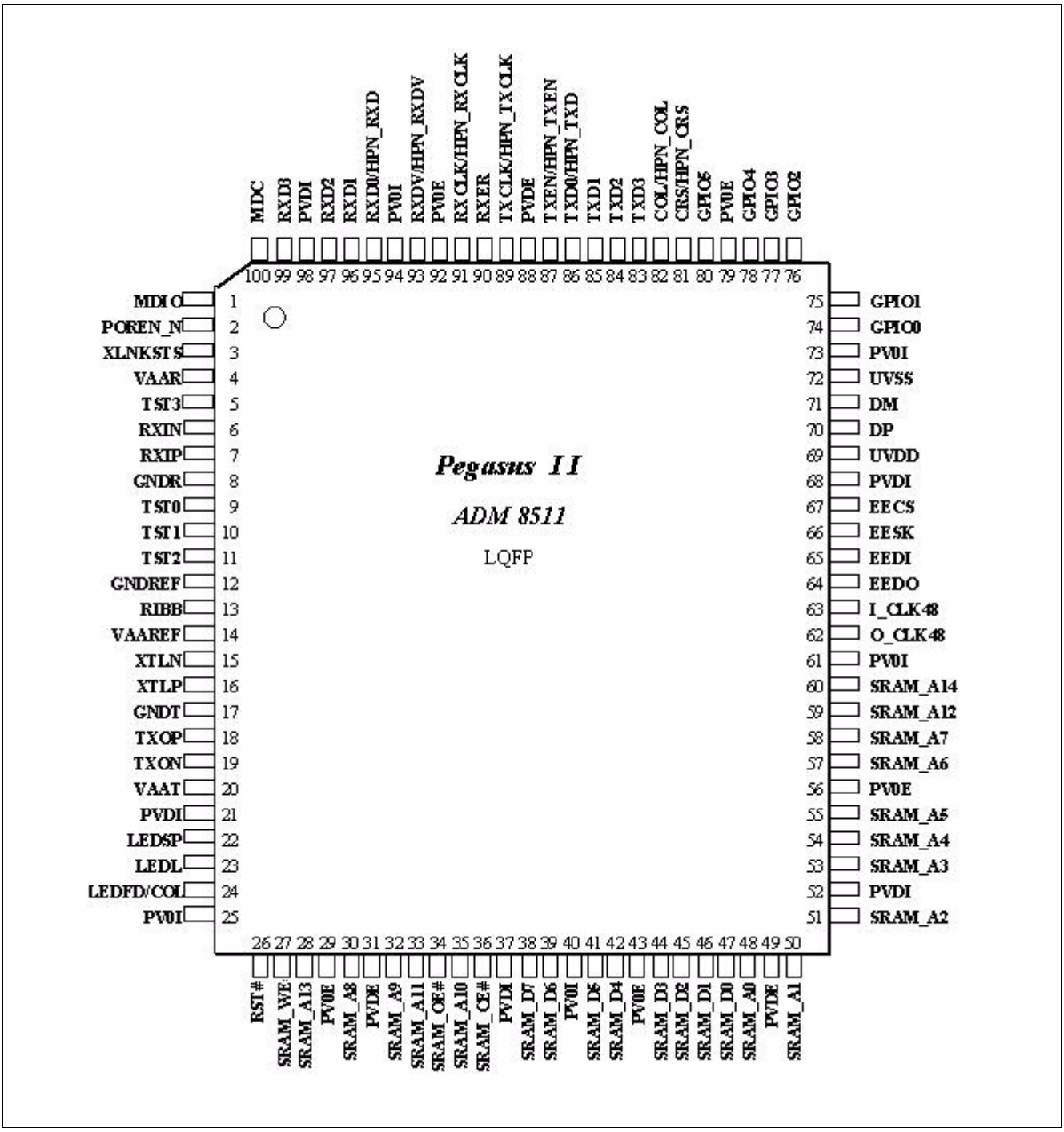

Figure 2 Pin Diagram

2.2 Pin Description

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU1	Pull up, 10 kΩ
PD1	Pull down, 10 kΩ
PD2	Pull down, 20 kΩ
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

2.2.1 Host Interface

Table 3 Host Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
63	I_CLK48	I		**48 MHz Clock Input from Crystal or Oscillator**
62	O_CLK48	O		**Output for Crystal**
26	RST#	I		**External Hardware Reset Input**
71	DM	I/O		**USB Data Minus Pin**
70	DP	I/O		**USB Data Plus Pin**

2.2.2 MII Interface

Program ADM8511/X as MAC-only mode, set 81_H[4:2]=001_B and 01_H bit 2 = 0

Table 4 MII Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
82	COL	I		**Collision Detected** This signal is asserted high asynchronously by the external physical unit upon detection of a collision on the medium. It will remain asserted as long as the collision condition persists.
81	CRS	I		**Carrier Sense** This signal is asserted high asynchronously by the external physical unit upon detection of a non-idle medium.
100	MDC	O		**Management Data Clock** Clock signal with a maximum rate of 2.5 MHz used to transfer management data for the external PMD on the MDIO pin.
1	MDIO	I/O		**Management Data I/O** Bi-directional signal used to transfer management information for the external PMD. Requires external 1.5 kΩ pull-up resistor.
91	RXCLK	I		**Receive Clock** A continuous clock that is recovered from the incoming data. During 100 Mbit/s operation RXCLK is 25 MHz, during 10 Mbit/s this is 2.5 MHz and during 1 Mbit/s operation this is 0.25 MHz.
95	RXD3	I		**Receive Data** This is a group of 4 data signals aligned on nibble boundary which are driven synchronous to the RXCLK by the external physical unit. RXD[3] is the most significant bit and RXD[0] is the least significant bit.
96	RXD2			
97	RXD1			
99	RXD0			

Table 4 MII Interface (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
93	RXDV	I		**Receive Data Valid** This indicates that the external physical unit is presenting recovered and decoded nibbles on the RXD[3:0] and that RXCLK is synchronous to the recovered data.
90	RXER	I		**Receive Error** This signal is asserted high synchronously by the external physical unit whenever it detects a media error and RXDV is asserted. If not used, it should be grounded, e.g. isolate internal phy and use external phy. However, if the external phy has RXER pin, the RXER of ADM8511/X should connect to this RXER of the external phy.
89	TXCLK	I		**Transmit Clock** A continuous clock sourced in the physical layer. During 100 Mbit/s operation this is 25 MHz ±100 ppm. During 10 Mbit/s operation this clock is 2.5 MHz ±100 ppm. During 1 Mbit/s operation this clock is 0.25 MHz ±100 ppm.
83	TXD3	O		**Transmit Data** This is a group of 4 data signals which are driven synchronously to the TXCLK for transmission to the external physical unit. TXD[3] is the most significant bit and TXD[0] is the least significant bit.
84	TXD2			
85	TXD1			
86	TXD0			
87	TXEN	O		**Transmit Enable** This signal is synchronous to TXCLK and provides precise framing for data carried on TXD[3:0]. It is asserted when TX[3:0] contains valid data to be transmitted. Requires external pull-down resistor 4.7 kΩ if external phy is used
3	XLNKSTS	I		**Link Status Indication** External PHY reports link status information to system and level change trigger. Pull-down to low if external phy is used.

2.2.3 1M8 Interface

Program ADM8511/X as MAC-only mode, set 81_H[4:2]=001_B and 01_H bit 2 = 1

Table 5 1M8 Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
82	HPN_COL	I		**Collision** Indicates a collision was detected by the 1M8 PHY on the 1M8 wiring network.
81	HPN_CRS	I		**Carrier Sense** Indicates the 1M8 PHY is receiving a valid 1M8 signal from the wiring network.

Table 5 1M8 Interface (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
91	HPN_RXCLK	I		**Receive Clock** Clock for RX_D.
95	HPN_RXD	I		**Receive Data** Data to the MAC is synchronously clocked by HPN_RXCLK.
93	HPN_RXDV	I		**Receive Data Valid** This indicates that the external physical unit is presenting recovered and decoded nibbles on the HPN_RXD and that HPN_RXCLK is synchronous to the recovered data.
89	HPN_TXCLK	I		**Transmit Clock** Clock for HPN_TXD.
86	HPN_TXD	O		**Transmit Data** Data to the PHY is synchronously clocked by HPN_TXCLK.
87	HPN_TXEN	O		**Transmit Enable** Transmits enable request from the MAC to begin sending data to the PHY.

2.2.4 Physical Interface

Table 6 Physical Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
16	XTLP	I		**Crystal inputs** To be connected to a 25 MHz crystal.
15	XTLN			
6	RXIN	I		The differential receives inputs of 100Base-TX or 10Base-T, these pins directly input from Magnetic.
7	RXIP			
18	TXOP	O		The differential Transmit outputs of 100Base-TX or 10Base-T, these pins directly output to Magnetic.
19	TXON			
13	RIBB	I		**Reference Bias Resistor** To be tied to an external 10.0K (1%) resistor which should be connected to the analog ground at the other end.
9	TST0	I		**Test pin**
10	TST1			
11	TST2			
5	TST3			

2.2.5 LED Display

Table 7 LED Display

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
22	LEDSP	O		**LED Display for 100 Mbit/s or 10 Mbit/s Speed** Active low indicates 100Base-TX, active high indicates 10 BaseT.
23	LEDL	O		**LED Display for Link and Activity Status** Active low when link is established.
24	LEDFD/COL	O		**LED Display for Full Duplex or Collision Status** Active low indicates full duplex, high indicates collision in half duplex.

2.2.6 SRAM Interface

Table 8 SRAM Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
48	SRAM_A14	O		**External SRAM Address Bus**
50	SRAM_A13			
51	SRAM_A12			
53	SRAM_A11			
54	SRAM_A10			
55	SRAM_A9			
57	SRAM_A8			
58	SRAM_A7			
30	SRAM_A6			
32	SRAM_A5			
35	SRAM_A4			
33	SRAM_A3			
59	SRAM_A2			
28	SRAM_A1			
60	SRAM_A0			
47	SRAM_D7	I/O	PD	**External SRAM Data Bus** Internal pull down
46	SRAM_D6			
45	SRAM_D5			
44	SRAM_D4			
42	SRAM_D3			
41	SRAM_D2			
39	SRAM_D1			
38	SRAM_D0			

Table 8 SRAM Interface (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
36	SRAM_CE#	O		**External SRAM Chip Enable**
34	SRAM_OE#	O		**External SRAM Output Enable**
27	SRAM_WE#	O		**External SRAM Write Enable**

2.2.7 EEPROM Interface

Table 9 EEPROM Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
67	EECS	O		**EEPROM Chip Select** This enables the EEPROM during loading of the Ethernet configuration data.
65	EEDI	O		**EEPROM Data In** The MAC will use this pin to serially write opcodes, addresses and data into the serial EEPROM.
64	EEDO	I		**EEPROM Data Out** The MAC will read the contents of the EEPROM serially through this pin.
66	EESK	O		**EEPROM Clock** After reset, the MAC if configured, will read the contents of the EEPROM using EESK, EEDO, and EEDI. This pin provides the clock for the EEPROM.

2.2.8 Miscellaneous

Table 10 Miscellaneous

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
80	GPIO5	I/O		These pins are used as general purpose Input/Output pins and offset 0A[1] = 0 in EEPROM. Default is internal pull-low
78	GPIO4			
77	GPIO3			
76	GPIO2			
75	GPIO1			
74	GPIO0			
2	POREN_N	I		**Internal Power On Reset Logic Enable** Default is enabled and internal pull - low. When external hardware reset is used, this pin should be connected to V_{cc} via 4.7 kΩ resistor.

2.2.9 Power Pins

Table 11 Power Pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
21, 37, 52, 68, 98	PVDI	P		**3.3 V Power Supply for Core**
31, 49, 88	PVDE	P		**3.3 V Power Supply for Pads**
25, 40, 61, 73, 94	PV0I	P		**Ground for PVDI**
29, 43, 56, 79, 92	PV0E	P		**Ground for PVDE**
69	UVDD	P		**3.3 V Power Supply for USB Transceiver**
72	UVSS	P		**Ground for UVDD**
4	VAAR	P	P	**Analog Power Pins, 3.3 V**
14	VAAREF			
20	VAAT			
8	GNDR	P		**Analog Ground Pins**
12	GNDREF			
17	GNDT			

3 Function Description

3.1 USB Interface

USB is a likely solution when you want to use a computer to communicate with devices outside the computer. The interface is suitable for one-of-kind and small-scale designs as well as mass-produced and standard peripheral. The benefits to USB are easy to use, fast and reliable data transfers, flexibility, low cost and power conservation.

3.1.1 SIE

SIE (Serial Interface Engine) is used to control USB communications and check USB protocol, and then transfer protocol to EP decoder. The SIE and USB transceivers, which provide the hardware interface to the USB cable, together comprise the USB engine

3.1.2 USB Command & EP Decoder

The detail description is in Appendix 4.

3.2 MAC Interface

3.2.1 MII

The Media Independent Interface (MII) is an 18 wire MAC/Phy interface described in 802.3 u. The purpose of the interface is to allow MAC layer devices to attach to a variety of Physical Layer devices through a common interface. MII operates at either 100 Mbit/s or 10 Mbit/s, dependant on the speed of the Physical Layer. With clocks running at either 25 MHz or 2.5 MHz, 4 bit data is clocked between the MAC and Phy, synchronous with Enable and Error signals.

On receipt of valid data from the wire interface, RX_DV will go active signaling to the MAC that the valid data will be presented on the RXD[3:0] pins at the speed of the RX_CLK.

On transmission of data from the MAC, TX_EN is presented to the phy indicating the presence of valid data on TXD[3:0]. TXD[3:0] are sampled by the phy synchronous to TX_CLK during the time that TX_EN is valid.

3.2.2 Adaptive Equalizer

The amplitude and phase distortions from cable cause inter-symbol interference (ISI) which makes clock and data recovery difficult. The adaptive equalizer is designed to closely match the inverse transfer function of the twisted-pairs cable. The equalizer has the ability to change its equalizer frequency response according to the cable length. The equalizer will tune itself automatically to any cable, compensating for the amplitude and phase distortion introduced by the cable.

3.2.3 LEDs

Individual LED output is available to indicate Speed, Duplex, Collision, Transmit, and Link. These multi-function pins are inputs during reset and LED output pins thereafter. The level of these pins during reset determines their active output states. If a multi-function pin is pulled up during reset to select a particular function, the LED output would become active low, and the LED circuit must be designed accordingly, and vice versa.

3.2.4 Jabber and SQE

After the MAC transmitter exceeds the jabber timer, the transmit and loopback functions will be disable and COL signal gets asserted. After TX_EN goes low for more than 500 ms, the TP transmitter will reactivate and COL gets de-asserted. Setting Jabber Disable will disable the jabber function.

When the SQE test is enabled, a COL pulse is asserted after each transmitted packet. SQE is enabled in 10Base-T by default.

3.2.5 Auto Polarity

Certain cable plants have crossed wiring on the twisted pairs; the reversal of TXIN and TXIP. Under normal circumstances this would cause the receive circuitry to reject all data. When the Auto Polarity Disable bit is cleared, the Phy is able to detect the fact that either 8 NLPs (normal link pulse) or a burst of FLPs are inverted and automatically reverses the receiver's polarity. The polarity state is stored in the Reverse Polarity bit.

3.2.6 Auto-Negotiation

It provides a linked device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the link, determines common abilities, and configures joint operations. Auto-Negotiation is performed out-of-band using a pulse code sequence that is compatible with the 10Base-T link integrity test sequence.

3.2.7 Baseline Wander Compensation

The 100BASE-TX data stream is not always DC balanced. The transformer blocks the DC components of the incoming signal, thus the DC offset of the differential receive inputs can drift. The shifting of the signal level, coupled with non-zero rise, and fall times of the serial stream, can cause pulse-width distortion. This creates jitter and possibly increases in the bit error rates. Therefore, a DC restoration circuit is needed to compensate the attenuation of the DC component. Unlike the traditional implementation, the circuit does not need the feedback information from the slicer or the clock recovery circuit. The design simplifies the circuit design. In 10Base-T, the baseline wander correction circuit is not required.

3.3 FIFO Controller

FIFO Controller in receive path is in charge of:

- Store received Ethernet packets to SRAM (internal 24 Kbyte or external 32 Kbyte) and total 32 (or 16) packets can be stored to SRAM. If more than maximum packet counts are received or total packet size is more than 32 K (or 24 K for internal SRAM) bytes, the subsequent coming Ethernet packet will be discarded.
- FIFO controller will load data from SRAM to internal RX FIFO then inform EP Decoder that 64-byte data or a packet is ready in RX FIFO. Before FIFO controller informs this, any USB access to bulk IN endpoint will return NAK. To maintain the data transfer on USB bus via bulk IN transfer must be continuously, thus a 64-byte internal RX FIFO is needed.
- If an Ethernet packet is being received and loading into SRAM while FIFO Controller is moving data from SRAM to internal RX FIFO, writing the Ethernet packet to SRAM will get the higher priority.

FIFO Controller in transmit path is in charge of:

- Store each individual USB packet to internal TX FIFO. When EP decoder informs end of packet, a complete Ethernet packet is stored in TX FIFO. FIFO Controller then informs MAC to transmit this packet.
- Total 4 Ethernet packets can be stored in TX FIFO. If all 4 Ethernet packets are stored in TX FIFO or total packet size is more than 2 K bytes, FIFO Controller will inform EP Decoder that TX FIFO is full and EP Decoder will return NAK if accessing bulk OUT endpoint is invoked. Thus additional USB packet won't be written into TX FIFO until TX FIFO has free space.

3.4 TX FIFO and RX FIFO

RX FIFO is a one-port 64-byte FIFO and TX FIFO is a two-port 2 Kbyte FIFO.

3.5 1/10/100 Ethernet/HomePNA MAC

The MAC controller takes in charge of:

- Generate CRC then transmit Ethernet packet.
- Check CRC for received packet CRC, filter the received packets.
- Polling PHY status.
- Magic packet detection.
- Automatically transmit PAUSE frame when received status meets the flow control criteria.
- Late collision transmit packets will be discarded.

3.6 10/100M Ethernet PHY

The internal Ethernet PHY is compliant to IEEE 802.3u 100Base-TX and IEEE802.3 10Base-T. It provides the whole physical layer functions for both 10M and 100M Ethernet speed. The internal PHY can be isolated by programming register offset $7B_H$, bit 1.

4 Registers Description

System Registers and Transceiver Registers.

4.1 System Registers

Table 12 Registers Address Space

Module	Base Address	End Address	Note
System Registers	0000 0000_H	0000 0081_H	

Table 13 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
EC0	Ethernet Control 0	00_H	29
EC1	Ethernet Control 1	01_H	30
EC2	Ethernet Control 2	02_H	31
Res0	Reserved 0	03_H	32
Res1	Reserved 1	04_H	32
Res2	Reserved 2	05_H	32
Res3	Reserved 3	06_H	32
Res4	Reserved 4	07_H	32
MC0	Multicast 0	08_H	32
MC1	Multicast 1	09_H	33
MC2	Multicast 2	$0A_H$	33
MC3	Multicast 3	$0B_H$	33
MC4	Multicast 4	$0C_H$	34
MC5	Multicast 5	$0D_H$	34
MC6	Multicast 6	$0E_H$	34
MC7	Multicast 7	$0F_H$	35
EID0	Ethernet ID 0	10_H	35
EID1	Ethernet ID 1	11_H	36
EID2	Ethernet ID 2	12_H	36
EID3	Ethernet ID 3	13_H	37
EID4	Ethernet ID 4	14_H	37
EID5	Ethernet ID 5	15_H	38
Res5	Reserved 5	16_H	38
Res6	Reserved 6	17_H	38
PTL	Pause Timer Low	18_H	39
Res7	Reserved 7	19_H	39
RPNBFC	Receive Packet Number Based Flow Control	$1A_H$	40
ORFBFC	Occupied Receive FIFO Based Flow Control	$1B_H$	40
EP1C	EP1 Control	$1C_H$	40
RXFC	RX FIFO Control	$1D_H$	41
BISTC	BIST Control	$1E_H$	41
Res8	Reserved 8	$1F_H$	42
EEPROMO	EEPROM Offset	20_H	42
EEPROMDL	EEPROM Data Low	21_H	43