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3.3 V, 50 Mbps to 4.25 Gbps, Single-Loop, Laser Diode Driver

Data Sheet **ADN2871**

FEATURES

- SFP/SFF and SFF-8472 MSA-compliant
- SFP reference design available
- 50 Mbps to 4.25 Gbps operation
- Automatic average power control
- Typical 60 ps rise/fall time
- VCSEL, DFB, and FP laser support
- Bias current range: 2 mA to 100 mA
- Modulation current range: 5 mA to 90 mA
- Laser fail alarm and automatic laser shutdown (ALS)
- Bias and modulation current monitoring
- 3.3 V supply
- 4 mm × 4 mm LFCSP
- Voltage setpoint control
- Resistor setpoint control
- Pin-compatible with ADN2870

APPLICATIONS

- 1×/2×/4× Fibre Channel SFP/SFF modules
- Multirate OC3 to OC48-FEC SFP/SFF modules
- LX-4 modules
- DWDM/CWDM SFP modules
- 1GE SFP/SFF transceiver modules
- VCSEL, DFB, and FP transmitters

GENERAL DESCRIPTION

The ADN2871 laser diode driver (LDD) is designed for advanced SFP and SFF modules, using SFF-8472 digital diagnostics. The ADN2871 supports operation from 50 Mbps up to 4.25 Gbps.

Average power and extinction ratios can be set with a voltage provided by a microcontroller DAC or by a trimmable resistor or digital potentiometer. The average power control loop is implemented using feedback from a monitor photodiode. The device provides bias and modulation current monitoring, as well as fail alarms and automatic laser shutdown (ALS). The device interfaces easily with the Analog Devices, Inc., ADuC7019 and ADuC7020 family of MicroConverter® devices and with the ADN2890, ADN2891, and ADN2892 family of limiting amplifiers to make a complete SFP/SFF transceiver solution. An SFP reference design is available.

The product is pin-compatible with the ADN2870 dual-loop LDD, allowing the same design to work with either device. For dual-loop control applications, refer to the ADN2870 data sheet. The product is available in a space-saving 4 mm × 4 mm LFCSP specified over the −40°C to +85°C temperature range.

Figure 1 shows an application diagram of the voltage setpoint control with single-ended laser interface. Figure 36 shows a differential-ended laser interface.

APPLICATIONS DIAGRAM

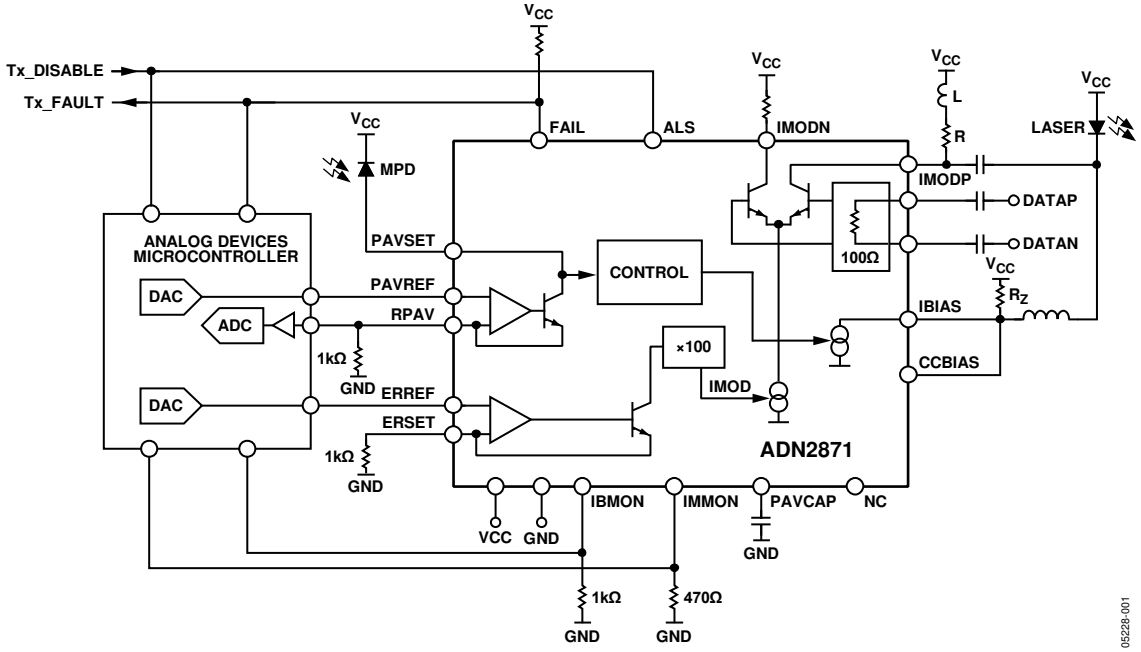

Figure 1. Typical Application Setup

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Technical Support www.analog.com

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADN2871 Evaluation Board

DOCUMENTATION

Data Sheet

- ADN2871: 3.3 V, 50 Mbps to 4.25 Gbps, Single-Loop, Laser Diode Driver Data Sheet

REFERENCE MATERIALS

Informational

- Optical and High Speed Networking ICs
- SFP Chipset and Reference Design Simplify 4.25 GBPS Transceivers

DESIGN RESOURCES

- ADN2871 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADN2871 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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6/2005—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 3.0 V to 3.6 V. All specifications T_{MIN} to T_{MAX}[1], unless otherwise noted. Typical values as specified at 25°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LASER BIAS CURRENT (IBIAS)					
Output Current (IBIAS)	2		100	mA	
Compliance Voltage	1.2		V_{CC}	V	
IBIAS when ALS is High			0.1	mA	
MODULATION CURRENT (IMODP, IMODN)[2]					
Output Current (IMOD)	5		90	mA	
Compliance Voltage	1.5		V_{CC}	V	
IMOD when ALS is High			0.1	mA	5 mA < IMOD < 90 mA
Rise Time, Single-Ended Output[2, 3]		60	104	ps	5 mA < IMOD < 90 mA
Fall Time, Single-Ended Output[2, 3]		60	96	ps	5 mA < IMOD < 90 mA
Random Jitter, Single-Ended Output[2, 3]		0.8	1.1	ps (rms)	5 mA < IMOD < 90 mA
Deterministic Jitter, Single-Ended Output[3, 4]		19	35	ps	20 mA < IMOD < 90 mA
Pulse-Width Distortion, Single-Ended Output[2, 3]		21	30	ps	20 mA < IMOD < 90 mA
Rise Time, Differential Output[3, 5]		47.1		ps	5 mA < IMOD < 30 mA
Fall Time, Differential Output[3, 5]		46		ps	5 mA < IMOD < 30 mA
Random Jitter, Differential Output[3, 5]		0.64		ps (rms)	5 mA < IMOD < 30 mA
Deterministic Jitter, Differential Output[3, 6]		12		ps	5 mA < IMOD < 30 mA
Pulse-Width Distortion, Differential Output[3, 5]		2.1		ps	5 mA < IMOD < 30 mA
Rise Time, Differential Output[3, 5]		56		ps	5 mA < IMOD < 90 mA
Fall Time, Differential Output[3, 5]		55		ps	5 mA < IMOD < 90 mA
Random Jitter, Differential Output[3, 5]		0.61		ps (rms)	5 mA < IMOD < 90 mA
Deterministic Jitter, Differential Output[3, 7]		17		ps	5 mA < IMOD < 90 mA
Pulse-Width Distortion, Differential Output[3, 5]		1.6		ps	5 mA < IMOD < 90 mA
AVERAGE POWER SET (PAVSET)					
Pin Capacitance			80	pF	
Voltage	1.1	1.2	1.3	V	
Photodiode Monitor Current (Average Current)	50		1200	µA	Resistor setpoint mode
EXTINCTION RATIO SET INPUT (ERSET)					
Resistance Range	1.5		25	kΩ	Resistor setpoint mode
	0.99	1	1.01	kΩ	Voltage setpoint mode
AVERAGE POWER REFERENCE VOLTAGE INPUT (PAVREF)					
Voltage Range	0.07		1	V	Voltage setpoint mode (RPAV fixed at 1 kΩ)
Photodiode Monitor Current (Average Current)	70		1000	µA	Voltage setpoint mode (RPAV fixed at 1 kΩ)
EXTINCTION RATIO REFERENCE VOLTAGE INPUT (ERREF)					
Voltage Range	0.05		0.9	V	Voltage setpoint mode (RERSET fixed at 1 kΩ)
ERREF Voltage to IMOD Gain		100		mA/V	
DATA INPUTS (DATAP, DATAN)[8]					
Input Voltage Swing (Differential)	0.4		2.4	V p-p	AC-coupled
Input Impedance (Single-Ended)		50		Ω	
LOGIC INPUTS (ALS)					
V_{IH}	2			V	
V_{IL}			0.8	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ALARM OUTPUT (FAIL)[9]					
V_{OFF}		>1.8		V	Voltage required at FAIL for IBIAS and IMOD to turn off when FAIL asserted
V_{ON}		<1.3		V	Voltage required at FAIL for IBIAS and IMOD to stay on when FAIL asserted
IBMON/IMMON DIVISION RATIO					
IBIAS/IBMON[3]	76	94	112	A/A	2 mA < IBIAS < 11 mA
IBIAS/IBMON[3]	85	100	115	A/A	11 mA < IBIAS < 50 mA
IBIAS/IBMON[3]	92	100	108	A/A	50 mA < IBIAS < 100 mA
IBIAS/IBMON Stability[3, 10]			±5	%	10 mA < IBIAS < 100 mA
IMOD/IMMON		42		A/A	
IBMON Compliance Voltage	0		1.3	V	
SUPPLY					
I_{CC}[11]		32		mA	When IBIAS = IMOD = 0 mA
V_{CC} (with Respect to GND)[12]	3.0	3.3	3.6	V	

[1] Temperature range: –40°C to +85°C.
[2] Measured into a single-ended 15 Ω load (22 Ω resistor in parallel with digital scope 50 Ω input) using a 1111111100000000 pattern at 2.5 Gbps, shown in Figure 2.
[3] Guaranteed by design and characterization. Not production tested.
[4] Measured into a single-ended 15 Ω load using a K28.5 pattern at 2.5 Gbps, shown in Figure 2.
[5] Measured into a differential 30 Ω (43 Ω differential resistor in parallel with a digital scope of 50 Ω input) load using a 1111111100000000 pattern at 4.25 Gbps, as shown in Figure 3.
[6] Measured into a differential 30 Ω load using a K28.5 pattern at 4.25 Gbps, as shown in Figure 3.
[7] Measured into a differential 30 Ω load using a K28.5 pattern at 2.7 Gbps, as shown in Figure 3.
[8] When the voltage on DATAP is greater than the voltage on DATAN, the modulation current flows into the IMODP pin.
[9] Guaranteed by design. Not production tested.
[10] IBIAS/IBMON ratio stability is defined in SFF-8472 Revision 9 over temperature and supply variation.
[11] See the I_{CC} minimum for power calculation in the Power Consumption section.
[12] All V_{CC} pins must be shorted together.

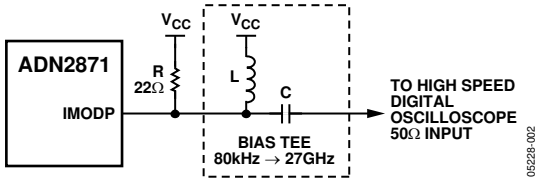


Figure 2. High Speed Electrical Test Single-Ended Output Circuit

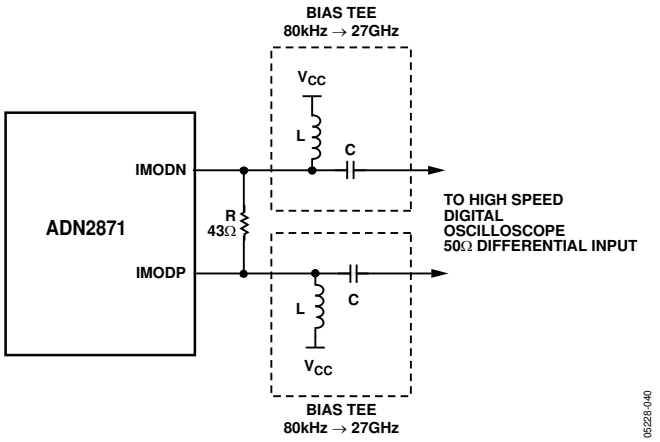


Figure 3. High Speed Electrical Test Differential Output Circuit

SFP TIMING SPECIFICATIONS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ALS Assert Time	$t_{\_OFF}$		1	5	µs	The time from the rising edge of ALS to when the optical output falls below 10% of nominal.
ALS Negate Time[1]	$t_{\_ON}$		0.15	0.4	ms	The time from the falling edge of ALS to the modulation current rises above 90% of nominal.
Initialize Time, Including Reset of FAIL[1]	$t_{\_INIT}$		25	275	ms	From the power-on or negation of FAIL using ALS.
FAIL Assert Time	$t_{\_FAULT}$			100	µs	The time from fault to FAIL on.
ALS to Reset Time	$t_{\_RESET}$			5	µs	Time ALS must be held high to reset FAULT.

[1] Guaranteed by design and characterization. Not production tested.

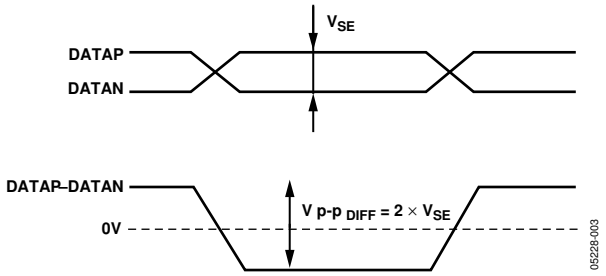


Figure 4. Signal Level Definition

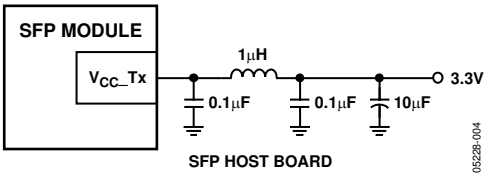


Figure 5. Recommended SFP Supply

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VCC to GND	4.2 V
IMODN, IMODP	−0.3 V to +4.8 V
All Other Pins	−0.3 V to +3.9 V
Junction Temperature	150°C
Operating Temperature Range, Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
Power Dissipation[1]	(T_J max − T_A)/θ_{JA} W
θ_{JA} Thermal Impedance[2]	30°C/W
θ_{JC} Thermal Impedance	29.5°C/W
Lead Temperature (Soldering 10 sec)	300°C

[1] Power consumption equations are provided in the Power Consumption section.
[2] θ_{JA} is defined when the device is soldered on a 4-layer board.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

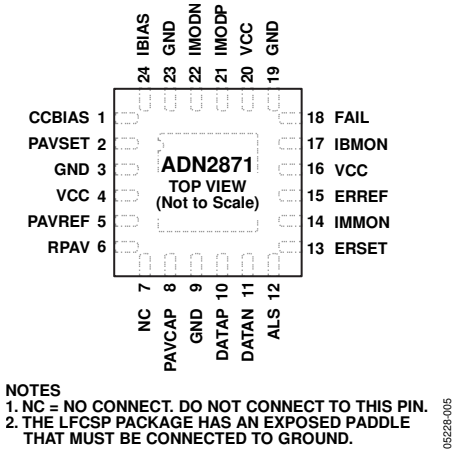


Figure 6. Pin Configuration—Top View

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CCBIAS	In ac-coupled mode, CCBIAS can connect to either IBIAS or VCC. In dc-coupled mode, CCBIAS can connect to VCC.
2	PAVSET	Average Optical Power Set Pin.
3	GND	Supply Ground.
4	VCC	Supply Voltage.
5	PAVREF	Reference Voltage Input for Average Optical Power Control.
6	RPAV	Average Power Resistor when Using PAVREF.
7	NC	No Connect.
8	PAVCAP	Average Power Loop Capacitor.
9	GND	Supply Ground.
10	DATAP	Data, Positive Differential Input.
11	DATAN	Data, Negative Differential Input.
12	ALS	Automatic Laser Shutdown.
13	ERSET	Extinction Ratio Set Pin.
14	IMMON	Modulation Current Monitor Current Source.
15	ERREF	Reference Voltage Input for Extinction Ratio Control.
16	VCC	Supply Voltage.
17	IBMON	Bias Current Monitor Current Source.
18	FAIL	Fail Alarm Output.
19	GND	Supply Ground.
20	VCC	Supply Voltage.
21	IMODP	Modulation Current Positive Output (Current Sink), Connect to Laser Diode.
22	IMODN	Modulation Current Negative Output (Current Sink).
23	GND	Supply Ground.
24	IBIAS	Laser Diode Bias (Current Sink to Ground).
	EP	Exposed Paddle. The LFCSP Package has an exposed paddle that must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

SINGLE-ENDED OUTPUT

These performance characteristics are measured using the high speed, electrical single-ended, output circuit shown in Figure 2.

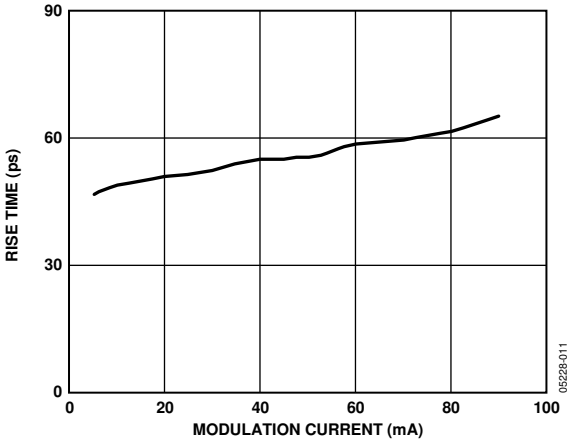


Figure 7. Rise Time vs. Modulation Current, I_{BIAS} = 20 mA

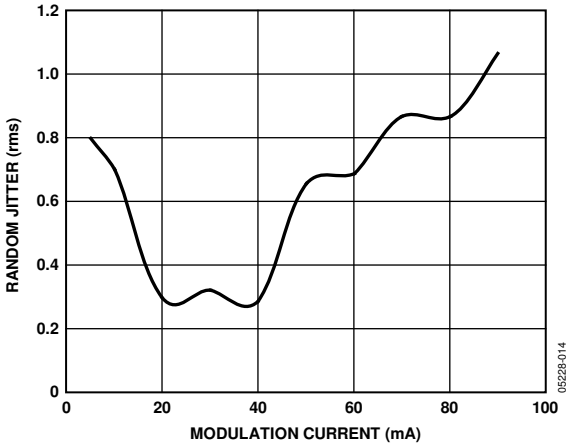


Figure 9. Random Jitter vs. Modulation Current, I_{BIAS} = 20 mA

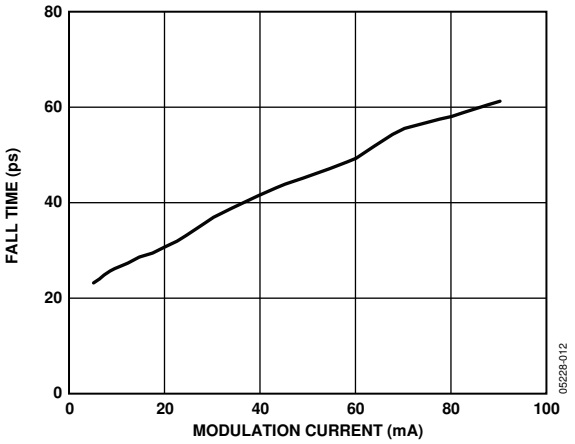


Figure 8. Fall Time vs. Modulation Current, I_{BIAS} = 20 mA

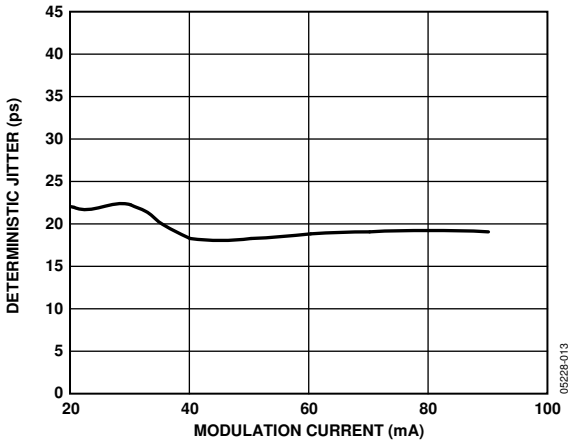


Figure 10. Deterministic Jitter at 2.488 Gbps vs. Modulation Current, I_{BIAS} = 20 mA

DIFFERENTIAL OUTPUT

These performance characteristics are measured using the high speed, electrical differential output circuit shown in Figure 3.

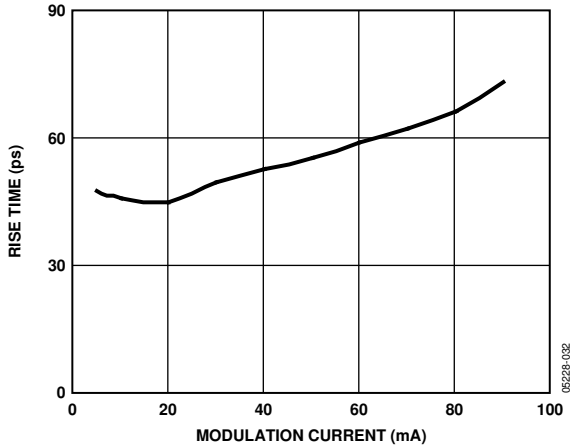


Figure 11. Rise Time vs. Modulation Current, I_{BIAS} = 20 mA

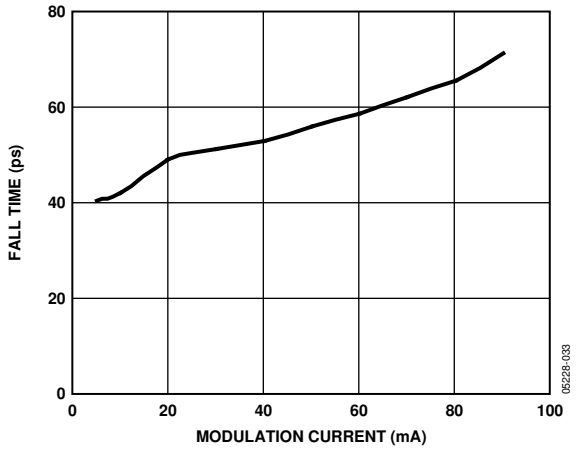


Figure 12. Fall Time vs. Modulation Current, I_{BIAS} = 20 mA

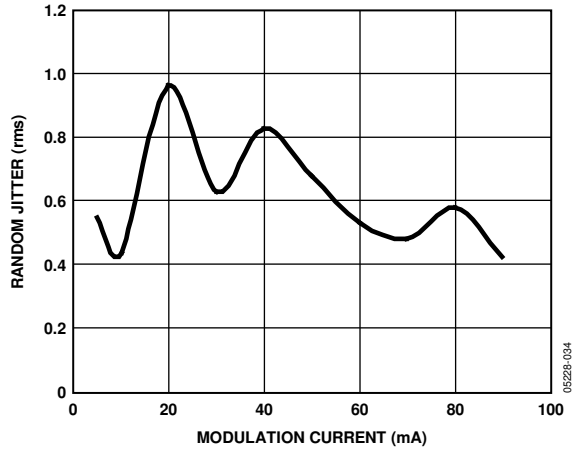


Figure 13. Random Jitter vs. Modulation Current, I_{BIAS} = 20 mA

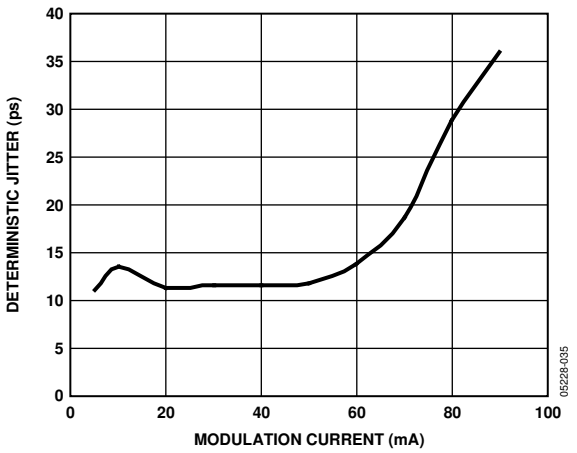


Figure 14. Deterministic Jitter at 4.25 Gbps vs. Modulation Current, I_{BIAS} = 20 mA

PERFORMANCE CHARACTERISTICS

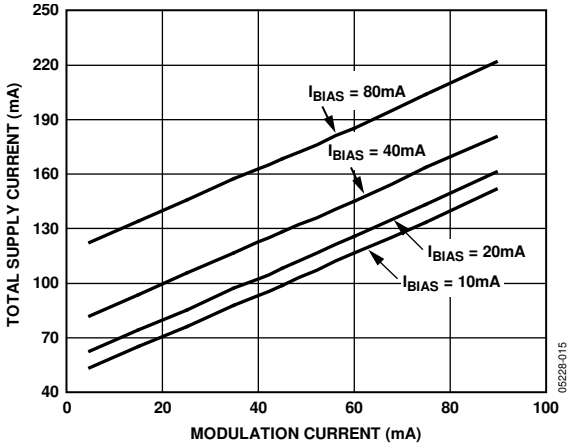


Figure 15. Total Supply Current vs. Modulation Current
Total Supply Current = ICC + I_{BIAS} + I_{MOD}

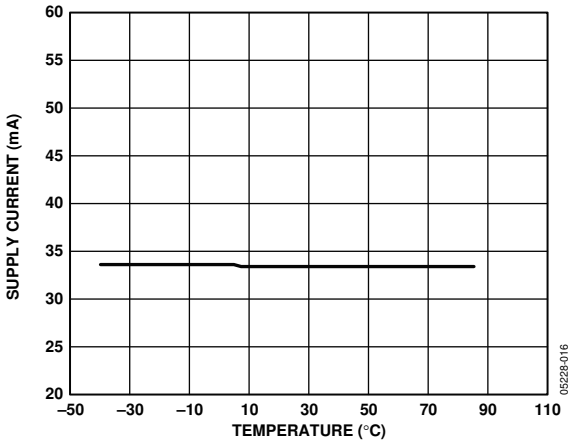


Figure 18. Supply Current (I_{CC}) vs. Temperature with ALS Asserted, I_{BIAS} = 20 mA

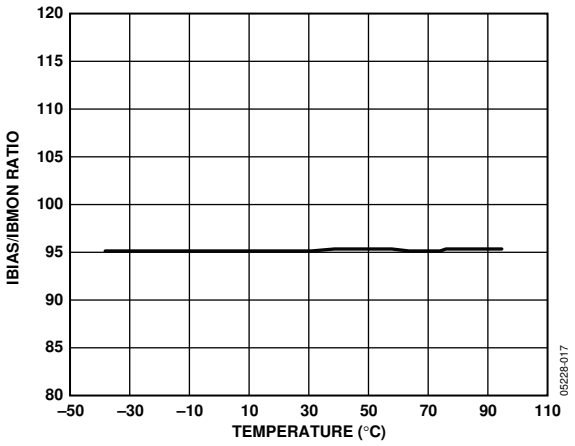


Figure 16. IBIAS/IBMON Gain vs. Temperature, I_{BIAS} = 20 mA

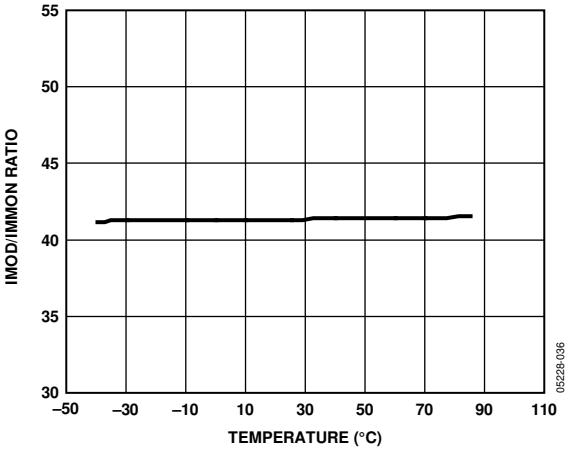


Figure 19. IMOD/IMMON Gain vs. Temperature, I_{MOD} = 30 mA

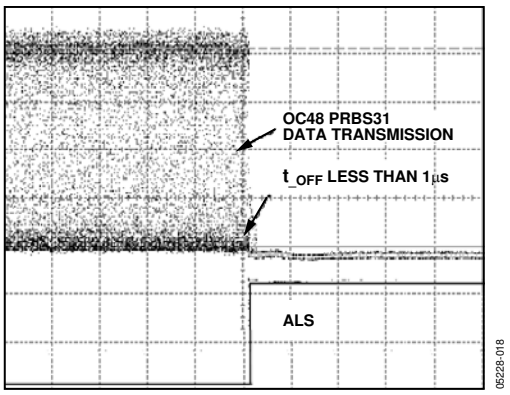


Figure 17. ALS Assert Time, 5 µs/DIV

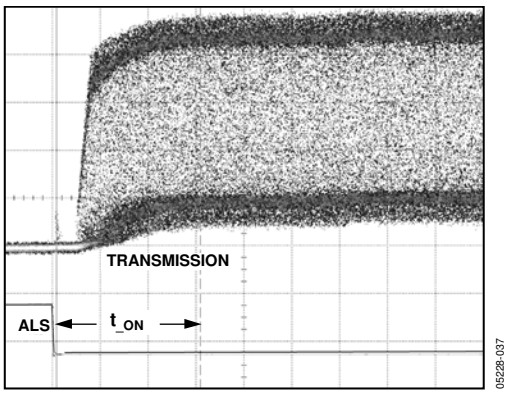


Figure 20. ALS Negate Time, 50 µs/DIV

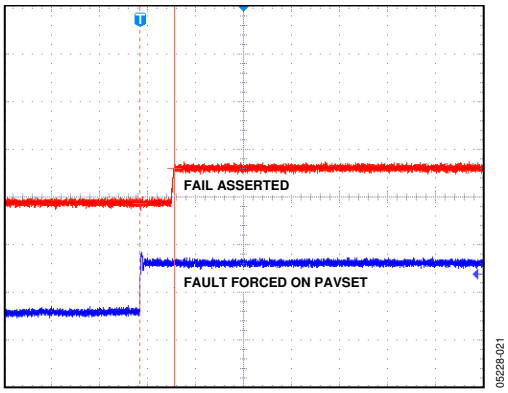


Figure 21. FAIL Assert Time,1 µs/DIV

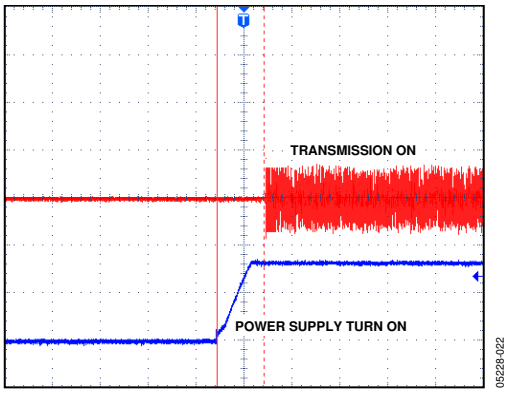


Figure 22. Time to Initialize, Including Reset, 40 ms/DIV

OPTICAL WAVEFORMS

V_{CC} = 3.3 V and T_A = 25°C, unless otherwise noted. Note that there is no change to PAVCAP and ERCAP values when different data rates are tested. Figure 23, Figure 24, and Figure 25 show multirate performance using the lowe cost Fabry Perot TOSA NEC NX7315UA; Figure 26 and Figure 27 show performance over temperature using the DFB TOSA Sumitomo SLT2486.

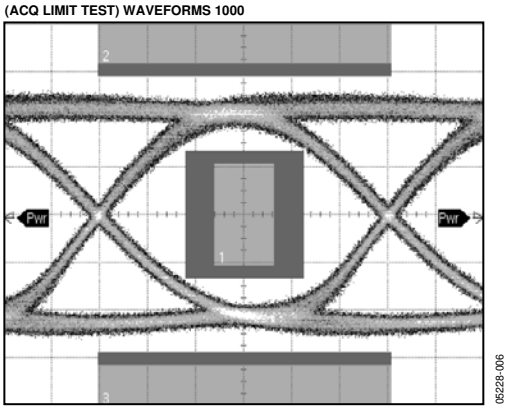


Figure 23. Optical Eye 2.488 Gbps, 65 ps/DIV, PRBS 2^{31-1} P_{AV} = −4.5 dBm, ER = 9 dB, Mask Margin 25%

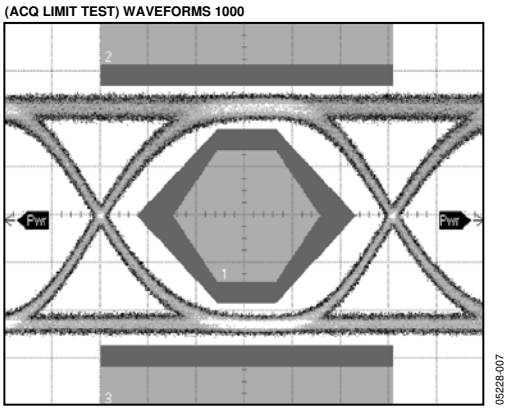


Figure 24. Optical Eye 622 Mbps, 264 ps/DIV, PRBS 2^{31-1} P_{AV} = −4.5 dBm, ER = 9 dB, Mask Margin 50%

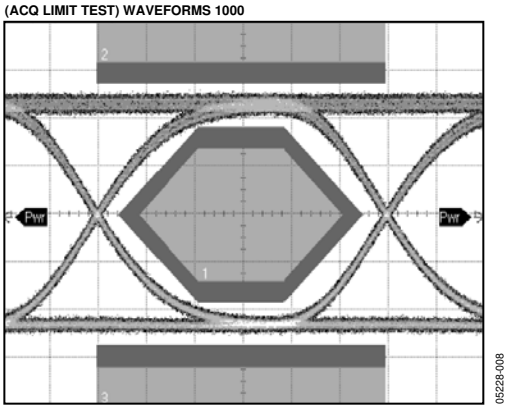


Figure 25. Optical Eye 155 Mbps,1.078 ns/DIV, PRBS 2^{31-1} P_{AV} = −4.5 dBm, ER = 9 dB, Mask Margin 50%

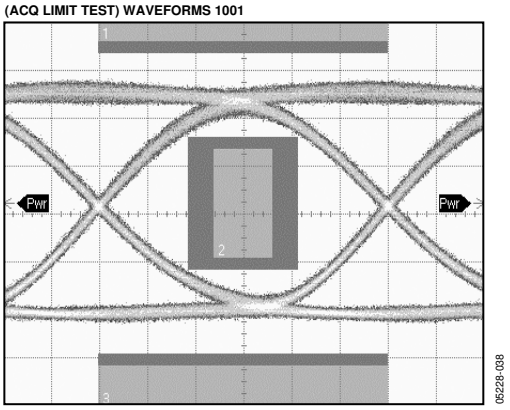


Figure 26. Optical Eye 2.488 Gbps, 65 ps/DIV, PRBS 2^{31-1} P_{AV} = 0 dBm, ER = 9 dB, Mask Margin 22%, T_A = 25°C

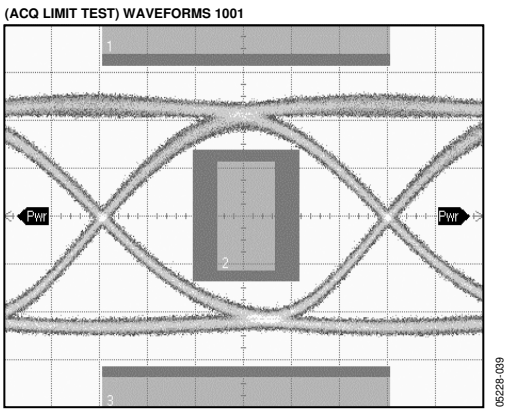


Figure 27. Optical Eye 2.488 Gbps, 65 ps/DIV, PRBS 2^{31-1} P_{AV} = −0.2 dBm, ER = 8.96 dB, Mask Margin 21%, T_A = 85°C

THEORY OF OPERATION

Laser diodes have a current-in to light-out transfer function, as shown in Figure 28. Two key characteristics of this transfer function are the threshold current, Ith, and the slope in the linear region beyond the threshold current, referred to as the slope efficiency, LI.

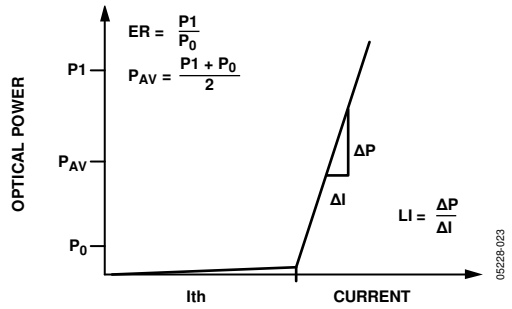


Figure 28. Laser Transfer Function

LASER CONTROL

Typically, laser threshold current and slope efficiency are both functions of temperature. For FP- and DFB-type lasers, the threshold current increases and the slope efficiency decreases with increasing temperature. In addition, these parameters vary as the laser ages. To maintain a constant optical average power and a constant optical extinction ratio over temperature and laser lifetime, it is necessary to vary the applied electrical bias current and modulation current to compensate for the changing LI characteristics of the laser.

Average Power Control Loop (APCL)

The APCL compensates for changes in Ith and LI by varying IBIAS. Average power control is performed by measuring the MPD current, I_{MPD}. This current is bandwidth-limited by the MPD. This is not a problem because the APCL is required to respond to the average current from the MPD.

Extinction Ratio (ER) Control

ER control is implemented by adjusting the modulation current. Temperature calibration is required to adjust the modulation current to compensate for variations of the laser characteristics with temperature.

CONTROL METHODS

The ADN2871 has two methods for setting the average power (P_{AV}) and extinction ratio (ER). The average power and extinction ratio can be voltage-set using the output of a microcontroller's voltage DACs to provide controlled reference voltages, PAVREF and ERREF. Alternatively, the average power and extinction ratio can be resistor-set using potentiometers at the PAVSET and ERSET pins, respectively.

VOLTAGE SETPOINT CALIBRATION

The ADN2871 allows interface to a microcontroller for both control and monitoring (see Figure 29). The average power and extinction ratio can be set using the microcontroller DACs to provide controlled reference voltages, PAVREF and ERREF.

$$PAVREF = P_{AV} \times R_{SP} \times R_{PAV} \quad \text{(V)}$$

$$ERREF = \frac{I_{MOD} \times R_{ERSET}}{100} \quad \text{(V)}$$

where:
R_{SP} is the MPD optical responsivity (in amperes per watt).
P_{AV} is the average power required.
$R_{PAV} = R_{ERSET} = 1\ k\Omega$.
I_{MOD} is the modulation current.

In voltage setpoint mode, R_{PAV} and R_{ERSET} must be 1 kΩ resistors with a 1% tolerance and a temperature coefficient of 50 ppm/°C.

Power-On Sequence in Voltage Setpoint Mode

During power-up, the ADN2871 goes through its programmed power-up sequence allowing 25 ms before enabling the alarms. Therefore, it is important to ensure the programmed voltages for PAVREF and ERREF are active within 20 ms after ramp-up of the power supply. If no PAVREF and ERREF voltages are applied before the enabled alarms, the ADN2871 alarms and FAIL detection circuits activate and report errors.

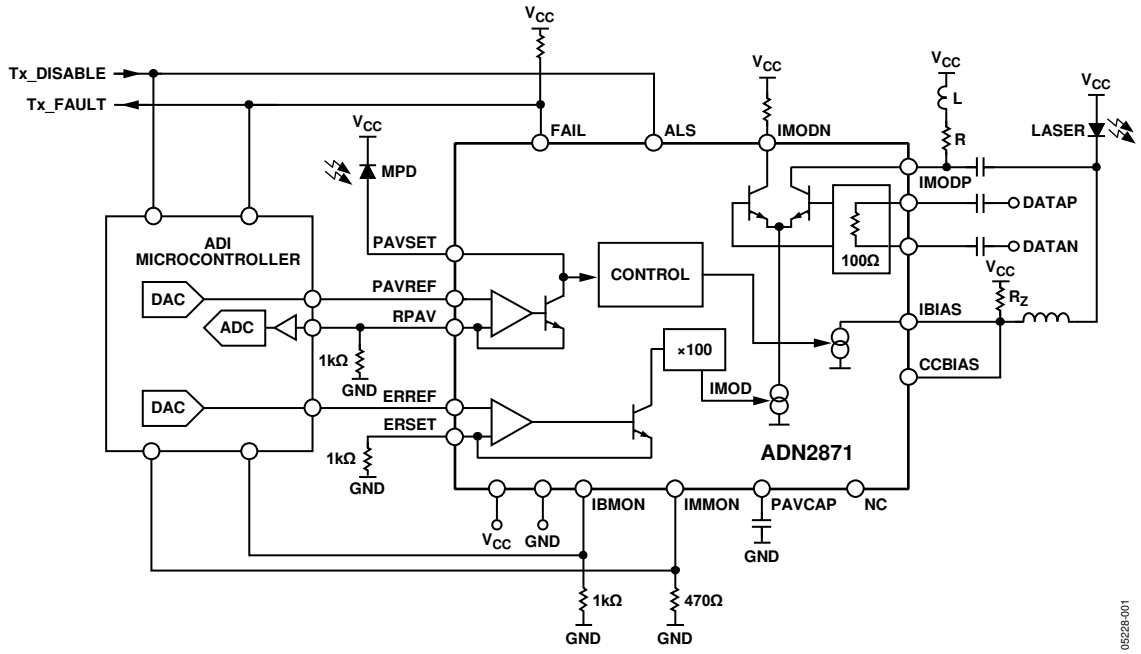


Figure 29. ADN2871 Using Microconverter Voltage Setpoint Calibration and Monitoring

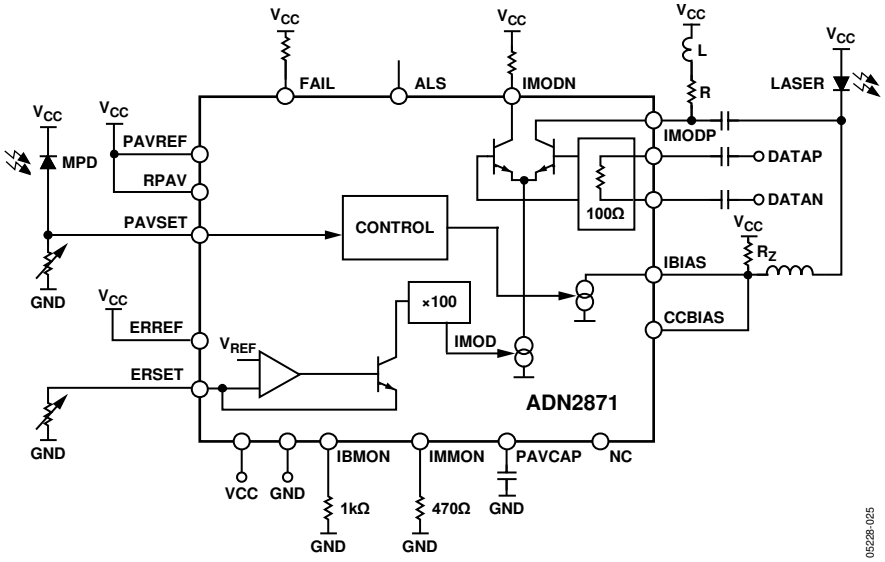


Figure 30. ADN2871 Using Resistor Setpoint Calibration of Average Power and Extinction Ratio

RESISTOR SETPOINT CALIBRATION

In resistor setpoint calibration, Pin PAVREF, Pin ERREF, and Pin RPAV must all be tied to VCC. The average power and extinction ratio can be set using the PAVSET and ERSET pins, respectively. A resistor placed between the pin and GND sets the current flow-ing in each pin, as shown in Figure 30. The ADN2871 ensures that both PAVSET and ERSET are kept 1.23 V above GND. The PAVSET and ERSET resistors are given by

$$R_{PAVSET} = \frac{1.23\ \text{V}}{P_{AV} \times R_{SP}} \quad (\Omega)$$

$$R_{ERSET} = \frac{1.23\ \text{V} \times 100}{I_{MOD}} \quad (\Omega)$$

where:
R_{SP} is the optical responsivity (in amperes per watt).
I_{MOD} is the modulation current required (mA).
P_{AV} is the average power required (mW).

Power-On Sequence in Resistor Setpoint Mode

After power-on, the ADN2871 starts an initial calibration processes that takes 25 ms before enabling the alarms. Therefore, the resistors connected to Pin PAVSET and Pin ERSET must stabilize within 20 ms after power-on. If the PAVSET and ERSET resistors do not stabilize within 20 ms after turning on the power supply, the ADN2871 alarm turns on and asserts a FAIL.

I_{MPD} MONITORING

In both voltage setpoint and resistor setpoint modes, several optional I_{MPD} monitoring setups are available as described in the following sections.

Voltage Setpoint

There are two I_{MPD} monitoring methods used in voltage setpoint calibration.

Method 1: Measuring Voltage at RPAV

The I_{MPD} current is equal to the voltage at RPAV divided by the value of RPAV (see Figure 31) as long as the laser is on and is under the control of theADN2871. This method does not provide a valid I_{MPD} reading when the laser is in shutdown or fail mode. A MicroConverter buffered ADC input can be connected to RPAV to make this measurement. No decoupling or filter capacitors must be placed on the RPAV node because this can disturb the control loop.

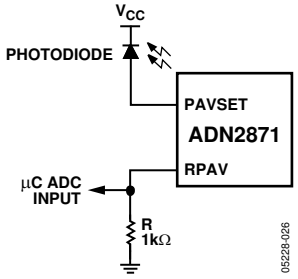


Figure 31. Single Measurement of I_{MPD} at RPAV in Voltage Setpoint Mode

Method 2: Measuring I_{MPD} Across a Sense Resistor

The second method has the advantage of providing a valid I_{MPD} reading at all times, but has the disadvantage of requiring a differential measurement across a sense resistor directly in series with the I_{MPD}. As shown in Figure 32, a small resistor, Rx, is placed in series with the I_{MPD}. If the laser used in the design has a pinout where the monitor photodiode cathode and the lasers anode are not connected, a sense resistor, Rx, can be placed in series with the photodiode cathode and V_{CC}, as shown in Figure 33. When choosing the value of the resistor, the user must take into account the expected I_{MPD} value in normal operation. The resistor must be large enough to make a significant signal for the buffered ADC to read, but small enough not to cause a significant voltage reduction across the PAVSET to ground. The voltage across the sense resistor must not exceed 250 mV when the laser is in normal operation. It is recommended that a 10 pF capacitor be placed in parallel with the sense resistor.

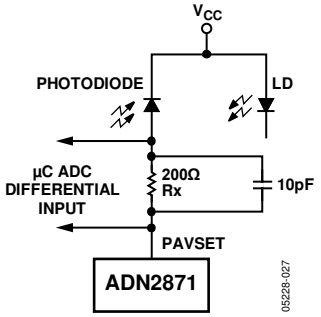


Figure 32. Differential Measurement of I_{MPD} Across a Sense Resistor

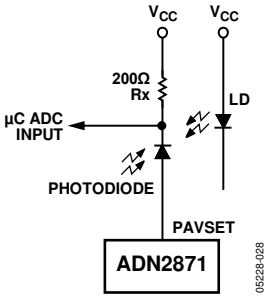


Figure 33. Single Measurement of I_{MPD} across a Sense Resistor

Resistor Setpoint

In resistor setpoint calibration, the current through the resistor from PAVSET to ground is the I_{MPD} current. The recommended method for measuring the I_{MPD} current is to place a small resistor in series with the PAVSET resistor (or potentiometer) and measure the voltage across this resistor, as shown in Figure 34. The I_{MPD} current is then equal to this voltage divided by the value of resistor used. In resistor setpoint calibration, PAVSET is held to 1.2 V nominal; it is recommended that the sense resistor be selected so that the voltage across the sense resistor does not exceed 250 mV.

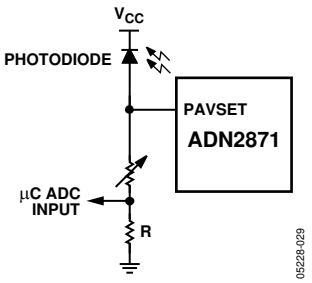


Figure 34. Single Measurement of I_{MPD} Across a Sense Resistor in Resistor Setpoint I_{MPD} Monitoring

LOOP BANDWIDTH SELECTION

To ensure that the ADN2871 control loop has sufficient bandwidth, the average power loop capacitor (PAVCAP) is calculated using the laser slope efficiency (watts/amps) and the average power required.

For resistor setpoint control:

$$PAVCAP = 3.2 \times 10^{-6} \times \frac{LI}{P_{AV}} \quad \text{(Farad)}$$

For voltage setpoint control:

$$PAVCAP = 1.28 \times 10^{-6} \times \frac{LI}{P_{AV}} \quad \text{(Farad)}$$

where:
P_{AV} is the average power required (mW).
LI is the typical slope efficiency at 25°C of a batch of lasers that are used in a design (mW/mA).

LI can be calculated as

$$LI = \frac{P1 - P0}{I_{MOD}} \quad \text{(mW/mA)}$$

where:
P1 is the optical power at the one level (mW).
P0 is the optical power at the zero level (mW).

The capacitor value equation gets a centered value for the particular type of laser that is used in a design and an average power setting. The laser LI not defined anywhere can vary by a factor of 7 between different physical lasers of the same type and across temperatures without the need to recalculate the PAVCAP value.

This capacitor is placed between the PAVCAP pin and ground. It is important that the capacitor is a low leakage, multilayer ceramic type with an insulation resistance greater than 100 GΩ or a time constant of 1000 seconds, whichever is less. Pick a standard off-the-shelf capacitor value such that the actual capacitance is within ±30% of the calculated value after the capacitor's own tolerance is taken into account.

POWER CONSUMPTION

The ADN2871 die temperature must be kept below 125°C. The LFCSP has an exposed paddle, which must be connected so that it is at the same potential as the ADN2871 ground pins. Power consumption can be calculated as

$$I_{CC} = I_{CC}\ typ + 0.3\ I_{MOD}$$
$$P = V_{CC} \times I_{CC} + (I_{BIAS} \times V_{BIAS\_PIN}) + I_{MOD}\ (V_{MODP\_PIN} + V_{MODN\_PIN})/2$$
$$T_{DIE} = T_{AMBIENT} + \theta_{JA} \times P$$

Thus, the maximum combination of I_{BIAS} + I_{MOD} must be calculated, where:
I_{CC} *typ* = 32 mA, the typical value of I_{CC} provided in Table 1 with $I_{BIAS} = I_{MOD} = 0$.
T_{DIE} is the die temperature.
$T_{AMBIENT}$ is the ambient temperature.
V_{BIAS_PIN} is the voltage at the IBIAS pin.
V_{MODP_PIN} is the voltage at the IMODP pin.
V_{MODN_PIN} is the voltage at the IMODN pin.

AUTOMATIC LASER SHUTDOWN (Tx_DISABLE)

ALS (Tx_DISABLE) is an input that shuts down the transmitter's optical output. The ALS pin is pulled up internally with a 6 kΩ resistor and conforms to SFP MSA specifications. When ALS is logic high or when open, both the bias and modulation currents are turned off. If an alarm has triggered, and the bias and modulation currents are turned off, ALS can be brought high and then low to clear the alarm.

BIAS AND MODULATION MONITOR CURRENTS

IBMON and IMMON are current-controlled current sources that mirror a ratio of the bias and modulation current. The monitor bias current (IBMON) and the monitor modulation current (IMMON) must both be connected to ground through a resistor to provide a voltage proportional to the bias current and modulation current, respectively. When using a microcontroller, the voltage developed across these resistors can be the input to two of the ADC channels, making available a digital representation of the bias and modulation current.

DATA INPUTS

Data inputs must be ac-coupled (10 nF capacitors are recommended) and are terminated via a 100 Ω internal resistor between the DATAP and DATAN pins. A high impedance circuit sets the common-mode voltage and is designed to allow maximum input voltage headroom over temperature. It is necessary to use ac coupling to eliminate the need for matching between common-mode voltages.

LASER DIODE INTERFACING

Figure 35 shows the recommended circuit for interfacing the ADN2871 to most TO-Can or coax lasers. DFB and FP lasers typically have impedances of 5 Ω to 7 Ω and have axial leads. The circuit shown works over the full range of data rates from 155 Mbps to 3.3 Gbps, including multirate operation (with no change to PAVCAP and ERCAP values); see Figure 23, Figure 24, and Figure 25section for multirate performance examples. Coax lasers have special characteristics that make them difficult to interface to. They tend to have higher inductance, and their impedance is not well controlled. The circuit in Figure 35 operates by deliberately misterminating the transmission line on the laser side while providing a very high quality matching network on the driver side.

The impedance of the driver side matching network is very flat in comparison to frequency and enables multirate operation. A series damping resistor must not be used.

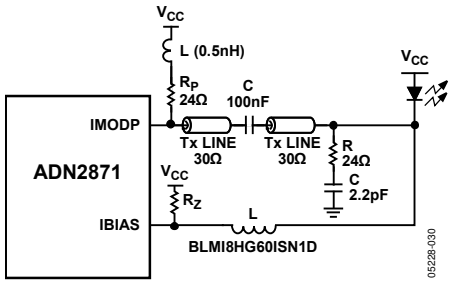


Figure 35. Recommended Interface for ADN2871 AC Coupling

The 30 Ω transmission line used is a compromise between drive current required and the total power consumed. Other transmission line values can be used, with some modification of the component values. In Figure 35, the R and C snubber values, 24 Ω and 2.2 pF respectively, represent a starting point and must be tuned for the particular model of laser being used. R_P, the pull-up resistor, is in series with a very small (0.5 nH) inductor. In some cases, an inductor is not required or can be accommodated with deliberate parasitic inductance, such as a thin trace or a via placed on the PC board.

Take care to mount the laser as close as possible to the PC board, minimizing the exposed lead length between the laser can and the edge of the board. The axial lead of a coax laser is very inductive (approximately 1 nH per mm). Long exposed leads result in slower edge rates and reduced eye margin.

Recommended component layouts and Gerber files are available by contacting Sales at Analog Devices. Note that the circuit in Figure 35 can supply up to 56 mA of modulation current to the laser, sufficient for most lasers available today. Higher currents can be accommodated by changing transmission lines and backmatch values. Contact Sales for recommendations. This interface circuit is not recommended for butterfly-style lasers or other lasers with 25 Ω characteristic impedance. Instead, a 25 Ω transmission line and inductive (instead of resistive) pull-up is recommended.

The ADN2871 single-ended application shown in Figure 35 is recommended for use up to 2.7 Gbps. From 2.7 Gbps to 4.25 Gbps, a differential drive is recommended when driving VCSELs or lasers that have slow fall times. Differential drive can be implemented by adding a few extra components. A possible implementation is shown in Figure 36. The bias and modulation currents that are programmed into the ADN2871 need to be larger than the bias and modulation current required at the laser due to the laser ac coupling interface and because some modulation current flows in pull-up Resistors R1 and R2.

In both circuits shown in Figure 35 and Figure 36, Resistor R_Z is required to achieve optimum eye quality. The recommended R_Z value is approximately 200 Ω ~ 500 Ω.

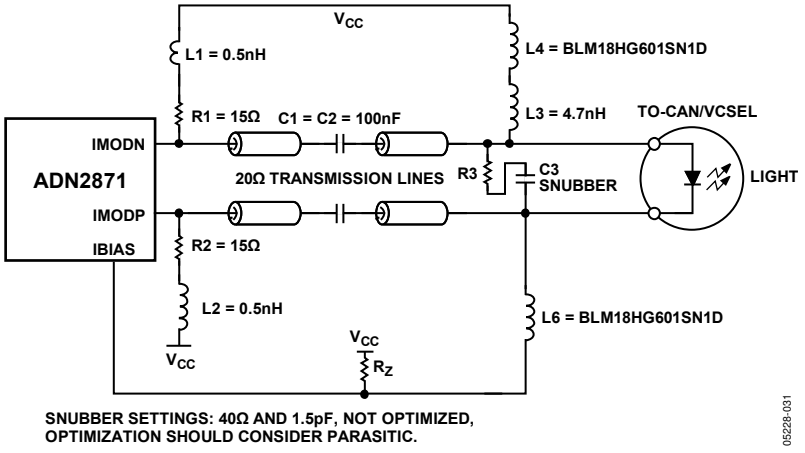


Figure 36. Recommended Differential Drive Circuit

ALARMS

The ADN2871 has a latched, active high monitoring alarm (FAIL). The FAIL alarm output is an open drain in conformance to SFP MSA specification requirements.

The ADN2871 has a three-fold alarm system that covers

- Use of a bias current higher than expected, most likely as a result of laser aging.
- Out-of-bounds average voltage at the monitor photodiode (MPD) input, indicating an excessive amount of laser power or a broken loop.
- Undervoltage in the IBIAS node (laser diode cathode) that increases the laser power.

The bias current alarm trip point is set by selecting the value of resistor on the IBMON pin to GND. The alarm is triggered when the voltage on the IBMON pin goes above 1.2 V. FAIL is activated when the single-point faults in Table 5 occur.

The circuit in Figure 37 can indicate that FAIL has been activated while allowing the bias and modulation currents to remain on. The transistor's V_{BE} clamps the FAIL voltage to below 1.3 V disabling the automatic shutdown of bias and modulation currents. If an alarm has triggered and FAIL is activated, ALS can be brought high and then low to clear the alarm.

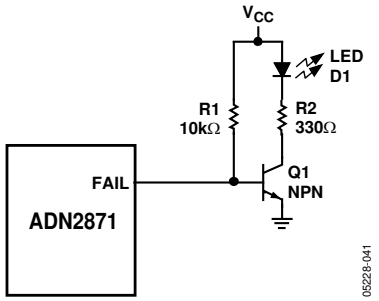


Figure 37. FAIL Indication Circuit

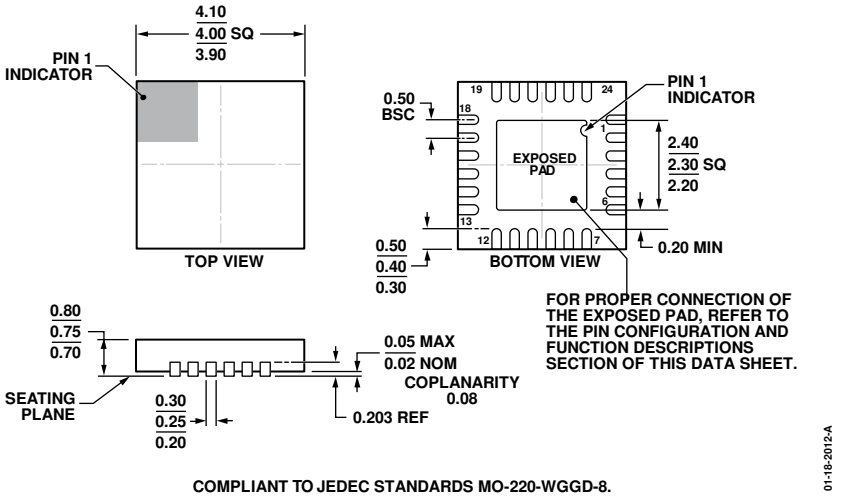
Table 5. ADN2871 Single-Point Alarms

Alarm Type	Mnemonic	Overvoltage or Short to V_{CC} Condition	Undervoltage or Short to GND Condition
Bias Current	IBMON	Alarm if > 1.2 V typical (±10% tolerance)	Ignore
MPD Current	PAVSET	Alarm if > threshold (typical threshold: 1.5 V to 2.1 V)	Alarm, if < threshold (typical threshold: 0.6 V to 1.1 V)
Crucial Nodes	ERREF (the ERRREF designed tied to V_{CC} in resistor setting mode)	Alarm if shorted to V_{CC} (the alarm is valid for voltage setting mode only)	Ignore
	IBIAS	Ignore	Alarm, if shorted to GND

Table 6. ADN2871 Response to Various Single-Point Faults in AC-Coupled Configuration (as shown in Figure 35)

Pin	Short to V_{CC}	Short to GND	Open
CCBIAS	Fault state occurs	Fault state occurs	Does not increase laser average power
PAVSET	Fault state occurs	Fault state occurs	Fault state occurs
PAVREF	Voltage mode: Fault state occurs	Fault state occurs	Fault state occurs
	Resistor mode: Tied to V_{CC}		Circuit designed to tie to V_{CC} in resistor setting mode, so no open case
RPAV	Voltage mode: Fault state occurs	Fault state occurs	Voltage mode: Fault state occurs
	Resistor mode: Tied to V_{CC}		Resistor mode: Does not increase average power
PAVCAP	Fault state occurs	Fault state occurs	Fault state occurs
DATAP	Does not increase laser average power	Does not increase laser average power	Does not increase laser average power
DATAN	Does not increase laser average power	Does not increase laser average power	Does not increase laser average power
ALS	Output currents shut off	Normal currents	Output currents shut off
ERSET	Does not increase laser average power	Does not increase laser average power	Does not increase laser average power
IMMON	Does not affect laser power	Does not increase laser average power	Does not increase laser average power
ERREF	Voltage mode: Fault state occurs	Voltage mode: Does not increase average power	Does not increase laser average power
	Resistor mode: Tied to V_{CC}	Resistor mode: Fault state occurs	
IBMON	Fault state occurs	Does not increase laser average power	Does not increase laser average power
FAIL	Fault state occurs	Does not increase laser average power	Does not increase laser average power
IMODP	Does not increase laser average power	Does not increase laser average power	Does not increase laser average power
IMODN	Does not increase laser average power	Does not increase laser average power	Does not increase laser power
IBIAS	Fault state occurs	Fault state occurs	Fault state occurs

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8.

Figure 38. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADN2871ACPZ	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-14
ADN2871ACPZ-RL7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-14

[1] Z = RoHS Compliant Part.

NOTES

D05228-0-1/17(B)