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4.25 Gbps 40 × 40 Digital Crosspoint Switch

Data Sheet

ADN4605

FEATURES

- DC to 4.25 Gbps per port NRZ data rate
- Adjustable receive equalization
  - 3 dB, 6 dB, or 12 dB boost
  - Compensates over 40 inches of FR4 at 4.25 Gbps
- Adjustable transmit preemphasis/deemphasis
  - Programmable boost and output level
  - Compensates over 40 inches of FR4 at 4.25 Gbps
- Low power
  - 105 mW per channel at 2.5 V (400 mV p-p differential output level swing)
- 40 × 40, fully differential, nonblocking array
  - Double rank connection programming with dual maps
- Low jitter, typically <25 ps
- Flexible 2.5 V to 3.3 V supply range
- DC- or ac-coupled differential PECL/CML inputs
- Differential CML outputs
- Per-lane polarity inversion for routing ease
- 50 Ω on-chip I/O termination with disable feature
- Supports 8b10b, scrambled or uncoded NRZ data
- Serial (I²C slave or SPI) control interface
- Parallel control interface

APPLICATIONS

- Digital video (HDMI, DVI, DisplayPort, 3G/HD/SD-SDI)
- Fiber optic network switching
- High speed serial backplane routing to OC-48 with FEC
- XAUI, 4x Fibre Channel, Infiniband®, and GbE over backplane
- Data storage networks

FUNCTIONAL BLOCK DIAGRAM

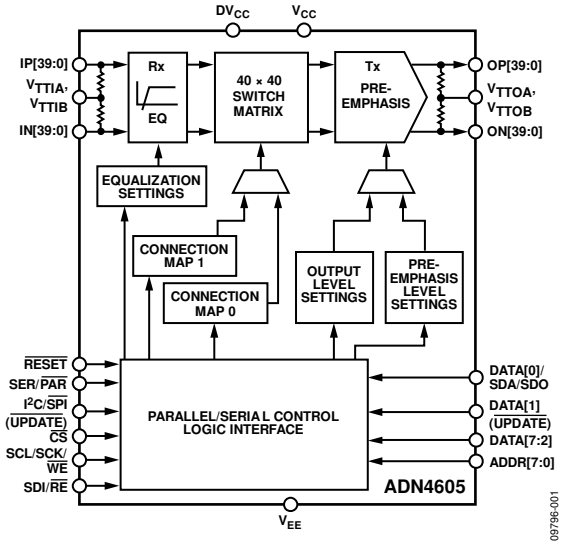

Figure 1.

GENERAL DESCRIPTION

The ADN4605 is a 40 × 40 asynchronous, protocol agnostic, digital crosspoint switch, with 40 differential PECL/CML-compatible inputs and 40 differential programmable CML outputs.

The ADN4605 is optimized for NRZ signaling with data rates of up to 4.25 Gbps per port. Each port offers adjustable levels of input equalization, programmable output swing, and output preemphasis/deemphasis.

The ADN4605 nonblocking switch core implements a 40 × 40 crossbar and supports independent channel switching through serial and parallel control interfaces. The ADN4605 has low latency and very low channel-to-channel skew.

An I²C, SPI, or parallel interface is used to communicate with the device for control of connectivity and other features.

The ADN4605 is assembled in a 35 mm × 35 mm, 352 BGA package and operates over a temperature range of −40°C to +85°C.

Rev. A

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ADN4605* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADN4605 Evaluation Board

DOCUMENTATION

Data Sheet

- ADN4605: 4.25 Gbps 40 x 40 Digital Crosspoint Switch Data Sheet

DESIGN RESOURCES

- ADN4605 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADN4605 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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REVISION HISTORY

11/11—Rev. 0 to Rev. A

Changes to Printed Circuit Board (PCB) Layout Guidelines ... 54
Removed Figure 55, Renumbered Sequentially ... 54

6/11—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{CC} = 2.5 V, V_{TTIx} = 2.5 V, V_{TTOx} = 2.5 V, DV_{CC} = 3.3 V, V_{EE} = 0 V, R_L = 50 Ω, output level (OLEV) = 4 (16 mA), preemphasis (PE) = 0 (0 dB), equalizer (EQ) = 1 (3 dB), data rate = 4.25 Gbps (PRBS7 data pattern), ac-coupled inputs and outputs, differential input swing = 800 mV p-p, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Data Rate (DR) per Channel (NRZ)		dc		4.25	Gbps
Deterministic Jitter	Data rate ≤ 4.25 Gbps, no channel		20		ps p-p
Random Jitter	RMS, no channel		0.8		ps rms
Residual Deterministic Jitter with Receive Equalization	Data rate = 4.25 Gbps, 20 in. FR4, EQ boost = 12 dB		14		ps p-p
	Data rate = 4.25 Gbps, 30 in. FR4, EQ boost = 12 dB		15		ps p-p
	Data rate = 4.25 Gbps, 40 in. FR4, EQ boost = 12 dB		25		ps p-p
Residual Deterministic Jitter with Transmit Preemphasis	Data rate = 4.25 Gbps, 20 in. FR4, PE boost = 5.6 dB		22		ps p-p
	Data rate = 4.25 Gbps, 30 in. FR4, PE boost = 6.8 dB		28		ps p-p
	Data rate = 4.25 Gbps, 40 in. FR4, PE boost = 9.5 dB		32		ps p-p
Propagation Delay	Input to output		920		ps
Channel-to-Channel Skew	Earliest input/output lane to latest input/output lane		200		ps
Switching Time	Update logic switching to 50% output data		20		ns
Output Rise/Fall Time	20% to 80%		108		ps
INPUT CHARACTERISTICS					
Minimum Differential Input Voltage Swing[1]	$V_{ICM} = V_{CC} - 0.6$ V		50		mV p-p diff
Maximum Differential Input Voltage Swing[1]	$V_{ICM} = V_{CC} - 0.6$ V		2000		mV p-p diff
Input Voltage Range	Single-ended absolute voltage level, V_L	V_{EE} + 1.0			V
	Single-ended absolute voltage level, V_H			V_{CC} + 0.3	V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Differential, PE boost = 0 dB, default output level, at dc	670	800	875	mV p-p diff
Output Voltage Range	Single-ended absolute voltage level, V_L		V_{CC} – 1.4		V
	Single-ended absolute voltage level, V_H		V_{CC} + 0.3		V
Per-Port Output Current	PE boost = 0 dB, default output level		16		mA
	PE boost = 6 dB, default output level		32		mA
TERMINATION CHARACTERISTICS					
Resistance	Differential, $V_{CC} = V_{MIN}$ to V_{MAX}, $T_A = T_{MIN}$ to T_{MAX}	88	100	114	Ω
Temperature Coefficient			0.015		Ω/°C
POWER SUPPLY					
Operating Range					
V_{CC}	V_{EE} = 0 V	2.25	2.5	3.6	V
DV_{CC}	V_{EE} = 0 V	3.0	3.3	3.6	V
V_{TTIA}, V_{TTIB}	V_{EE} = 0 V		2.5	V_{CC} + 0.3	V
V_{TTOA}, V_{TTOB}	V_{EE} = 0 V		2.5	V_{CC} + 0.3	V
Supply Current	Inputs/outputs disabled (reset condition)				
I_{CC}			55	64	mA
I_{DVCC}			0.3	1.1	mA
I_{TTIA} + I_{TTIB}	Inputs floating		0	1.5	mA
I_{TTOA}+ I_{TTOB}	Outputs floating		0	1.5	mA

Parameter	Conditions	Min	Typ	Max	Unit
Supply Current	All outputs enabled, ac-coupled I/O, 200 mV I/O swings (400 mV p-p differential), PE boost = 0 dB, 50 Ω far-end terminations				
I_{CC}			1320	1410	mA
I_{DVCC}			0.3	1.1	mA
$I_{TTIA} + I_{TTIB}$			11	15	mA
$I_{TTOA} + I_{TTOB}$			335	360	mA
Supply Current	All outputs enabled, ac-coupled I/O, 400 mV I/O swings (800 mV p-p differential), PE boost = 0 dB, 50 Ω far-end terminations				
I_{CC}			1370	1460	mA
I_{DVCC}			0.3	1.1	mA
$I_{TTIA} + I_{TTIB}$			11	15	mA
$I_{TTOA} + I_{TTOB}$			665	715	mA
Supply Current	All outputs enabled, ac-coupled I/O, 400 mV I/O swings (800 mV p-p differential), PE boost = 6 dB, 50 Ω far-end terminations				
I_{CC}			1850	1960	mA
I_{DVCC}			0.3	1.1	mA
$I_{TTIA} + I_{TTIB}$			11	15	mA
$I_{TTOA} + I_{TTOB}$			1340	1380	
THERMAL CHARACTERISTICS					
Operating Temperature[2]		−40		+85	°C
θ_{JA}	Still air; JEDEC multilayer test board		11.6		°C/W
θ_{JB}	1 m/s air velocity		5.4		°C/W
θ_{JC}	1 m/s air velocity		0.72		°C/W
LOGIC CHARACTERISTICS					
Input High Voltage Threshold (V_{IH})	DV_{CC} = 3.3 V	0.7 × DV_{CC}			V
Input Low Voltage Threshold (V_{IL})	DV_{CC} = 3.3 V			0.25 × DV_{CC}	V
Output High Voltage (V_{OH})	I_{OH} = −3 mA (I^2C/SPI mode only)	0.75 × DV_{CC}		DV_{CC}	V
Output Low Voltage (V_{OL})	I_{OL} = +3 mA	V_{EE}		0.4	V

[1] V_{ICM} is the input common-mode voltage.
[2] Junction temperature cannot exceed 125°C (see the Absolute Maximum Ratings section).

I²C TIMING SPECIFICATIONS

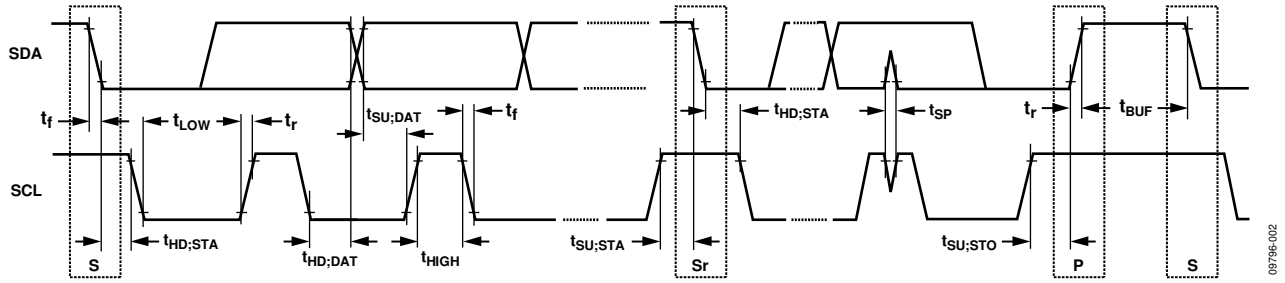

Figure 2. I²C Timing Diagram

Table 2. I²C Timing Specifications

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{SCL}	0	500+	kHz
Hold Time for a Start Condition	$t_{HD; STA}$	0.5		µs
Setup Time for a Repeated Start Condition	$t_{SU; STA}$	0.5		µs
Low Period of the SCL Clock	t_{LOW}		1.4	µs
High Period of the SCL Clock	t_{HIGH}	0.6		µs
Data Hold Time	$t_{HD; DAT}$	0.02		µs
Data Setup Time	$t_{SU; DAT}$	0.02		µs
Rise Time for Both SDA and SCL	t_r	1	300	ns
Fall Time for Both SDA and SCL	t_f	1	300	ns
Setup Time for Stop Condition	$t_{SU; STO}$	0.5		µs
Bus Free Time Between a Stop Condition and a Start Condition	t_{BUF}	1		ns
Bus Idle Time After a Reset		20		ns
Reset Pulse Width		20		ns

SPI TIMING SPECIFICATIONS

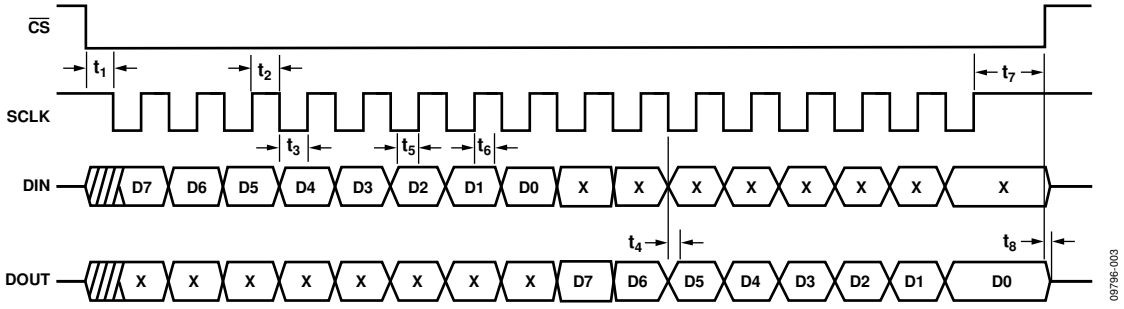

Figure 3. SPI Timing Diagram

Table 3. SPI Timing Specifications

Parameter	Symbol	Min	Max	Unit
SCK Clock Frequency	f_{SCK}		10	MHz
$\overline{CS}$ to SCLK Setup Time	t_1	0		ns
SCLK High Pulse Width	t_2	30		ns
SCLK Low Pulse Width	t_3	30		ns
Data Access Time After SCLK Falling Edge	t_4		45	ns
Data Setup Time Prior to SCLK Rising Edge	t_5	10		ns
Data Hold Time After SCLK Rising Edge	t_6	30		ns
$\overline{CS}$ to SCLK Hold Time	t_7	0		ns
$\overline{CS}$ to SDO High Impedance	t_8		45	ns
Reset Pulse Width		20		ns

PARALLEL MODE SPECIFICATIONS

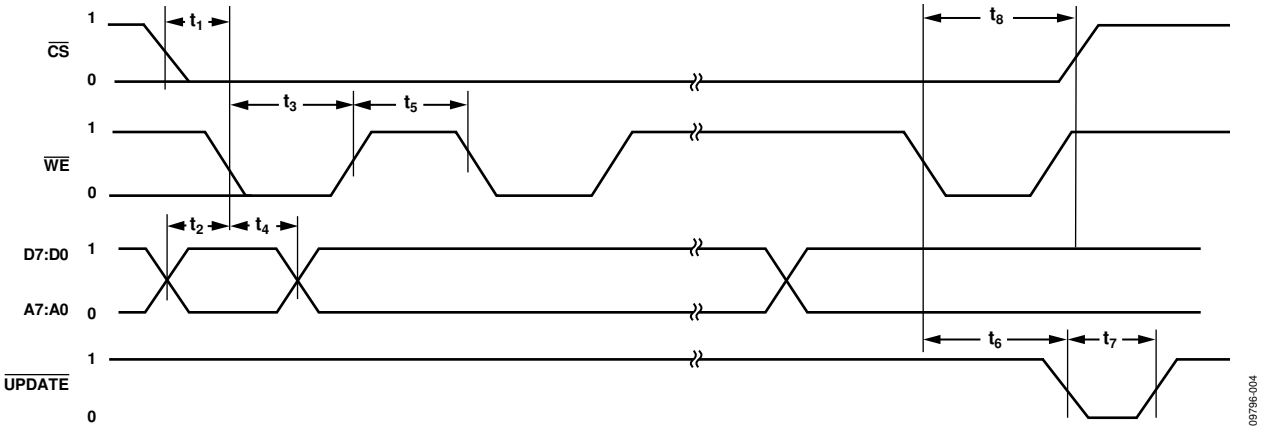

Figure 4. Parallel Mode Write Cycle

Table 4. Parallel Mode Write Cycle Timing Specifications

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Chip Select Setup Time	t_1	0			ns
Parallel Data Setup Time	t_2	0			ns
$\overline{WE}$ Pulse Width	t_3	30	50		ns
Parallel Data Hold Time	t_4	25			ns
$\overline{WE}$ Pulse Separation	t_5		25		ns
$\overline{WE}$ to $\overline{UPDATE}$ Delay	t_6		40		ns
$\overline{UPDATE}$ Pulse Width	t_7	30			ns
Chip Select Hold Time	t_8	0			ns
Reset Pulse Width		20			ns

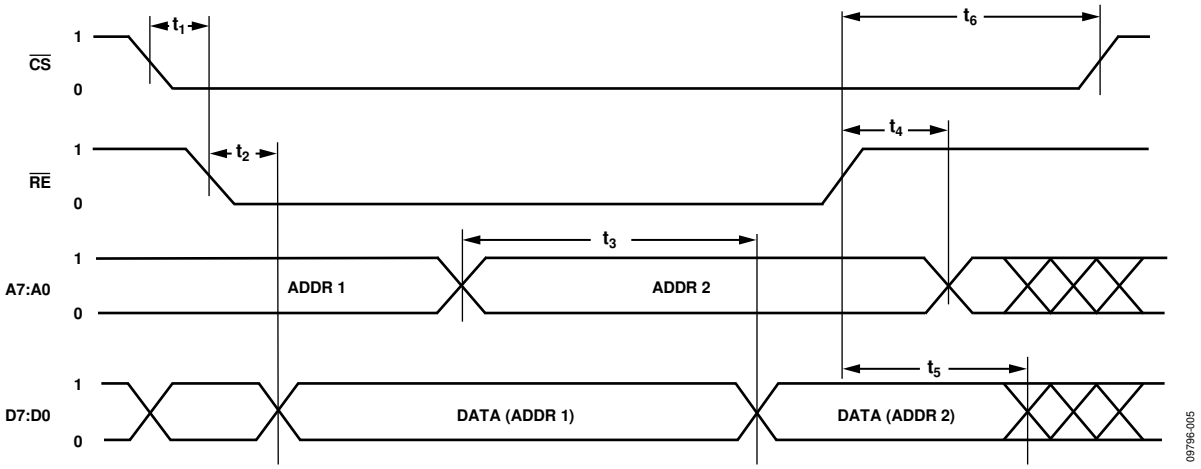

Figure 5. Parallel Mode Read Cycle

Table 5. Parallel Mode Read Cycle Timing Specifications

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Chip Select Setup Time	t_1	0			ns
Parallel $\overline{RE}$ Setup to Valid Time	t_2	10			ns
Data Access Time	t_3	25	50		ns
Address to $\overline{RE}$ Hold Time	t_4	25			ns
Data to $\overline{RE}$ Hold Time	t_5	25			ns
Chip Select Hold Time	t_6	5			ns

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
V_{CC} to V_{EE}	3.7 V
DV_{CC} to V_{EE}	3.7 V
V_{TTIA}, V_{TTIB}	V_{CC} + 0.6 V
V_{TTOA}, V_{TTOB}	V_{CC} + 0.6 V
Internal Power Dissipation[1]	8.4 W
Differential Input Voltage	2.0 V
Logic Input Voltage	V_{EE} − 0.3 V < V_{IN} < V_{CC} + 0.6 V
Storage Temperature Range	−65°C to +125°C
Junction Temperature	125°C

[1] Internal power dissipation is for the device in free air.
T_A = 27° C; θ_{JA} = 11.6°C/W in still air.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

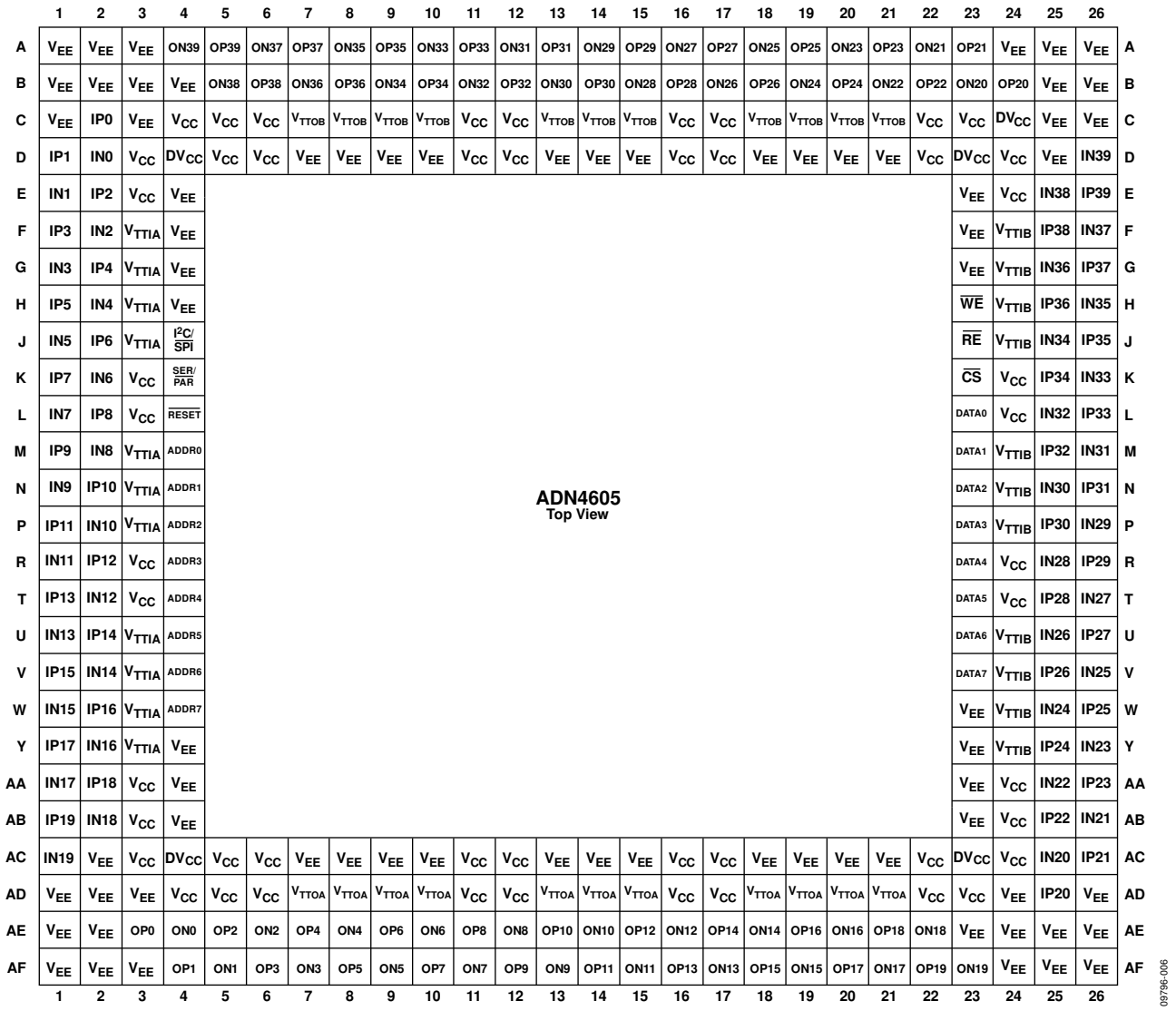

Figure 6. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
A1	V_{EE}	Power	Negative Supply.
A2	V_{EE}	Power	Negative Supply.
A3	V_{EE}	Power	Negative Supply.
A4	ON39	Output	High Speed Output Complement.
A5	OP39	Output	High Speed Output.
A6	ON37	Output	High Speed Output Complement.
A7	OP37	Output	High Speed Output.
A8	ON35	Output	High Speed Output Complement.
A9	OP35	Output	High Speed Output.
A10	ON33	Output	High Speed Output Complement.
A11	OP33	Output	High Speed Output.
A12	ON31	Output	High Speed Output Complement.
A13	OP31	Output	High Speed Output.
A14	ON29	Output	High Speed Output Complement.
A15	OP29	Output	High Speed Output.
A16	ON27	Output	High Speed Output Complement.
A17	OP27	Output	High Speed Output.
A18	ON25	Output	High Speed Output Complement.
A19	OP25	Output	High Speed Output.
A20	ON23	Output	High Speed Output Complement.
A21	OP23	Output	High Speed Output.
A22	ON21	Output	High Speed Output Complement.
A23	OP21	Output	High Speed Output.
A24	V_{EE}	Power	Negative Supply.
A25	V_{EE}	Power	Negative Supply.
A26	V_{EE}	Power	Negative Supply.
B1	V_{EE}	Power	Negative Supply.
B2	V_{EE}	Power	Negative Supply.
B3	V_{EE}	Power	Negative Supply.
B4	V_{EE}	Power	Negative Supply.
B5	ON38	Output	High Speed Output Complement.
B6	OP38	Output	High Speed Output.
B7	ON36	Output	High Speed Output Complement.
B8	OP36	Output	High Speed Output.
B9	ON34	Output	High Speed Output Complement.
B10	OP34	Output	High Speed Output.
B11	ON32	Output	High Speed Output Complement.
B12	OP32	Output	High Speed Output.
B13	ON30	Output	High Speed Output Complement.
B14	OP30	Output	High Speed Output.
B15	ON28	Output	High Speed Output Complement.
B16	OP28	Output	High Speed Output.
B17	ON26	Output	High Speed Output Complement.
B18	OP26	Output	High Speed Output.
B19	ON24	Output	High Speed Output Complement.
B20	OP24	Output	High Speed Output.
B21	ON22	Output	High Speed Output Complement.
B22	OP22	Output	High Speed Output.

Pin No.	Mnemonic	Type	Description
B23	ON20	Output	High Speed Output Complement.
B24	OP20	Output	High Speed Output.
B25	V_{EE}	Power	Negative Supply.
B26	V_{EE}	Power	Negative Supply.
C1	V_{EE}	Power	Negative Supply.
C2	IP0	Input	High Speed Input.
C3	V_{EE}	Power	Negative Supply.
C4	V_{CC}	Power	Positive Supply.
C5	V_{CC}	Power	Positive Supply.
C6	V_{CC}	Power	Positive Supply.
C7	V_{TTOB}	Power	Output Termination Supply (B). The V_{TTOB} pins are normally tied to the V_{TTOA} pins.
C8	V_{TTOB}	Power	Output Termination Supply (B). The V_{TTOB} pins are normally tied to the V_{TTOA} pins.
C9	V_{TTOB}	Power	Output Termination Supply (B). T The V_{TTOB} pins are normally tied to the V_{TTOA} pins.
C10	V_{TTOB}	Power	Output Termination Supply (B). The V_{TTOB} pins are normally tied to the V_{TTOA} pins.
C11	V_{CC}	Power	Positive Supply.
C12	V_{CC}	Power	Positive Supply.
C13	V_{TTOB}	Power	Output Termination Supply (B). The V_{TTOB} pins are normally tied to the V_{TTOA} pins.
C14	V_{TTOB}	Power	Output Termination Supply (B). The V_{TTOB} pins are normally tied to the V_{TTOA} pins.
C15	V_{TTOB}	Power	Output Termination Supply (B). The V_{TTOB} pins are normally tied to the V_{TTOA} pins.
C16	V_{CC}	Power	Positive Supply.
C17	V_{CC}	Power	Positive Supply.
C18	V_{TTOB}	Power	Output Termination Supply (B). The V_{TTOB} pins are normally tied to the V_{TTOA} pins.
C19	V_{TTOB}	Power	Output Termination Supply (B). The V_{TTOB} pins are normally tied to the V_{TTOA} pins.
C20	V_{TTOB}	Power	Output Termination Supply (B). The V_{TTOB} pins are normally tied to the V_{TTOA} pins.
C21	V_{TTOB}	Power	Output Termination Supply (B). The V_{TTOB} pins are normally tied to the V_{TTOA} pins.
C22	V_{CC}	Power	Positive Supply.
C23	V_{CC}	Power	Positive Supply.
C24	DV_{CC}	Power	Digital Positive Supply.
C25	V_{EE}	Power	Negative Supply.
C26	V_{EE}	Power	Negative Supply.
D1	IP1	Input	High Speed Input.
D2	IN0	Input	High Speed Input Complement.
D3	V_{CC}	Power	Positive Supply.
D4	DV_{CC}	Power	Digital Positive Supply.
D5	V_{CC}	Power	Positive Supply.
D6	V_{CC}	Power	Positive Supply.
D7	V_{EE}	Power	Negative Supply.
D8	V_{EE}	Power	Negative Supply.
D9	V_{EE}	Power	Negative Supply.
D10	V_{EE}	Power	Negative Supply.
D11	V_{CC}	Power	Positive Supply.
D12	V_{CC}	Power	Positive Supply.

Pin No.	Mnemonic	Type	Description
D13	V_{EE}	Power	Negative Supply.
D14	V_{EE}	Power	Negative Supply.
D15	V_{EE}	Power	Negative Supply.
D16	V_{CC}	Power	Positive Supply.
D17	V_{CC}	Power	Positive Supply.
D18	V_{EE}	Power	Negative Supply.
D19	V_{EE}	Power	Negative Supply.
D20	V_{EE}	Power	Negative Supply.
D21	V_{EE}	Power	Negative Supply.
D22	V_{CC}	Power	Positive Supply.
D23	DV_{CC}	Power	Digital Positive Supply.
D24	V_{CC}	Power	Positive Supply.
D25	V_{EE}	Power	Negative Supply.
D26	IN39	Input	High Speed Input Complement.
E1	IN1	Input	High Speed Input Complement.
E2	IP2	Input	High Speed Input.
E3	V_{CC}	Power	Positive Supply.
E4	V_{EE}	Power	Negative Supply.
E23	V_{EE}	Power	Negative Supply.
E24	V_{CC}	Power	Positive Supply.
E25	IN38	Input	High Speed Input Complement.
E26	IP39	Input	High Speed Input
F1	IP3	Input	High Speed Input
F2	IN2	Input	High Speed Input Complement.
F3	V_{TTIA}	Power	Input Termination Supply (A). The V_{TTIA} pins are normally tied to the V_{TTIB} pins.
F4	V_{EE}	Power	Negative Supply.
F23	V_{EE}	Power	Negative Supply.
F24	V_{TTIB}	Power	Input Termination Supply (B). The V_{TTIB} pins are normally tied to the V_{TTIA} pins.
F25	IP38	Input	High Speed Input.
F26	IN37	Input	High Speed Input Complement.
G1	IN3	Input	High Speed Input Complement.
G2	IP4	Input	High Speed Input.
G3	V_{TTIA}	Power	Input Termination Supply (A). The V_{TTIA} pins are normally tied to the V_{TTIB} pins.
G4	V_{EE}	Power	Negative Supply.
G23	V_{EE}	Power	Negative Supply.
G24	V_{TTIB}	Power	Input Termination Supply (B). The V_{TTIB} pins are normally tied to the V_{TTIA} pins.
G25	IN36	Input	High Speed Input Complement.
G26	IP37	Input	High Speed Input.
H1	IP5	Input	High Speed Input.
H2	IN4	Input	High Speed Input Complement.
H3	V_{TTIA}	Power	Input Termination Supply (A). The V_{TTIA} pins are normally tied to the V_{TTIB} pins.
H4	V_{EE}	Power	Negative Supply.
H23	$\overline{WE}$/SCL/SCK	Control	Parallel control interface: First-Rank Write Strobe ($\overline{WE}$) Active Low. I^2C Control Interface: I^2C Clock (SCL). SPI Control Interface: SPI Clock (SCK).
H24	V_{TTIB}	Power	Input Termination Supply (B). The V_{TTIB} pins are normally tied to the V_{TTIA} pins.

Pin No.	Mnemonic	Type	Description
H25	IP36	Input	High Speed Input.
H26	IN35	Input	High Speed Input Complement.
J1	IN5	Input	High Speed Input Complement.
J2	IP6	Input	High Speed Input.
J3	V_{TTIA}	Power	Input Termination Supply (A). The V_{TTIA} pins are normally tied to the V_{TTIB} pins.
J4	$I^2C/\overline{SPI}/\overline{UPDATE}$	Control	I^2C Control Interface Selection (I^2C). SPI Control Interface Selection ($\overline{SPI}$) Active Low. Parallel Control Interface ($\overline{UPDATE}$) Active Low.
J23	$\overline{RE}$/SDI	Control	Parallel Control Interface: Read Strobe ($\overline{RE}$) Active Low. SPI Control Interface: Data Input (SDI) SPI Control.
J24	V_{TTIB}	Power	Input Termination Supply (B). The V_{TTIB} pins are normally tied to the V_{TTIA} pins.
J25	IN34	Input	High Speed Input.
J26	IP35	Input	High Speed Input Complement.
K1	IP7	Input	High Speed Input.
K2	IN6	Input	High Speed Input Complement.
K3	V_{CC}	Power	Power Supply.
K4	SER/$\overline{PAR}$	Control	Serial Control Interface Selection (SER). Parallel Control Interface Selection ($\overline{PAR}$) Active Low.
K23	$\overline{CS}$	Control	Chip Select Active Low.
K24	V_{CC}	Power	Positive Supply.
K25	IP34	Input	High Speed Input.
K26	IN33	Input	High Speed Input Complement.
L1	IN7	Input	High Speed Input Complement.
L2	IP8	Input	High Speed Input.
L3	V_{CC}	Power	Positive Supply.
L4	$\overline{RESET}$	Control	Configuration Registers: Reset (Active Low). This pin is normally pulled up to DV_{CC}.
L23	DATA0/SDA/SDO	Control	Parallel Control Interface: Register Data Bit 0 (DATA0). I^2C Control Interface: Data In (SDA). SPI Control Interface: Data Out (SDO).
L24	V_{CC}	Power	Positive Supply.
L25	IN32	Input	High Speed Input Complement.
L26	IP33	Input	High Speed Input.
M1	IP9	Input	High Speed Input.
M2	IN8	Input	High Speed Input Complement.
M3	V_{TTIA}	Power	Input Termination Supply (A). The V_{TTIA} pins are normally tied to the V_{TTIB} pins.
M4	ADDR0	Control	Parallel Control Interface: Register Address Bit 0. I^2C Control Interface: Slave Address Bit 0.
M23	DATA1/$\overline{UPDATE}$	Control	Parallel Control Interface: Register (DATA1). Data Bit 1. I^2C or SPI Serial Control Interface ($\overline{UPDATE}$). Active Low.
M24	V_{TTIB}	Power	Input Termination Supply (B). The V_{TTIB} pins are normally tied to the V_{TTIA} pins.
M25	IP32	Input	High Speed Input
M26	IN31	Input	High Speed Input Complement.
N1	IN9	Input	High Speed Input Complement.
N2	IP10	Input	High Speed Input.
N3	V_{TTIA}	Power	Input Termination Supply (A). The V_{TTIA} pins are normally tied to the V_{TTIB} pins.
N4	ADDR1	Control	Parallel Control Interface: Register Address Bit 1. I^2C Control Interface: Slave Address Bit 1.

Pin No.	Mnemonic	Type	Description
N23	DATA2	Control	Parallel Control Interface: Register Data Bit 2.
N24	V_{TTIB}	Power	Input Termination Supply (B). The V_{TTIB} pins are normally tied to the V_{TTIA} pins.
N25	IN30	Input	High Speed Input Complement.
N26	IP31	Input	High Speed Input.
P1	IP11	Input	High Speed Input.
P2	IN10	Input	High Speed Input Complement.
P3	V_{TTIA}	Power	Input Termination Supply (A). The V_{TTIA} pins are normally tied to the V_{TTIB} pins.
P4	ADDR2	Control	Parallel Control Interface: Register Address Bit 2. I^2C Control Interface: Slave Address Bit 2.
P23	DATA3	Control	Parallel Control Interface: Register Data Bit 3.
P24	V_{TTIB}	Power	Input Termination Supply (B). The V_{TTIB} pins are normally tied to the V_{TTIA} pins.
P25	IP30	Input	High Speed Input.
P26	IN29	Input	High Speed Input Complement.
R1	IN11	Input	High Speed Input Complement.
R2	IP12	Input	High Speed Input.
R3	V_{CC}	Power	Positive Supply.
R4	ADDR3	Control	Parallel Control Interface: Register Address Bit 3. I^2C Control Interface: Slave Address Bit 3.
R23	DATA4	Control	Parallel Control Interface: Register Data Bit 4.
R24	V_{CC}	Power	Positive Supply.
R25	IN28	Input	High Speed Input Complement.
R26	IP29	Input	High Speed Input.
T1	IP13	Input	High Speed Input.
T2	IN12	Input	High Speed Input Complement.
T3	V_{CC}	Power	Positive Supply.
T4	ADDR4	Control	Parallel Control Interface: Register Address Bit 4. I^2C Control Interface: Slave Address Bit 4.
T23	DATA5	Control	Parallel Control Interface: Register Data Bit 5.
T24	V_{CC}	Power	Positive Supply.
T25	IP28	Input	High Speed Input.
T26	IN27	Input	High Speed Input Complement.
U1	IN13	Input	High Speed Input Complement.
U2	IP14	Input	High Speed Input.
U3	V_{TTIA}	Power	Input Termination Supply (A). The V_{TTIA} pins are normally tied to the V_{TTIB} pins.
U4	ADDR5	Control	Parallel Control Interface: Register Address Bit 5. I^2C Control Interface: Slave Address Bit 5.
U23	DATA6	Control	Parallel Control Interface: Register Data Bit 6.
U24	V_{TTIB}	Power	Input Termination Supply (B). The V_{TTIB} pins are normally tied to the V_{TTIA} pins.
U25	IN26	Input	High Speed Input Complement.
U26	IP27	Input	High Speed Input.
V1	IP15	Input	High Speed Input.
V2	IN14	Input	High Speed Input Complement.
V3	V_{TTIA}	Power	Input Termination Supply (A). The V_{TTIA} pins are normally tied to the V_{TTIB} pins.
V4	ADDR6	Control	Parallel Control Interface: Register Address Bit 6. I^2C Control Interface: Slave Address Bit 6.
V23	DATA7	Control	Parallel Control Interface: Register Data Bit 7.

Pin No.	Mnemonic	Type	Description
V24	V_{TTIB}	Power	Input Termination Supply (B). The V_{TTIB} pins are normally tied to the V_{TTIA} pins.
V25	IP26	Input	High Speed Input.
V26	IN25	Input	High Speed Input Complement.
W1	IN15	Input	High Speed Input Complement.
W2	IP16	Input	High Speed Input.
W3	V_{TTIA}	Power	Input Termination Supply (A). The V_{TTIA} pins are normally tied to the V_{TTIB} pins.
W4	ADDR7	Control	Parallel Control Interface: Register Address Bit 7. I^2C Control Interface: Slave Address Bit 7.
W23	V_{EE}	Power	Negative Supply.
W24	V_{TTIB}	Power	Input Termination Supply (B). The V_{TTIB} pins are normally tied to the V_{TTIA} pins.
W25	IN24	Input	High Speed Input Complement.
W26	IP25	Input	High Speed Input.
Y1	IP17	Input	High Speed Input.
Y2	IN16	Input	High Speed Input Complement.
Y3	V_{TTIA}	Power	Input Termination Supply (A). The V_{TTIA} pins are normally tied to the V_{TTIB} pins.
Y4	V_{EE}	Power	Negative Supply.
Y23	V_{EE}	Power	Negative Supply.
Y24	V_{TTIB}	Power	Input Termination Supply (B). The V_{TTOB} pins are normally tied to the V_{TTIA} pins.
Y25	IP24	Input	High Speed Input.
Y26	IN23	Input	High Speed Input Complement.
AA1	IN17	Input	High Speed Input Complement.
AA2	IP18	Input	High Speed Input.
AA3	V_{CC}	Power	Positive Supply.
AA4	V_{EE}	Power	Negative Supply.
AA23	V_{EE}	Power	Negative Supply.
AA24	V_{CC}	Power	Positive Supply.
AA25	IN22	Input	High Speed Input Complement.
AA26	IP23	Input	High Speed Input.
AB1	IP19	Input	High Speed Input.
AB2	IN18	Input	High Speed Input Complement.
AB3	V_{CC}	Power	Positive Supply.
AB4	V_{EE}	Power	Negative Supply.
AB23	V_{EE}	Power	Negative Supply.
AB24	V_{CC}	Power	Positive Supply.
AB25	IP22	Input	High Speed Input.
AB26	IN21	Input	High Speed Input Complement.
AC1	IN19	Input	High Speed Input Complement.
AC2	V_{EE}	Power	Negative Supply.
AC3	V_{CC}	Power	Positive Supply.
AC4	DV_{CC}	Power	Digital Positive Supply.
AC5	V_{CC}	Power	Positive Supply.
AC6	V_{CC}	Power	Positive Supply.
AC7	V_{EE}	Power	Negative Supply.
AC8	V_{EE}	Power	Negative Supply.
AC9	V_{EE}	Power	Negative Supply.
AC10	V_{EE}	Power	Negative Supply.

Pin No.	Mnemonic	Type	Description
AC11	V_{CC}	Power	Positive Supply.
AC12	V_{CC}	Power	Positive Supply.
AC13	V_{EE}	Power	Negative Supply.
AC14	V_{EE}	Power	Negative Supply.
AC15	V_{EE}	Power	Negative Supply.
AC16	V_{CC}	Power	Positive Supply.
AC17	V_{CC}	Power	Positive Supply.
AC18	V_{EE}	Power	Negative Supply.
AC19	V_{EE}	Power	Negative Supply.
AC20	V_{EE}	Power	Negative Supply.
AC21	V_{EE}	Power	Negative Supply.
AC22	V_{CC}	Power	Positive Supply.
AC23	DV_{CC}	Power	Digital Positive Supply.
AC24	V_{CC}	Power	Positive Supply.
AC25	IN20	Input	High Speed Input Complement.
AC26	IP21	Input	High Speed Input.
AD1	V_{EE}	Power	Negative Supply.
AD2	V_{EE}	Power	Negative Supply.
AD3	V_{EE}	Power	Negative Supply.
AD4	V_{CC}	Power	Positive Supply.
AD5	V_{CC}	Power	Positive Supply.
AD6	V_{CC}	Power	Positive Supply.
AD7	V_{TTOA}	Power	Output Termination Supply (A). The V_{TTOA} pins are normally tied to the V_{TTOB} pins.
AD8	V_{TTOA}	Power	Output Termination Supply (A). The V_{TTOA} pins are normally tied to the V_{TTOB} pins.
AD9	V_{TTOA}	Power	Output Termination Supply (A). The V_{TTOA} pins are normally tied to the V_{TTOB} pins.
AD10	V_{TTOA}	Power	Output Termination Supply (A). The V_{TTOA} pins are normally tied to the V_{TTOB} pins.
AD11	V_{CC}	Power	Positive Supply.
AD12	V_{CC}	Power	Positive Supply.
AD13	V_{TTOA}	Power	Output Termination Supply (A). The V_{TTOA} pins are normally tied to the V_{TTOB} pins.
AD14	V_{TTOA}	Power	Output Termination Supply (A). The V_{TTOA} pins are normally tied to the V_{TTOB} pins.
AD15	V_{TTOA}	Power	Output Termination Supply (A). The V_{TTOA} pins are normally tied to the V_{TTOB} pins.
AD16	V_{CC}	Power	Positive Supply.
AD17	V_{CC}	Power	Positive Supply.
AD18	V_{TTOA}	Power	Output Termination Supply (A). The V_{TTOA} pins are normally tied to the V_{TTOB} pins.
AD19	V_{TTOA}	Power	Output Termination Supply (A). The V_{TTOA} pins are normally tied to the V_{TTOB} pins.
AD20	V_{TTOA}	Power	Output Termination Supply (A). The V_{TTOA} pins are normally tied to the V_{TTOB} pins.
AD21	V_{TTOA}	Power	Output Termination Supply (A). The V_{TTOA} pins are normally tied to the V_{TTOB} pins.
AD22	V_{CC}	Power	Positive Supply.
AD23	V_{CC}	Power	Positive Supply.
AD24	V_{EE}	Power	Negative Supply.
AD25	IP20	Input	High Speed Input.
AD26	V_{EE}	Power	Negative Supply.

Pin No.	Mnemonic	Type	Description
AE1	V_{EE}	Power	Negative Supply.
AE2	V_{EE}	Power	Negative Supply.
AE3	OP0	Output	High Speed Output.
AE4	ON0	Output	High Speed Output Complement.
AE5	OP2	Output	High Speed Output.
AE6	ON2	Output	High Speed Output Complement.
AE7	OP4	Output	High Speed Output.
AE8	ON4	Output	High Speed Output Complement.
AE9	OP6	Output	High Speed Output.
AE10	ON6	Output	High Speed Output Complement.
AE11	OP8	Output	High Speed Output.
AE12	ON8	Output	High Speed Output Complement.
AE13	OP10	Output	High Speed Output.
AE14	ON10	Output	High Speed Output Complement.
AE15	OP12	Output	High Speed Output.
AE16	ON12	Output	High Speed Output Complement.
AE17	OP14	Output	High Speed Output.
AE18	ON14	Output	High Speed Output Complement.
AE19	OP16	Output	High Speed Output.
AE20	ON16	Output	High Speed Output Complement.
AE21	OP18	Output	High Speed Output.
AE22	ON18	Output	High Speed Output Complement.
AE23	V_{EE}	Power	Negative Supply.
AE24	V_{EE}	Power	Negative Supply.
AE25	V_{EE}	Power	Negative Supply.
AE26	V_{EE}	Power	Negative Supply.
AF1	V_{EE}	Power	Negative Supply.
AF2	V_{EE}	Power	Negative Supply.
AF3	V_{EE}	Power	Negative Supply.
AF4	OP1	Output	High Speed Output.
AF5	ON1	Output	High Speed Output Complement.
AF6	OP3	Output	High Speed Output.
AF7	ON3	Output	High Speed Output Complement.
AF8	OP5	Output	High Speed Output.
AF9	ON5	Output	High Speed Output Complement.
AF10	OP7	Output	High Speed Output.
AF11	ON7	Output	High Speed Output Complement.
AF12	OP9	Output	High Speed Output.
AF13	ON9	Output	High Speed Output Complement.
AF14	OP11	Output	High Speed Output.
AF15	ON11	Output	High Speed Output Complement.
AF16	OP13	Output	High Speed Output.
AF17	ON13	Output	High Speed Output Complement.
AF18	OP15	Output	High Speed Output.
AF19	ON15	Output	High Speed Output Complement.
AF20	OP17	Output	High Speed Output.
AF21	ON17	Output	High Speed Output Complement.
AF22	OP19	Output	High Speed Output.

Pin No.	Mnemonic	Type	Description
AF23	ON19	Output	High Speed Output Complement.
AF24	V_{EE}	Power	Negative Supply.
AF25	V_{EE}	Power	Negative Supply.
AF26	V_{EE}	Power	Negative Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 2.5 V, V_{TTIx} = 2.5 V, V_{TTOx} = 2.5 V, DV_{CC} = 3.3 V, V_{EE} = 0 V, R_L = 50 Ω, output level (OLEV) = 4 (16 mA), preemphasis (PE) = 0 (0 dB), equalizer (EQ) = 1 (3 dB), data rate = 4.25 Gbps (PRBS7 data pattern), ac-coupled inputs and outputs, differential input swing = 800 mV p-p, T_A = 25°C, unless otherwise noted.

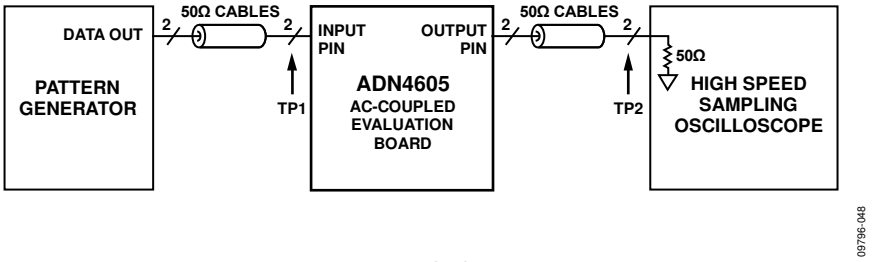

Figure 7. Standard Test Circuit

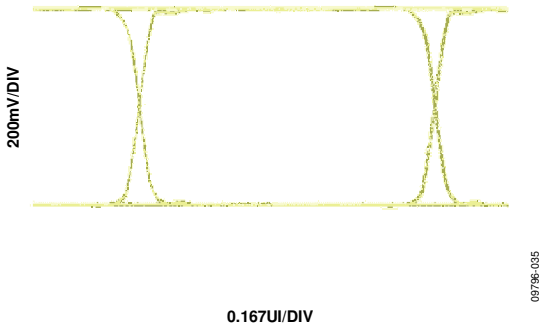

Figure 8. 3.25 Gbps Input Eye (TP1 from Figure 7)

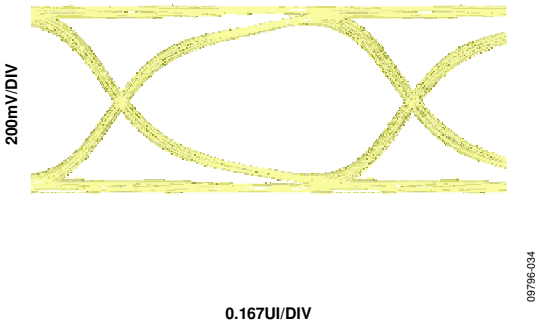

Figure 10. 3.25 Gbps Output Eye (TP2 from Figure 7)

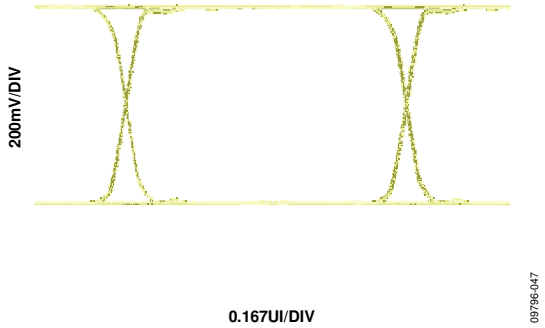

Figure 9. 4.25 Gbps Input Eye (TP1 from Figure 7)

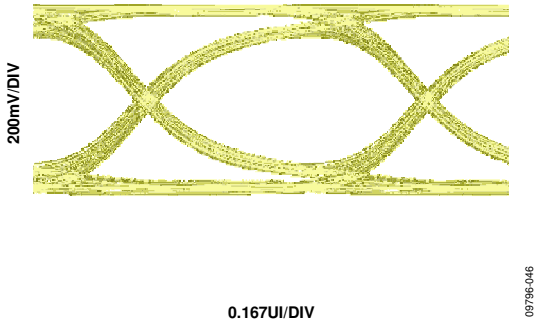

Figure 11. 4.25 Gbps Output Eye (TP2 from Figure 7)

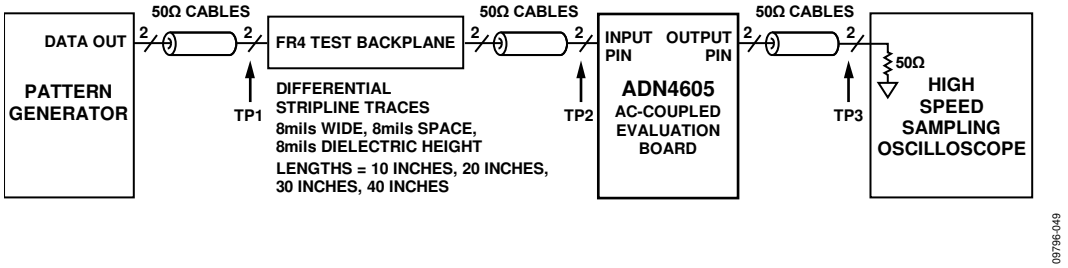

Figure 12. Equalization Test Circuit

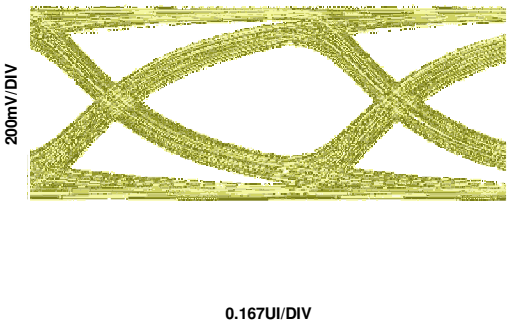

Figure 13. 4.25 Gbps Input Eye, 20 Inch FR4 Input Channel (TP2 from Figure 12)

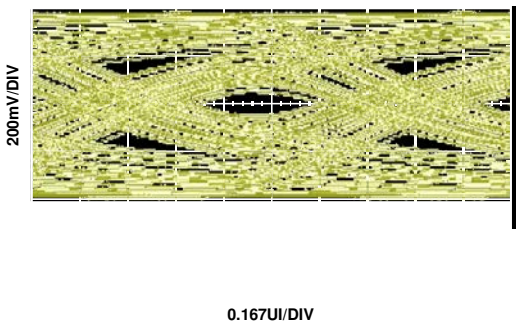

Figure 14. 4.25 Gbps Input Eye, 40-Inch FR4 Input Channel (TP2 from Figure 12)

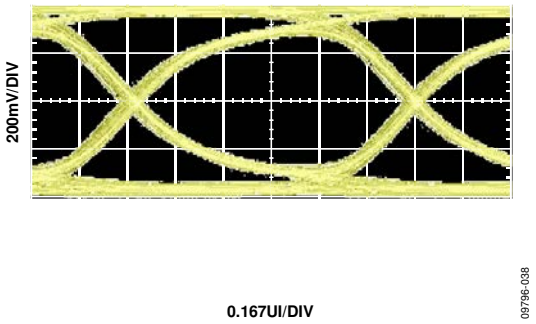

Figure 15. 4.25 Gbps Output Eye, 20-Inch FR4 Input Channel, EQ = 12 dB (TP3 from Figure 12)

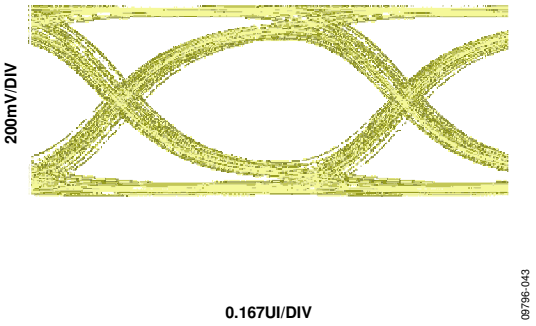

Figure 16. 4.25 Gbps Output Eye, 40-Inch FR4 Input Channel, EQ = 12 dB (TP3 from Figure 12)

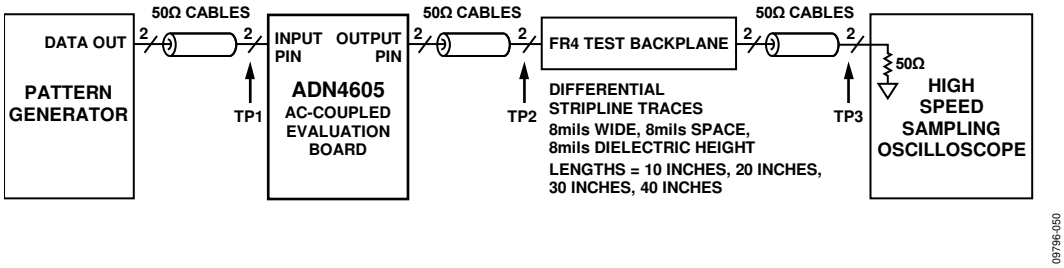

Figure 17. Preemphasis Test Circuit

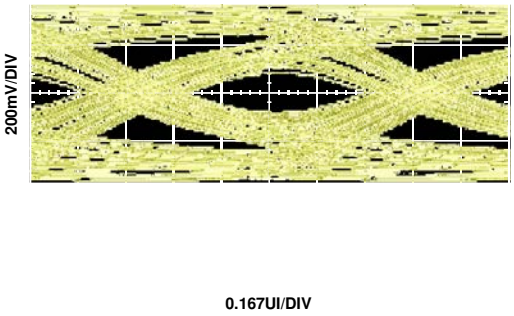

Figure 18. 4.25 Gbps Output Eye, 20-Inch FR4 Output Channel, PE = 0 dB (TP3 from Figure 17)

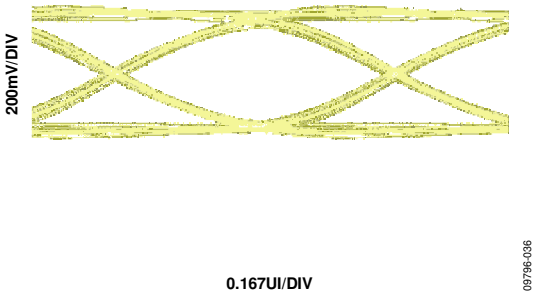

Figure 20. 4.25 Gbps Output Eye, 20-Inch FR4 Input Channel, PE = 5.6 dB (TP3 from Figure 17)

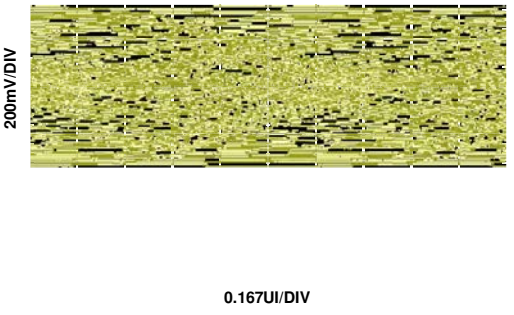

Figure 19. 4.25 Gbps Output Eye, 40-Inch FR4 Input Channel, PE = 0 dB (TP3 from Figure 17)

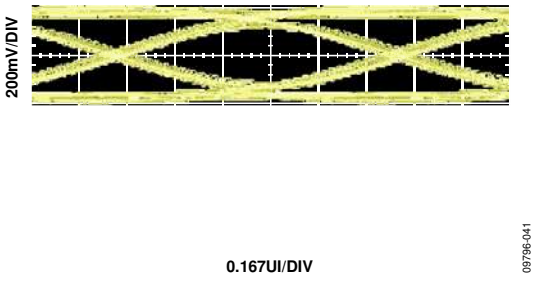

Figure 21. 4.25 Gbps Output Eye, 40-Inch FR4 Input Channel, PE = 9.5 dB (TP3 from Figure 17)

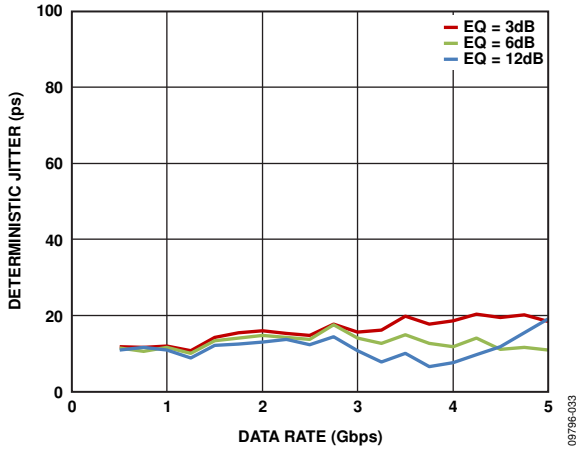

Figure 22. Deterministic Jitter vs. Data Rate

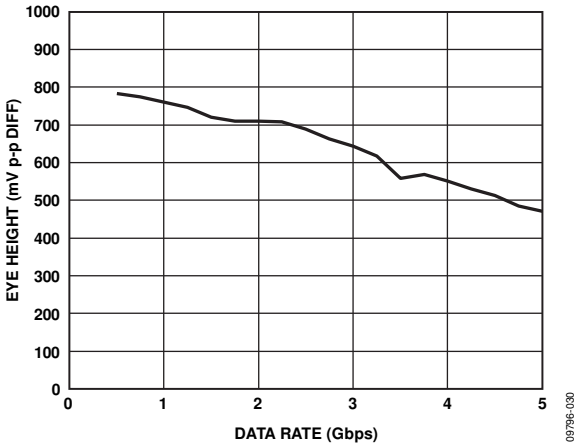

Figure 25. Eye Height vs. Data Rate

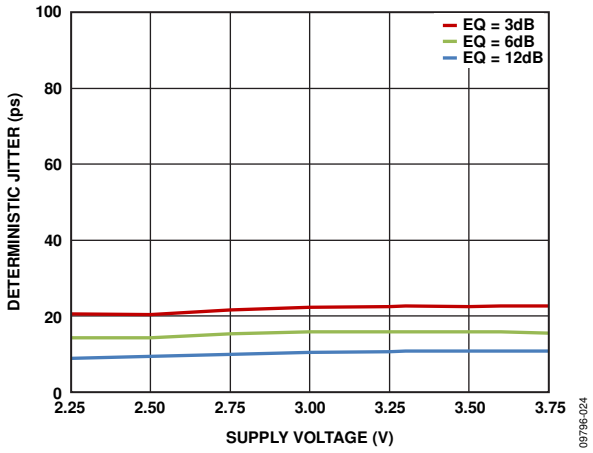

Figure 23. Deterministic Jitter vs. Supply Voltage

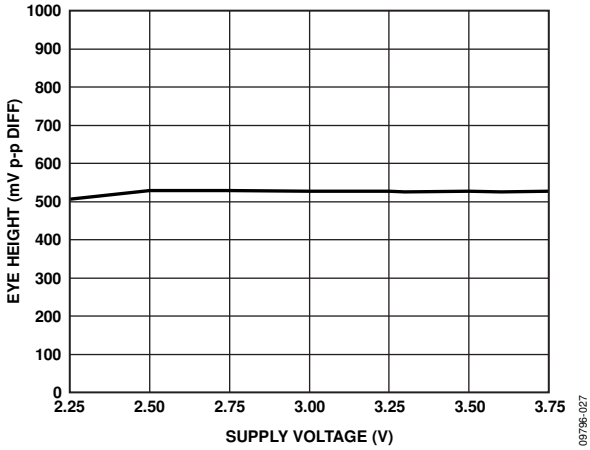

Figure 26. Eye Height vs. Supply Voltage

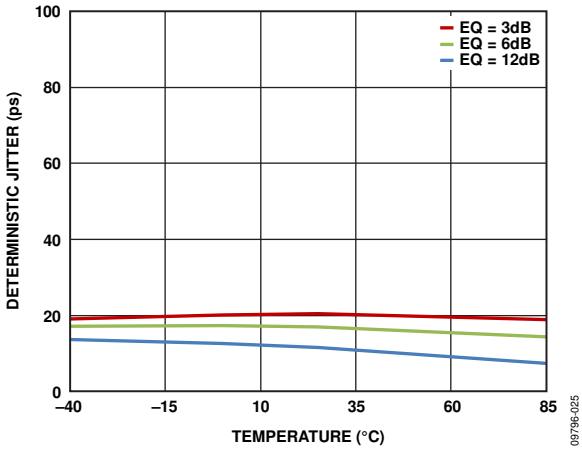

Figure 24. Deterministic Jitter vs. Temperature

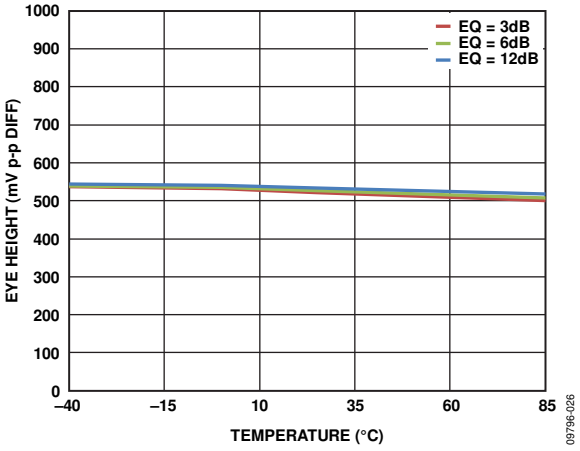

Figure 27. Eye Height vs. Temperature

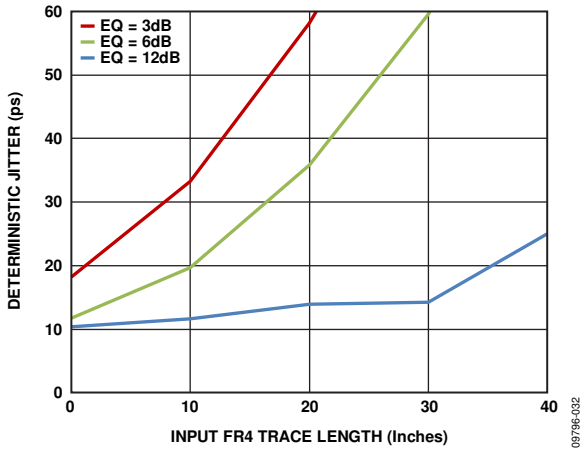

Figure 28. Deterministic Jitter vs. Input FR4 Channel Length

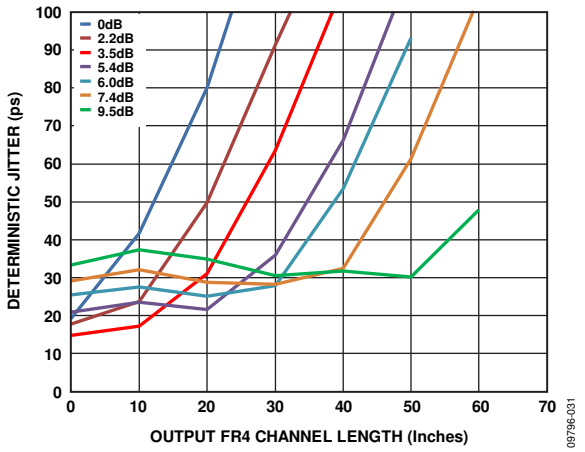

Figure 31. Deterministic Jitter vs. Output FR4 Channel Length

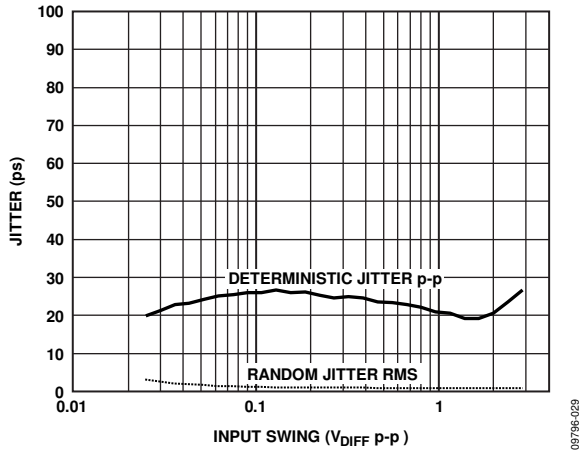

Figure 29. Jitter vs. Differential Input Swing

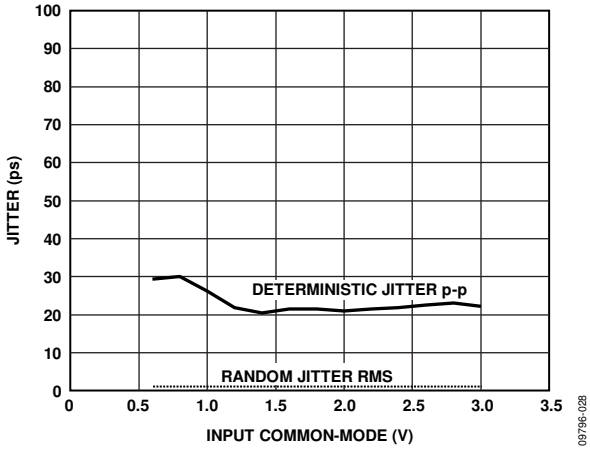

Figure 32. Jitter vs. Input Common-Mode Voltage

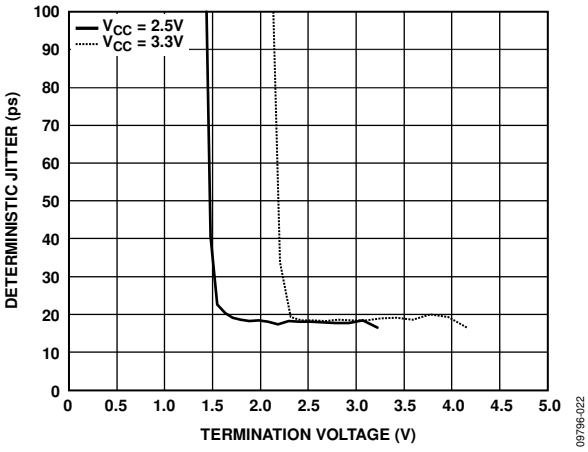

Figure 30. Deterministic Jitter vs. Output Termination Voltage (V_{TTO})

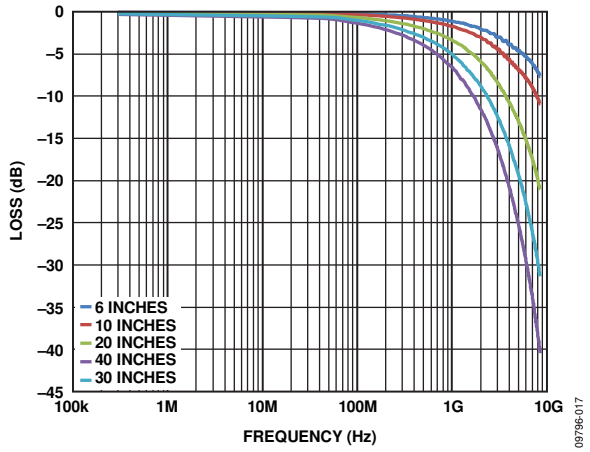

Figure 33. S21 Test Traces

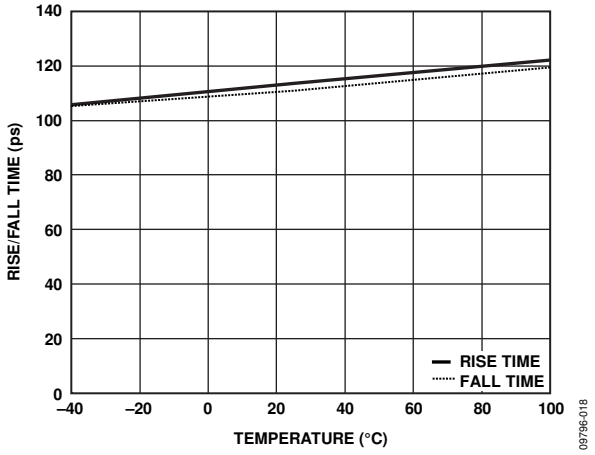

Figure 34. Rise/Fall Time vs. Temperature

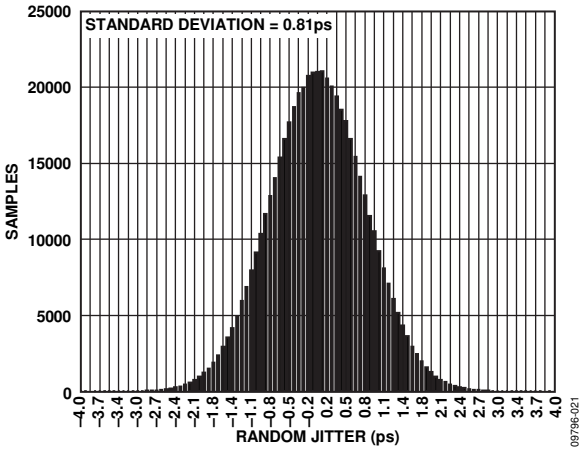

Figure 37. Random Jitter Histogram

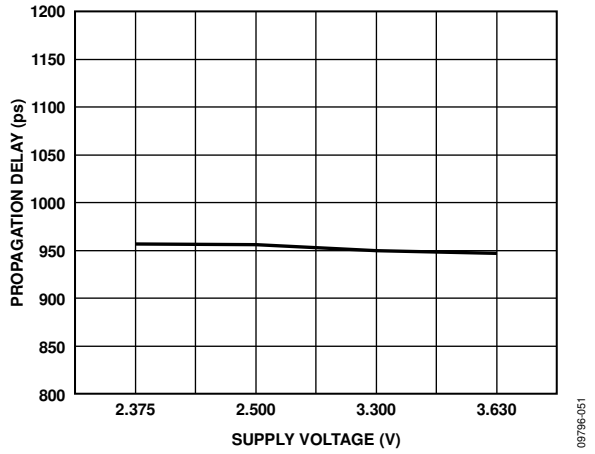

Figure 35. Propagation Delay vs. Supply Voltage

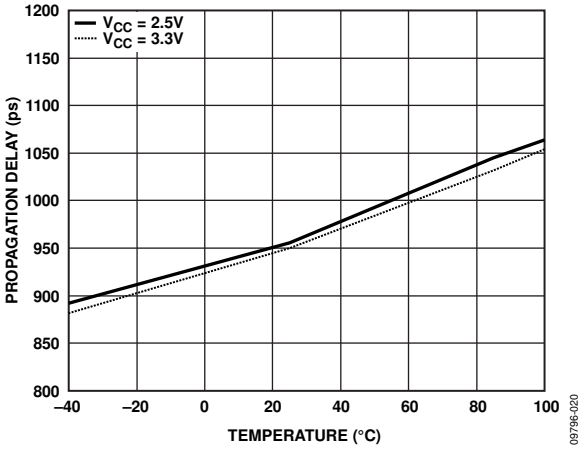

Figure 38. Propagation Delay vs. Temperature

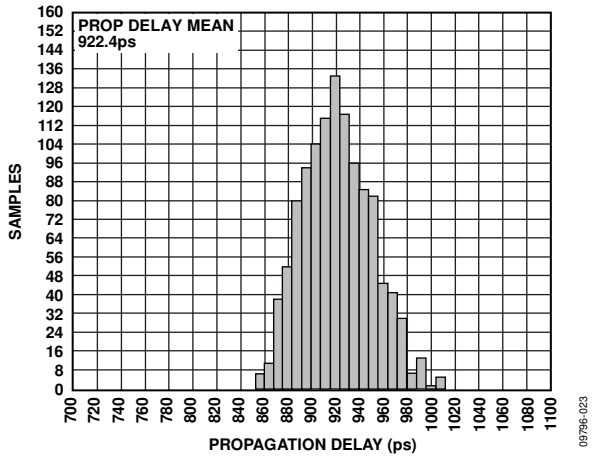

Figure 36. Propagation Delay Histogram

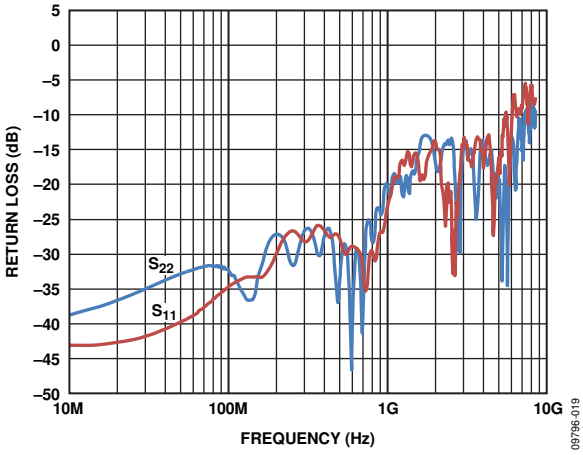

Figure 39. Return Loss (S11, S22)

THEORY OF OPERATION

INTRODUCTION

The ADN4605 is a 40 × 40, buffered, asynchronous crosspoint switch that provides input equalization, output preemphasis, and output level programming capabilities. The receivers integrate an equalizer that is optimized to compensate for typical backplane losses. The switch supports multicast and broadcast operation, allowing the ADN4605 to work in redundancy and port replication applications.

The ADN4605 is configured through either the serial or parallel control interface. The serial or parallel control interface is selected using the SER/$\overline{\text{PAR}}$ dedicated control pin. The serial interface supports both I²C and SPI protocols selected using the I²C/$\overline{\text{SPI}}$ dedicated control pin. The ADN4605 control pins function differently depending on which programming interface is selected, as described in Table 8.

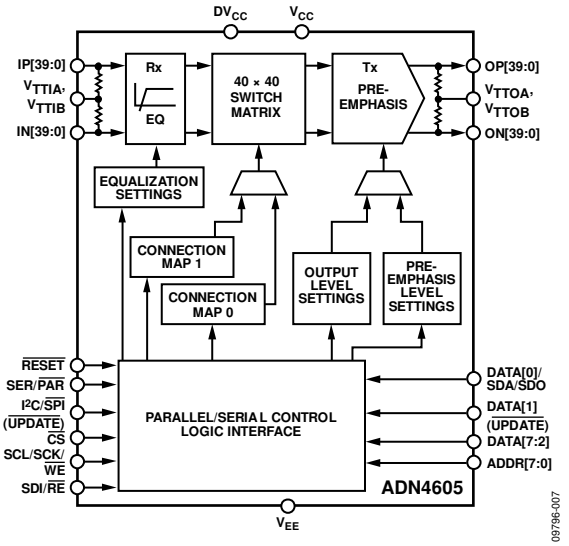

Figure 40. Block Diagram

Table 8. Parallel/Serial Interface Pin Control

		Parallel Mode (SER/$\overline{\text{PAR}}$ = 0)	**I²C Mode (SER/$\overline{\text{PAR}}$ = 1, I²C/$\overline{\text{SPI}}$ = 1)**	**SPI Mode (SER/$\overline{\text{PAR}}$ = 1, I²C/$\overline{\text{SPI}}$ = 0)**
Pin No.	**Pin Name**	**Pin Function**	**Pin Function**	**Pin Function**
K4	SER/$\overline{\text{PAR}}$	Serial/parallel control interface selection	Serial/parallel control interface selection	Serial/parallel control interface selection
J4	I²C/$\overline{\text{SPI}}$/$\overline{\text{UPDATE}}$	Update strobe	I²C/$\overline{\text{SPI}}$ control interface selection	I²C/$\overline{\text{SPI}}$ control interface selection
H23	$\overline{\text{WE}}$/SCL/SCK	Parallel write strobe	I²C clock	SPI clock
J23	$\overline{\text{RE}}$/SDI	Parallel read strobe	N/A	SPI data input
K23	$\overline{\text{CS}}$	Chip select	N/A	Chip select
L23	DATA0/SDA/SDO	Parallel register data bit (LSB)	I²C data input	SPI data output
M23	DATA1/$\overline{\text{UPDATE}}$	Parallel register data bits	Update strobe	Update strobe
N23, P23, R23, T23, U23, V23	DATA2 to DATA7	Parallel register data bits	N/A	N/A
L4	$\overline{\text{RESET}}$	Device register reset (active low)	Device register reset (active low)	Device register reset (active low)
M4	ADDR0	Parallel register address bit (LSB)	N/A	N/A
N4, P4, R4, T4, U4, V4, W4	ADDR1to ADDR7	Parallel register address bits	I²C LSB device address to I²C MSB device address	N/A