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Programmable Low Voltage 1:10 LVDS Clock Driver

ADN4670

FEATURES

- **Low output skew <30 ps (typical)**
- **Distributes one differential clock input to 10 LVDS clock outputs**
- **Programmable—one of two differential clock inputs can be selected (CLK0, CLK1) and individual differential clock outputs enabled/disabled**
- **Signaling rate up to 1.1 GHz (typical)**
- **2.375 V to 2.625 V power supply range**
- **±100 mV differential input threshold**
- **Input common-mode range from rail-to-rail**
- **I/O pins fail-safe during power-down: V_{DD} = 0 V**
- **Available in 32-lead LFCSP and LQFP packages**
- **Industrial operating temperature range: −40°C to +85°C**

APPLICATIONS

Clock distribution networks

FUNCTIONAL BLOCK DIAGRAM

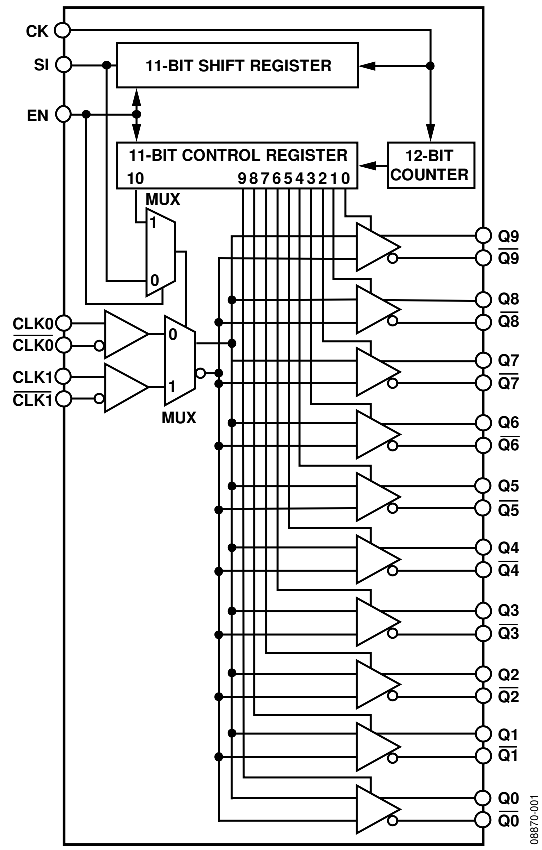

Figure 1.

GENERAL DESCRIPTION

The ADN4670 is a low voltage differential signaling (LVDS) clock driver that expands a differential clock input signal to 10 differential clock outputs. The device is programmable using a simple serial interface, so that one of two clock inputs can be selected (CLK0/$\overline{CLK0}$ or CLK1/$\overline{CLK1}$) and any of the differential outputs (Q0/$\overline{Q0}$ to Q9/$\overline{Q9}$) can be enabled or disabled (tristated). The ADN4670 is designed for use in 50 Ω transmission line environments.

When the enable input EN is high, the device may be programmed by clocking 11 data bits into the shift register. The first 10 bits determine which outputs are enabled (0 = disabled, 1 = enabled), while the 11th bit selects the clock input (0 = CLK0, 1 = CLK1). A 12th clock pulse transfers data from the shift register to the control register.

The ADN4670 is fully specified over the industrial temperature range and is available in a 32-lead LFCSP and LQFP packages.

Rev. A

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ADN4670* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-1176: Component Footprints and Symbols in the Binary .Bxl File Format
- AN-1177: LVDS and M-LVDS Circuit Implementation Guide
- AN-1179: Junction Temperature Calculation for Analog Devices RS-485/RS-422, CAN, and LVDS/M-LVDS Transceivers

Data Sheet

- ADN4670: Programmable Low Voltage 1:10 LVDS Clock Driver

DESIGN RESOURCES

- ADN4670 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADN4670 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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REVISION HISTORY

1/12—Rev. 0 to Rev. A

Added LQFP Package .... Throughout
Updated Outline Dimensions 9
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4/10—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.375 V to 2.625 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Comments
RECEIVER						
Input High Threshold at CLK0/$\overline{\text{CLK0}}$ or CLK1/$\overline{\text{CLK1}}$	V_{TH}			100	mV	
Input Low Threshold at CLK0/$\overline{\text{CLK0}}$ or CLK1/$\overline{\text{CLK1}}$	V_{TL}	−100			mV	
Differential Input Voltage	$\|V_{ID}\|$	200			mV	
Input Common-Mode Voltage	V_{IC}	$0.5\|V_{ID}\|$		$V_{DD} - 0.5\|V_{ID}\|$		
Input Current at CLK0, $\overline{\text{CLK0}}$, CLK1, or $\overline{\text{CLK1}}$	I_{IH}, I_{IL}	−5		+5	μA	$V_I = V_{DD}$ or V_I = 0 V
Input Capacitance	C_I		3		pF	$V_I = V_{DD}$ or GND
DRIVER						
Differential Output Voltage	$\|V_{OD}\|$	250	450	600	mV	R_L = 100 Ω
V_{OD} Magnitude Change	ΔV_{OD}			50	mV	
Offset Voltage	V_{OS}	0.95	1.2	1.45	V	−40°C to +85°C
V_{OS} Magnitude Change	ΔV_{OS}			350	mV	
Output Short Circuit Current	I_{OS}			−20	mA	V_O = 0 V
				20	mA	$\|V_{OD}\|$ = 0 V
Reference Output Voltage	V_{BB}	1.15	1.25	1.35	V	V_{DD} = 2.5 V, I = −100 μA
Output Capacitance	C_O		3		pF	$V_O = V_{DD}$ or GND
SUPPLY CURRENT						
Supply Current	I_{DD}			35	mA	All outputs tristated, f = 0 Hz
			100	110	mA	All outputs enabled and loaded, R_L = 100 Ω, f = 100 MHz
			150	160	mA	All outputs enabled and loaded, R_L = 100 Ω, f = 800 MHz

JITTER CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Comments
Additive Phase Jitter from Input to LVDS Outputs, Q3 and $\overline{\text{Q3}}$	$t_{JITTER\ LVDS}$		281		f_S rms	12 kHz to 5 MHz, f_{OUT} = 30.72 MHz
			111		f_S rms	12 kHz to 20 MHz, f_{OUT} = 125 MHz

LVDS SWITCHING CHARACTERISTICS

V_{DD} = 2.375 V to 2.625 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max[1]	Unit	Conditions/Comments
Propagation Delay Low to High	t_{PLHx}		2	3	ns	From CLK0/$\overline{CLK0}$ or CLK1/ $\overline{CLK1}$ to any Qx/$\overline{Qx}$
Propagation Delay High to Low	t_{PHLx}		2	3	ns	From CLK0/$\overline{CLK0}$ or CLK1/ $\overline{CLK1}$ to any Qx/$\overline{Qx}$
Duty Cycle	t_{DUTY}	45		55	%	From CLK0/$\overline{CLK0}$ or CLK1/ $\overline{CLK1}$ to any Qx/$\overline{Qx}$
Output Skew[2]	$t_{SK(O)}$		30		ps	Any Qx/$\overline{Qx}$
Pulse Skew[3]	$t_{SK(P)}$			50	ps	Any Qx/$\overline{Qx}$
Part-to-Part Output Skew[4]	$t_{SK(PP)}$			600	ps	Any Qx/$\overline{Qx}$
Output Rise Time	t_r			350	ps	Any Qx/$\overline{Qx}$, 20% to 80%, R_L = 100 Ω C_L = 5 pF
Output Fall Time	t_f			350		Any Qx/$\overline{Qx}$, 80% to 20%, R_L = 100 Ω C_L = 5 pF
Maximum Input Frequency	f_{CLK}	900	1100		MHz	From CLK0/$\overline{CLK0}$ or CLK1/ $\overline{CLK1}$ to any Qx/$\overline{Qx}$

[1] Guaranteed by design and characterization.
[2] Output skew is defined as the difference between the largest and smallest values of T_{PLHx} within a device or the difference between the largest and smallest values of T_{PHLx} within a device, whichever of the two is greater.
[3] Pulse skew is defined as the magnitude of the maximum difference between t_{PLH} and t_{PHL} for any channel of a device, that is, $|t_{PHLx} – t_{HLPx}|$.
[4] Part-to-part output skew is defined as the difference between the largest and smallest values of T_{PLHx} across multiple devices or the difference between the largest and smallest values of T_{PHLx} across multiple devices, whichever of the two is greater.

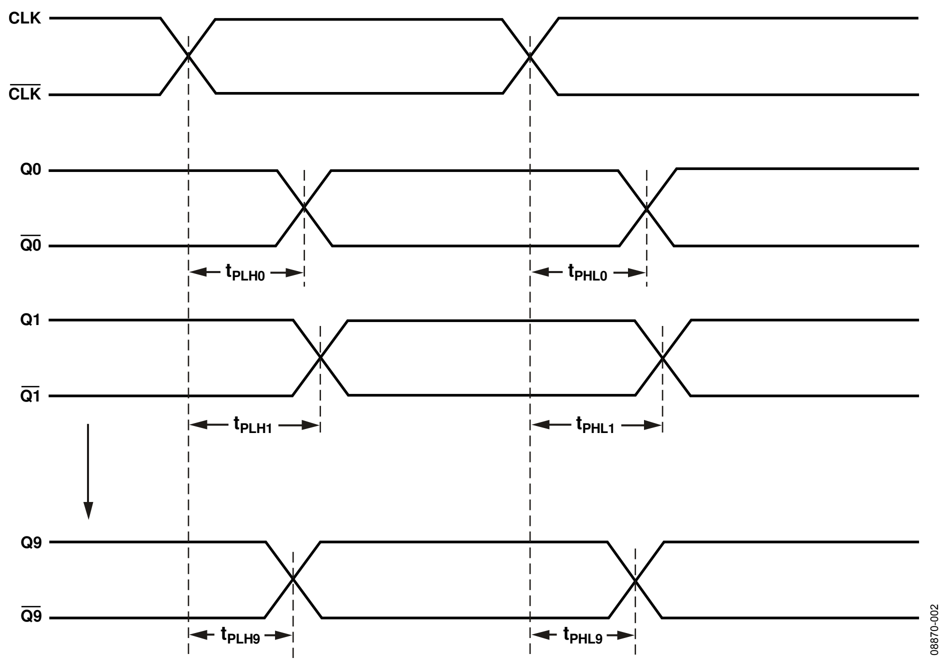


Figure 2. Waveforms for Calculation of $t_{SK(O)}$ and $t_{SK(PP)}$

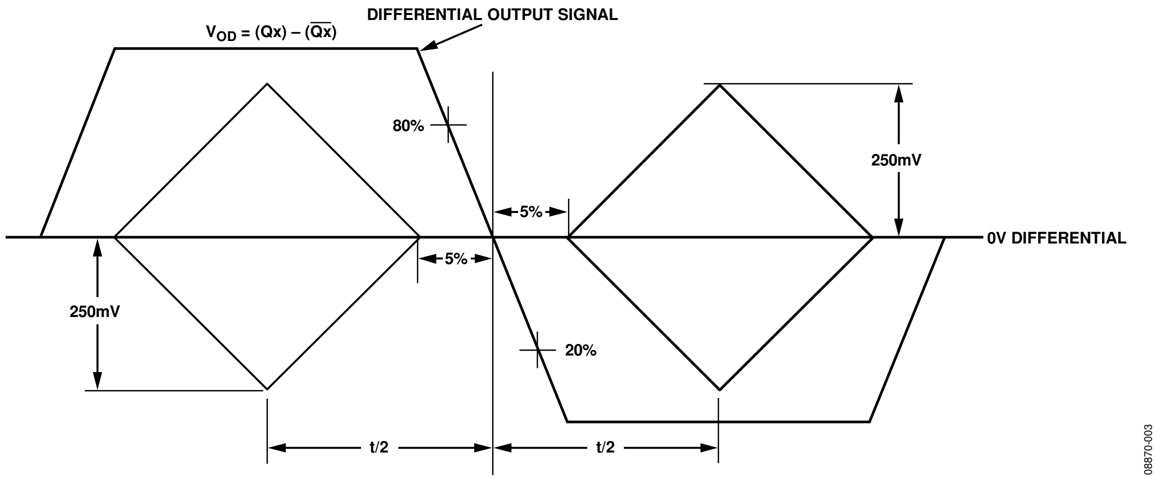


Figure 3. Test Criteria for f_{CLK}, t_r, t_f, and V_{OD}

PROGRAMMING LOGIC AC CHARACTERISTICS

V_{DD} = 2.375 V to 2.625 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Comments
Maximum Frequency at CK Input	f_{MAX}	100	150		MHz	
Setup Time, SI to CK	t_{SU}			2	ns	Time for which SI must not change before the CK 0-to-1 transition
Hold Time, CK to SI	t_H			1.5	ns	Time for which SI must not change after the CK 0-to-1 transition
EN to CK Removal Time	$t_{REMOVAL}$			1.5	ns	Removal time, EN to CK
Start-Up Time	$t_{STARTUP}$			1	µs	Start-up time after disable through SI
Minimum Clock Pulse Width	t_W	3			ns	
Logic Input High Level	V_{IH}	2			V	V_{DD} = 2.5 V
Logic Input Low Level	V_{IL}			0.8	V	V_{DD} = 2.5 V
High Level Logic Input Current, CK	I_{IH}	−5		+5	µA	$V_I = V_{DD}$
High Level Logic Input Current, SI and EN		+10		−30	µA	$V_I = V_{DD}$
Low Level Logic Input Current, CK	I_{IL}	−10		+30	µA	V_I = GND
Low Level Logic Input Current, SI and EN		−5		+5	µA	V_I = GND

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

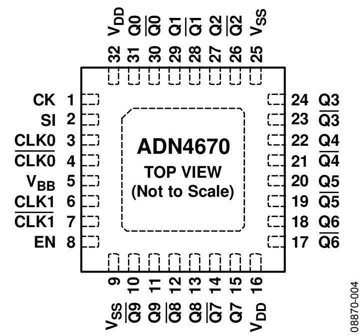
Parameter	Rating
V_{CC} to GND	−0.3 V to +2.8 V
Input Voltage to GND	−0.2 V to (V_{DD} + 0.2) V
Output Voltage to GND	−0.2 V to (V_{DD} + 0.2) V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
Power Dissipation	(T_J max − T_A)/θ_{JA}
LFCSP Package	
θ_{JA} Thermal Impedance	32.5°C/W
LQFP Package	
θ_{JA} Thermal Impedance	59°C/W
Reflow Soldering Peak Temperature	
Pb-Free	260°C ± 5°C
ESD (Human Body Model, 1.5 kΩ 100 pF)	4000 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD CAN BE CONNECTED TO GROUND OR LEFT FLOATING.

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CK	Programming Clock. Programming data is clocked in on a low-to-high transition at this input. If left open-circuit, it is pulled high by a 120 kΩ resistor.
2	SI	Serial Data Input. This is the input for programming data. If left open-circuit, it is pulled low by a 120 kΩ resistor.
3	CLK0	Noninverting Differential Clock Input 0.
4	$\overline{\text{CLK0}}$	Inverting Differential Clock Input 0.
5	V_{BB}	Reference Voltage Output.
6	CLK1	Noninverting Differential Clock Input 1.
7	$\overline{\text{CLK1}}$	Inverting Differential Clock Input 1.
8	EN	Active-High Enable Input. When this input is high, programming is enabled. If left open-circuit, it is pulled low by a 120 kΩ resistor.
9, 25	V_{SS}	Device Ground.
10, 12, 14, 17, 19, 21, 23, 26, 28, 30	$\overline{\text{Q9}}$ to $\overline{\text{Q0}}$	Inverted Clock Output. When the differential input voltage is between CLKx and $\overline{\text{CLKx}}$ > 100 mV, this output sinks current. When the differential input voltage is between CLKx and $\overline{\text{CLKx}}$ < −100 mV, this output sources current.
11, 13, 15, 18, 20, 22, 24, 27, 29, 31	Q9 to Q0	Noninverted Clock Output. When the differential input voltage is between CLKx and $\overline{\text{CLKx}}$ > 100 mV, this output sources current. When the differential input voltage is between CLKx and $\overline{\text{CLKx}}$ < −100 mV, this output sinks current.
16, 32	V_{DD}	Power Supply Input. This part can be operated from 2.375 V to 2.625 V.

THEORY OF OPERATION

The ADN4670 is a clock driver/expander for low voltage differential signaling (LVDS). It takes a differential clock signal of typically 350 mV and expands it to 10 differential clock outputs with very low skew (typically < 30 ps). The device receives a differential current signal from a source such as a twisted pair cable, which develops a voltage of typically ±350 mV across a 100 Ω terminating resistor. This signal passes via a differential multiplexer to 10 drivers that each output a differential current signal.

The device is programmable using a simple serial interface. One of two differential clock inputs (CLK0/$\overline{\text{CLK0}}$ or CLK1/ $\overline{\text{CLK1}}$), can be selected and any of the differential outputs (Q0/$\overline{\text{Q0}}$ to Q9/$\overline{\text{Q9}}$) can be enabled or disabled.

LVDS RECIEVER INPUT TERMINATION

Terminate the clock inputs with 100 Ω resistors from CLK0 to $\overline{\text{CLK0}}$ and CLK1 to /$\overline{\text{CLK1}}$, placed as close as possible to the input pins.

FAIL-SAFE OPERATION

In power-down mode (V_{DD} = 0 V), the ADN4670 has fail-safe input and output pins. In power-on mode, fail-safe biasing can be achieved by connecting 10 kΩ pull-up resistors from CLK0 and CLK1 to V_{DD} and 10 kΩ pull-down resistors from $\overline{\text{CLK0}}$ and $\overline{\text{CLK1}}$ to GND.

PROGRAMMING

Three control inputs are provided for programming the ADN4670. EN is the enable input, which allows programming when high, SI is the serial data input, and CK is the serial clock input, which clocks data into the device on a low-to-high clock transition. Each of these inputs has an internal pull-up or pull-down resistor of 120 kΩ. EN and SI are pulled low if left open-circuit while CK is pulled high.

The default condition if these inputs are left open-circuit is that all outputs are enabled, and the state of SI selects the inputs (0 = CLK0/$\overline{\text{CLK0}}$, 1 = CLK1/$\overline{\text{CLK1}}$). This is the standard operating mode for which no programming of the device is required.

Programming is enabled by taking EN high. The data on SI is then clocked into the device on each 0-to-1 transition of CK. Data on SI must be stable for the setup time (t_{SU}) before the clock transition and remain stable for the hold time (t_H) after the clock transition. To program the device, 11 bits of data are needed, starting with Bit 0, which enables or disables outputs Q9/$\overline{\text{Q9}}$, through to Bit 10, which selects either CLK0/$\overline{\text{CLK0}}$ or CLK1/$\overline{\text{CLK1}}$ as the inputs. A 12th clock pulse is then required to transfer data from the shift register to the control register.

A low-to-high transition on EN resets the control register and the next 12 CK pulses are programmed.

Table 5. Control Logic Truth Table

CK	EN	SI	CLK0	$\overline{\text{CLK0}}$	CLK1	$\overline{\text{CLK1}}$	Q0 to Q9	$\overline{\text{Q0}}$ to $\overline{\text{Q9}}$
L	L	L	L	H	X	X	L	H
L	L	L	H	L	X	X	H	L
L	L	L	Open	Open	X	X	L	H
L	L	H	X	X	L	H	L	H
L	L	H	X	X	H	L	H	L
L	L	H	X	X	Open	Open	L	H

Table 6. State Machine Inputs

EN	SI	CK	Output
L	L	X	Default state with all outputs enabled, CLK0 selected, and the control register disabled
L	H	X	All outputs enabled, CLK1 selected, and the control register disabled
H	L	↑	First stage stores low, other stage stores data of previous stage
H	H	↑	First stage stores high, other stage stores data of previous stage
L	X	X	Reset the state machine, control register, and shift register

Table 7. Serial Input Sequence

Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLK_SEL	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9

Table 8. Control Register

Bit 10	Bit[9:0]	Qx[9:0]
L	H	CLK0
H	H	CLK1
X	L	Outputs disabled

OUTLINE DIMENSIONS

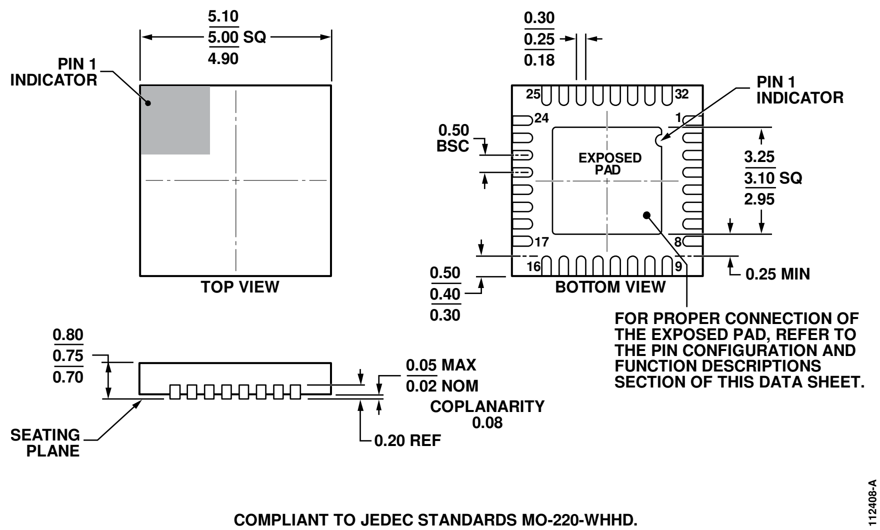


Figure 5. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-7)
Dimensions shown in millimeters

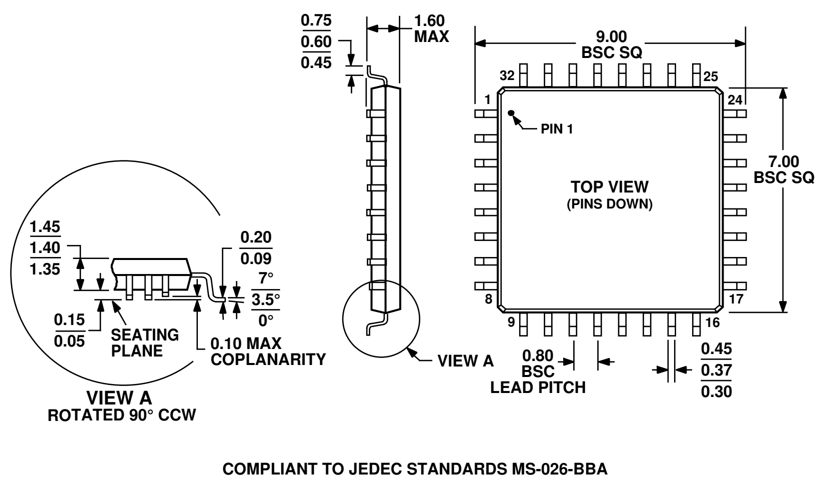


Figure 6. 32-Lead Low Profile Quad Flat Package [LQFP]
(ST-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADN4670BCPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-7
ADN4670BCPZ-REEL7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-7
ADN4670BSTZ	−40°C to +85°C	32-Lead Low Profile Quad Flat Package [LQFP]	ST-32-2
ADN4670BSTZ-REEL7	−40°C to +85°C	32-Lead Low Profile Quad Flat Package [LQFP]	ST-32-2

[1] Z = RoHS Compliant Part.

NOTES

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