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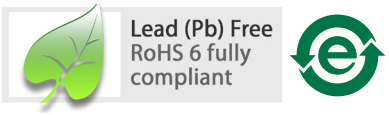
ADNS-5070
Optical Mouse Sensor

Data Sheet



Description

The ADNS-5070 is a mainstream, small form factor optical mouse sensor. It is used to implement a non mechanical tracking engine for computer mice.

It is based on optical navigation technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement.

The sensor is housed in an 8-pin staggered dual inline package (DIP). It is designed for use with the HDNS-2100 round lens or HDNS-2100#001 trim lens, HLMP-ED80-xx000, and the HDNS-2200 LED Clip, providing an optical mouse solution that is compact and affordable. There are no moving parts, so precision optical alignment is not required, thereby facilitating high volume assembly.

The output format is a two wire serial port. The current X and Y information are available in registers accessed via the serial port.

The ADNS-5070 is capable of high-speed motion detection – up to 30ips and 8g. In addition, it has an on-chip oscillator and built-in LED driver to minimize external components. Frame rate is also adjusted internally.

Features

- Small form factor, pin-to-pin compatible with ADNS-26x0
- Register-to-register compatible with ADNS-26x0
- Built-in LED driver for simpler circuitry
- High speed motion detection up to 30ips and 8g
- Self-adjusting frame rate for optimum performance
- Internal oscillator – no clock input needed
- Default 1050cpi resolution, adjustable from 150 to 1350cpi via 150cpi step
- Operating voltage: 5V nominal
- Two-wire serial interface

Applications

- Optical Mice
- Optical trackballs
- Integrated input devices

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Theory of Operation

The ADNS-5070 is based on Optical Navigation Technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement.

The ADNS-5070 contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a two wire serial port.

The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Δx and Δy relative displacement values.

An external microcontroller reads the Δx and Δy information from the sensor serial port. The microcontroller then translates the data into PS2 or USB signals before sending them to the host PC.

Pinout of ADNS-5070 Optical Mouse Sensor

Pin	Name	Description	I/O type
1	NC	No Connect	
2	NC	No Connect	
3	SDIO	Serial Port Data	I/O
4	SCLK	Serial Port Clock	I
5	LED_CNTL	Digital Shutter Signal Out	O
6	GND	System Ground	Ground
7	VDD5	5V DC Input	Power
8	REFA	Internal Reference	O

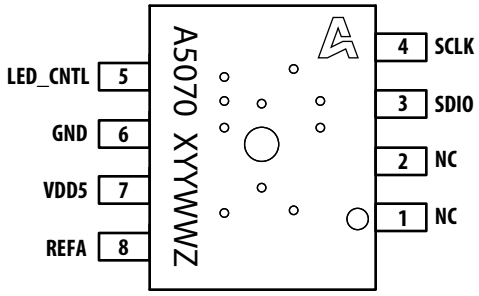


Figure 1. Package outline drawing (top view)

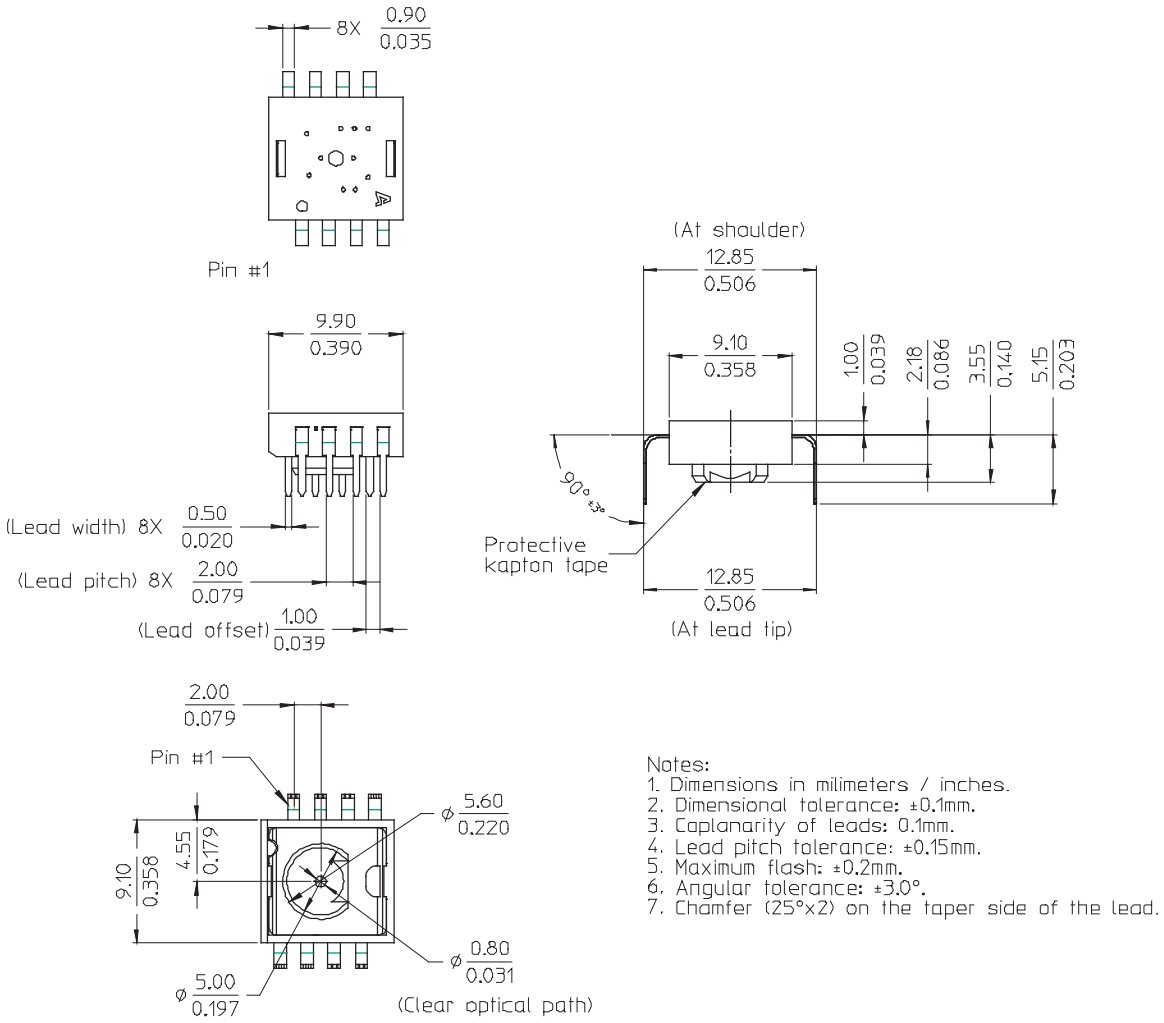


Figure 2. Package outline drawing

Overview of Optical Mouse Sensor Assembly

Avago Technologies provides an IGES file drawing describing the base plate molding features for lens and PCB alignment.

The ADNS-5070 sensor is designed for mounting on a through-hole PCB, looking down. There is an aperture stop and features on the package that align to the lens.

The HDNS-2100/2100#001 lens provides optics for the imaging of the surface as well as illumination of the surface at the optimum angle. Features on the lens align it to the sensor, base plate, and clip with the LED.

The HDNS-2200 clip holds the LED in relation to the lens. The LED must be inserted into the clip and the LED's leads formed prior to loading on the PCB.

The HLMP-ED80 LED is recommended for illumination.

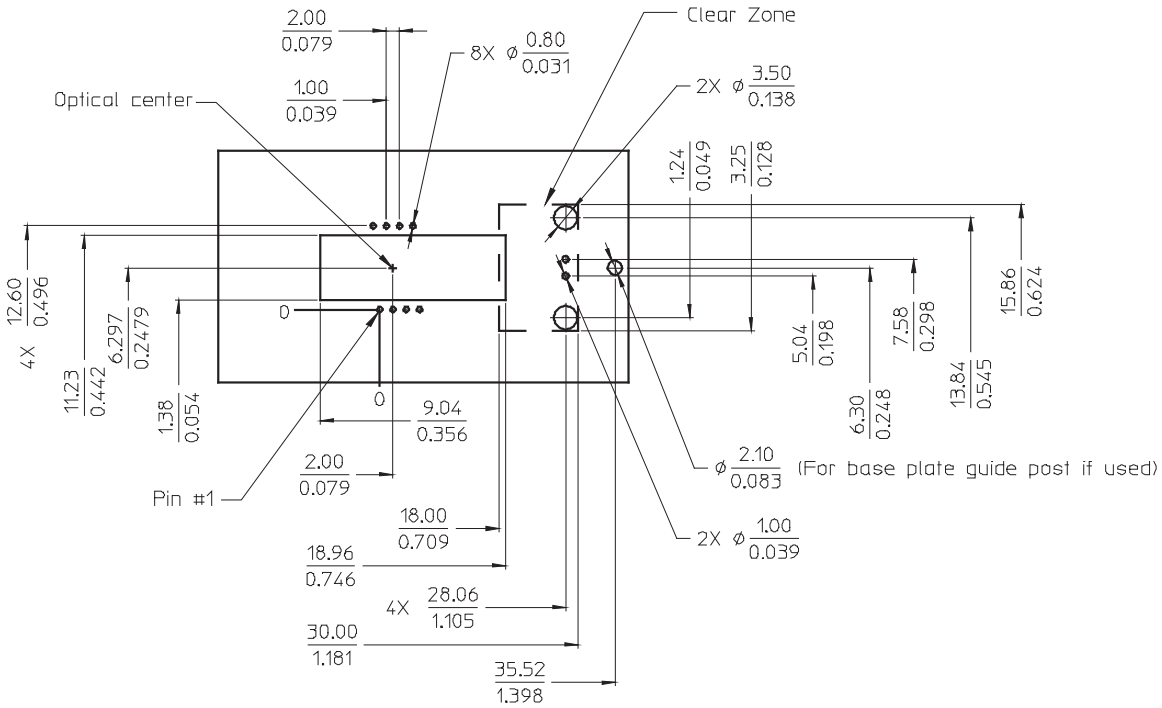


Figure 3. Recommended PCB mechanical cutouts and spacing

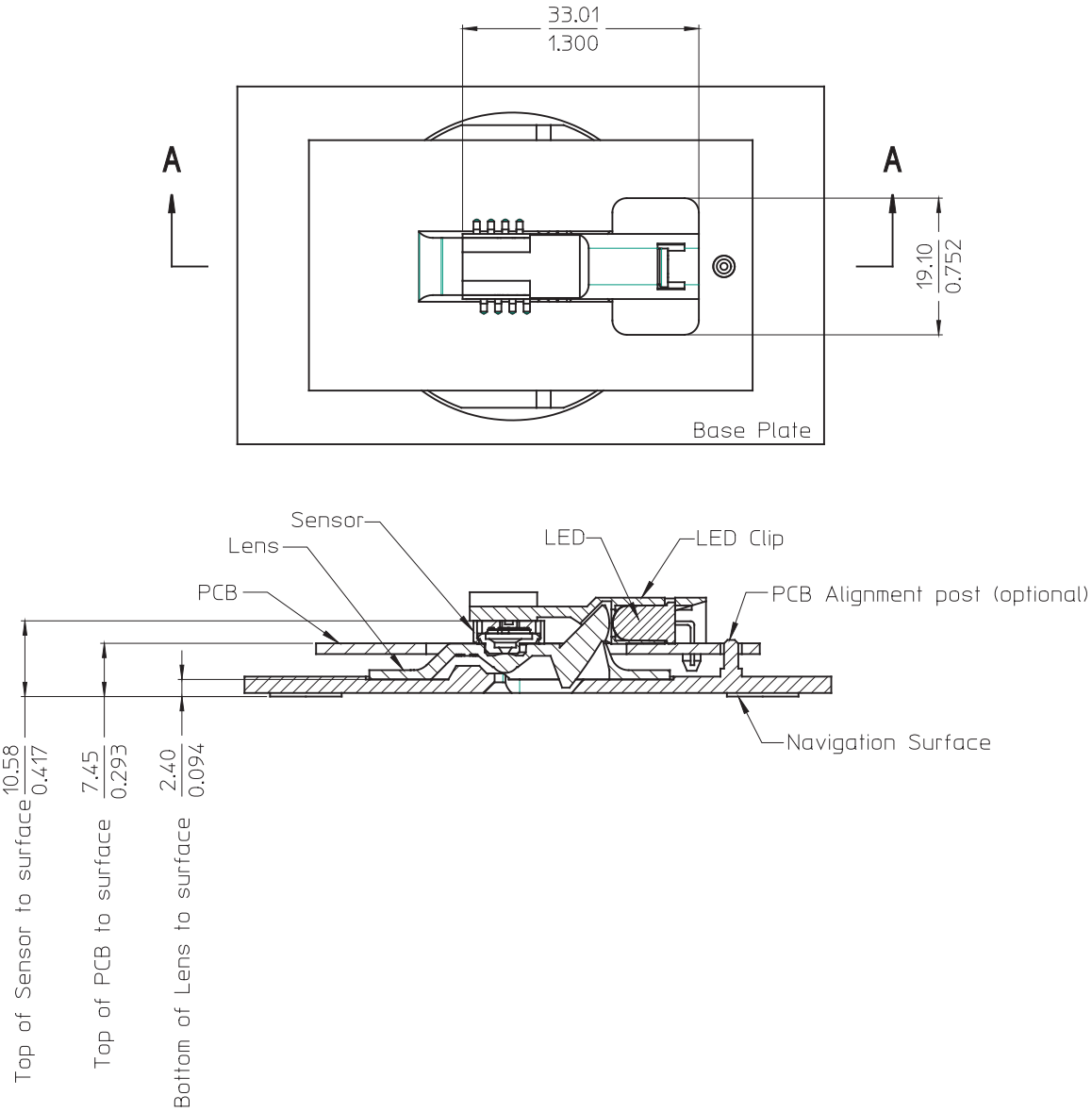


Figure 4. 2D Assembly drawing of ADNS-5070 (top and side view)

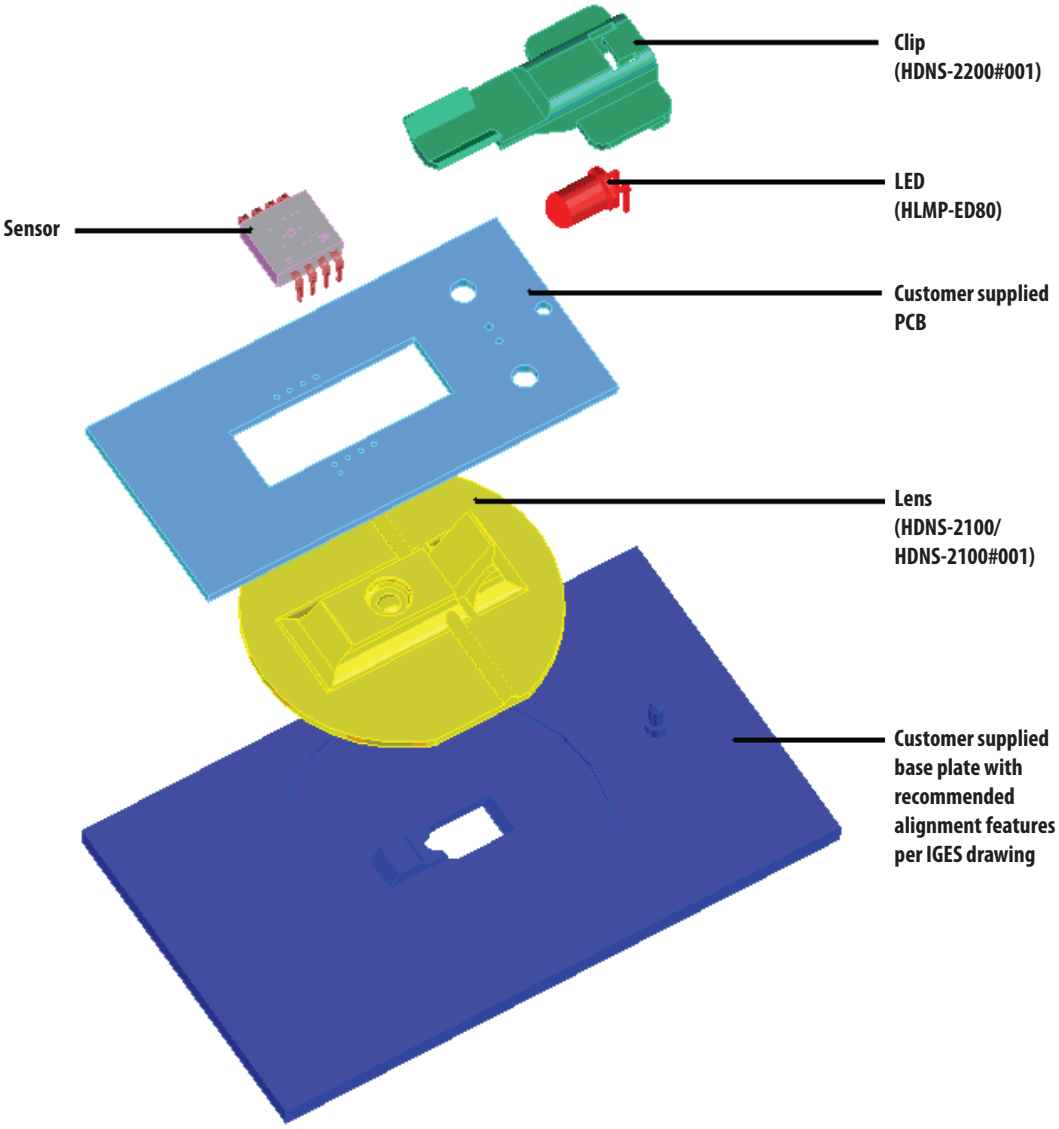


Figure 5. Exploded view drawing

PCB Assembly Considerations

1. Insert the sensor and all other electrical components into PCB.
2. Insert the LED into the assembly clip and bend the leads 90 degrees.
3. Insert the LED clip assembly into PCB.
4. Wave solder the entire assembly in a no-wash solder process utilizing solder fixture. The solder fixture is needed to protect the sensor during the solder process. It also sets the correct sensor-to-PCB distance as the lead shoulders do not normally rest on the PCB surface. The fixture should be designed to expose the sensor leads to solder while shielding the optical aperture from direct solder contact.
5. Place the lens onto the base plate.
6. Remove the protective kapton tape from optical aperture of the sensor. Care must be taken to keep contaminants from entering the aperture. Recommend not to place the PCB facing up during the entire mouse assembly process. Recommend to hold the PCB first vertically for the kapton removal process.
7. Insert PCB assembly over the lens onto the base plate aligning post to retain PCB assembly. The sensor aperture ring should self-align to the lens.
8. The optical position reference for the PCB is set by the base plate and lens. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
9. Install mouse top case. There **MUST** be a feature in the top case to press down onto the PCB assembly to ensure all components are interlocked to correct vertical height.

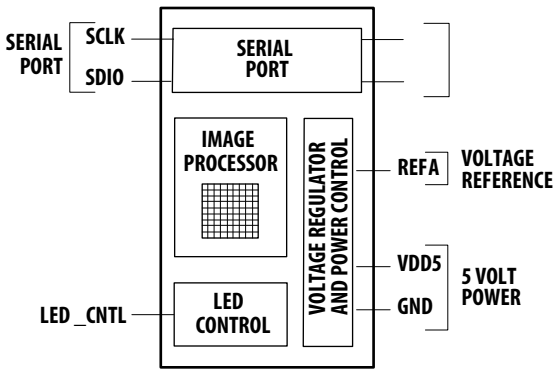


Figure 6. Block diagram of ADNS-5070 optical mouse sensor

Design considerations for improved ESD Performance

For improved electrostatic discharge performance, typical system creepage and clearance distance are shown in the table below.

Assumption: Base plate construction as per the Avago Technologies supplied IGES file and HDNS-2100/2100#001 lens.

Typical Distance	HDNS-2100 round lens	HDNS-2100#001 trim lens
Creepage (mm)	40.5	17.9
Clearance (mm)	32.6	9.2

Note that the lens material is polycarbonate and therefore, cyanoacrylate based adhesives or other adhesives that may damage the lens should **NOT** be used.

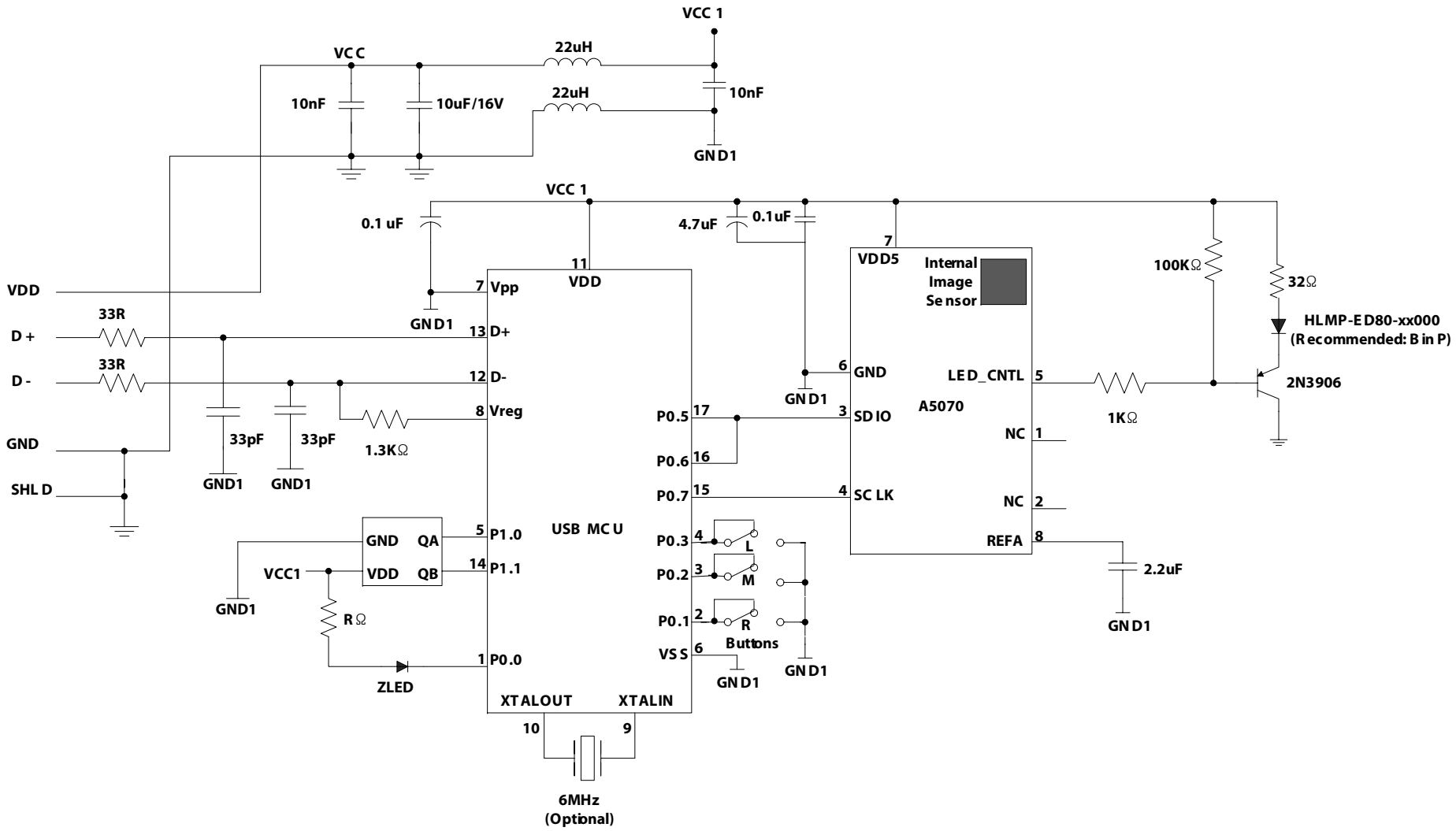


Figure 7a. Schematic Diagram for Interface between ADNS-5070 and Microcontroller (compatible with A26x0 sensors)

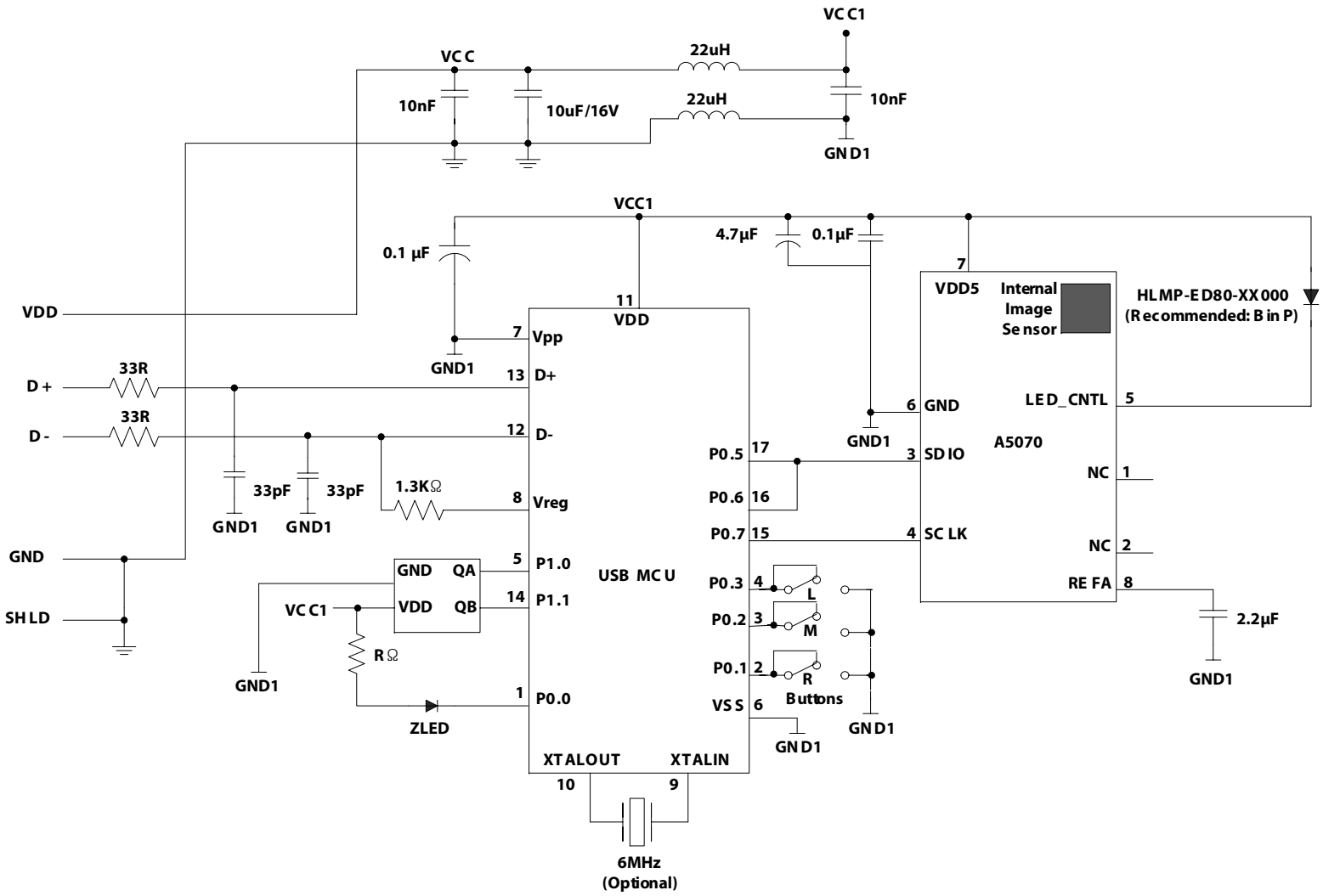


Figure 7b. Schematic Diagram for Interface between ADNS-5070 and Microcontroller (using internal LED driver)

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- Passes IEC-1000-4-3 radiated susceptibility level when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- Passes EN61000-4-4/IEC801-4 EFT tests when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- UL flammability level UL94 HB.
- Provides sufficient ESD creepage/clearance distance to avoid discharge up to 15kV when assembled into a mouse using HDNS-2100 round lens according to usage instructions above.

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Operating Temperature	T_A	-15	55	°C	
Lead Solder Temp			260	°C	For 10 seconds, 1.6mm below seating plane.
Supply Voltage	V_{DD}	-0.5	5.5	V	
ESD			2	kV	All pins, human body model MIL 883 Method 3015
Input Voltage	V_{IN}	-0.5	V_{DD}+0.5	V	SDIO, SCLK, LED_CNTL
Input Voltage	V_{IN}	-0.5	3.6	V	REFA

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Operating Temperature	T_A	0		40	°C	
Power supply voltage	V_{DD}	4.10	5.0	5.5	Volts	Register values retained for voltage transients below 4.10V but greater than 3.9V.
Power supply rise time	V_{RT}			100	ms	
Supply noise	V_N			100	mV	Peak to peak within 0-50 MHz bandwidth
Serial Port Clock Frequency	f_{SCLK}			3	MHz	550% duty cycle.
Resonator Impedance	X_{RES}			55	Ω	
Distance from lens reference plane to surface	Z	2.3	2.4	2.5	mm	Results in ±0.1 mm DOF, (See Figure 8)
Speed	S		30		in/sec	
Acceleration	A			8	g	
Light level onto IC	IRR_{INC}	80 100		25,000 30,000	mW/m^2	λ = 639 nm λ = 875 nm
SDIO read hold time	t_{HOLD}	100			ns	Hold time for valid data (Refer to Figure 20)
SDIO serial write-write time	t_{SWW}	100			us	Time between two write commands. (Refer to Figure 22)
SDIO serial write-read time	t_{SWR}	100			us	Time between write and read operation. (Refer to Figure 23)
SDIO serial read-write time	t_{SRW}	250			ns	Time between read and write operation. (Refer to Figure 24)
SDIO serial read-read time	t_{SRR}	250			ns	Time between two read commands. (Refer to Figure 24)
SPI Read Address-Data Delay	t_{SRAD}	4			us	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read. (Refer to Figure 24)
Data delay after PD deactivated	$t_{COMPUTE}$	3.1			ms	After $t_{COMPUTE}$, all registers contain data from first image after wakeup from Power-Down mode. Note that an additional 75 frames for AGC stabilization may be required if mouse movement occurred while Power Down. (refer to Figure 9)
SDIO write setup time	t_{setup}	60			ns	Data valid time before the rising of SCLK. (refer to Figure 17)

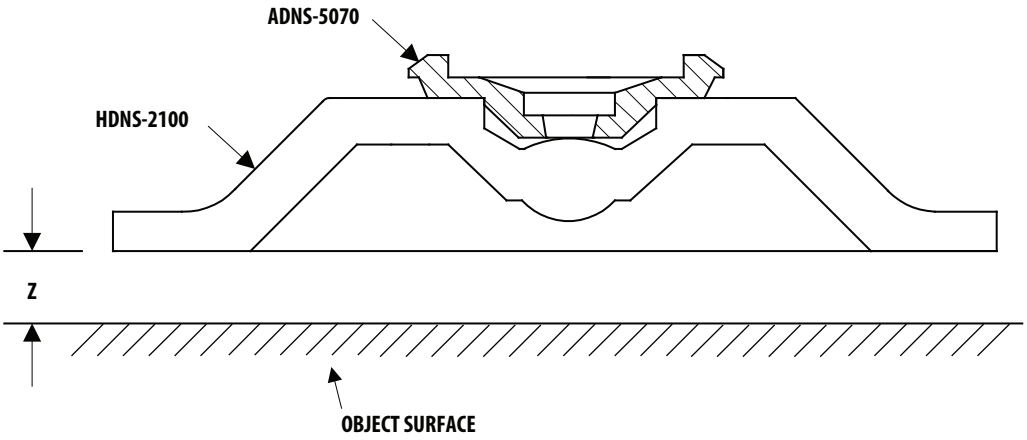


Figure 8. Distance from Lens Reference Plane to Surface

AC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25°C, V_{DD}=5.0 V

Parameter	Symbol	Min.	Typical	Max.	Units	Notes
Power Down (PD)	t_{PD}	1.33			us	32 clock cycle minimum after setting bit 6 in the Configuration register. (refer to Figure 11)
Power Up after Power-Down mode deactivated	t_{PUPD}			50	ms	From Power-Down mode deactivation to accurate reports 610 us + 75 frames (refer to Figure 9)
Power Up from V_{DD} ↑	t_{PU}			40	ms	From V_{DD} valid to accurate reports 610 us + 50 frames
Rise and Fall Times: SDIO	t_r		30		ns	C_L = 30 pF (the rise time is between 10% to 90%)
	t_f		16		ns	C_L = 30 pF (the fall time is between 10% to 90%)
Serial Port transaction timer	t_{SPTT}		90		ms	Serial port will reset if current transaction is not complete within t_{SPTT}. (refer to Figure 26)
Transient Supply Current	I_{DDT}			70	mA	Max supply current during a V_{DD} ramp from 0 to 5.0 V with > 500 us rise time. Does not include charging currents for bypass capacitors.

DC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25°C, V_{DD}=5.0 V.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Supply Current (mouse moving)	$I_{DD\ AVG}$		17.5	20	mA	Average sensor only current, at max frame rate. No load on SDIO.
Supply Current (mouse not moving)	I_{DD}		13		mA	
Power-down Mode Current	I_{DDPD}		180	250	uA	
SCLK pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input Capacitance	C_{IN}			10	pF	
Input Resistance	R_{IN}	1			MΩ	
SDIO pin						V_{DD}=4V, Load = 50pF, 80ns rise & fall
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.5	V	
Output High Voltage	V_{OH}	0.8*V_{DD}			V	
Drive Low Current	I_L	2.0			mA	
Drive High Current	I_H	2.0			mA	
Input Capacitance	C_{IN}			10	pF	
Input Resistance	R_{IN}	1			MΩ	
LED_CNTL pin (Schematic A)						
Output Low Voltage	V_{OL}			0.1	V	
Output High Voltage	V_{OH}	0.8*V_{DD}			V	
Drive Low Current	I_L	250			uA	With 1kΩ connected to base of transistor
Drive High Current	I_H	250			µA	
LED_CNTL pin (Schematic B)						
LED_CNTL Current during run mode (pin voltage range should be greater than 0.8V)	$I_{LED\_CNTL\_run}$		45		mA	Average current at maximum frame rate
LED_CNTL Peak Current (pin voltage range should be greater than 0.8V)	I_{XY_PK}		45	50	mA	Peak current at maximum frame rate
LED_CNTL Current during mouse not moving	$I_{LED\_CNTL\_rest}$		25		mA	
LED_CNTL Current during power down	$I_{LED\_CNTL\_pd}$		0.1		µA	

Power Down Deactivation Timing

Note: All timing circuits shown, from Figure 9 onwards, are based on the 24MHz resonator frequency.

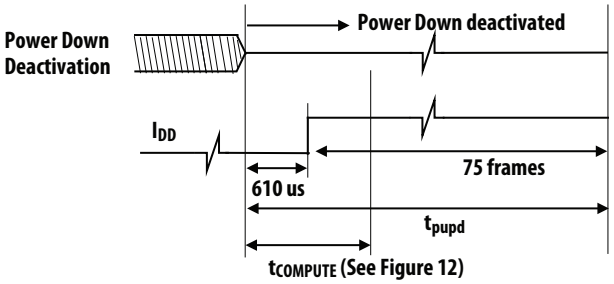


Figure 9. Power-up timing mode

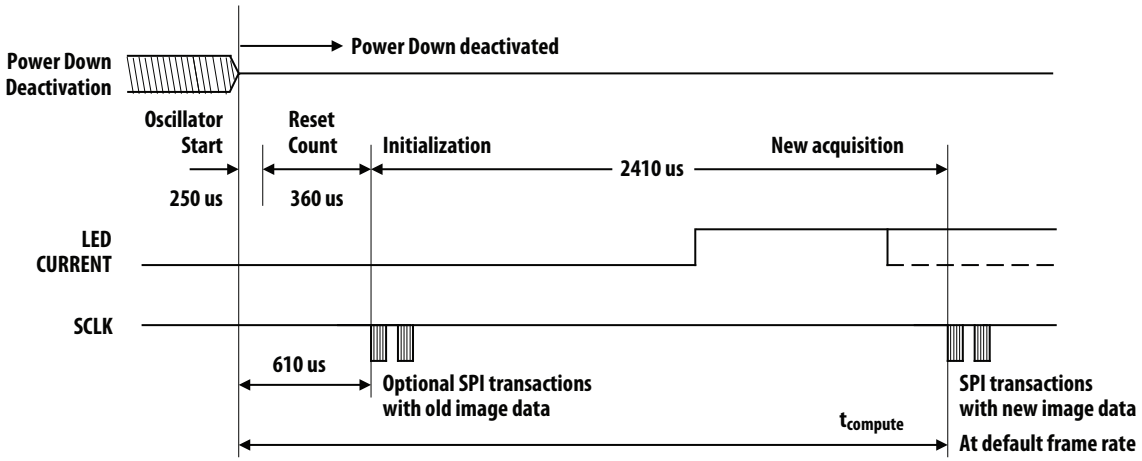


Figure 10. Detail of wake-up timing after PD

Power-down Mode (PD) and Timing

ADNS-5070 Power-down mode

ADNS-5070 can be placed in a power-down mode by setting bit 6 in the configuration register via a serial I/O port write operation. Note that while writing a "1" to bit 6 of the configuration register, all other bits must be written with their original value in order to keep the current configuration. After setting the configuration register, wait at least 32 system clock cycles. To get the chip out of the power-down mode, clear bit 6 in the configuration register via a serial I/O port write operation. (CAUTION! In power-down mode, the SPI timeout (t_{SPTT}) will not function. Therefore, no partial SPI command should be sent. Otherwise, the sensor may go into a hang-up state). While the sensor is in power-down mode, only the bit 6 data will be written to the configuration register. Writing the other configuration register values will not have any effect. For an accurate report after power-up, wait for a total period of 50ms before the microcontroller is able to issue any write/read operation to the ADNS-5070. The sensor register settings, prior to power-down mode, will remain during power-down mode.

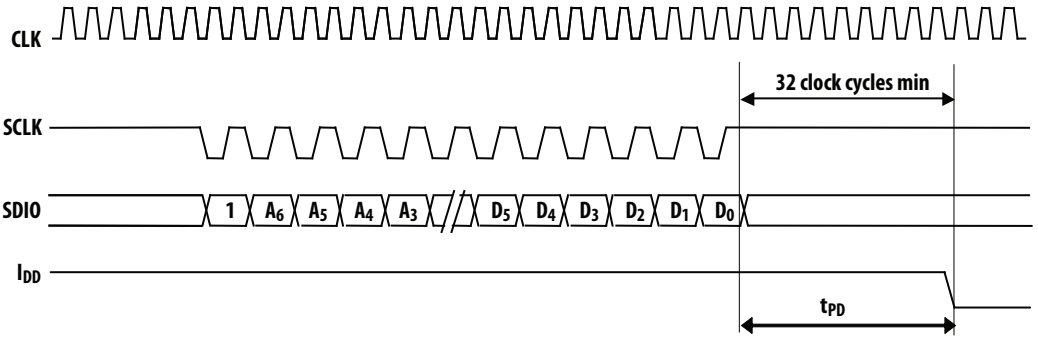


Figure 11: Power-down timing

The address of the configuration register is 1000000 (retail option).Assume that the original content of the configuration register is 0x00.

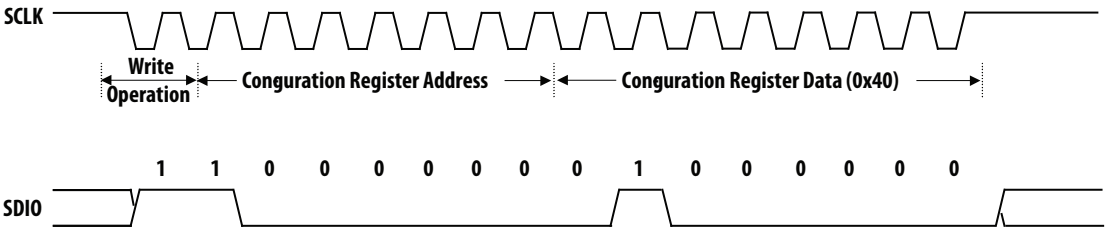


Figure 12: Power Down configuration register writing operation

Setting the power down bit simply sets the analog circuitry into a no current state.

Note: LED_CNTL and SDIO will be tri-stated during power down mode.

Typical Performance Characteristics

The following graphs (Figures 13-15) are the typical performance of the ADNS-5070 sensor, assembled as shown in the 2D assembly drawing with the HDNS-2100 Lens, the HDNS-2200 clip, and the HLMP-ED80-xx000 (See Figure 4).

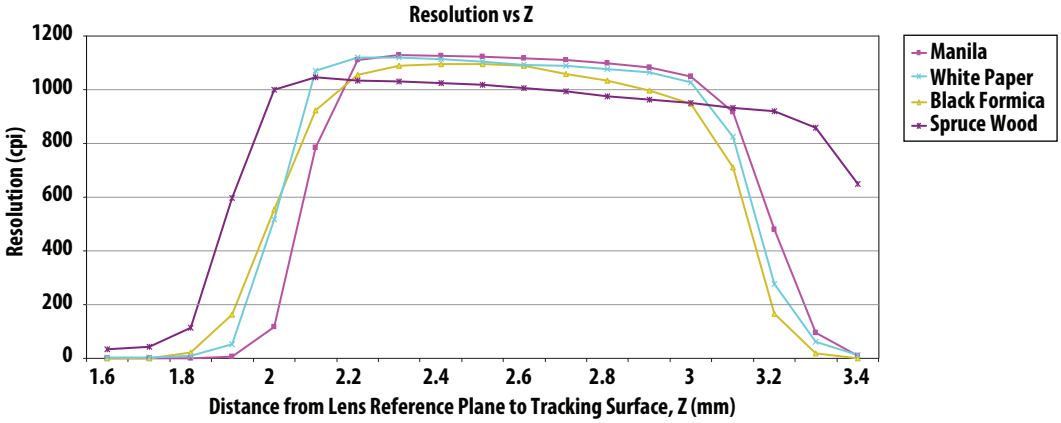


Figure 13. Resolution (based on 1050cpi setting) vs. Z (mm)

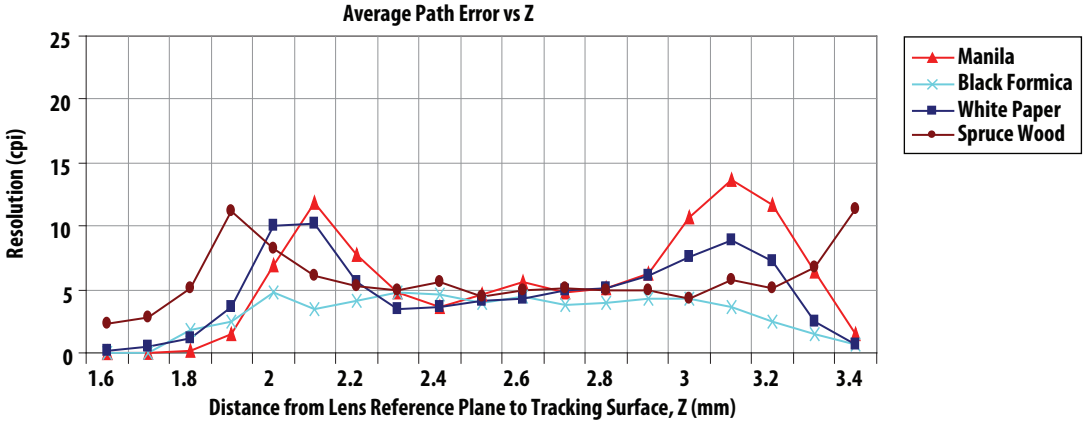


Figure 14. Average error vs. distance (mm)

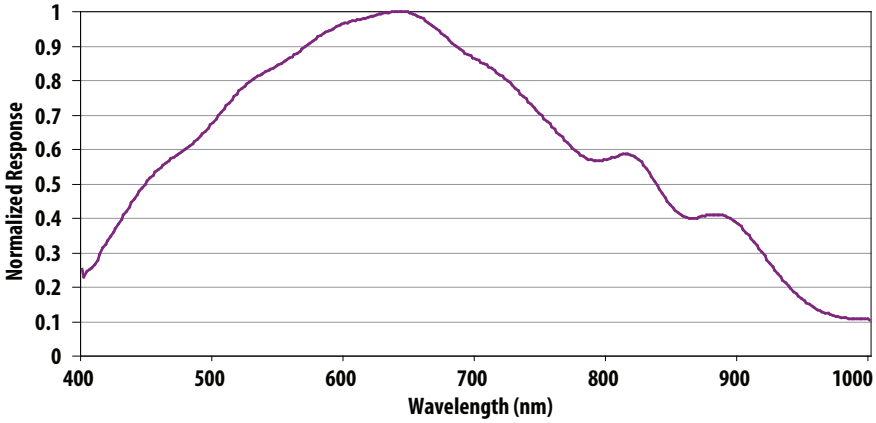


Figure 15. Relative wavelength responsivity

LED Mode

For optimized tracking performance, the LED is in DC mode when motion is detected, and ADNS-5070 will pulse the LED when the mouse is in idle state.

Synchronous Serial Port

The synchronous serial port is used to set and read parameters in the ADNS-5070, and to read out the motion information.

The port is a two wire, half duplex serial port. The host micro-controller always initiates communication; the ADNS-5070 never initiates data transfers.

The lines that comprise the SPI port:

SCLK: Clock input. It is always generated by the master (the micro-controller).

SDIO: Input and Output data.

Write Operation

Write operations, where data is going from the microcontroller to the ADNS-5070, is always initiated by the microcontroller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The transfer is synchronized by **SCLK**. The microcontroller changes **SDIO** on falling edges of **SCLK**. The ADNS-5070 reads **SDIO** on rising edges of **SCLK**.

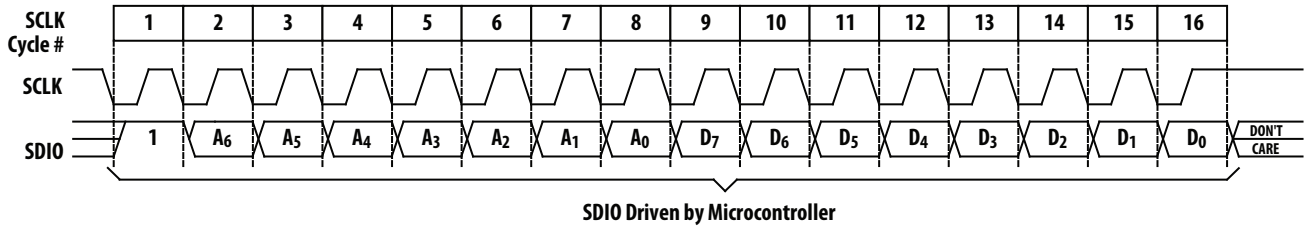


Figure 16. Write operation

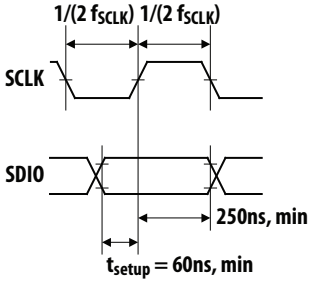


Figure 17. SDIO setup and hold times SCLK pulse width

Read Operation

A read operation, means data that is going from the ADNS-5070 to the microcontroller, is always initiated by the microcontroller and consists of two bytes. The first byte that contains the address is written by the microcontroller and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the ADNS-5070. The transfer is synchronized by **SCLK**. **SDIO** is changed on falling edges of **SCLK** and read on every rising edge of **SCLK**. The microcontroller must go to a high-Z state after the last address data bit. The ADNS-5070 will go to the high-Z state after the last data bit. Another thing to note during a read operation is that SCLK needs to be delayed after the last address data bit to ensure that the ADNS-5070 has at least 100 us to prepare the requested data. This is shown in the timing diagrams below (See Figures 18 to 20).

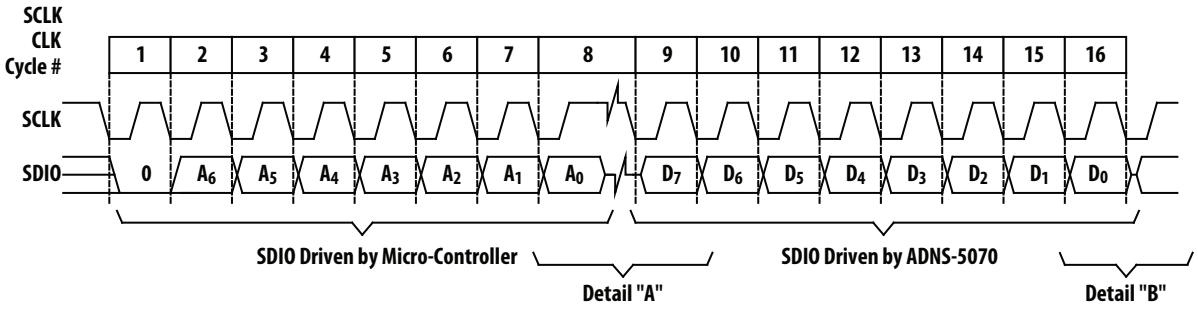


Figure 18. Read operation

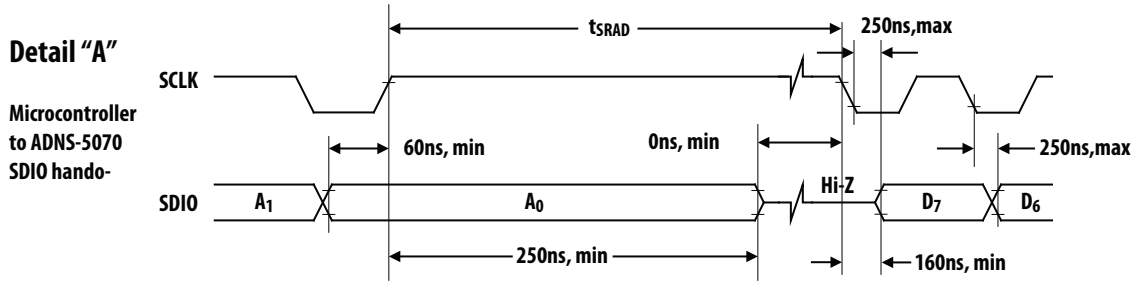


Figure 19. Microcontroller to ADNS-5070 SDIO handoff

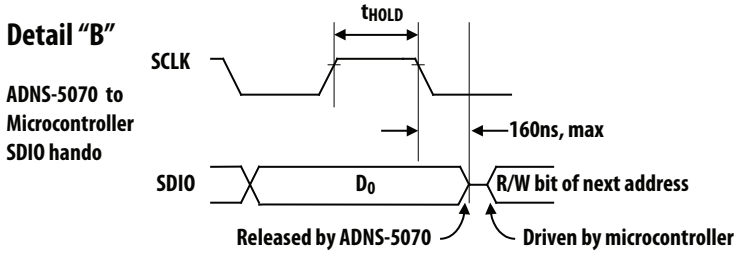


Figure 20. ADNS-5070 to microcontroller SDIO handoff

NOTE: The 250 ns high state of SCLK is the minimum data hold time of the ADNS-5070. Since the falling edge of SCLK is actually the start of the next read or write command, the ADNS-5070 will hold the state of D_0 on the SDIO line until the falling edge of SCLK. In both write and read operations, SCLK is driven by the microcontroller.

Forcing the SDIO line to the Hi-Z state

There are times when the SDIO line from the ADNS-5070 should be in the Hi-Z state. For example, if the microprocessor has completed a write to the ADNS-5070, the SDIO line will go into a Hi-Z state because the SDIO pin was configured as an input. However, if the last operation from the microprocessor was a read, the ADNS-5070 will hold the D0 state on SDIO until a falling edge of SCLK.

To place the SDIO pin into a Hi-Z state, activate the power-down mode by writing to the configuration register. Then, the power-down mode can stay activated, with the ADNS-5070 in the shutdown state. Or the powerdown mode can be deactivated, returning the ADNS-5070 to normal operation. In both conditions, the SDIO line will go into the Hi-Z state.

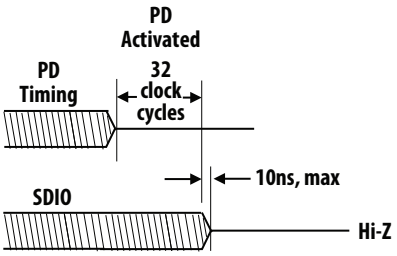


Figure 21. SDIO Hi-Z state and timing

Another method to put the SDIO line into the Hi-Z state, while maintaining the ADNS-5070 at normal mode, is to write any data to an invalid address such as 0x00 to address 0x77. The SDIO line will go into the Hi-Z state after the write operations.

Required Timing between Read and Write Commands (tsxx)

There are minimum timing requirements between read and write commands on the serial port.

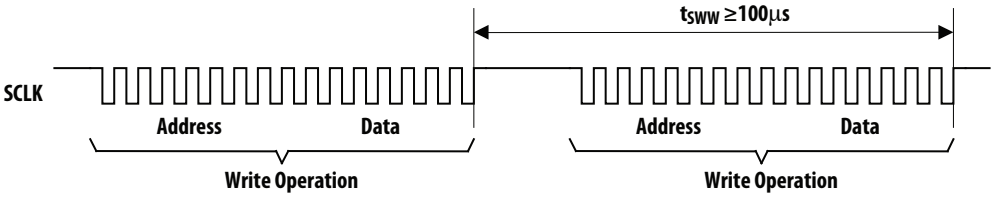


Figure 22. Timing between two write commands

If the rising edge of the SCLK for the last data bit of the second write command occurs before the 100 us required delay, then the first write command may not complete correctly.

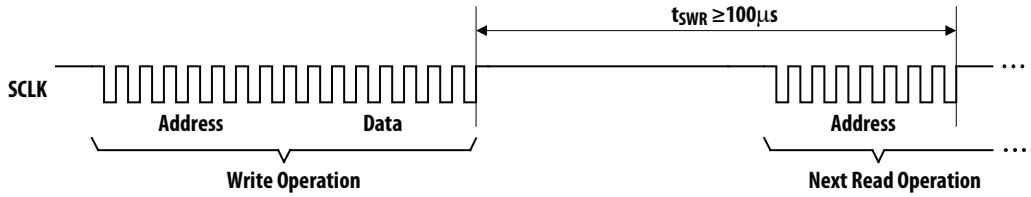


Figure 23. Timing between write and read commands

If the rising edge of SCLK for the last address bit of the read command occurs before the 100 us required delay, then the write command may not complete correctly.

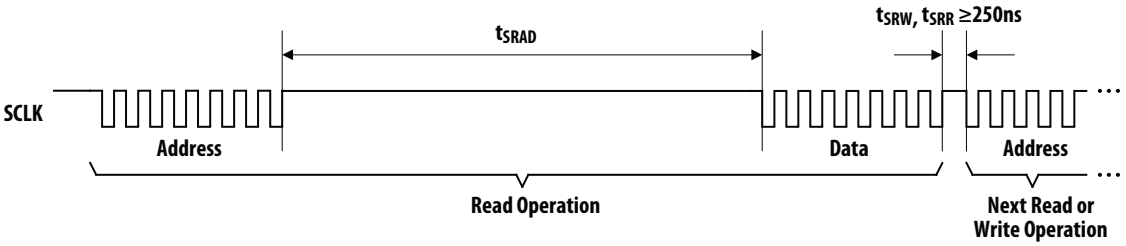


Figure 24. Timing between read and either write or subsequent read commands

The falling edge of SCLK for the first address bit of either the read or write command must be at least 250 ns after the last SCLK rising edge of the last data bit of the previous read operation.

Error Detection and Recovery

1. The ADNS-5070 and the microcontroller might get out of synchronization due to ESD events, power supply droops or microcontroller firmware flaws.
2. The ADNS-5070 has a transaction timer for the serial port. If the sixteenth SCLK rising edge is spaced more than approximately 90 milliseconds from the first SCLK edge of the current transaction, the serial port will reset.
3. Invalid addresses:
   - Writing to an invalid address will have no effect. Reading from an invalid address will return all zeros.
4. Collision detection on SDIO
   - The only time that the ADNS-5070 drives the SDIO line is during a READ operation. To avoid data collisions, the microcontroller should relinquish SDIO before the falling edge of SCLK after the last address bit. Then the ADNS-5070 begins to drive SDIO after the next rising edge of SCLK. Next, the ADNS-5070 relinquishes SDIO within 160 ns of the falling SCLK edge after the last data bit. The microcontroller can begin driving SDIO any time after that. In order to maintain low power consumption in normal operation or when the PD pin is set high, the microcontroller should not leave SDIO floating until the next transmission (although that will not cause any communication difficulties).
5. In case of synchronization failure, both the ADNS-5070 and the microcontroller may drive SDIO. The ADNS-5070 can withstand 30 mA of short circuit current and will withstand infinite duration short circuit conditions.
6. The microcontroller can verify a successful write operation by issuing a read command to the same address and comparing the written data to the read data.
7. The microcontroller can verify the synchronization of the serial port by periodically reading the product ID from status register (Address: 0x41).

Notes on Power-up and the Serial Port

The sequence in which V_{DD}, SCLK and SDIO are set during power-up can affect the operation of the serial port. The diagram below shows what can happen shortly after power-up when the microprocessor tries to read data from the serial port.

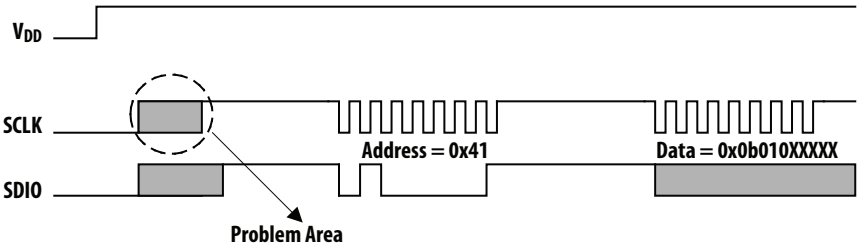


Figure 25. Power-up serial port sequence

This diagram shows the V_{DD} rising to valid levels, at some point the microcontroller starts it's program, sets the SCLK and SDIO lines to be outputs, and sets them high. Then, the microcontroller waits to ensure the ADNS-5070 has powered up and is ready to communicate. The microprocessor then tries to read from location 0x41, Status register, and is expecting a value of 0x0b010XXXXX. If it receives this value, then it knows the communication to the ADNS-5070 is operational.

The problem occurs if the ADNS-5070 powers up before the microprocessor sets the SCLK and SDIO lines to be outputs and high. The ADNS-5070 sees the raising of the SCLK as a valid rising edge, and clocks in the state of the SDIO as the first bit of the address (sets either a read or a write, depending upon the state).

In the case of a SDIO low, a read operation will start. When the microprocessor actually begins to send the address, the ADNS-5070 already has the first bit of an address. When the seventh bit is sent by the microprocessor, the ADNS-5070 has a valid address, and drives the SDIO line high within 250 ns (see detail "A" in Figure 18 and Figure 19). This results in a bus fight for SDIO. Since the address is wrong, the data sent back would be incorrect.

In the case of a SDIO high, a write operation will start. The address and data will be out of synchronization, causing the wrong data written to the wrong address.

Solution

One way to solve the problem is by waiting for the serial port timer to time out.

1. Serial Port Timer Timeout

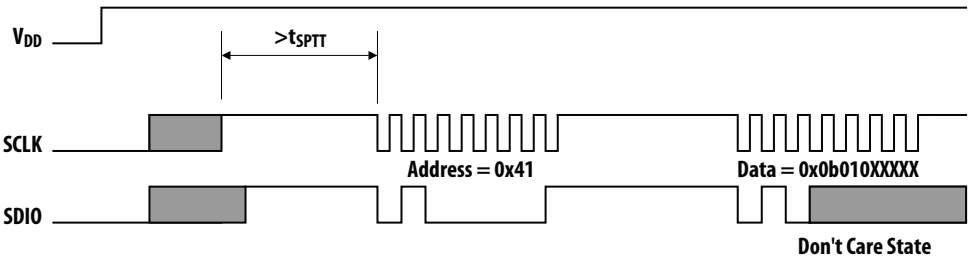


Figure 26. Power up serial port timer sequence

If the microprocessor waits at least t_{SPTT} from V_{DD} valid, it will ensure that the ADNS-5070 has powered up and the timer has timed out. This assumes that the microprocessor and the ADNS-5070 share the same power supply. If not, then the microprocessor must wait for t_{SPTT} from ADNS-5070 V_{DD} valid. Then when the SCLK toggles for the address, the ADNS-5070 will be in-sync with the microprocessor.

Resync Note

If the microprocessor and the ADNS-5070 get out of sync, then the data either written or read from the registers will be incorrect. An easy way to solve this is to use watchdog timer timeout sequence to resync the parts after an incorrect read.

Power-up

ADNS-5070 has an on-chip internal power-up reset (POR) circuit, which will reset the chip when VDD reaches the valid value for the chip to function.

Soft Reset

ADNS-5070 may also be given the reset command at any time via the serial I/O port. The timing and transactions are the same as those just specified for the power-up mode in the previous section.

The proper way to perform soft reset on ADNS-5070 is:

1. The microcontroller starts the transaction by sending a write operation containing the address of the configuration register and the data value of 0x80. Since the reset bit is set, ADNS-5070 will reset and any other bits written into the configuration register at this time is properly written into the Configuration Register. After the chip has been reset, very quickly, ADNS-5070 will clear the reset bit so there is no need for the microcontroller to re-write the Configuration Register to reset it.
2. The digital section is now ready to go. It takes 3 frames for the analog section to settle.

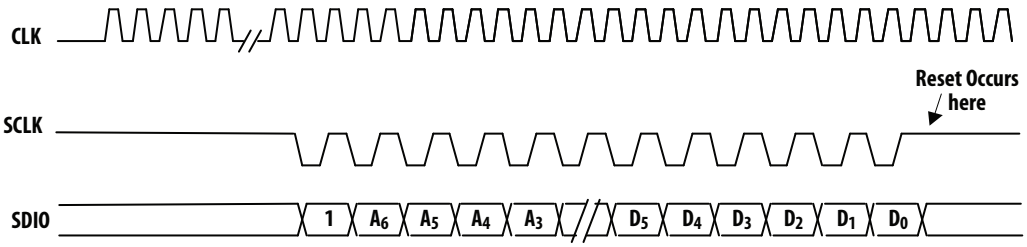


Figure 27. ADNS-5070 soft reset sequence timing

Soft reset will occur when writing 0x80 to the configuration register.

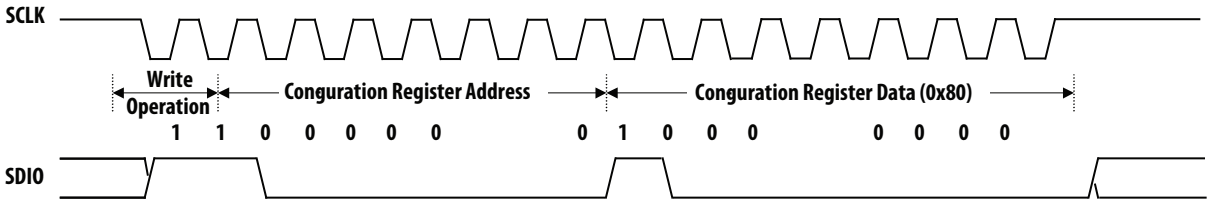


Figure 28. Soft reset configuration register writing operation

Registers

The ADNS-5070 registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Address	Register	Read/Write	Default Value
0x00	Configuration1	R/W	0x00
0x01	Status1	R	0x01
0x02	Delta_Y1	R	0x00
0x03	Delta_X1	R	0x00
0x04	SQUAL1	R	0x00
0x05	Maximum_Pixel1	R	0x00
0x06	Minimum_Pixel1	R	0x3f
0x07	Pixel_Sum1	R	0x00
0x08	Pixel_Data1	R	0x00
0x09	Shutter_Upper1	R	0x01
0x0a	Shutter_Lower1	R	0x00
0x0b	Pixel_Grab	R/W	0x00
0x14	Product_ID2a	R	0x10
0x15	Product_ID2b	R	0x2N
0x16	Motion2	R	0x00
0x17	Delta_X2	R	0x00
0x18	Delta_Y2	R	0x00
0x19	SQUAL2	R	0x00
0x1a	Operation_Mode2	R/W	0x04
0x1b	Configuration2	R/W	0x00
0x33	Mouse_Control	R/W	0x07
0x40	Configuration3	R/W	0x00
0x41	Status3	R	0x41
0x42	Delta_Y3	R	0x00
0x43	Delta_X3	R	0x00
0x44	SQUAL3	R	0x00
0x45	Maximum_Pixel3	R	0x00
0x46	Minimum_Pixel3	R	0x3f
0x47	Pixel_Sum3	R	0x00
0x48	Pixel_Data3	R	0x00
0x49	Shutter_Upper3	R	0x01
0x4a	Shutter_Lower3	R	0x00

Configuration1 Address: 0x00
Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Reset	PD	Reserved [1:5]					FWake

Data Type: Bit field

USAGE: The Configuration register allows the user to change the configuration of the sensor. Shown below are the bits, their default values, and optional values.

Field Name	**Description**
Reset	Reset **0 = Normal operation** 1 = Reset the part
PD	Power down **0 = Normal operation** 1 = power down all analog circuitry
FWake	Forced Awake Mode **0 = Normal, fall asleep after one second of no movement** 1 = Always awake

Status1 Address: 0x01
Access: Read Reset Value: 0x01

Bit	7	6	5	4	3	2	1	0
Field	ID_2	ID_1	ID_0			Reserved		Awake

Data Type: Bit field

USAGE: Status information and type of mouse sensor, current state of the mouse.

Field Name	**Description**
ID_2 - ID_0	Product ID (0b000)
Awake	Mouse State **0 = Asleep** 1 = Awake

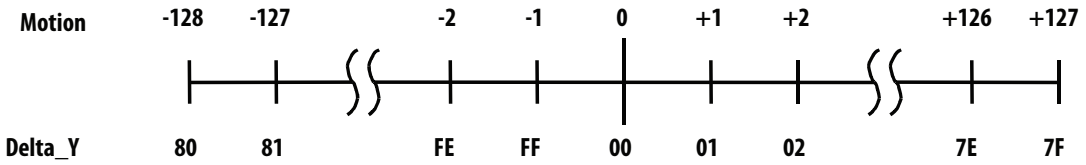
Delta_Y1
Access: Read

Address: 0x02
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0

Data Type: Eight bit 2's complement number.

USAGE: Y movement is counted since last report. Absolute value is determined by resolution. Reading clears the register.



NOTES: Register 0x02 MUST be read prior to Register 0x03.

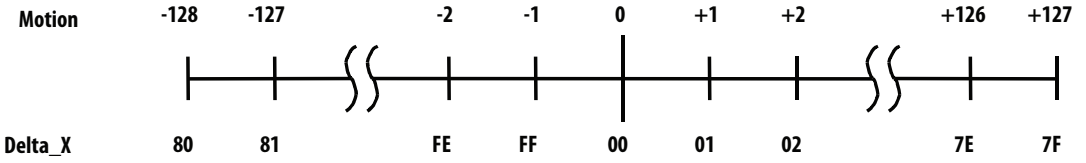
Delta_X1
Access: Read

Address: 0x03
Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0

Data Type: Eight bit 2's complement number.

USAGE: X movement is counted since last report. Absolute value is determined by resolution. Reading clears the register.



NOTES: Register 0x02 MUST be read prior to Register 0x03.