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ADNS-6090

Gaming Laser Mouse Sensor

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

Description

The Avago Technologies ADNS-6090 sensor along with the ADNS-6120 or ADNS-6130-001 lens, ADNS-6230-001 clip and ADNV-6340 laser diode form a complete and compact laser mouse tracking system. It is the laser illuminated gaming mouse system enabled for high performance navigation. Driven by Avago's LaserStream Technology, it can operate on many surfaces that prove difficult for traditional LED-based optical navigation. It's high performance architecture is capable of sensing high-speed mouse motion - with resolution up to 1600 counts per inch, velocities up to max of 65 inches per second and acceleration up to 20g. This sensor is powered for the high sensitive user.

There is no moving part in the complete assembly for ADNS-6090 laser mouse system, thus it is high reliability and less maintenance for the end user. In additional, precision optical alignment is not required, facilitating high volume assembly.

Theory of Operation

The ADNS-6090 is based on LaserStream technology, which measures changes in position by optically acquiring sequential images (frames) and mathematically determining the direction and magnitude of movement.

ADNS-6090 contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a four wire serial port. The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Δx and Δy relative displacement values.

An external microcontroller reads the Δx and Δy information from the sensor serial port. The microcontroller then translates the data into PS2 or USB signals before sending them to the host PC or game console.

Features

- High speed motion detection – up to max of 65ips and 20g
- LaserStream architecture for greatly improved optical navigation technology
- Programmable frame rate over 7200 frames per second
- SmartSpeed self-adjusting frame rate for optimum performance
- Serial port burst mode for fast data transfer
- 800/1200/1600/2000/2400/3000cpi selectable resolution
- Single 3.3 volts power supply
- Four-wire serial port along with Power Down and Reset pins
- Laser fault detect circuitry on-chip

Applications

- Laser mice for game consoles and computer games
- Laser mice for desktop PC's, Workstations, and portable PC's
- Laser trackballs
- Integrated input devices

Pinout

Pin	Name	Description
1	NCS	Chip select (active low input)
2	MISO	Serial data output (Master In/Slave Out)
3	SCLK	Serial clock input
4	MOSI	Serial data input (Master Out/Slave In)
5	NC	No Connection
6	RESET	Reset input
7	NPD	Power down (active low input)
8	OSC_OUT	Oscillator output
9	GUARD	Oscillator GND for PCB guard (optional)
10	OSC_IN	Oscillator input
11	REFC	Reference capacitor
12	REFB	Reference capacitor
13	R_{BIN}	Binning Resistor to set XY_LASER current
14	XY_LASER	LASER current output
15	NC	No Connection
16	V_{DD3}	Supply voltage
17	GND	Ground
18	V_{DD3}	Supply voltage
19	GND	Ground
20	LASER_ NEN	Laser enable (active low)

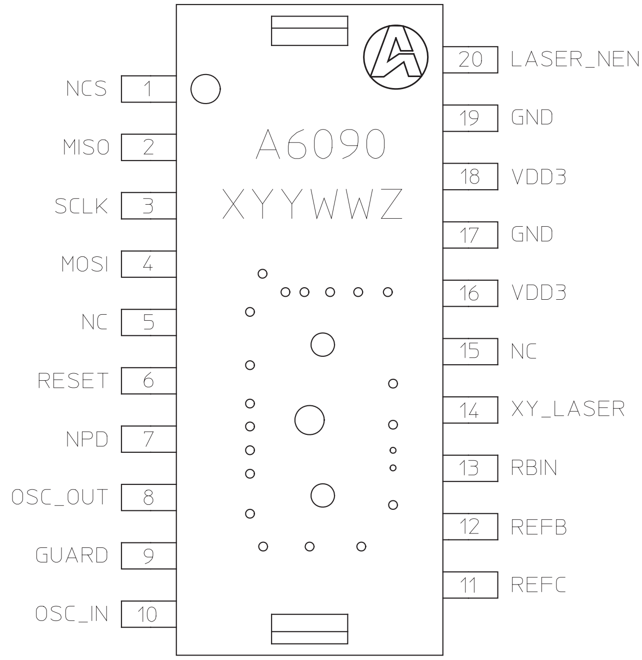
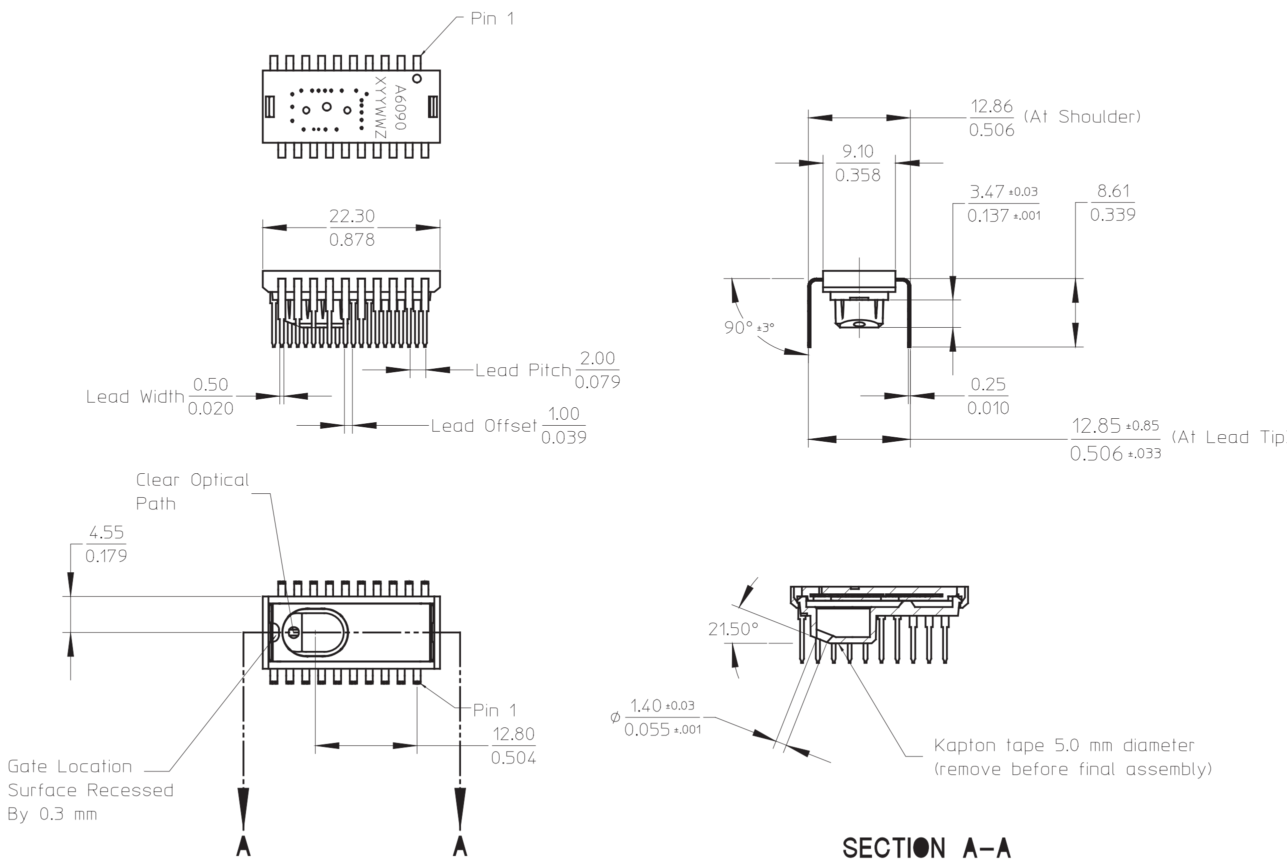


Figure 1. Package outline drawing (top view)



Notes:
1. Dimensions in millimeters (inches).
2. Dimensional tolerance: ±0.1 mm.
3. Coplanarity of leads: 0.1 mm.
4. Lead pitch tolerance: ± 0.15 mm.
5. Cummulative pitch tolerance: ± 0.15 mm.
6. Angular tolerance: ± 3.0°.
7. Maximum flash + 0.2 mm.
8. Chamfer (25° x 2) on the taper side of the lead.

Figure 2. Package outline drawing

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Overview of Laser Mouse Sensor Assembly

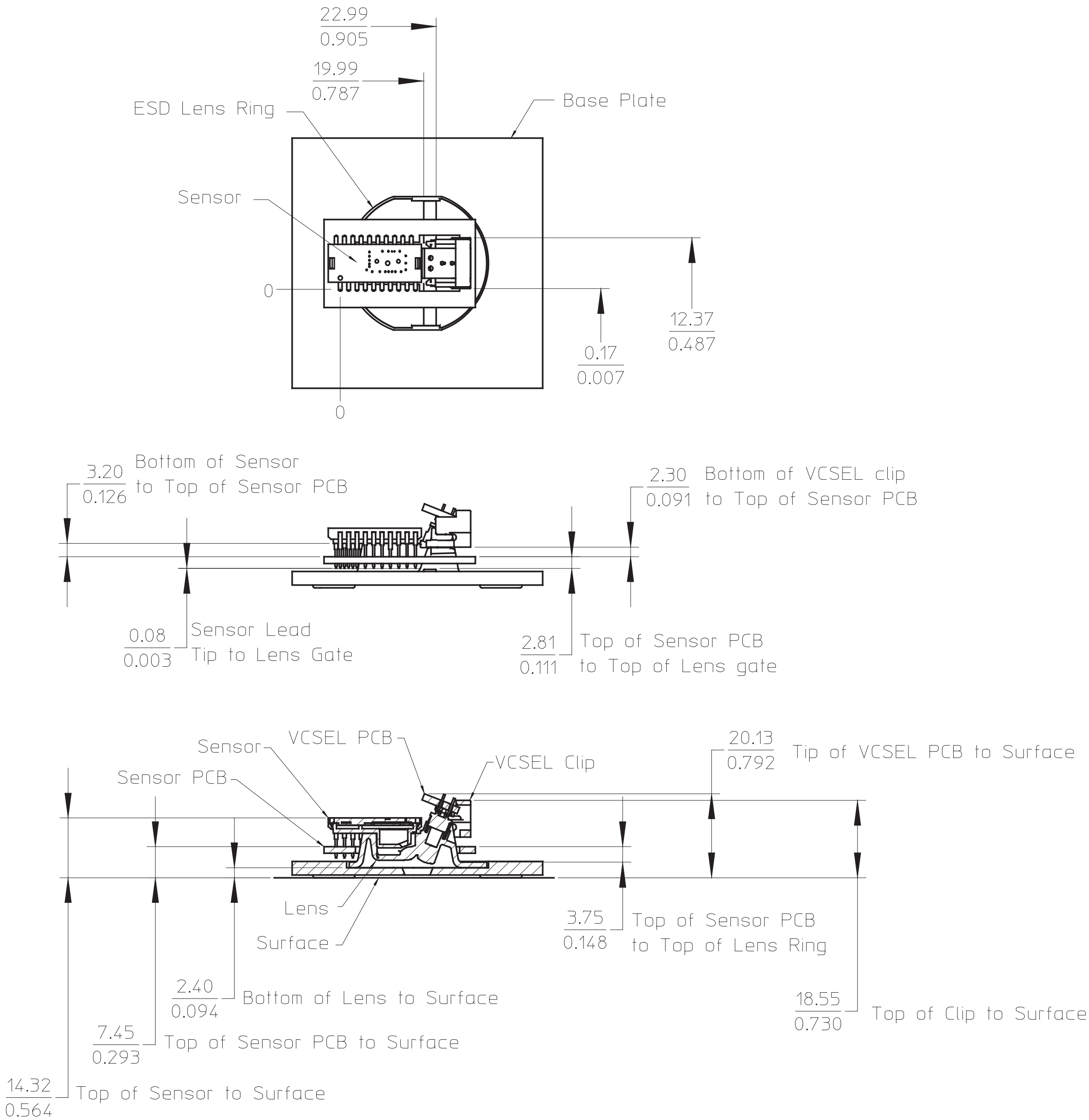


Figure 3. Assembly drawing of ADNS-6090 (top, front and cross-sectional view)

2D Assembly Drawing of ADNS-6090, PCBs and Base Plate

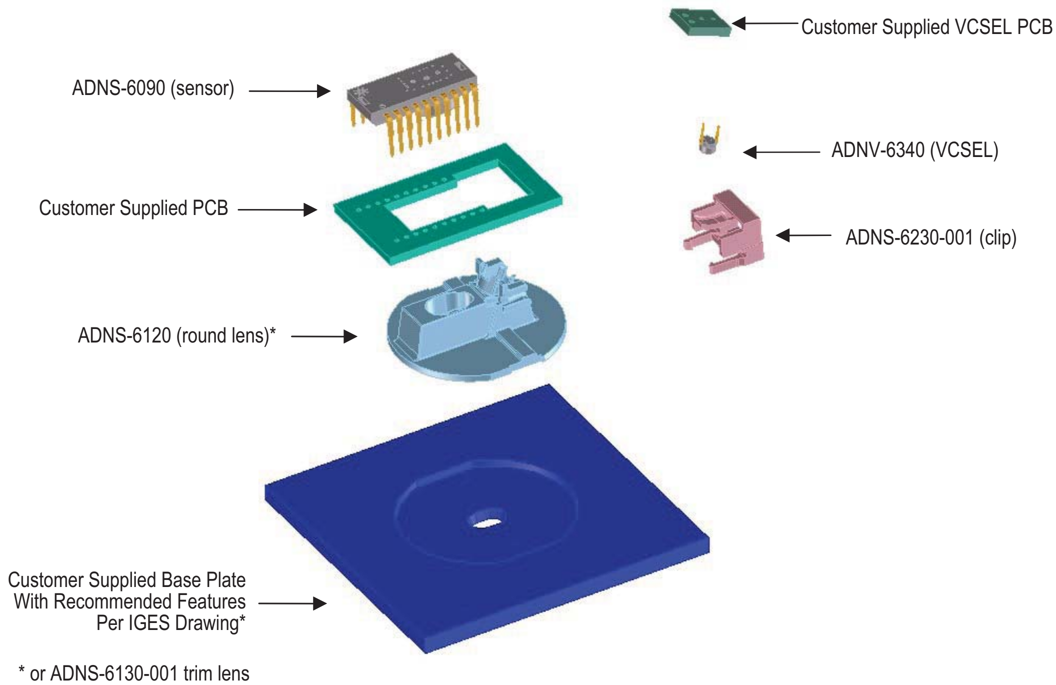


Figure 4. Exploded view drawing

Shown with ADNS-6120 Laser Mouse Lens, ADNS-6230-001 VCSEL Assembly Clip and ADNV-6340 VCSEL. The components interlock as they are mounted onto defined features on the base plate.

The ADNS-6090 laser mouse sensor is designed for mounting on a through-hole PCB, looking down. There is an aperture stop and features on the package that align to the lens.

The ADNV-6340 VCSEL provides a laser diode with a single longitudinal and a single transverse mode. It is particularly suited as lower power consumption and highly coherent replacement of LEDs. It also provides wider operation range while still remaining within single-mode, reliable operating conditions.

The ADNS-6120 or ADNS-6130-001 Laser Mouse Lens is designed for use with ADNS-6090 sensor and the illumination subsystem provided by the assembly clip and the VCSEL. Together with the VCSEL, the ADNS-6120 or ADNS-6130-001 lens provides the directed illumination and optical imaging necessary for proper operation of the Laser Mouse Sensor. ADNS-6120 and ADNS-6130-001 are precision molded optical component and should be handled with care to avoid scratching of the optical surfaces. ADNS-6120 also has a large round flange to provide a long creepage path for any ESD events that occur at the opening of the base plate.

The ADNS-6230-001 VCSEL Assembly Clip is designed to provide mechanical coupling of the ADNV-6340 VCSEL to the ADNS-6120 or ADNS-6130-001lens. This coupling is essential to achieve the proper illumination alignment required for the sensor to operate on a wide variety of surfaces.

Avago Technologies provides an IGES file drawing describing the base plate molding features for lens and PCB alignment.

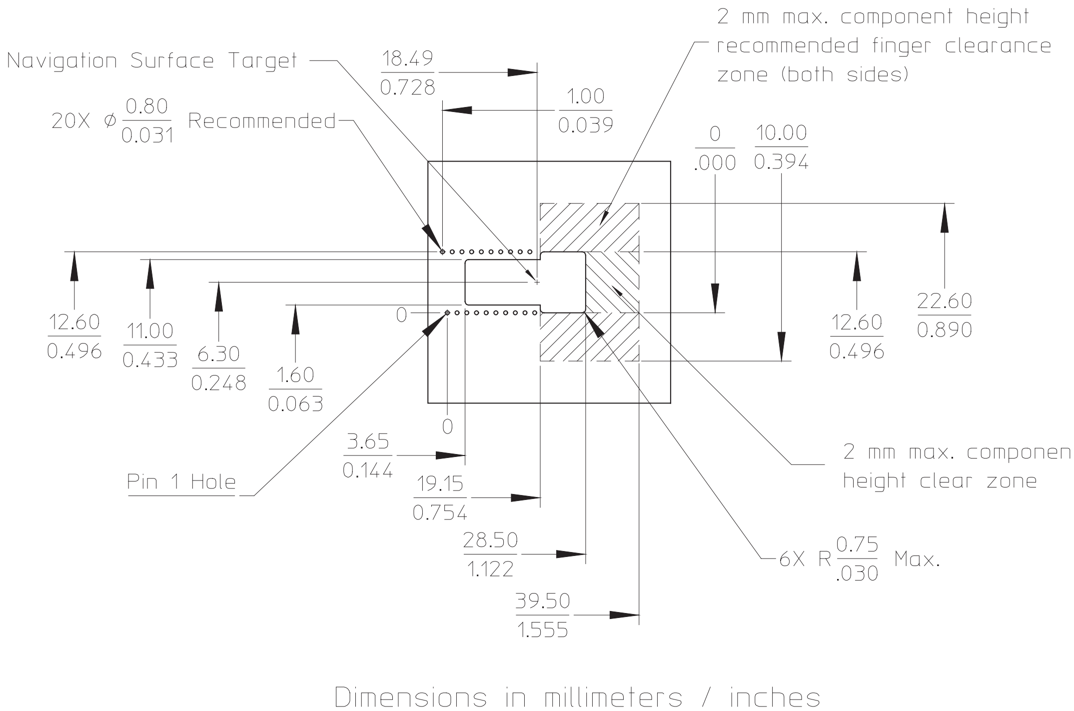


Figure 5. Recommended PCB mechanical cutouts and spacing

Assembly Recommendation

1. Insert the sensor and all other electrical components into the application PCB (main PCB board and VCSEL PCB board).
2. Wave Solder the entire assembly in a no-wash solder process utilizing a solder fixture. The solder fixture is needed to protect the sensor during the solder process. It also sets the correct sensor-to -PCB distance, as the lead shoulders do not normally rest on the PCB surface. The fixture should be designed to expose the sensor leads to solder while shielding the optical aperture from direct solder contact.
3. Place the lens onto the base plate.
4. Remove the protective kapton tape from the optical aperture of the sensor. Care must be taken to keep contaminants from entering the aperture.
5. Insert the PCB assembly over the lens onto the base plate. The sensor aperture ring should self-align to the lens. The optical position reference for the PCB is set by the base plate and lens. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
6. Remove the protective kapton tape from the VCSEL.
7. Insert the VCSEL assembly into the lens.
8. Slide the clip in place until it latches. This locks the VCSEL and lens together.
9. Install the mouse top case. There must be a feature in the top case (or other area) to press down onto the sensor to ensure the sensor and lens are interlocked to the correct vertical height.

Design considerations for improving ESD Performance

For improved electrostatic discharge performance, typical creepage and clearance distance are shown in the table below. Assumption: base plate construction as per the Avago supplied IGES file for ADNS-6120 round lens.

Typical Distance	Millimeters
Creepage	12.0
Clearance	2.1

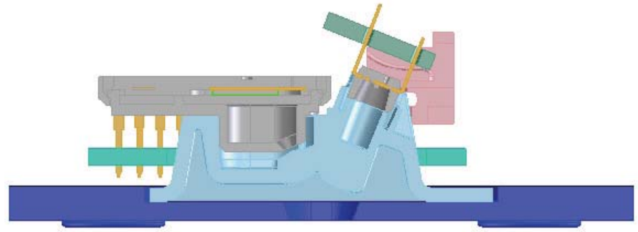


Figure 6. Cross section of PCB assembly

The lens flange can be sealed (i.e. glued) to the base plate. Note that the lens material is polycarbonate and therefore, cyanoacrylate based adhesives or other adhesives that may damage the lens should NOT be used.

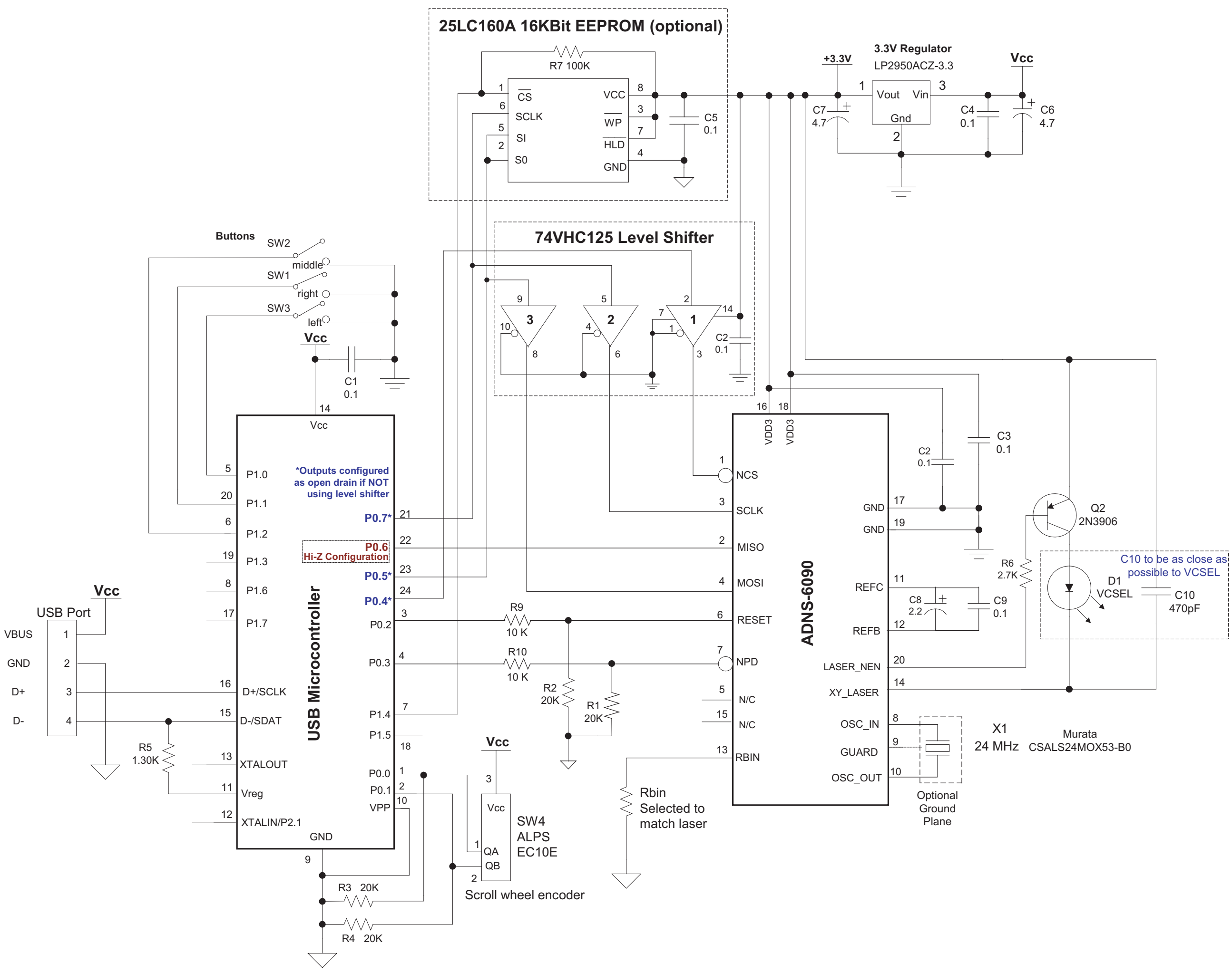


Figure 7. Schematic Diagram for 3-Button Scroll Wheel USB PS/2 Mouse - Regulator Bypass

Laser Bin Table

Bin Number	Rbin Resistor Value (kohm)
2A	18.7
3A	12.7

Notes

- Caps for pins 11, 12, 16 and 18 MUST have trace lengths LESS than 5 mm on each side.
- Pins 16 and 18 caps MUST use pin 17 GND.
- Pin 9, if used, should not be connected to PCB GND to reduce potential RF emissions.
- The 0.1 µF caps must be ceramic.
- Caps should have less than 5 nH of self inductance.
- Caps should have less than 0.2 Ω ESR.
- NC pins should not be connected to any traces.
- Surface mount parts are recommended.
- Care must be taken when interfacing a 5V microcontroller to the ADNS-6090. Serial port inputs on the sensor should be connected to open-drain outputs from the microcontroller or use an active drive level shifter. NPD and RESET should be connected to 5V microcontroller outputs through a resistor divider or other level shifting technique.
- V_{DD3} and GND should have low impedance connections to the power supply.
- Because the R_{BIN} pin sets the XY_LASER current, the following PC board layout practices should be followed to reduce the chance of uncontrolled laser drive current caused from a leakage path between R_{BIN} and ground. One hypothetical source of such a leakage path is PC board contamination due to a liquid, such as a soft drink, being deposited on the printed circuit board.
- The R_{BIN} resistor should be located close to the sensor pin 13. The traces between the resistor and the sensor should be short.
- The pin 13 solder pad and all exposed conductors connected to pin 13 should be surrounded by a guard trace connected to V_{DD3} and devoid of solder mask.
- The pin 13 solder pad, the traces connected to pin 13, and the R_{BIN} resistor should be covered with a conformal coating.
- The R_{BIN} resistor should be a thru-hole style to increase the distance between its terminals. This does not apply if a conformal coating is used.

External PROM

The ADNS-6090 must operate from externally loaded programming. This architecture enables immediate adoption of new features and improved performance algorithms. The external program is supplied by Avago as a file, which may be burned into a programmable device. The example application shown in this document uses an EEPROM to store and load the external program memory. A micro-controller with sufficient memory may be used instead. On power-up and reset, the ADNS-6090 program is downloaded into volatile memory using the burst-mode procedure described in the Synchronous Serial Port section. The program size is 1986 x 8 bits.

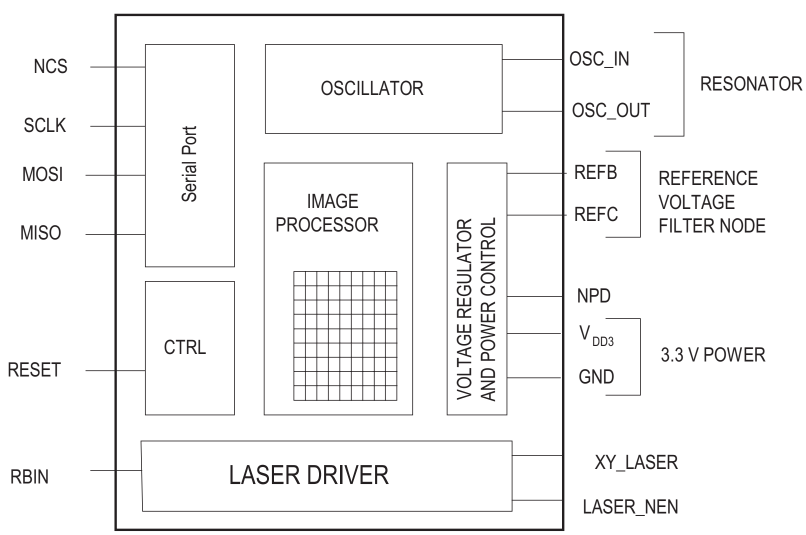


Figure 8. Block diagram of ADNS-6090 optical mouse sensor

LASER Drive Mode

The LASER has 2 modes of operation: DC and Shutter. In DC mode, the LASER is on at all times the chip is powered except when in the power down mode via the NPD pin. In shutter mode the LASER is on only during the portion of the frame that light is required. The LASER mode is set by the LASER_MODE bit in the Configuration_bits register. For optimum product lifetime, Avago recommends the default Shutter mode setting (except for calibration and test).

Eye Safety

The ADNS-6090 and the associated components in the schematic of Figure 7 are intended to comply with Class 1 Eye Safety Requirements of IEC 60825-1. Avago Technologies suggests that manufacturers perform testing to verify eye safety on each mouse. It is also recommended to review possible single fault mechanisms beyond those described below in the section "Single Fault Detection".

Under normal conditions, the ADNS-6090 generates the drive current for the laser diode (ADNV-6340). In order to stay below the Class 1 power requirements, resistor R_{bin} must be set at least as high as the value in the bin table of Figure 7, based on the bin number of the laser diode and LP_CFG0 and LP_CFG1 must be programmed to appropriate values. Avago recommends using the exact R_{bin} value specified in the bin table to ensure sufficient laser power for navigation. The system comprised of the ADNS-6090 and ADNV-6340 is designed to maintain the output beam power within Class 1 requirements over component manufacturing tolerances and the recommended temperature range when adjusted per the procedure below and when implemented as shown in the recommended application circuit of Figure 7. For more information, please refer to Application Note AN5088 on the eye safety calculation.

LASER Power Adjustment Procedure

1. The ambient temperature should be 25°C +/- 5°C.
2. Set V_{DD3} to its permanent value.
3. Ensure that the laser drive is at 100% duty cycle.
4. Program the LP_CFG0 and LP_CFG1 registers to achieve an output power as close to 506uW as possible without exceeding it.

Good engineering practices should be used to guarantee performance, reliability and safety for the product design. Avago has additional information and detail, such as firmware practices, PCB layout suggestions, and manufacturing procedures and specifications that could be provided.

LASER Output Power

The laser beam output power as measured at the navigation surface plane is specified below. The following conditions apply:

1. The system is adjusted according to the above procedure.
2. The system is operated within the recommended operating temperature range.
3. The V_{DD3} value is no greater than 50mV above its value at the time of adjustment.
4. No allowance for optical power meter accuracy is assumed.

Disabling the LASER

LASER_NEN is connected to the base of a PNP transistor which when ON connects V_{DD3} to the LASER. In normal operation, LASER_NEN is low. In the case of a fault condition (ground at XY_LASER or R_{BIN}), LASER_NEN goes high to turn the transistor off and disconnect V_{DD3} from the LASER.

Single Fault Detection

ADNS-6090 is able to detect a short circuit, or fault, condition at the R_{BIN} and XY_LASER pins, which could lead to excessive laser power output. A low resistance path to ground on either of these pins will trigger the fault detection circuit, which will turn off the laser drive current source and set the LASER_NEN output high. When used in combination with external components as shown in the block diagram below, the system will prevent excess laser power for a single short to ground at R_{BIN} or XY_LASER by shutting off the laser. Refer to the PC board layout notes for recommendations to reduce the chance of high resistance paths to ground existing due to PC board contamination.

In addition to the continuous fault detection described above, an additional test is executed automatically whenever the LP_CFG0 register is written to. This test will check for a short to ground on the XY_LASER pin, a short to V_{DD3} on the XY_LASER pin, and will test the fault detection circuit on the XY_LASER pin.

Parameter	Symbol	Minimum	Maximum	Units	Notes
Laser output power	LOP		716	µW	Per conditions above

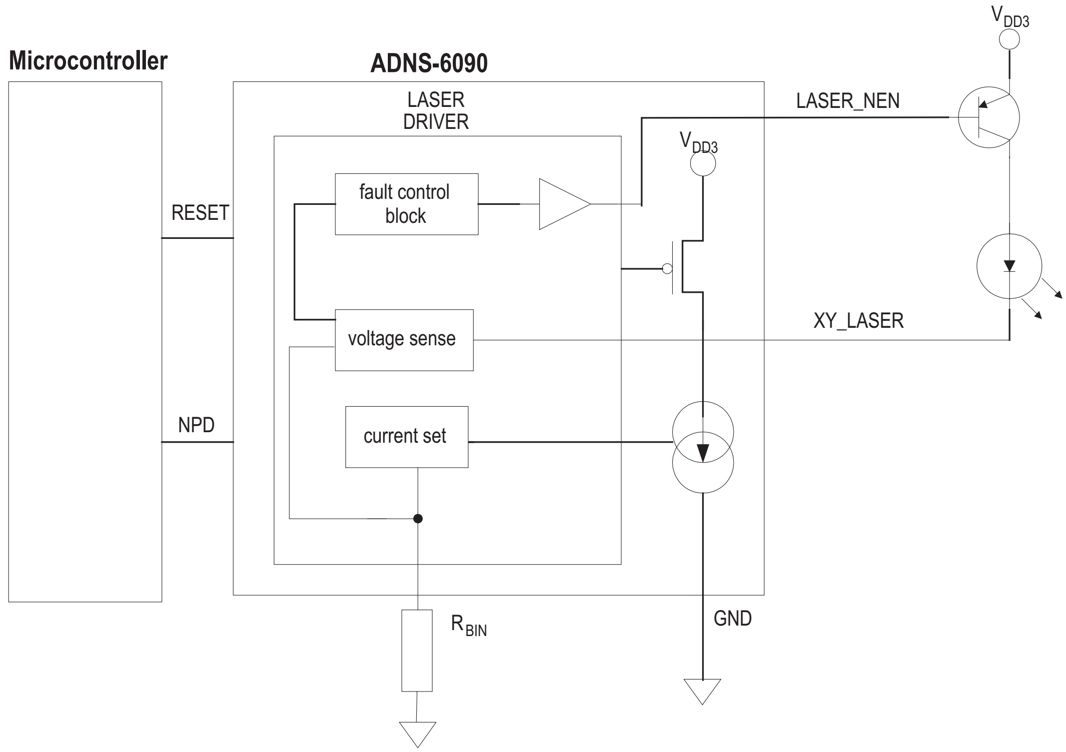


Figure 9. Single Fault Detection and Eye-safety Feature Block Diagram

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with shielded cable and following Avago recommendations.
- Passes IEC-1000-4-3 radiated susceptibility level when assembled into a mouse with shielded cable and following Avago recommendations.
- Passes EN61000-4-4/IEC801-4 EFT tests when assembled into a mouse with shielded cable and following Avago recommendations.
- UL flammability level UL94 V-0.

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Operating Temperature	T_A	-15	55	°C	
Lead Solder Temp			260	°C	For 10 seconds, 1.6mm below seating plane.
Supply Voltage	V_{DD3}	-0.5	3.7	V	
ESD			2	kV	All pins, human body model MIL 883 Method 3015
Input Voltage	V_{IN}	-0.5	V_{DD3}+0.5	V	NPD, NCS, MOSI, SCLK, RESET, OSC_IN, OSC_OUT, REFC, R_{BIN}
Output current	I_{OUT}		7	mA	MISO, LASER_NEN
Input Current	I_{IN}		15	mA	XY_LASER current with RBIN 12.7KΩ LP_CFG0=0x00; LP_CFG1=0xFF

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Operating Temperature	T_A	0		40	°C	
Power supply voltage	V_{DD3}	3.10	3.30	3.60	Volts	
Power supply rise time	V_{RT}	1			µs	0 to 3.0V
Supply noise (Sinusoidal)	V_{NB}			30 80	mV p-p	10kHz- 300KHZ 300KHz-50MHz
Oscillator Frequency	f_{CLK}	23	24	25	MHz	Set by ceramic resonator
Serial Port Clock Frequency	f_{SCLK}			2 500	MHz kHz	Active drive, 50% duty cycle Open drain drive with pull-ups on, 50 pF load
Resonator Impedance	X_{RES}			55	Ω	
Distance from lens reference plane to surface	Z	2.18	2.40	2.62	mm	Results in +/- 0.22 mm minimum DOF, see Figure 10
Speed	S		45	65	in/sec	Max limit is based on these surfaces : White Paper, Photo Paper, White Formica, Black Formice, Spruce/White Pine
Acceleration	A			20	g	
Frame Rate	FR	2000		7200	Frames/ second	See Frame_Period register section
Resistor value for LASER Drive Current set	R_{bin}	See Laser Bin Table in Figure 7			kΩ	Using ADNV-6340 VCSEL
Voltage at XY_LASER	V_{XY_LASER}	0.7		V_{DD3}	V	

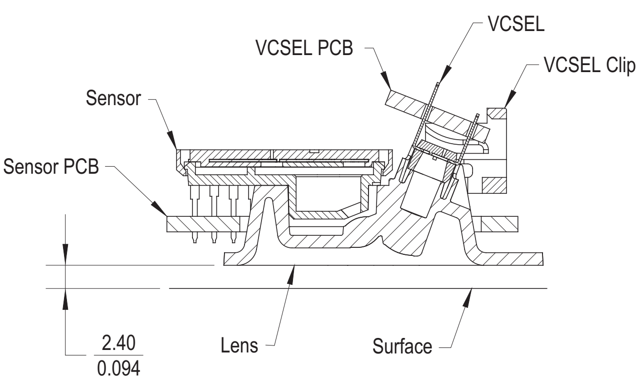


Figure 10. Distance from lens reference plane to surface

AC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, V_{DD3}=3.3V, fclk=24MHz.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
VDD to RESET	t_{OP}			250	µs	From VDD = 3.0V to RESET sampled
Data delay after RESET	$t_{PU\text{-}RESET}$			180	ms	From RESET falling edge to valid motion data at 2000 fps and shutter bound 20k.
Input delay after reset	$t_{IN\text{-}RST}$			550	µs	From RESET falling edge to inputs active (NPD, MOSI, NCS, SCLK)
Power Down	t_{PD}			600	µs	From NPD falling edge to initiate the power down cycle at 2000fps (t_{PD} = 1 frame period + 100µs)
Wake from NPD	t_{PUPD}		$t_{COMPUTE}$	75	ms	From NPD rising edge to valid motion data at 2000 fps and shutter bound 8610. Max assumes surface change while NPD is low
Data delay after NPD	$t_{COMPUTE}$			3.1	ms	From NPD rising edge to all registers contain data from new images at 2000fps (See Figure 11).
RESET pulse width	$t_{PW\text{-}RESET}$	10			µs	
MISO rise time	$t_{r\text{-}MISO}$		40	200	ns	C_L = 50pF
MISO fall time	$t_{f\text{-}MISO}$		40	200	ns	C_L = 50pF
MISO delay after SCLK	$t_{DLY\text{-}MISO}$			120	ns	From SCLK falling edge to MISO data valid, no load conditions
MISO hold time	$t_{hold\text{-}MISO}$	250			ns	Data held until next falling SCLK edge
MOSI hold time	$t_{hold\text{-}MOSI}$	200			ns	Amount of time data is valid after SCLK rising edge
MOSI setup time	$t_{setup\text{-}MOSI}$	120			ns	From data valid to SCLK rising edge
SPI time between write commands	t_{SWW}	50			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI time between write and read commands	t_{SWR}	50			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte.
SPI time between read and subsequent commands	t_{SRW} t_{SRR}	250			ns	From rising SCLK for last bit of the first data byte, to falling SCLK for first bit of the second address byte.
SPI read address-data delay	t_{SRAD}	50			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read. All registers except Motion & Motion_Burst
SPI motion read address-data delay	$t_{SRAD\text{-}MOT}$	75			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read. Applies to 0x02 Motion, and 0x50 Motion_Burst, registers
NCS to SCLK active	$t_{NCS\text{-}SCLK}$	120			ns	From NCS falling edge to first SCLK rising edge
SCLK to NCS inactive	$t_{SCLK\text{-}NCS}$	120			ns	From last SCLK falling edge to NCS rising edge, for valid MISO data transfer
NCS to MISO high-Z	$t_{NCS\text{-}MISO}$			250	ns	From NCS rising edge to MISO high-Z state
PROM download and frame capture byte-to-byte delay	t_{LOAD}	10			µs	(See Figure 24 and 25)
NCS to burst mode exit	t_{BEXIT}	4			µs	Time NCS must be held high to exit burst mode
Transient Supply Current	I_{DDT}			68	mA	Max supply current during a V_{DD3} ramp from 0 to 3.67 V
Input Capacitance	C_{IN}		14-22		pF	OSC_IN, OSC_OUT

DC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, V_{DD3}=3.3 V.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
DC Supply Current	I_{DD_AVG}			53	mA	DC average at 7200 fps. No DC load on XY_LASER, MISO.
Power Down Supply Current	I_{DDPD}		5	9	µA	NPD=GND; SCLK, MOSI, NCS=GND or V_{DD3}; RESET=V_{DD3}
Input Low Voltage	V_{IL}			0.8	V	SCLK, MOSI, NPD, NCS, RESET
Input High Voltage	V_{IH}	0.7 * V_{DD3}			V	SCLK, MOSI, NPD, NCS, RESET
Input hysteresis	V_{I_HYS}		200		mV	SCLK, MOSI, NPD, NCS, RESET
Input current, pull-up disabled	I_{IH_DPU}		0	±10	µA	Vin = 0.8*VDD3, SCLK, MOSI, NCS
Input current, CMOS inputs	I_{IH}		0	±10	µA	NPD, RESET, Vin=0.8*V_{DD3}
Output current, pulled-up inputs	I_{OH_PU}	150	300	600	µA	Vin = 0.2V, SCLK, MOSI, NCS; See bit 2 in Extended_Config register
XY_LASER Current	I_{LAS}		146/R_{bin}		A	V_{XY_LASER} >= 0.7 V LP_CFG0 = 0x00, LP_CFG1 = 0xFF
XY_LASER Current (fault mode)	I_{LAS}			500	µA	R_{bin} < 50 Ohms, or V_{XY_LASER} <0.2V
Output Low Voltage, MISO, LASER_NEN	V_{OL}			0.6	V	Iout=2mA, MISO Iout= 1mA, LASER_NEN
Output High Voltage, MISO, LASER_NEN	V_{OH}	0.8*V_{DD3}			V	Iout=-2mA, MISO Iout= -0.5mA, LASER_NEN
XY_LASER Current (no R_{bin})	I_{LAS_NRB}			1	mA	R_{bin} = open

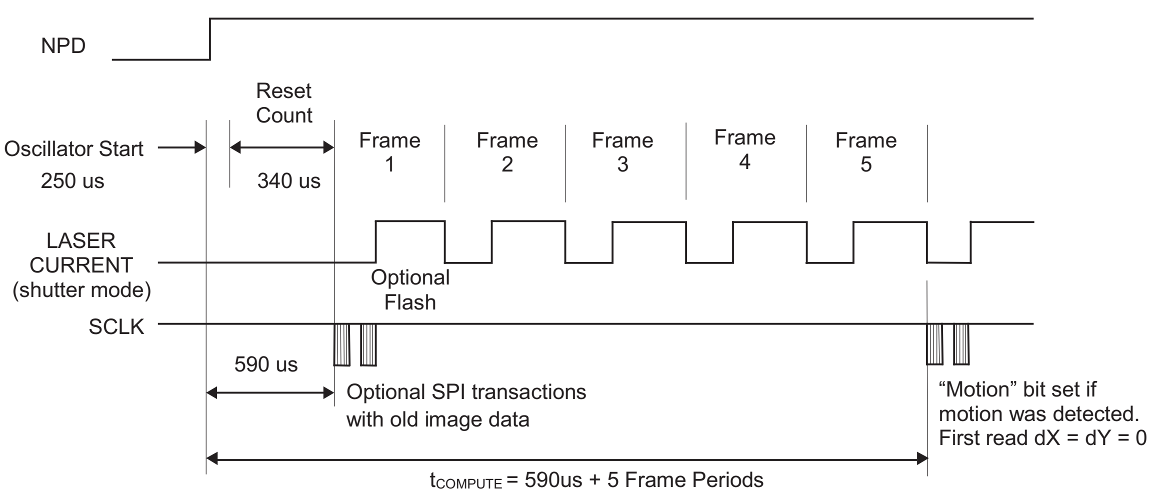


Figure 11. NPD Rising Edge Timing Detail

Typical Performance Characteristics

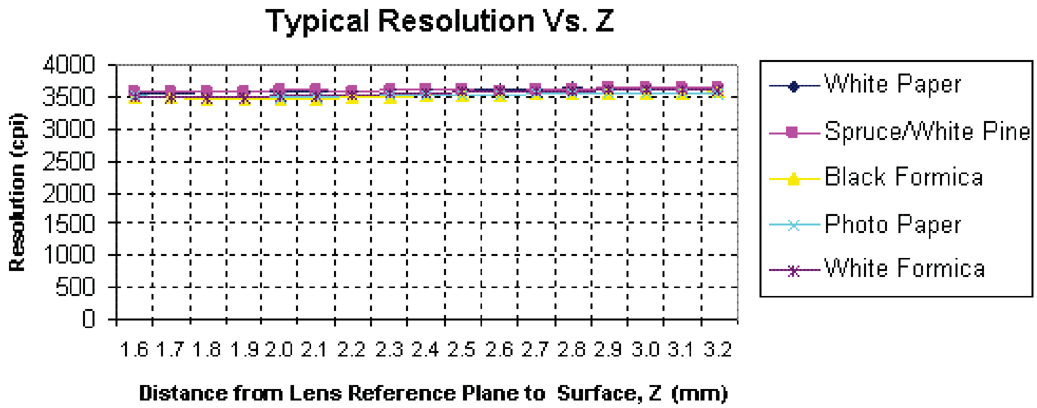
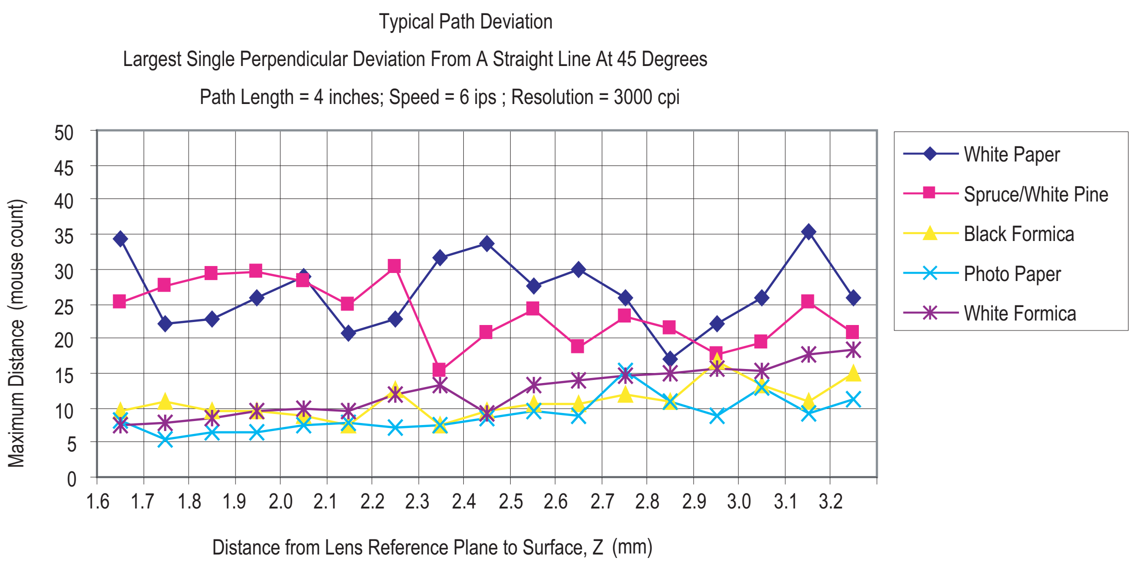


Figure 12. Mean Resolution vs. Z (at 3000cpi setting)



Relationship of mouse count to distance = m (mouse count) / n (cpi)

Figure 13. Average error vs. Z (at 3000cpi setting)

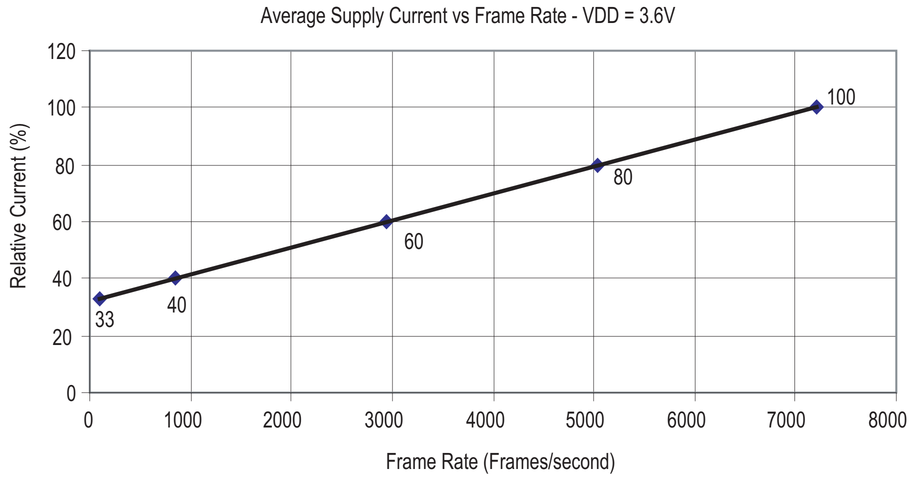


Figure 14. Average Supply Current vs. Frame Rate

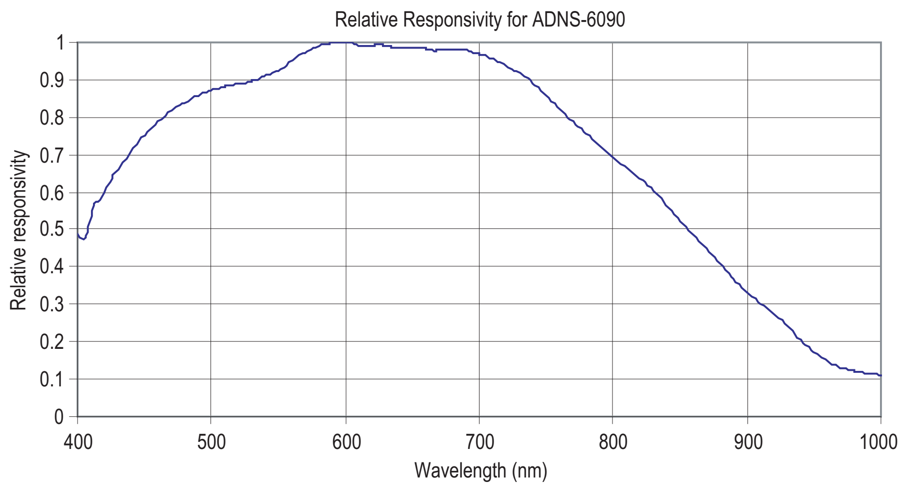


Figure 15. Wavelength Responsivity

Synchronous Serial Port

The synchronous serial port is used to set and read parameters in the ADNS-6090, and to read out the motion information. The serial port is also used to load PROM data into the ADNS-6090.

The port is a four wire port. The host micro-controller always initiates communication; the ADNS-6090 never initiates data transfers. The serial port cannot be activated while the chip is in power down mode (NPD low) or reset (RESET high). SCLK, MOSI, and NCS may be driven directly by a 3.3V output from a micro-controller, or they may be driven by an open drain configuration by enabling on-chip pull-up current sources. The open drain drive allows the use of a 5V micro-controller without any level shifting components. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is tri-stated.

The lines that comprise the SPI port are:

SCLK:	Clock input. It is always generated by the master (the micro-controller.)
MOSI:	Input data. (Master Out/Slave In)
MISO:	Output data. (Master In/Slave Out)
NCS:	Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. This is true for all transactions including PROM download. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD and EFT/B events could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

Write Operation

Write operation, defined as data going from the micro-controller to the ADNS-6090, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The ADNS-6090 reads MOSI on rising edges of SCLK.

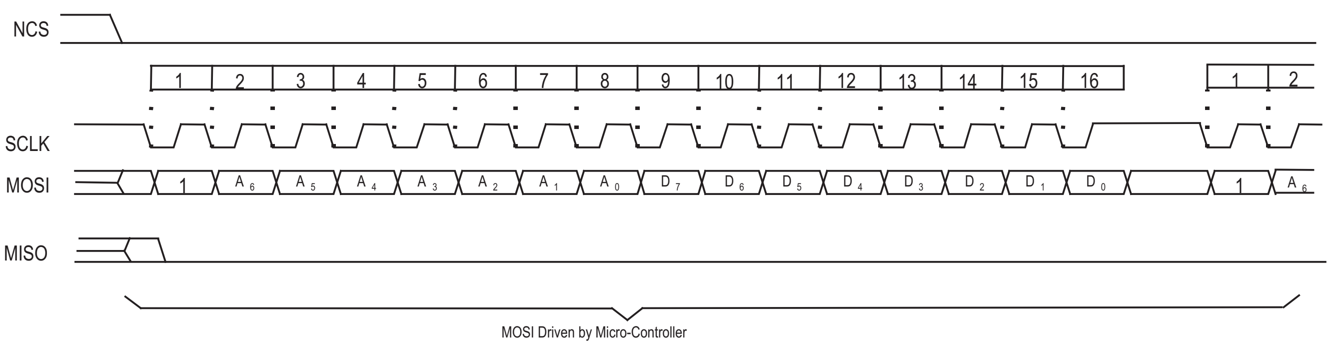


Figure 16. Write Operation

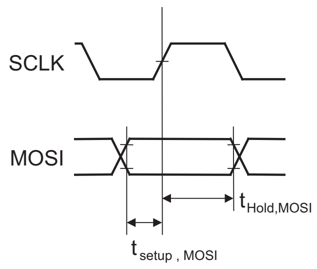


Figure 17. MOSI Setup and Hold Time

Read Operation

A read operation, defined as data going from the ADNS-6090 to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the ADNS-6090 over MISO. The sensor outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.

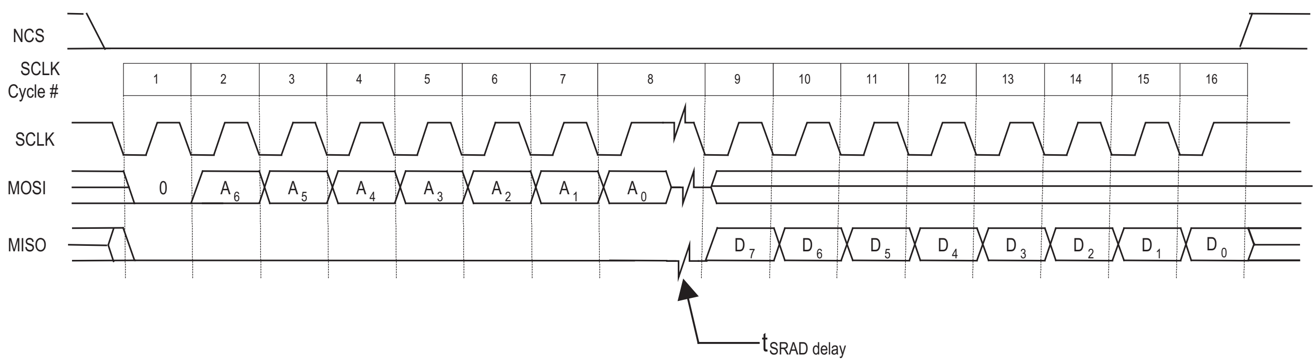


Figure 18. Read Operation

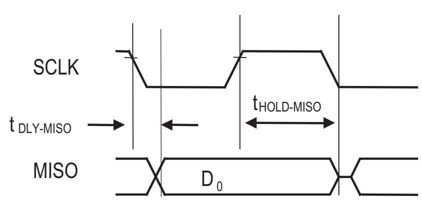


Figure 19. MISO Delay and Hold Time

NOTE: The 250 ns minimum high state of SCLK is also the minimum MISO data hold time of the ADNS-6090. Since the falling edge of SCLK is actually the start of the next read or write command, the ADNS-6090 will hold the state of data on MISO until the falling edge of SCLK.

Required timing between Read and Write Commands (tsxx)

There are minimum timing requirements between read and write commands on the serial port.

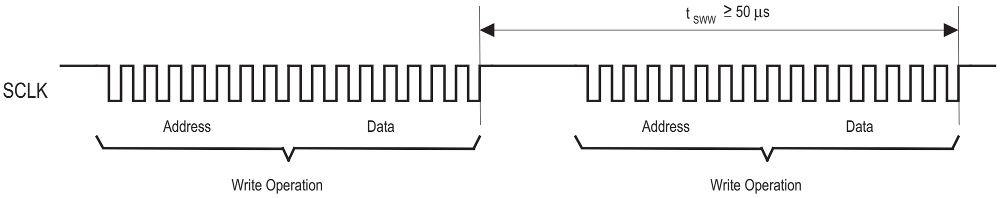


Figure 20. Timing between two write commands

If the rising edge of the SCLK for the last data bit of the second write command occurs before the 50 microsecond required delay, then the first write command may not complete correctly.

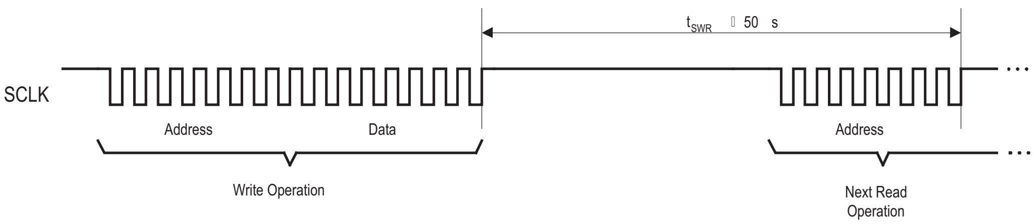


Figure 21. Timing between write and read commands

If the rising edge of SCLK for the last address bit of the read command occurs before the 50 microsecond required delay, the write command may not complete correctly.

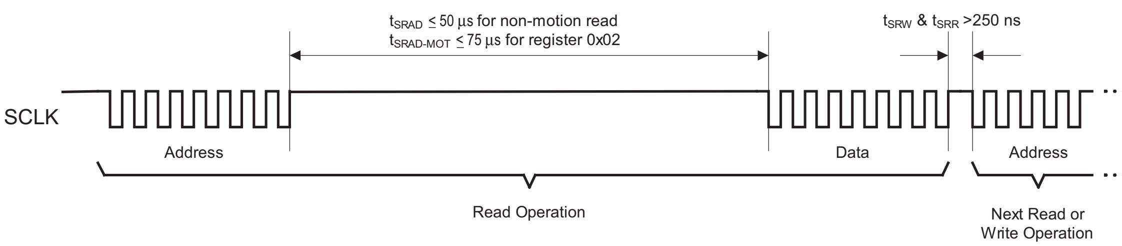


Figure 22. Timing between read and either write or subsequent read commands

The falling edge of SCLK for the first address bit of either the read or write command must be at least 250 ns after the last SCLK rising edge of the last data bit of the previous read operation. In addition, during a read operation SCLK should be delayed after the last address data bit to ensure that the ADNS-6090 has time to prepare the requested data.

Burst Mode Operation

Burst mode is a special serial port operation mode which may be used to reduce the serial transaction time for three predefined operations: motion read and PROM download and frame capture. The speed improvement is achieved by continuous data clocking to or from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

Motion Read

Reading the Motion_Burst register activates this mode. The ADNS-6090 will respond with the contents of the Motion, Delta_X, Delta_Y, SQUAL, Shutter_Upper, Shutter_Lower and Maximum_Pixel registers in that order. After sending the register address, the micro-controller must wait tSRAD-MOT and then begin reading data. All 64 data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data are latched into the output buffer after the last address bit is received. After the burst transmission is complete, the micro-controller must raise the NCS line for at east tBEXIT to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

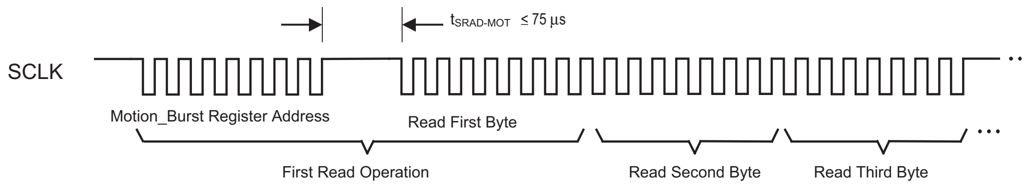


Figure 23. Motion burst timing.

PROM Download

This function is used to load the Avago-supplied firmware file contents into the ADNS-6090. The firmware file is an ASCII text file with each 2-character byte on a single line.

The following steps activate this mode:

1. Perform hardware reset by toggling the RESET pin
2. Write 0x1D to register 0x14 (SROM_Enable register)
3. Wait at least 1 frame period
4. Write 0x18 to register 0x14 (SROM_Enable register)
5. Begin burst mode write of data file to register 0x60 (SROM_Load register)

After the first data byte is complete, the PROM or micro-controller must write subsequent bytes by presenting the data on the MOSI line and driving SCLK at the normal rate. A delay of at least tLOAD must exist between data bytes as shown. After the download is complete, the micro-controller must raise the NCS line for at least tBEXIT to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

Avago recommends reading the SROM_ID register to verify that the download was successful. In addition, a self-test may be executed, which performs a CRC on the SROM contents and reports the results in a register. The test is initiated by writing a particular value to the SROM_Enable register; the result is placed in the Data_Out register. See those register descriptions for more details.

Avago provides the data file for download; the file size is 1986 data bytes. The chip will ignore any additional bytes written to the SROM_Load register after the SROM file.

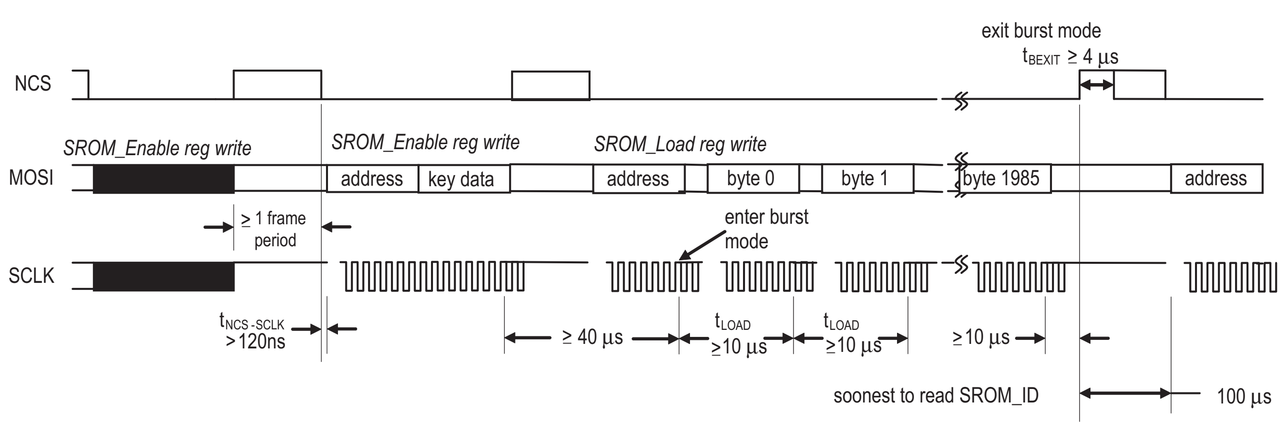


Figure 24. PROM Download Burst Mode

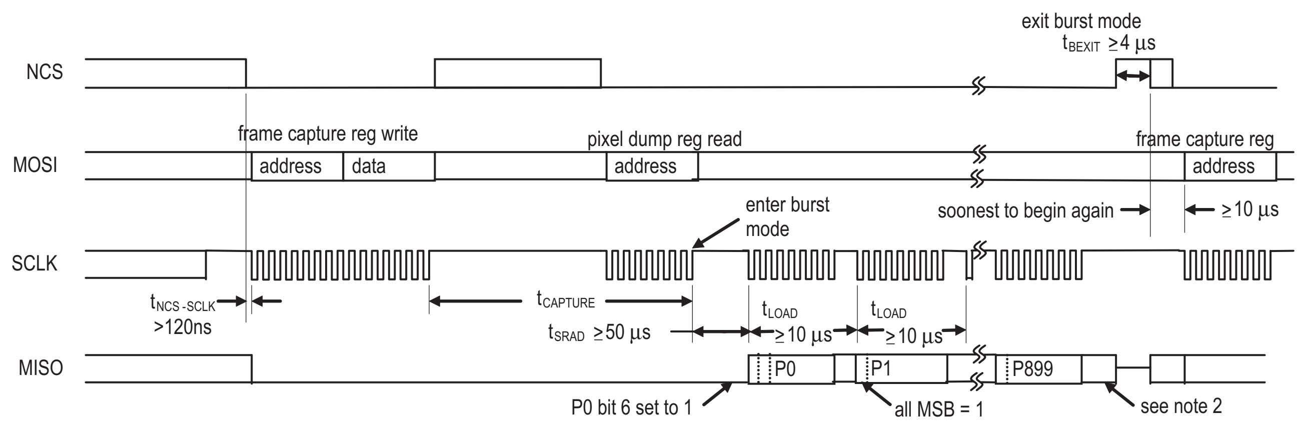
Frame Capture

This is a fast way to download a full array of pixel values from a single frame. This mode disables navigation and overwrites any downloaded firmware. A hardware reset is required to restore navigation, and the firmware must be reloaded.

To trigger the capture, write to the Frame_Capture register. The next available complete 1 2/3 frames (1536 values) will be stored to memory. The data are retrieved by reading the Pixel_Burst register once using the normal read method, after which the remaining bytes are clocked out by driving SCLK at the normal rate. The byte time must be at least tLOAD. If the Pixel_Burst register is read before the data is ready, it will return all zeros.

To read a single frame, read a total of 900 bytes. The next 636 bytes will be approximately 2/3 of the next frame. The first pixel of the first frame (1st read) has bit 6 set to 1 as a start-of-frame marker. The first pixel of the second partial frame (901st read) will also have bit 6 set to 1. All other bytes have bit 6 set to zero. The MSB of all bytes is set to 1. If the Pixel_Burst register is read past the end of the data (1537 reads and on) , the data returned will be zeros. Pixel data is in the lower six bits of each byte.

After the download is complete, the micro-controller must raise the NCS line for at least tBEXIT to terminate burst mode. The read may be aborted at any time by raising NCS. Alternatively, the frame data can also be read one byte at a time from the Frame_Capture register. See the register description for more information.



Notes:

1. MSB = 1 for all bytes. Bit 6 = 0 for all bytes except pixel 0 of both frames which has bit 6 = 1 for use as a frame marker.
2. Reading beyond pixel 899 will return the first pixel of the second partial frame.
3. $t_{CAPTURE}$ = 10 µs + 3 frame periods.
4. This figure illustrates reading a single complete frame of 900 pixels. An additional 636 pixels from the next frame are available.

Figure 25. Frame capture burst mode timing

The pixel output order as related to the surface is shown below.

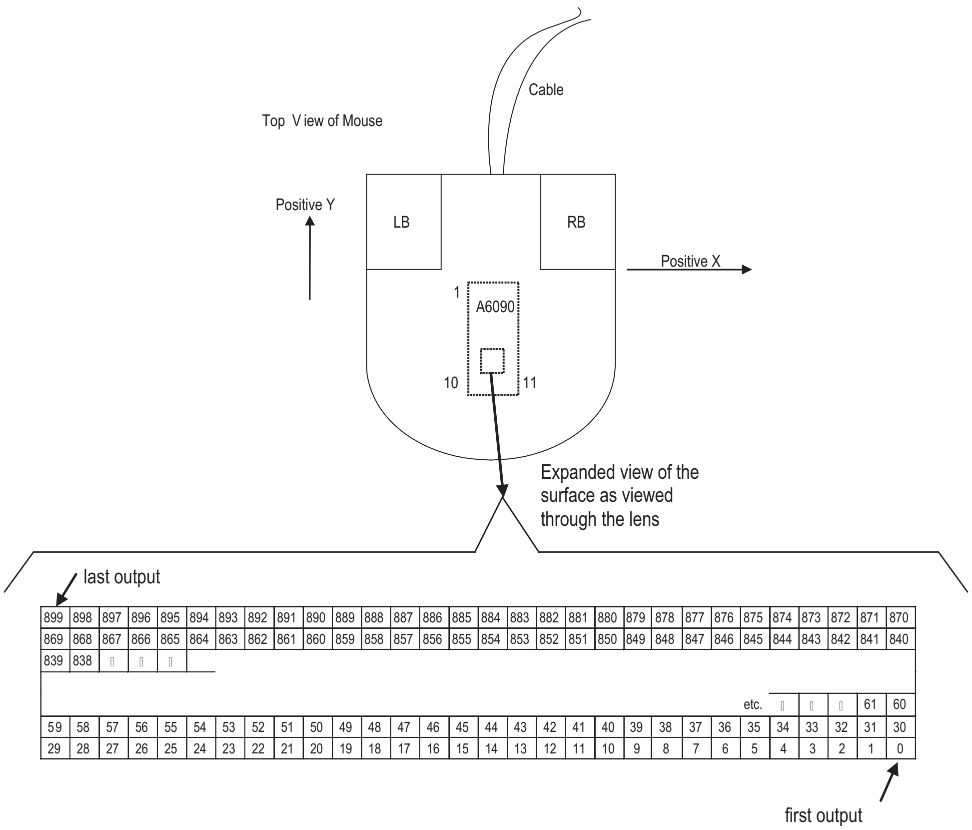


Figure 26. Pixel address map of navigation surface image (Sensor looking at the navigation surface through the ADNS-6120/ADNS-6130-001 lens from the top of mouse)

Error detection and recovery

1. The ADNS-6090 and the micro-controller might get out of synchronization due to ESD events, power supply droops or micro-controller firmware flaws. In such a case, the micro-controller should pulse NCS high for at least 1µs. The ADNS-6090 will reset the serial port (but not the control registers) and will be prepared for the beginning of a new transmission after the normal transaction delay.
2. Invalid addresses: Writing to an invalid address will have no effect. Reading from an invalid address will return all zeros.
3. Termination of a transmission by the micro-controller may sometimes be required (for example, due to a USB suspend interrupt during a read operation). To accomplish this, the micro-controller should raise NCS. The ADNS-6090 will not write to any register and will reset the serial port (but not the control registers) and be prepared for the beginning of future transmissions after NCS goes low. The normal delays between reads or writes (t_{SWW}, t_{swr}, t_{SRAD}, $t_{SRAD-mot}$) are still required after aborted transmissions.
4. The micro-controller can verify success of write operations by issuing a read command to the same address and comparing written data to read data.
5. The micro-controller can verify the synchronization of the serial port by periodically reading the product ID and inverse product ID registers.
6. The microcontroller can read the SROM_ID register to verify that the sensor is running downloaded PROM code. ESD or similar noise events may cause the sensor to revert to native ROM execution. If this should happen, pulse RESET and reload the SROM code.

Notes on Power-up and the serial port

Reset Circuit

The ADNS-6090 does not perform an internal power up self-reset; the reset pin must be raised and lowered to reset the chip. This should be done every time power is applied. During power-up there will be a period of time after the power supply is high but before any clocks are available. The table below shows the state of the various pins during power-up and reset when the RESET pin is driven high by a micro-controller.

State of Signal Pins After VDD is Valid

Pin	Before Reset	During Reset	After Reset
SPI pull-ups	undefined	off	on (default)
NCS	hi-Z control functional	hi-Z control functional	functional
MISO	driven or hi-Z (per NCS)	driven or hi-Z (per NCS)	low or hi-Z (per NCS)
SCLK	undefined	ignored	functional
MOSI	undefined	ignored	functional
XY_LASER	undefined	hi-Z	functional
RESET	functional	high (externally driven)	functional
NPD	undefined	ignored	functional
LASER_NEN	undefined	high (off)	functional

Power Down Circuit

The following table lists the pin states during power down.

State of Signal Pins During Power Down

Pin	NPD low	After wake from PD
SPI pull-ups	off	pre-PD state
NCS	hi-Z control functional	functional
MISO	low or hi-Z (per NCS)	pre-PD state or hi-Z
SCLK	ignored	functional
MOSI	ignored	functional
XY_LASER	high (off)	functional
RESET	functional	functional
NPD	low (driven externally)	functional
REFC	V_{DD3}	REFC
OSC_IN	low	OSC_IN
OSC_OUT	high	OSC_OUT
LASER_NEN	high (off)	functional

The chip is put into the power down (PD) mode by lowering the NPD input. When in PD mode, the oscillator is stopped but all register contents are retained. To achieve the lowest current state, all inputs must be held externally within 200mV of a rail, either ground or V_{DD3}. The chip outputs are driven low or hi-Z during PD to prevent current consumption by an external load.

Registers

The ADNS-6090 registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Address	Register	Read/Write	Default Value
0x00	Product_ID	R	0x1C
0x01	Revision_ID	R	0x20
0x02	Motion	R	0x25
0x03	Delta_X	R	0x00
0x04	Delta_Y	R	0x00
0x05	SQUAL	R	0x00
0x06	Pixel_Sum	R	0x00
0x07	Maximum_Pixel	R	0x00
0x08	Reserved		
0x09	Resolution	R/W	0x04
0x0a	Configuration_bits	R/W	0x5D
0x0b	Extended_Config	R/W	0x08
0x0c	Data_Out_Lower	R	Any
0x0d	Data_Out_Upper	R	Any
0x0e	Shutter_Lower	R	0x85
0x0f	Shutter_Upper	R	0x00
0x10	Frame_Period_Lower	R	Any
0x11	Frame_Period_Upper	R	Any
0x12	Motion_Clear	W	Any
0x13	Frame_Capture	R/W	0x00
0x14	SROM_Enable	W	0x00
0x15	Reserved		
0x16	Configuration II	R/W	0x34
0x17-0x18	Reserved		
0x19	Frame_Period_Max_Bound Lower	R/W	0x90
0x1a	Frame_Period_Max_Bound_Upper	R/W	0x65
0x1b	Frame_Period_Min_Bound_Lower	R/W	0x7E
0x1c	Frame_Period_Min_Bound_Upper	R/W	0x0E
0x1d	Shutter_Max_Bound_Lower	R/W	0x20
0x1e	Shutter_Max_Bound_Upper	R/W	0x4E
0x1f	SROM_ID	R	Version dependent
0x20-0x2b	Reserved		
0x2c	LP_CFG0	R/W	0x7F
0x2d	LP_CFG1	R/W	0x80
0x2e-0x3c	Reserved		
0x3d	Observation	R/W	0x80
0x3e	Reserved		
0x3f	Inverse Product ID	R	0xE3
0x40	Pixel_Burst	R	0x00
0x50	Motion_Burst	R	0x00
0x60	SROM_Load	W	Any

Product_ID Address: 0x00

Access: Read Default Value: 0x1C

Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Data Type: 8-Bit unsigned integer

Usage: This register contains a unique identification assigned to the ADNS-6090. The value in this register does not change; it can be used to verify that the serial communications link is functional.

Revision_ID Address: 0x01

Access: Read Default Value: 0x20

Bit	7	6	5	4	3	2	1	0
Field	RID_7	RID_6	RID_5	RID_4	RID_3	RID_2	RID_1	RID_0

Data Type: 8-Bit unsigned integer

Usage: This register contains the IC revision. It is subjected to change when new IC versions are released.

Note: The downloaded SROM firmware revision is a separate value and is available in the SROM_ID register.

Motion	Address: 0x02
Access: Read	Default Value: 0x20

Bit	7	6	5	4	3	2	1	0
Field	MOT	Reserved	LP_Valid	OVF	Reserved	Reserved	Fault	Reserved

Data Type: Bit field.

Usage: Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If so, then the user should read registers 0x03 and 0x04 to get the accumulated motion. It also tells if the motion buffers have overflowed, if fault is detected and the current resolution setting.

Field Name	Description
MOT	Motion since last report 0 = No motion 1 = Motion occurred, data ready for reading in Delta_X and Delta_Y registers
LP_Valid	This bit is an indicator of complementary value contained in registers 0x2C and 0X2D. 0 = register 0x2C and 0x2D do not have complementary values 1 = register 0x2C and 0x2D contain complementary values
OVF	Motion overflow, ΔY and/or ΔX buffer has overflowed since last report 0 = no overflow 1 = overflow has occurred
Fault	Indicates that the R_{BIN} and/or XY_LASER pin is shorted to GND. 0 = no fault detected 1 = fault detected

Notes for Motion:

1. Reading this register freezes the Delta_X and Delta_Y register values. Read this register before reading the Delta_X and Delta_Y registers. If Delta_X and Delta_Y are not read before the motion register is read a second time, the data in Delta_X and Delta_Y will be lost.
2. Avago RECOMMENDS that registers 0x02, 0x03 and 0x04 to be read sequentially.
   See Motion burst mode also.
3. Internal buffers can accumulate more than eight bits of motion for X or Y. If one of the internal buffers overflows, then absolute path data is lost and the OVF bit is set. This bit is cleared once some motion has been read from the Delta_X and Delta_Y registers, and if the buffers are not at full scale. Since more data is present in the buffers, the cycle of reading the Motion, Delta_X and Delta_Y registers should be repeated until the motion bit (MOT) is cleared. Until MOT is cleared, either the Delta_X or Delta_Y registers will read either positive or negative full scale. If the motion register has not been read for long time, at 800 cpi it may take up to 32 read cycles to clear the buffers, at 1600 cpi, up to 64 cycles and so on. Alternatively, writing to the Motion_Clear register (register 0x12) will clear all stored motion at once.