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# ADNS-7050

## Laser Mouse Sensor



### Data Sheet



Lead (Pb) Free  
RoHS 6 fully  
compliant



#### Description

The Avago Technologies ADNS-7050 sensor along with the ADNS-6120 or ADNS-6130-001 lens, ADNS-6130-001 clip and ADNV-6340 VCSEL form a complete and laser mouse tracking system. It is the laser illuminated system enabled for cordless application. Powered by Avago Technologies LaserStream™ technology, it can operate on many surface that proved difficult for traditional LED-based optical navigation. It's low power architecture is capable of sensing mouse motion while prolonging battery life, two performance areas essential in demanding cordless applications.

There is no moving part, in the complete assembly for ADNS-7050 laser mouse system, thus it is high reliability and less maintenance for the end user. In addition, precision optical alignment is not required, facilitating high volume assembly.

#### Theory of Operation

The ADNS-7050 is based on LaserStream™ Technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement.

The ADNS-7050 contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a four wire serial port. The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the  $\Delta x$  and  $\Delta y$  relative displacement values. An external microcontroller reads the  $\Delta x$  and  $\Delta y$  information from the sensor serial port. The microcontroller then translates the data into PS2, USB, or RF signals before sending them to the host PC or game console.

#### Features

- Low power architecture
- New LaserStream™ technology
- Self-adjusting power-saving modes for longest battery life
- Speed motion detection up to 20 ips and 8g
- Enhanced SmartSpeed self-adjusting frame rate for optimum performance
- Motion detect pin output
- Internal oscillator – no clock input needed
- Selectable 400 and 800 cpi resolution
- Wide operating voltage: 2.7 V-3.6 V nominal
- Four wire serial port
- Minimal number of passive components
- Laser fault detect circuitry on-chip for Eye Safety Compliance

#### Applications

- Laser mice
- Optical trackballs
- Integrated input devices
- Battery-powered input devices

**Pinout of ADNS-7050 Optical Mouse Sensor**

Pin	Name	Description
1	NCS	Chip Select (Active Low Input)
2	MISO	Serial Data Output (Master In/Slave Out)
3	SCLK	Serial Clock Input
4	MOSI	Serial Data Input (Master Out/Slave In)
5	MOTION	Motion Detect (Active Low Output)
6	LASER_NEN	LASER Enable (Active LOW)
7	GND	Ground
8	XY_LASER	LASER Control
9	AGND	Analog Ground
10	AVDD	Analog Supply Voltage
11	AGND	Analog Ground
12	GND	Ground
13	GND	Ground
14	NC	No Connection
15	GND	Ground
16	VDD	Supply Voltage
17	NC	No Connection
18	NC	No Connection

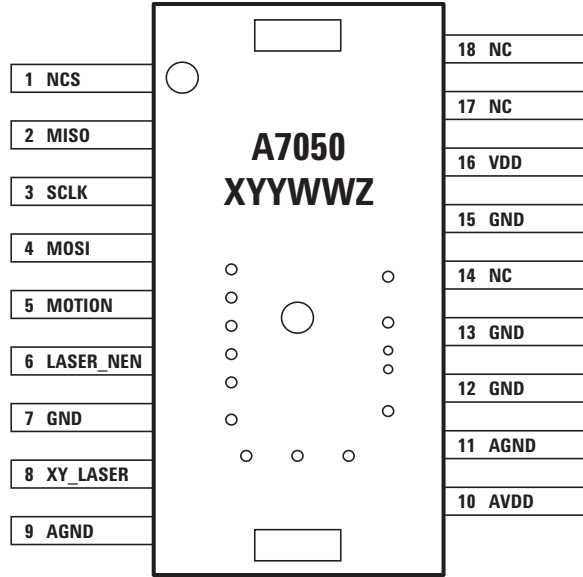
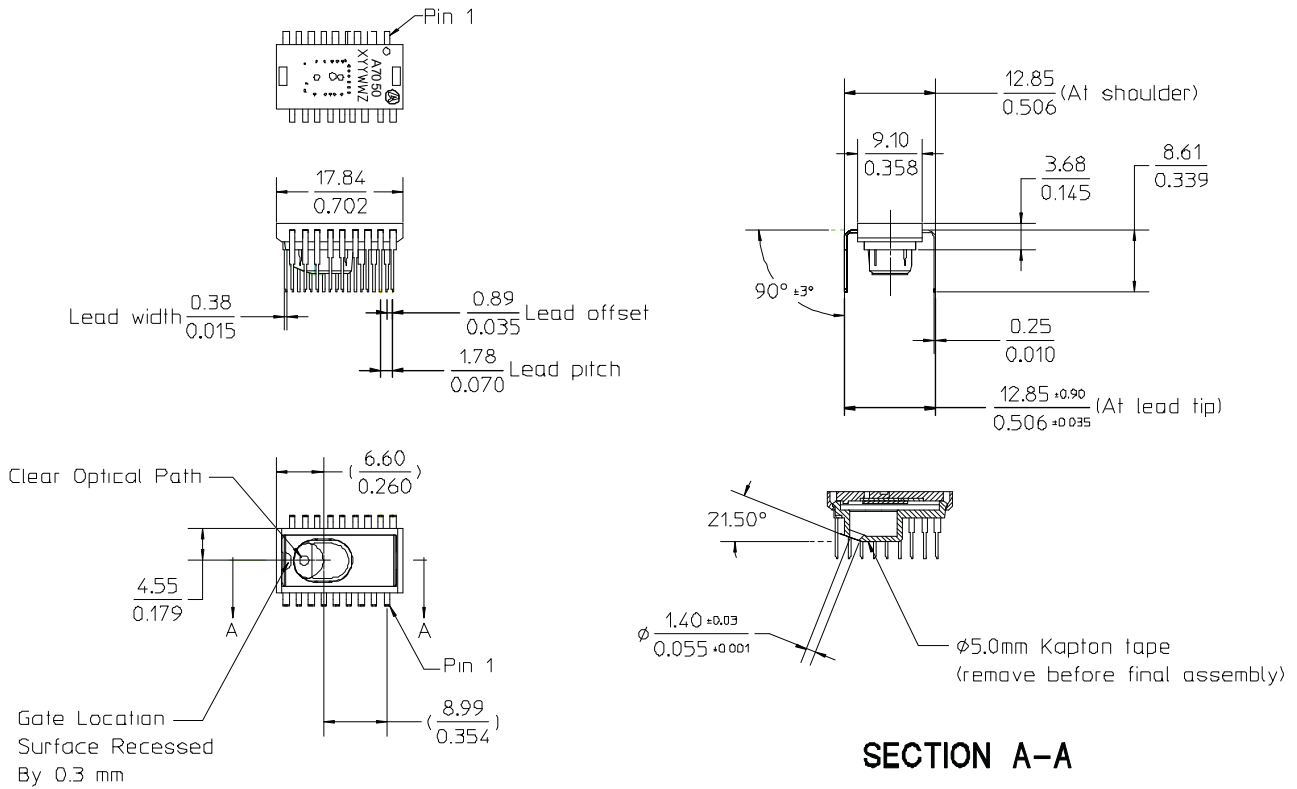


Figure 1. Package outline drawing (top view).



- Notes:
1. Dimensions in millimeters / inches.
  2. Dimensional tolerance: ±0.1mm.
  3. Coplanarity of Leads: ±0.1mm.
  4. Lead pitch tolerance: ±0.15mm.
  5. Non-cumulative pitch tolerance: ±0.15mm.
  6. Angular tolerance: ±3.0°
  7. Maximum flash: +0.2mm
  8. Chamfer (25° X 2) on the taper side of lead.
  9. ( ) Bracket dimensions are for reference only and should not be used to mechanically reference the sensor.

Figure 2. Package outline drawing.

**CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

### Overview of Laser Mouse Sensor Assembly

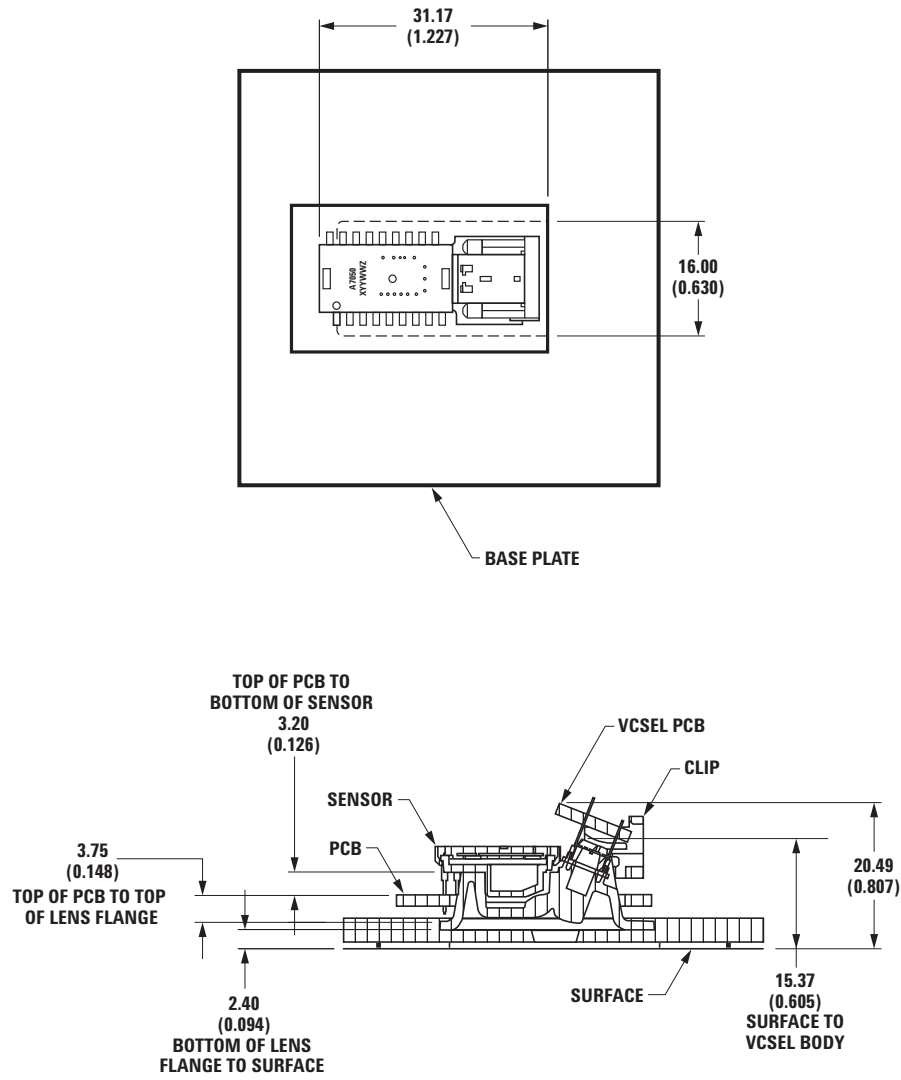
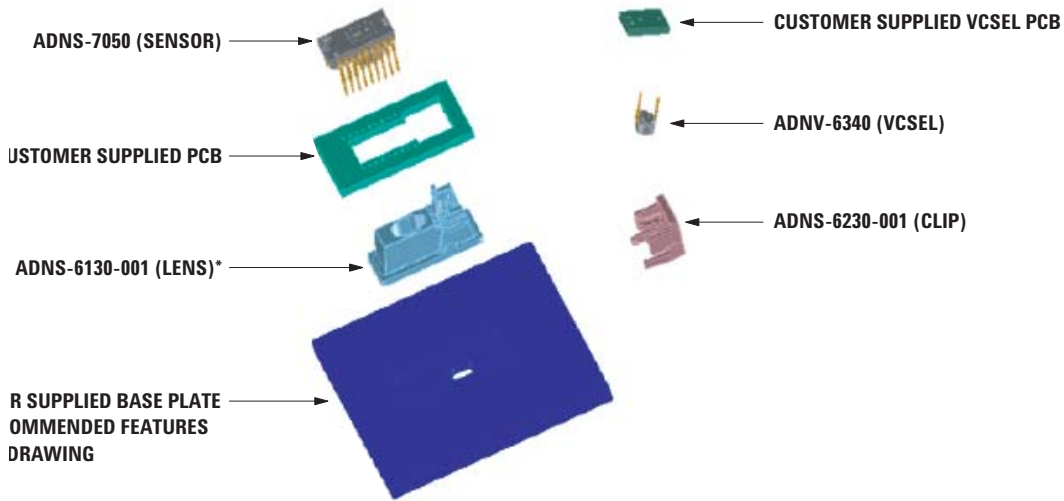


Figure 3. 2D Assembly drawing of ADNS-7050 (top and cross-sectional view).

## 2D Assembly Drawing of ADNS-7050, PCBs and Base Plate



*S-6120 FOR ROUND LENS*

Figure 4. Exploded view drawing.

Shown with ADNS-6130-001 Laser Mouse Lens, ADNS-6230-001 VCSEL Assembly Clip and ADNV-6340 VCSEL. The components interlock as they are mounted onto defined features on the base plate.

The ADNS-7050 laser mouse sensor is designed for mounting on a through hole PCB, looking down. There is an aperture stop and features on the package that align to the lens.

The ADNV-6340 VCSEL is recommended for illumination, provides a laser diode with a single longitudinal and a single transverse mode. It is particularly suited as lower power consumption and highly coherent replacement of LEDs. It also provides wider operation range while still remaining within single-mode, reliable operating conditions.

The ADNS-6120 or ADNS-6130-001 Laser Mouse Lens is designed for use with ADNS-7050 sensor and the illumination subsystem provided by the assembly clip and

the VCSEL. Together with the VCSEL, the lens provides the directed illumination and optical imaging necessary for proper operation of the Laser Mouse Sensor. ADNS-6120 and ADNS-6130-001 are precision molded optical components and should be handled with care to avoid scratching of the optical surfaces. ADNS-6120 also has a large round flange to provide a long creepage path for any ESD events that occur at the opening of the base plate.

The ADNS-6230-001 VCSEL Assembly Clip is designed to provide mechanical coupling of the ADNV-6340 VCSEL to the ADNS-6120 or ADNS-6130-001 lens. This coupling is essential to achieve the proper illumination alignment required for the sensor to operate on a wide variety of surfaces.

Avago Technologies provides an IGES file drawing describing the base plate molding features for lens and PCB alignment.

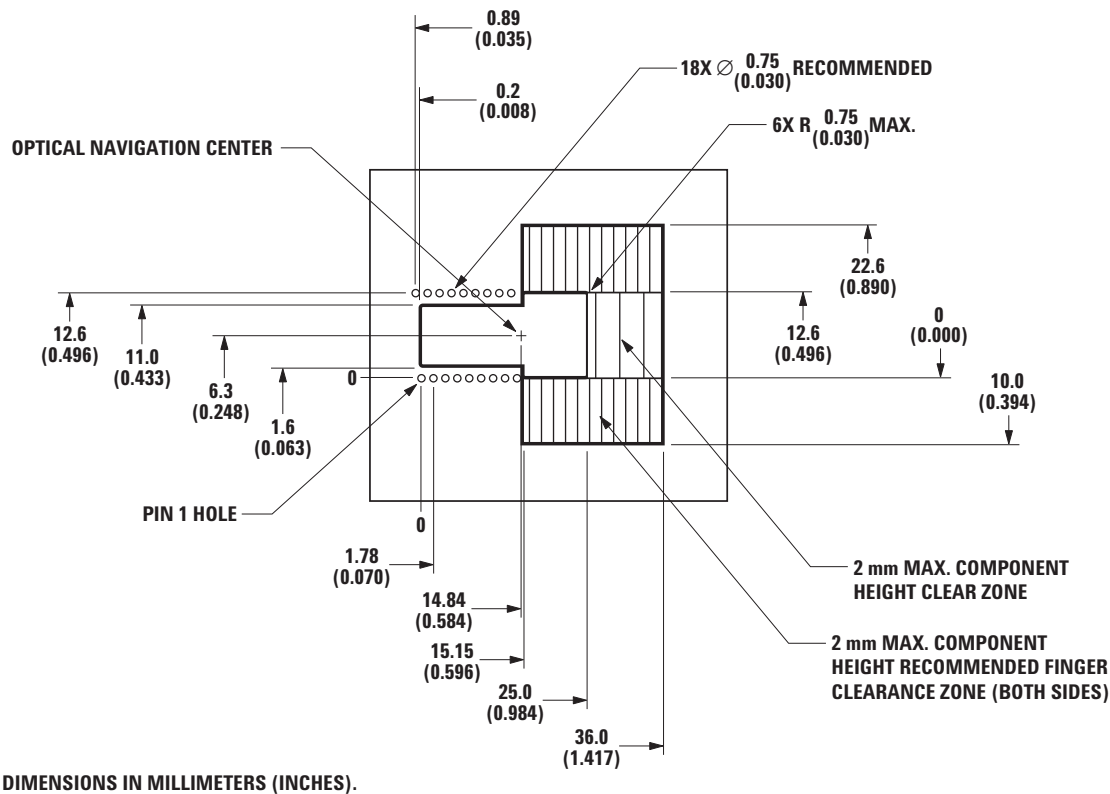


Figure 5. Recommended PCB mechanical cutouts and spacing.

### Assembly Recommendation

- Insert the sensor and all other electrical components into the application PCB (main PCB board and VCSEL PCB board).
- Wave-solder the entire assembly in a no-wash solder process utilizing a solder fixture. The solder fixture is needed to protect the sensor during the solder process. It also sets the correct sensor-to-PCB distance, as the lead shoulders do not normally rest on the PCB surface. The fixture should be designed to expose the sensor leads to solder while shielding the optical aperture from direct solder contact.
- Place the lens onto the base plate.
- Remove the protective kapton tape from the optical aperture of the sensor. Care must be taken to keep contaminants from entering the aperture.
- Insert the PCB assembly over the lens onto the base plate. The sensor aperture ring should self-align to the lens. The optical position reference for the PCB is set by the base plate and lens. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
- Remove the protective cap from the VCSEL.
- Insert the VCSEL assembly into the lens.

- Slide the clip in place until it latches. This locks the VCSEL and lens together.
- Tune the laser output power from the VCSEL to meet the Eye Safe Class I Standard as detailed in the LASER Power Adjustment Procedure.
- Install the mouse top case. There must be a feature in the top case (or other area) to press down onto the sensor to ensure the sensor and lens are interlocked to the correct vertical height.

### Design Considerations for Improving ESD Performance

For improved electrostatic discharge performance, typical creepage and clearance distance are shown in the table below. Assumption: base plate construction as per the Avago Technologies supplied IGES file and ADNS-6130-001 trim lens (or ADNS-6120 round lens).

Typical Distance	Millimeters
Creepage	12.0
Clearance	2.1

Note that the lens material is polycarbonate and therefore, cyanoacrylate based adhesives or other adhesives that may damage the lens should NOT be used.

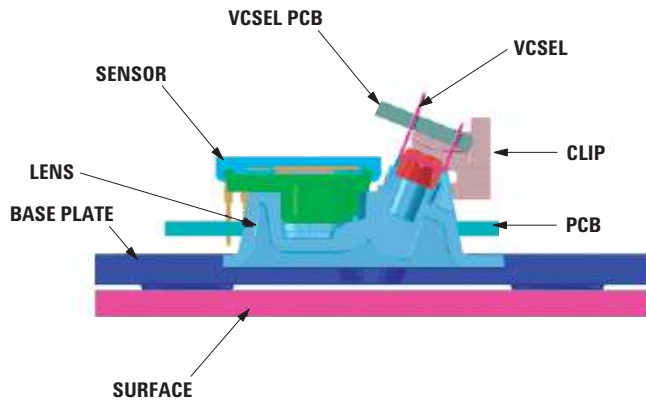


Figure 6. Sectional view of PCB assembly highlighting optical mouse components.

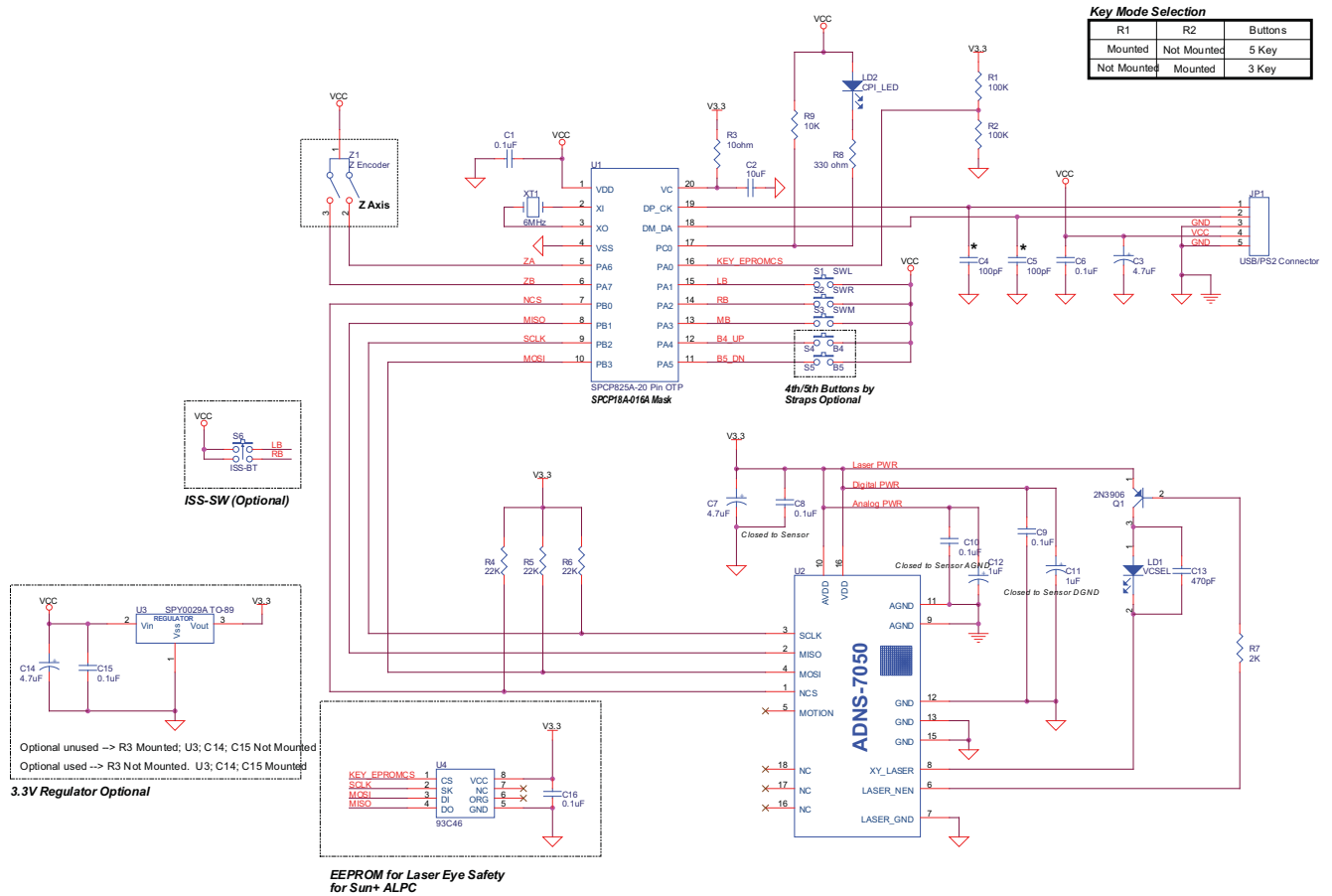


Figure 7a. Schematic diagram for 3-button scroll wheel corded mouse.



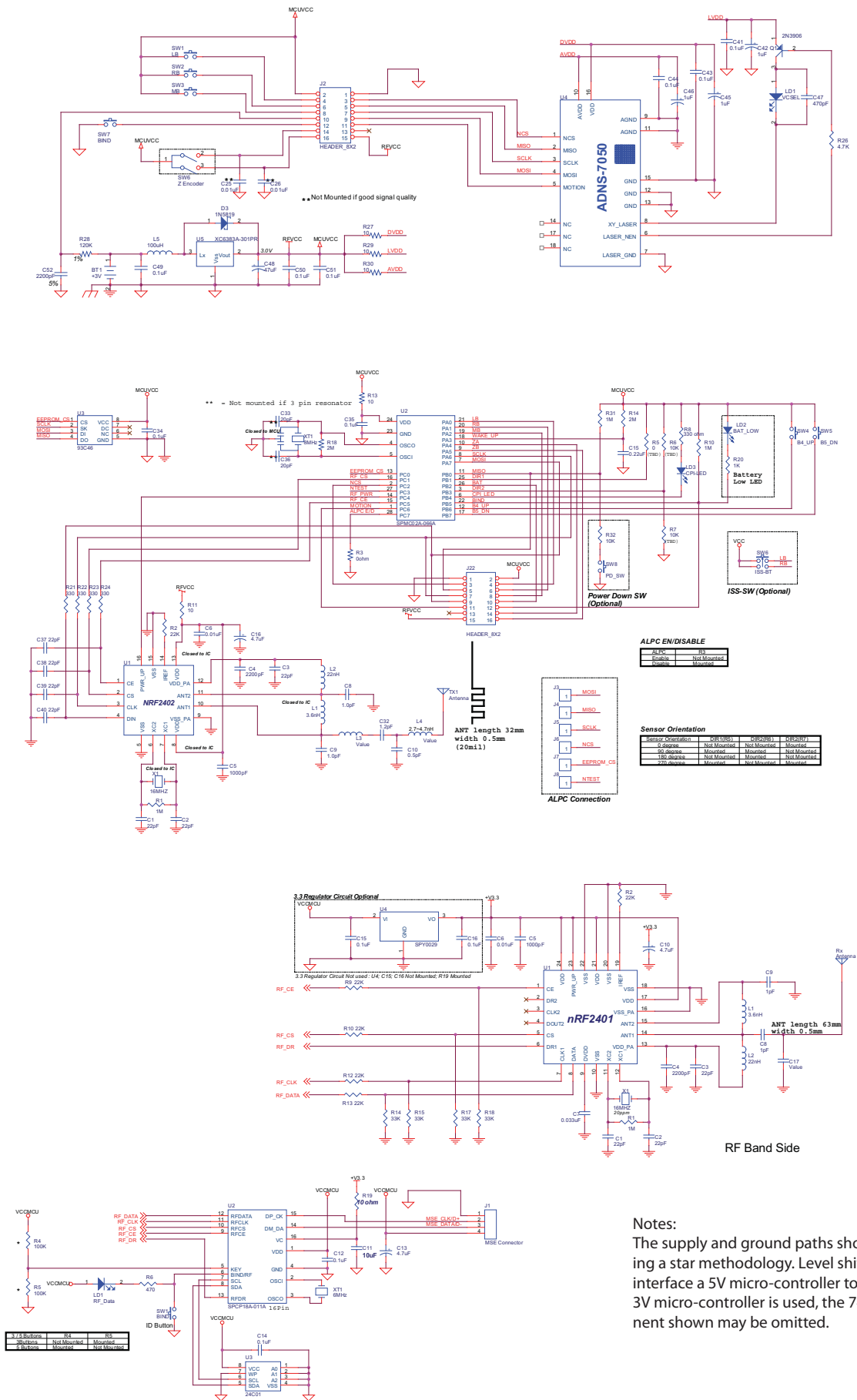


Figure 7b. Schematic diagram for 3-button scroll wheel cordless mouse.

## LASER Drive Mode

The laser is driven in pulsed mode during normal operation. A calibration mode is provided which drives the laser in continuous (CW) operation.

## Eye Safety

The ADNS-7050 and the associated components in the schematic of Figure 7 are intended to comply with Class 1 Eye Safety Requirements of IEC 60825-1. Avago Technologies suggests that manufacturers perform testing to verify eye safety on each mouse. It is also recommended to review possible single fault mechanisms beyond those described below in the section “Single Fault Detection”. Under normal conditions, the ADNS-7050 generates the drive current for the laser diode (ADNV-6340).

In order to stay below the Class 1 power requirements, LASER\_CTRL0 (register 0x1a), LASER\_CTRL1 (register 0x1f), LSRPWR\_CFG0 (register 0x1c) and LSRPWR\_CFG1 (register 0x1d) must be programmed to appropriate values. The system comprised of the ADNS-7050 and ADNV-6340, is designed to maintain the output beam power within Class 1 requirements over components manufacturing tolerances and the recommended temperature range when adjusted per the procedure below and implemented as shown in the recommended application circuit of Figure 7. For more information, please refer to Eye Safety Application Note AN 5230.

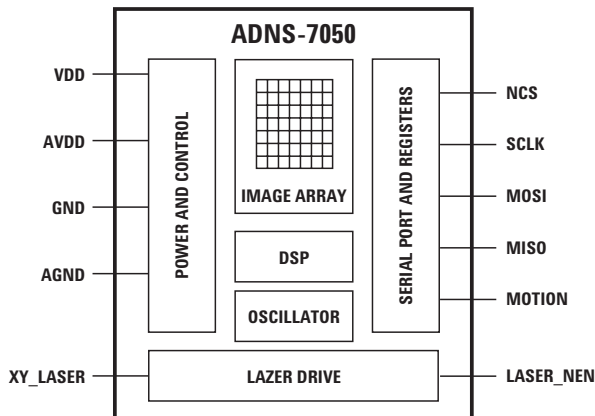


Figure 8. Block diagram of ADNS-7050 optical mouse sensor.

## LASER Power Adjustment Procedure

- The ambient temperature should be  $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ .
- Set VDD to its permanent value.
- Set the Range bit (bit 7 of register 0x1a) to 0.
- Set the Range\_C complement bit (bit 7 of register 0x1f) to 1.
- Set the Match\_bit (bit 5 of register 0x1a) to the correct value for the bin designation of the laser being used.
- Set the Match\_C\_bit (bit 5 of register 0x1f) to the complement of the Match\_bit.
- Enable the Calibration mode by writing to bits [3,2,1] of register 0x1A so the laser will be driven with 100% duty cycle.
- Write the Calibration mode complement bits to register 0x1f.
- Set the laser current to the minimum value by writing 0x00 to register 0x1c, and the complementary value 0xFF to register 0x1d.
- Program registers 0x1c and 0x1d with increasing values to achieve an output power as close to 506uW as possible without exceeding it. If this power is obtained, the calibration is complete, skip to step 14.
- If it was not possible to achieve the power target, set the laser current to the minimum value by writing 0x00 to register 0x1c, and the complementary value 0xff to register 0x1d.
- Set the Range and Range\_C bits in registers 0x1a and 0x1f, respectively, to choose to the higher laser current range.
- Program registers 0x1c and 0x1d with increasing values to achieve an output power as close to 506uW as possible without exceeding it.
- Save the value of registers 0x1a, 0x1c, 0x1d, and 0x1f in non-volatile memory in the mouse. These registers must be restored to these values every time the ADNS-7050 is reset.
- Reset the mouse, reload the register values from non-volatile memory, enable Calibration mode, and measure the laser power to verify that the calibration is correct.

Good engineering practices such as regular power meter calibration, random quality assurance retest of calibrated mice, etc. should be used to guarantee performance, reliability and safety for the product design.

## LASER Output Power

The laser beam output power as measured at the navigation surface plane is specified below. The following conditions apply:

1. The system is adjusted according to the above procedure.
2. The system is operated within the recommended operating temperature range.
3. The VDD value is no greater than 300mV above its value at the time of adjustment.
4. No allowance for optical power meter accuracy is assumed.

## Disabling the LASER

LASER\_NEN is connected to the gate of a P-channel MOSFET transistor which when ON connects VDD to the LASER. In normal operation, LASER\_NEN is low. In the case of a fault condition (ground or VDD3 at XY\_LASER), LASER\_NEN goes high to turn the transistor off and disconnect VDD3 from the LASER.

## Single Fault Detection

ADNS-7050 is able to detect a short circuit or fault condition at the XY\_LASER pin, which could lead to excessive laser power output. A path to ground on this pin will trigger the fault detection circuit, which will turn off the laser drive current source and set the LASER\_NEN output

high. When used in combination with external components as shown in the block diagram below, the system will prevent excess laser power for a resistive path to ground at XY\_LASER by shutting off the laser. In addition to the ground path fault detection described above, the fault detection circuit is continuously checked for proper operation by internally generating a path to ground with the laser turned off via LASER\_NEN. If the XY\_LASER pin is shorted to VDD3, this test will fail and will be reported as a fault.

## Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- Passes IEC-1000-4-3 radiated susceptibility level when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- Passes EN61000-4-4/IEC801-4 EFT tests when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- UL flammability level UL94 V-0.
- Provides sufficient ESD creepage/clearance distance to avoid discharge up to 15 kV when assembled into a mouse according to usage instructions above.

Parameter	Symbol	Minimum	Maximum	Units	Notes
Laser output power	LOP	716	$\mu$ W		Class 1 limit with recommended VCSEL and lens.

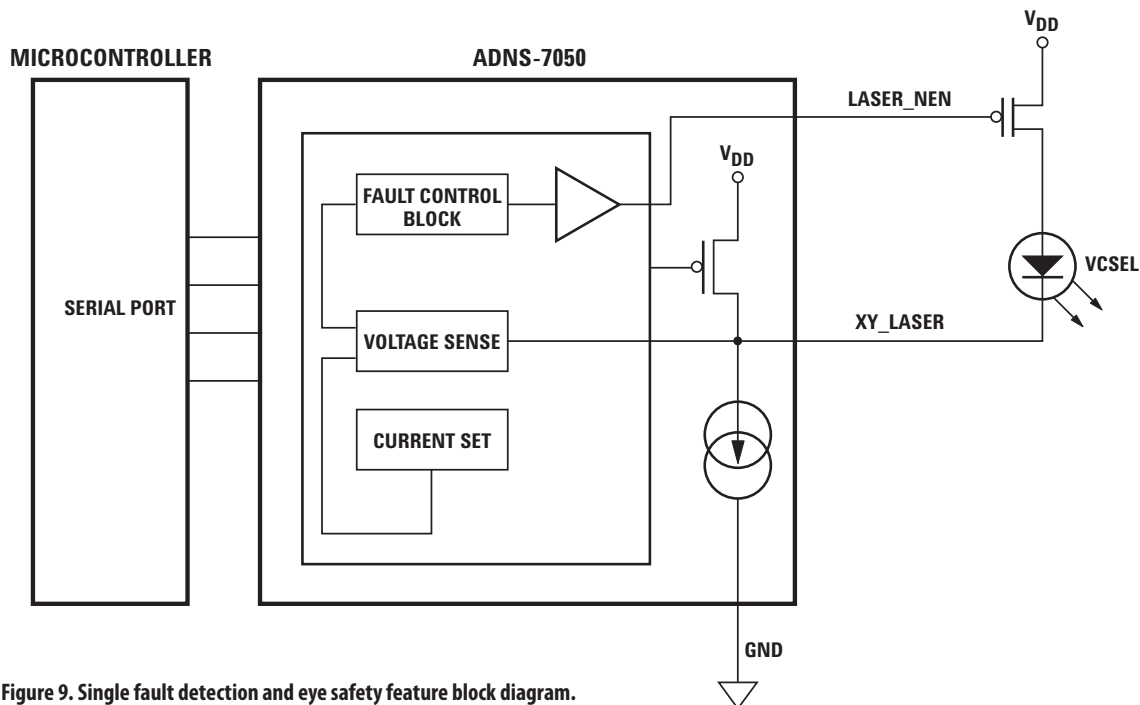


Figure 9. Single fault detection and eye safety feature block diagram.

## Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	$T_S$	-40	85	°C	
Lead Solder Temp			260	°C	For 10 seconds, 1.6 mm below seating plane.
Supply Voltage	$V_{DD}$	-0.5	3.7	V	
ESD			2	kV	All pins, human body model MIL 883 Method 3015
Input Voltage	$V_{IN}$	-0.5	$V_{DD} + 0.5$	V	All Pins
Latchup Current	$I_{out}$		20	mA	All Pins

## Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Operating Temperature	$T_A$	0		40	°C	
Power Supply Voltage	$V_{DD}$	2.7	2.8	3.6	V	Including noise
Power Supply Rise Time	$V_{RT}$	1		100	ms	0 to 2.8 V
Supply Noise (Sinusoidal)	$V_{NA}$			100	mVp-p	10 kHz - 50 MHz
Serial Port Clock Frequency	$f_{SCLK}$			1	MHz	Active drive, 50% duty cycle
Distance from Lens Reference Plane to Surface	$Z$	2.18	2.40	2.62	mm	Results in $\pm 0.2$ mm minimum DOF. See Figure 10.
Speed	$S$			20	in/sec	
Acceleration	$A$			8	g	
Load Capacitance	$C_{out}$			100	pF	MOTION, MISO
Voltage at XY_LASER	$V_{xy\_laser}$	0.3		$V_{DD}$	V	

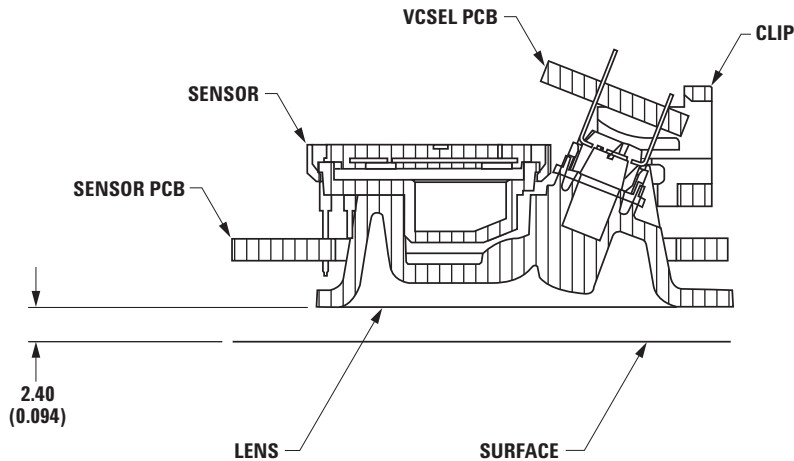


Figure 10. Distance from lens reference plane to surface, Z.

## AC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C,  $V_{DD}=2.8V$ .

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Motion Delay after Reset	$t_{MOT-RST}$			23	ms	From SW_RESET register write to valid motion, assuming motion is present
Shutdown	$t_{STDWN}$			50	ms	From Shutdown mode active to low current
Wake from Shutdown	$t_{WAKEUP}$	23			ms	From Shutdown mode inactive to valid motion. Notes: A RESET must be asserted after a shutdown. Refer to section "Notes on Shutdown and Forced Rest", also note $t_{MOT-RST}$
Forced Rest Enable	$t_{REST-EN}$			1	s	From RESTEN bits set to low current
Wake from Forced Rest	$t_{REST-DIS}$			1	s	From RESTEN bits cleared to valid motion
MISO Rise Time	$t_{r-MISO}$		150	300	ns	$C_L = 100$ pF
MISO Fall Time	$t_{f-MISO}$		150	300	ns	$C_L = 100$ pF
MISO Delay after SCLK	$t_{DLY-MISO}$			120	ns	From SCLK falling edge to MISO data valid, no load conditions
MISO Hold Time	$t_{hold-MISO}$	0.5		$1/f_{SCLK}$	$\mu s$	Data held until next falling SCLK edge
MOSI Hold Time	$t_{hold-MOSI}$	200			ns	Amount of time data is valid after SCLK rising edge
MOSI Setup Time	$t_{setup-MOSI}$	120			ns	From data valid to SCLK rising edge
SPI Time between Write Commands	$t_{SWW}$	30			$\mu s$	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI Time between Write and Read Commands	$t_{SWR}$	20			$\mu s$	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second addressbyte.
SPI Time between Read and Subsequent Commands	$t_{SRW}$ and $t_{SRR}$	500			ns	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command.
SPI Read Address-Data Delay	$t_{SRAD}$	4			$\mu s$	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read.
NCS Inactive after Motion Burst	$t_{BEXIT}$	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS to SCLK Active	$t_{NCS-SCLK}$	120			ns	From NCS falling edge to first SCLK rising edge
SCLK to NCS Inactive (for Read Operation)	$t_{SCLK-NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK to NCS Inactive (for Write Operation)	$t_{SCLK-NCS}$	20			$\mu s$	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS to MISO High-Z	$t_{NCS-MISO}$			500	ns	From NCS rising edge to MISO high-Z state
MOTION Rise Time	$t_{r-MOTION}$		150	300	ns	$C_L = 100$ pF
MOTION Fall Time	$t_{f-MOTION}$		150	300	ns	$C_L = 100$ pF
Transient Supply Current	$I_{DDT}$			45	mA	Max supply current during a $V_{DD}$ ramp from 0 to 2.8 V

## DC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, V<sub>DD</sub>=2.8 V.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
DC Supply Current in Various Modes	I <sub>DD_RUN</sub>		4	10	mA	Average current, including LASER current. No load on MISO, MOTION.
	I <sub>DD_REST1</sub>		0.5	1.8		
	I <sub>DD_REST2</sub>		0.15	0.4		
	I <sub>DD_REST3</sub>		0.05	0.15		
Peak Supply Current				40	mA	
Shutdown Supply Current	I <sub>DDSTDWN</sub>		1	12	μA	NCS, SCLK = VDD MOSI = GND MISO = Hi-Z
Input Low Voltage	V <sub>IL</sub>			0.5	V	SCLK, MOSI, NCS
Input High Voltage	V <sub>IH</sub>	V <sub>DD</sub> - 0.5			V	SCLK, MOSI, NCS
Input Hysteresis	V <sub>I_HYS</sub>		100		mV	SCLK, MOSI, NCS
Input Leakage Current	I <sub>leak</sub>		±1	±10	μA	V <sub>in</sub> = VDD - 0.6 V, SCLK, MOSI, NCS
XY_LASER Current	I <sub>LAS</sub>		0.8		mA	V <sub>xy_laser</sub> ≥ 0.3 V LASER_CTRL0 = 0X80 LASER_CTRL1 = 0X20 LP_CFG0 = 0xFF LP_CFG1 = 0x00
LASER Current (Fault Mode)	I <sub>LAS_FAULT</sub>			300	uA	XY_LASER R <sub>leakage</sub> < 75 kOhms to GND
Output Low Voltage, MISO, LASER_NEN	V <sub>OL</sub>			0.7	V	I <sub>out</sub> = 1 mA, MISO, MOTION I <sub>out</sub> = 1 mA, LASER_NEN
Output High Voltage, MISO, LASER_NEN	V <sub>OH</sub>	V <sub>DD</sub> - 0.7			V	I <sub>out</sub> = -1 mA, MISO, MOTION I <sub>out</sub> = -0.5 mA, LASER_NEN
Input Capacitance	C <sub>in</sub>			10	pF	MOSI, NCS, SCLK

## Typical Performance Characteristics

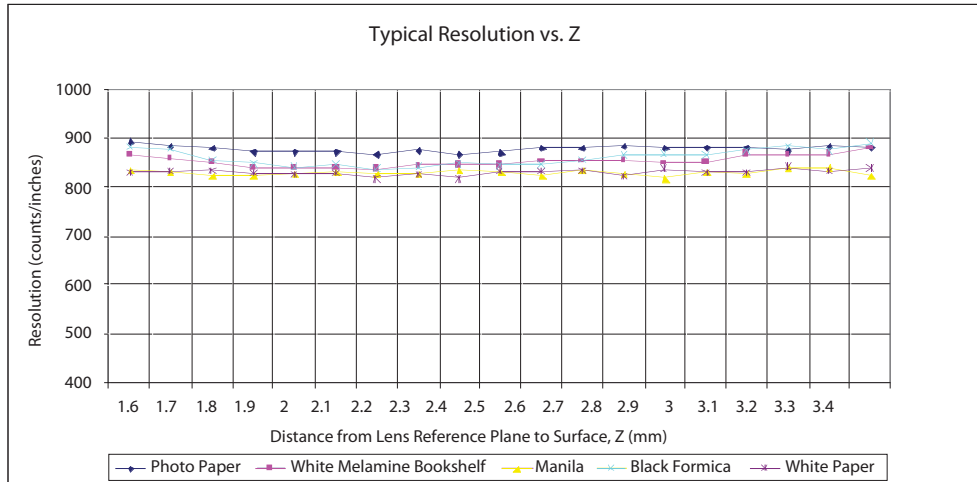


Figure 11. Mean resolution vs. Z at 800 cpi.

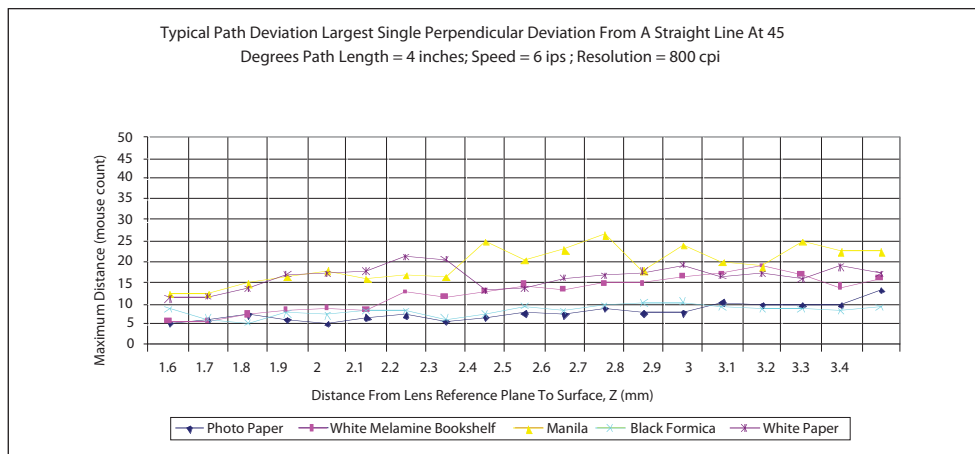


Figure 12. Average error vs. distance at 800 cpi .

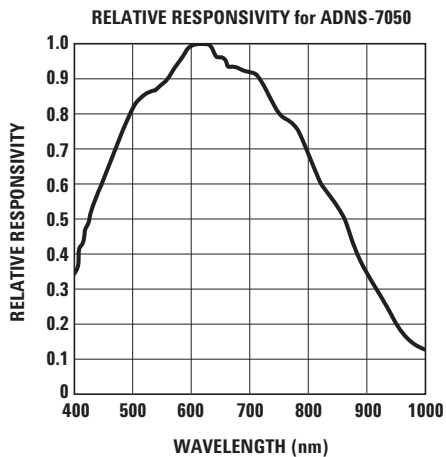


Figure 13. Wavelength responsivity.

## Power Management Modes

The ADNS-7050 has three power-saving modes. Each mode has a different motion detection period, affecting response time to mouse motion (Response Time). The sensor automatically changes to the appropriate mode, depending on the time since the last reported motion (Downshift Time). The parameters of each mode are shown in the following table.

Mode	Response Time (nominal)	Downshift Time (nominal)
Rest 1	16.5 ms	237 ms
Rest 2	82 ms	8.4 s
Rest 3	410 ms	504 s

## Motion Pin Timing

The motion pin is a level-sensitive output that signals the micro-controller when motion has occurred. The motion pin is lowered whenever the motion bit is set; in other words, whenever there is data in the Delta\_X or Delta\_Y registers. Clearing the motion bit (by reading Delta\_X and Delta\_Y, or writing to the Motion register) will put the motion pin high.

## LASER Mode

For power savings, the VCSEL will not be continuously on. ADNS-7050 will flash the VCSEL only when needed.

## Synchronous Serial Port

The synchronous serial port is used to set and read parameters in the ADNS-7050, and to read out the motion information.

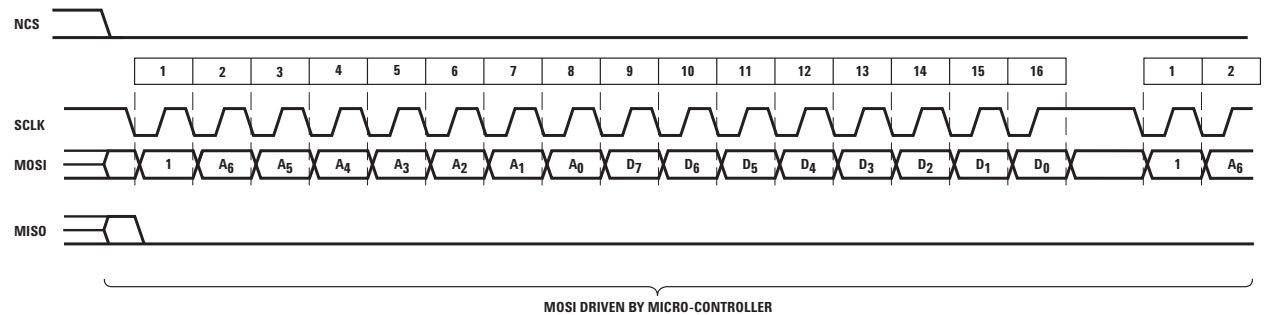


Figure 14. Write operation.

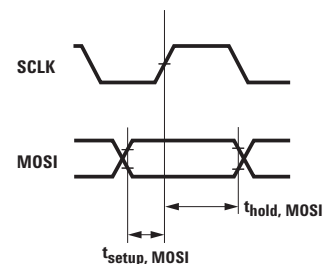


Figure 15. MOSI setup and hold time.

The port is a four-wire port. The host micro-controller always initiates communication; the ADNS-7050 never initiates data transfers. SCLK, MOSI, and NCS may be driven directly by a micro-controller. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is tri-stated.

## The lines that comprise the SPI port:

SCLK: Clock input. It is always generated by the master (the microcontroller).

MOSI: Input data. (Master Out/Slave In)

MISO: Output data. (Master In/Slave Out)

NCS: Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

## Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. This is true for all transactions. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD and EFT/B events could be interpreted as



serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

### Write Operation

Write operation, defined as data going from the micro-controller to the ADNS-7050, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The ADNS-7050 reads MOSI on rising edges of SCLK.

### Read Operation

A read operation, defined as data going from the ADNS-7050 to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the ADNS-7050 over MISO. The sensor outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.

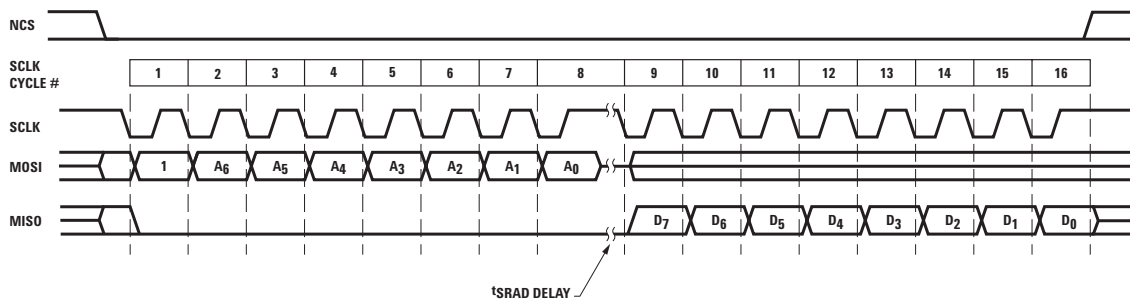


Figure 16. Read operation.

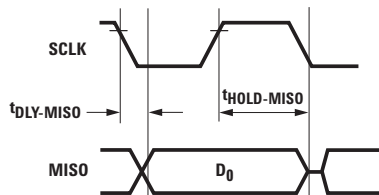


Figure 17. MISO delay and hold time.

Note:

The  $0.5/f_{SCLK}$  minimums high state of SCLK is also the minimum MISO data hold time of the ADNS-7050. Since the falling edge of SCLK is actually the start of the next read or write command, the ADNS-7050 will hold the state of data on MISO until the falling edge of SCLK.

### Required Timing Between Read and Write Commands

There are minimum timing requirements between read and write commands on the serial port.

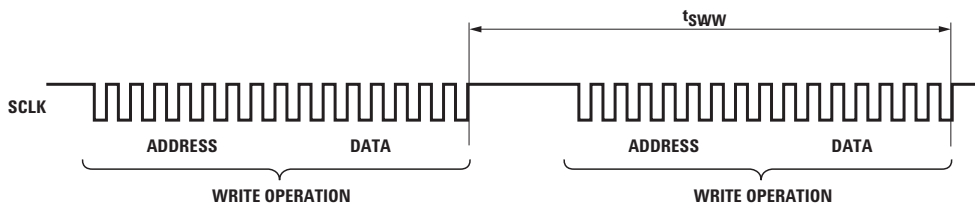


Figure 18. Timing between two write commands.

If the rising edge of the SCLK for the last data bit of the second write command occurs before the required delay ( $t_{SWW}$ ), then the first write command may not complete correctly.

If the rising edge of SCLK for the last address bit of the read command occurs before the required delay ( $t_{SWR}$ ), the write command may not complete correctly.

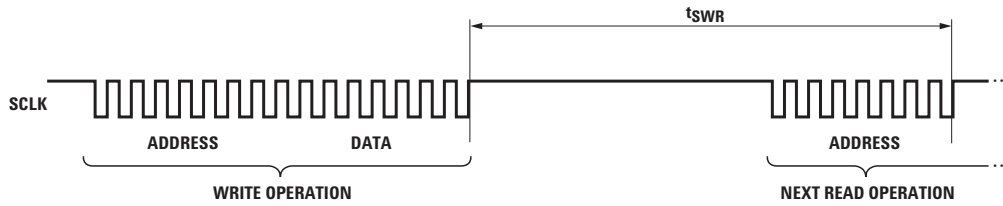


Figure 19. Timing between write and read commands.

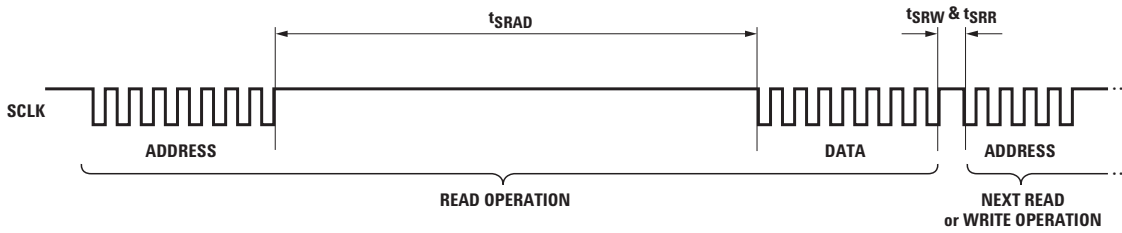


Figure 20. Timing between read and either write or subsequent read commands.

During a read operation SCLK should be delayed at least  $t_{SRAD}$  after the last address data bit to ensure that the ADNS-7050 has time to prepare the requested data. The falling edge of SCLK for the first address bit of either the read or write command must be at least  $t_{SRR}$  or  $t_{SRW}$  after the last SCLK rising edge of the last data bit of the previous read operation.

### Burst Mode Operation

Burst mode is a special serial port operation mode that may be used to reduce the serial transaction time for a motion read. The speed improvement is achieved by continuous data clocking to or from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

Burst mode is activated by reading the Motion\_Burst register. The ADNS-7050 will respond with the contents of the Motion, Delta\_X, Delta\_Y, SQUAL, Shutter\_Upper, Shutter\_Lower, and Maximum\_Pixel registers in that order. The burst transaction can be terminated anywhere in the sequence after the Delta\_X value by bringing the NCS pin high. After sending the register address, the micro-controller must wait  $t_{SRAD}$  and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data are latched into the output buffer after the last address bit is received. After the burst transmission is complete, the micro-controller must raise the NCS line for at least  $t_{BEXIT}$  to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

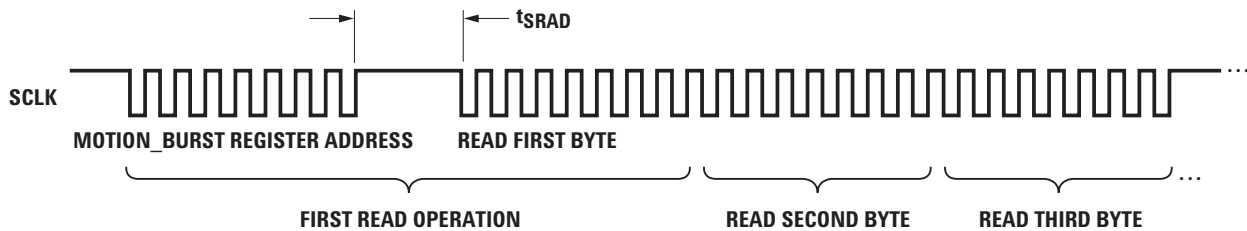


Figure 21. Motion burst timing.

## Notes on Power-up

The ADNS-7050 does not perform an internal power up self-reset; the POWER\_UP\_RESET register must be written every time power is applied. The appropriate sequence is as follows:

1. Apply power
2. Drive NCS high, then low to reset the SPI port
3. Write 0x5a to register 0x3a
4. Wait for  $t_{WAKEUP}$
5. Write 0xFE to register 0x28
6. Read from registers 0x02, 0x03, and 0x04 (or read these same 3 bytes from burst motion register 0x42) one time regardless of the motion pin state.

During power-up there will be a period of time after the power supply is high but before any clocks are available. The table below shows the state of the various pins during power-up and reset.

### State of Signal Pins after VDD is Valid

Pin	On Power-Up	NCS High before Reset	NCS Low before Reset	After Reset
NCS	Functional	Hi	Low	Functional
MISO	Undefined	Undefined	Functional	Depends on NCS
SCLK	Ignored	Ignored	Functional	Depends on NCS
MOSI	Ignored	Ignored	Functional	Depends on NCS
XY_LASER	Undefined	Undefined	Undefined	Functional
MOTION	Undefined	Undefined	Undefined	Functional
LASER_NEN	Undefined	Undefined	Undefined	Functional

Pin	Status when Shutdown Mode
NCS	Functional*1
MISO	Undefined*2
SCLK	Ignore if NCS = 1*3
MOSI	Ignore if NCS = 1*4
XYLASER	High(Off)
LASER_NEN	High(Off)
MOTION	Undefined *2

## Notes on Shutdown and Forced Rest

The ADNS-7050 can be set in Rest mode through the Configuration\_Bits register (0x11). This is to allow for further power savings in applications where the sensor does not need to operate all the time.

The ADNS-7050 can be set in Shutdown mode by writing 0xe7 to register 0x3b. The SPI port should not be accessed when Shutdown mode is asserted, except the power-up command (writing 0x5a to register 0x3a). (Other ICs on the same SPI bus can be accessed, as long as the sensor's NCS pin is not asserted.) The table below shows the state of various pins during shutdown. To deassert Shutdown mode:

1. Write 0x5a to register 0x3a.
2. Wait for  $t_{WAKEUP}$ .
3. Write 0xFE to register 0x28.
4. Any register settings must then be reloaded.

\*1 NCS pin must be held to 1 (high) if SPI bus is shared with other devices. It is recommended to hold to 1 (high) during Power Down unless powering up the Sensor. It must be held to 0 (low) if the sensor is to be re-powered up from shutdown (writing 0x5a to register 0x3a).

\*2 Depend on last state.

\*3 SCLK is ignore if NCS is 1 (high). It is functional if NCS is 0 (low).

\*4 MOSI is ignore if NCS is 1 (high). If NCS is 0 (low), any command present on the MOSI pin will be ignored except power-up command (writing 0x5a to register 0x3a).

Note:

There are long wakeup times from shutdown and forced Rest. These features should not be used for power management during normal mouse motion.

## Registers

The ADNS-7050 registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Address	Register	Read/Write	Default Value
0x00	Product_ID	R	0x23
0x01	Revision_ID	R	0x03
0x02	Motion	R/W	0x00
0x03	Delta_X	R	0x00
0x04	Delta_Y	R	0x00
0x05	SQUAL	R	0x00
0x06	Shutter_Upper	R	0x00
0x07	Shutter_Lower	R	0x64
0x08	Maximum_Pixel	R	0xd0
0x09	Pixel_Sum	R	0x80
0x0a	Minimum_Pixel	R	0x00
0x0b	Pixel_Grab	R/W	0x00
0x0c	CRC0	R	0x00
0x0d	CRC1	R	0x00
0x0e	CRC2	R	Undefined
0x0f	CRC3	R	Undefined
0x10	Self_Test	W	NA
0x11	Configuration_Bits	R/W	0x03
0x12-0x19	Reserved		
0x1a	LASER_CTRL0	R/W	0x00
0x1b	Reserved		
0x1c	LSRPWR_CFG0	R/W	0x00
0x1d	LSRPWR_CFG1	R/W	0x00
0x1e	Reserved		
0x1f	LASER_CTRL1	R/W	0x01
0x20-0x2d	Reserved		
0x2e	Observation	R/W	Undefined
0x2f-0x39	Reserved		
0x3a	POWER_UP_RESET	W	NA
0x3b	Shutdown	W	NA
0x3c-0x3d	Reserved		
0x3e	Inverse_Revision_ID	R	0xfc
0x3f	Inverse_Product_ID	R	0xdc
0x42	Motion_Burst	R	0x00

---

**Product\_ID**      Address: 0x00  
Access: Read      Reset Value: 0x23

Bit	7	6	5	4	3	2	1	0
Field	PID <sub>7</sub>	PID <sub>6</sub>	PID <sub>5</sub>	PID <sub>4</sub>	PID <sub>3</sub>	PID <sub>2</sub>	PID <sub>1</sub>	PID <sub>0</sub>

Data Type: 8-Bit unsigned integer

USAGE: This register contains a unique identification assigned to the ADNS-7050. The value in this register does not change; it can be used to verify that the serial communications link is functional.

---

**Revision\_ID**      Address: 0x01  
Access: Read      Reset Value: 0x03

Bit	7	6	5	4	3	2	1	0
Field	RID <sub>7</sub>	RID <sub>6</sub>	RID <sub>5</sub>	RID <sub>4</sub>	RID <sub>3</sub>	RID <sub>2</sub>	RID <sub>1</sub>	RID <sub>0</sub>

Data Type: 8-Bit unsigned integer

USAGE: This register contains the IC revision. It is subject to change when new IC versions are released.

---

**Motion** Address: 0x02

Access: Read/Write      Reset Value: 0x00

---

<b>Bit</b>	7	6	5	4	3	2	1	0
<b>Field</b>	MOT	PIXRDY	PIXFIRST	OVF	LP_VALID	FAULT	Reserved	Re- served

---

Data Type: Bit field

USAGE: Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If the MOT bit is set, then the user should read registers 0x03 and 0x04 to get the accumulated motion. Read this register before reading the Delta\_X and Delta\_Y registers.

Writing anything to this register clears the MOT and OVF bits, Delta\_X and Delta\_Y registers. The written data byte is not saved.

Internal buffers can accumulate more than eight bits of motion for X or Y. If either one of the internal buffers overflows, then absolute path data is lost and the OVF bit is set. To clear the overflow, write anything to this register.

Check the OVR bit if more than 4" of motion is accumulated without reading it. If bit set, discard the motion as erroneous. Write anything to this register to clear the overflow condition.

The PIXRDY bit will be set whenever a valid pixel data byte is available in the Pixel\_Dump register. Check that this bit is set before reading from Pixel\_Dump. To ensure that the Pixel\_Grab pointer has been reset to pixel 0,0 on the initial write to Pixel\_Grab, check to see if PIXFIRST is set to high.

---

<b>Field Name</b>	<b>Description</b>
MOT	Motion since last report 0 = No motion 1 = Motion occurred, data ready for reading in Delta_X and Delta_Y registers
PIXRDY	Pixel Dump data byte is available in Pixel_Dump register. 0 = Data not available 1 = Data available
PIXFIRST	This bit is set when the Pixel_Grab register is written to or when a complete pixel array has been read, initiating an increment to pixel 0,0. 0 = Pixel_Grab data not from pixel 0,0 1 = Pixel_Grab data is from pixel 0,0
OVF	Motion overflow, ΔY and/or ΔX buffer has overflowed since last report. 0 = No overflow 1 = Overflow has occurred
LP_VALID	Laser Power Settings 0 = Register 0x1a and register 0x1f or register 0x1c and register 0x1d do not have complementary values. 1 = Laser power is valid
FAULT	Indicates that XY_LASER is shorted to GND or VDD 0 = No fault detected 1 = Fault detected.

---

NOTE: Avago Technologies recommends that registers 0x02, 0x03, and 0x04 be read sequentially.

**Delta X**      Address: 0x03  
 Access: Read    Reset Value: 0x00

<b>Bit</b>	7	6	5	4	3	2	1	0
<b>Field</b>	X <sub>7</sub>	X <sub>6</sub>	X <sub>5</sub>	X <sub>4</sub>	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>

Data Type: Eight bit 2's complement number

USAGE: X movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.



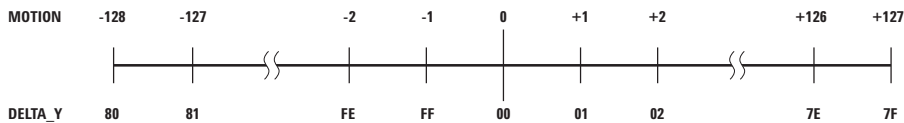
NOTE: Avago Technologies recommends that registers 0x02, 0x03, and 0x04 be read sequentially.

**Delta Y**      Address: 0x04  
 Access: Read    Reset Value: 0x00

<b>Bit</b>	7	6	5	4	3	2	1	0
<b>Field</b>	Y <sub>7</sub>	Y <sub>6</sub>	Y <sub>5</sub>	Y <sub>4</sub>	Y <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>

Data Type: Eight bit 2's complement number

USAGE: Y movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.



NOTE: Avago Technologies recommends that registers 0x02, 0x03, and 0x04 be read sequentially.

**Squal** Address: 0x05  
 Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	SQ <sub>7</sub>	SQ <sub>6</sub>	SQ <sub>5</sub>	SQ <sub>4</sub>	SQ <sub>3</sub>	SQ <sub>2</sub>	SQ <sub>1</sub>	SQ <sub>0</sub>

Data Type: Upper 8 bits of a 9-bit unsigned integer

USAGE: SQUAL (Surface Quality) is a measure of the number of valid features visible by the sensor in the current frame.

The maximum SQUAL register value is 162. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected. The graph below shows 250 sequentially acquired SQUAL values, while a sensor was moved slowly over white paper. SQUAL is nearly equal to zero, if there is no surface below the sensor. SQUAL is typically maximized when the navigation surface is at the optimum distance from the imaging lens (the nominal Z-height).

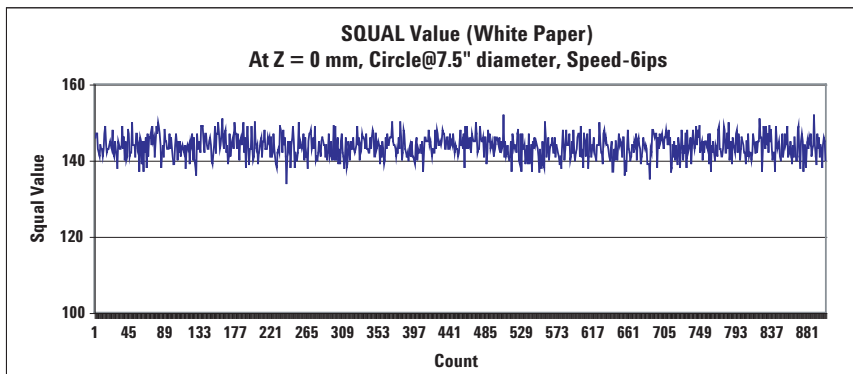


Figure 22. SQUAL values at 800dpi (white paper).

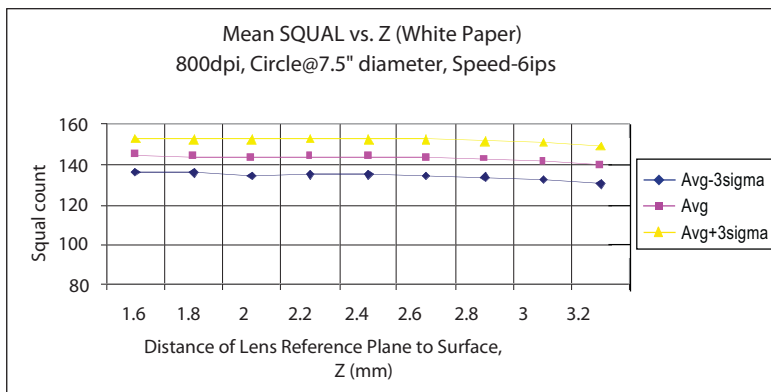


Figure 23. Mean SQUAL vs. Z (white paper).



**Shutter\_Upper** Address: 0x06  
 Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	S <sub>15</sub>	S <sub>14</sub>	S <sub>13</sub>	S <sub>12</sub>	S <sub>11</sub>	S <sub>10</sub>	S <sub>9</sub>	S <sub>8</sub>

**Shutter\_Lower** Address: 0x07  
 Access: Read Reset Value: 0x64

Bit	7	6	5	4	3	2	1	0
Field	S <sub>7</sub>	S <sub>6</sub>	S <sub>5</sub>	S <sub>4</sub>	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>

Data Type: Sixteen bit unsigned integer

USAGE: Units are clock cycles. Read Shutter\_Upper first, then Shutter\_Lower. They should be read consecutively. The shutter is adjusted to keep the average and maximum pixel values within normal operating ranges. The shutter value is automatically adjusted.

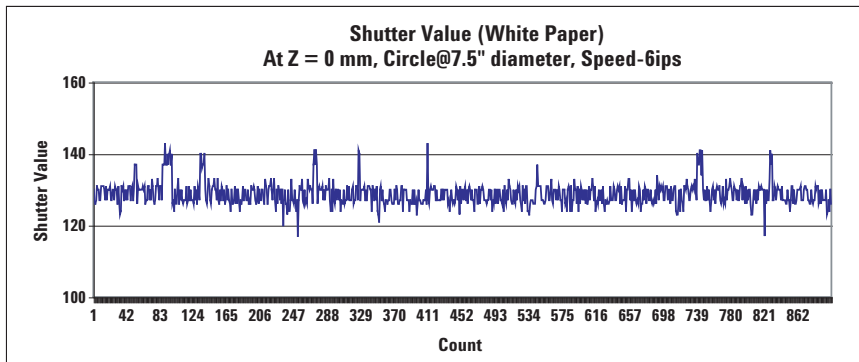


Figure 24. Shutter values at 800dpi (white paper).

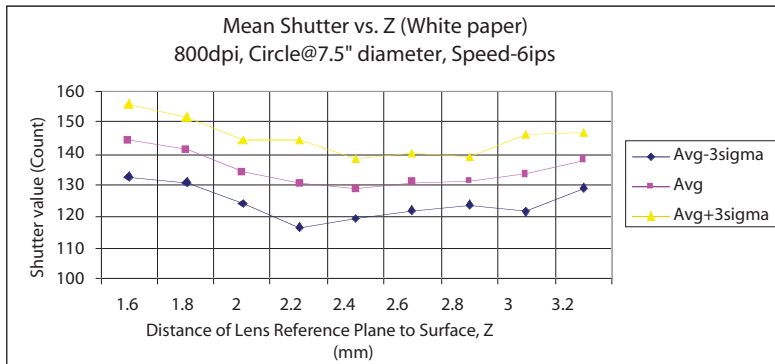


Figure 25. Mean shutter vs. Z (white paper).

---

**Maximum\_Pixel**    Address: 0x08

Access: Read    Reset Value: 0xd0

Bit	7	6	5	4	3	2	1	0
Field	MP <sub>7</sub>	MP <sub>6</sub>	MP <sub>5</sub>	MP <sub>4</sub>	MP <sub>3</sub>	MP <sub>2</sub>	MP <sub>1</sub>	MP <sub>0</sub>

Data Type: Eight-bit number

USAGE: Maximum Pixel value in current frame. Minimum value = 0, maximum value = 254. The maximum pixel value can vary with every frame.

---

**Pixel\_Sum**    Address: 0x09

Access: Read    Reset Value: 0x80

Bit	7	6	5	4	3	2	1	0
Field	AP <sub>7</sub>	AP <sub>6</sub>	AP <sub>5</sub>	AP <sub>4</sub>	AP <sub>3</sub>	AP <sub>2</sub>	AP <sub>1</sub>	AP <sub>0</sub>

Data Type: High 8 bits of an unsigned 17-bit integer

USAGE: This register is used to find the average pixel value. It reports the upper eight bits of a 17-bit counter, which sums all pixels in the current frame. It may be described as the full sum divided by 512. To find the average pixel value, use the following formula:

$$\text{Average Pixel} = \text{Register Value} * 512/484 = \text{Register Value} * 1.058$$

The maximum register value is 241. The minimum is 0. The pixel sum value can change on every frame.