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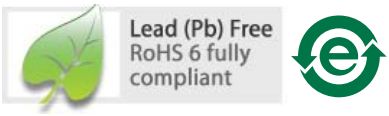
ADNS-7700

One chip USB LaserStream™ Mouse Sensors

Data Sheet



Description

The ADNS-7700 series are compact, low cost, one chip USB LaserStream™ mouse sensors designed for implemention of a non-mechanical tracking engine in computer mice.

This ADNS-7700 sensor is a 22-pin integrated molded lead-frame DIP package. It comprises a USB controller and LaserStream navigation sensor with VCSEL integrated within a single package. It is designed to be used with the ADNS-6180-001 trim lens or ADNS-6180-002 wide trim lens to achieve the LaserStream performance featured in this document. These parts provide a complete and compact navigation system with no moving parts and precision optical alignment to facilitate high volume assembly. Avago has pre-calibrated the laser power prior shipment, thus NO laser power calibration is required at manufacturer site, therefore reducing assembly time and associated cost.

The motion output is a selectable 8/12/16-bit USB data reporting format. This device is compliant to USB Revision 2.0 low speed specification. The ADNS-7700 series are designed with on-chip One-Time-Programmable (OTP) memory. This enables device configuration flexibility for the manufacturer to cater for various market segments.

Theory of Operation

The ADNS-7700 is based on Laser-Stream navigation technology that measures changes in position by optically acquiring sequential surface images (per frames) and mathematically determining the direction and magnitude of motion movement.

It contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP) and USB stream output. The IAS acquires microscopic surface images via the lens. These images are processed by the DSP to determine the direction and distance of motion. The DSP generates the Δx and Δy relative displacement values which are converted to USB motion data.

Features

- One chip USB laser mouse sensor with VCSEL integrated in single package
- LaserStream™ navigation technology
- USB 2.0 Low Speed Compliance
- Meets HID Revision 1.11
- Single 5.0 volts power supply
- Compliance to IEC/EN 60825-1 Class 1 Eye Safety
  - Pre-calibrated laser power prior shipment
  - Class 1 eye safety AEL
  - On-chip Laser fault detect circuitry
- High speed motion detection at 45 inches per second (ips) and acceleration up to 20g
- Input buttons: 3 or 5-buttons
- Mechanical Z-Wheel interface for vertical scroll
- On-chip OTP memory for device configuration flexibility without any external software driver:
  - Enable/Disable Tilt-Wheel* function that supports horizontal scroll in Microsoft Vista OS.
  - 8/12/16-bit USB motion data reporting
  - Resolution
    - Programmable from 400-2400 counts per inch (cpi) with ~100cpi incremental step
    - 3 selections of On-the-Fly (OTF) resolution mode setting
- KeyMap (KM) for keyboard shortcut key
- Customizable VID, PID, Manufacturer string and Product string
- 4-axis sensor rotations: 0°, 90°, 180° or 270°

Applications

- Corded laser mice
- Integrated input devices

* Disclaimer: All designers and manufacturers of this design must assure that they have all necessary intellectual property rights

Ordering Part Numbers:

	Description for USB LaserStream Mouse Sensor			
Part Number	**Input Button**	**Tilt-Wheel**	**OTF Resolution**	**KeyMap**
ADNS-7700-H4MY	3-buttons	Programmable	–	–
ADNS-7700-HAMY	3-buttons	Programmable	Programmable	–
ADNS-7700-HCMY	5-buttons	Programmable	Programmable	–
ADNS-7700-HMMY	5-buttons	Programmable	Programmable	Programmable

Package Pinout

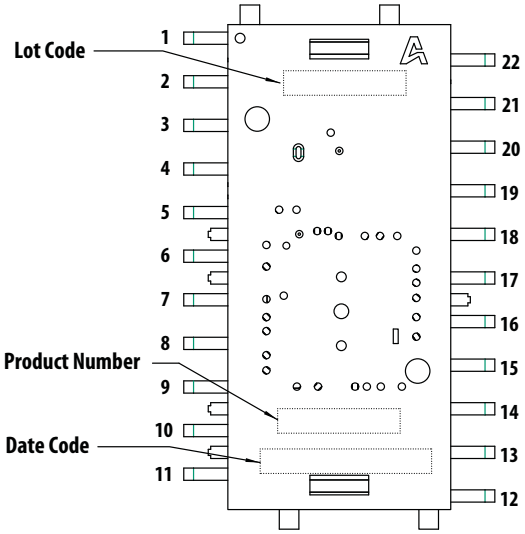


Figure 1. Device Pinout

Item	Marking	Remarks
Product Number	A7700	
Date Code	XYYWWZV	X = Subcon Code YYWW = Date Code Z = Sensor Die Source V = VCSEL Die Source
Lot Code	VVV	Numeric

Table 1. Pin Name Description

Pin Name	Description	Pin Name	Description
-VCSEL	Negative terminal of VCSEL	B1	Left button input (LB)
+VCSEL	Positive terminal of VCSEL	B2	Right button input (RB)
D+	USB D+ line	B3	Middle button input (MB)
D-	USB D- line	B4	Back button input (BB)
OSC_IN	Ceramic resonator input	B5	Forward button input (FB)
OSC_OUT	Ceramic resonator output	TW1*	Left tilt input
VDD5	5-Volt Power (USB VBUS)	TW2*	Right tilt input
DGND	System ground	LED0	Resolution LED indicator output
AGND	Analog ground	LED1	Resolution LED indicator output
LASER_GND	LASER ground	LED2	Resolution LED indicator output
REFA	Reference voltage capacitor	ZA	Z-Wheel quadrature input
REFB	Reference voltage capacitor	ZB	Z-Wheel quadrature input
REFC	Reference coupling	KM1	KeyMap 1 button input
OTF	OTF Resolution button input	KM2	KeyMap 2 button input
OTF_L	OTF Resolution Long Press button input	NC	No Connection

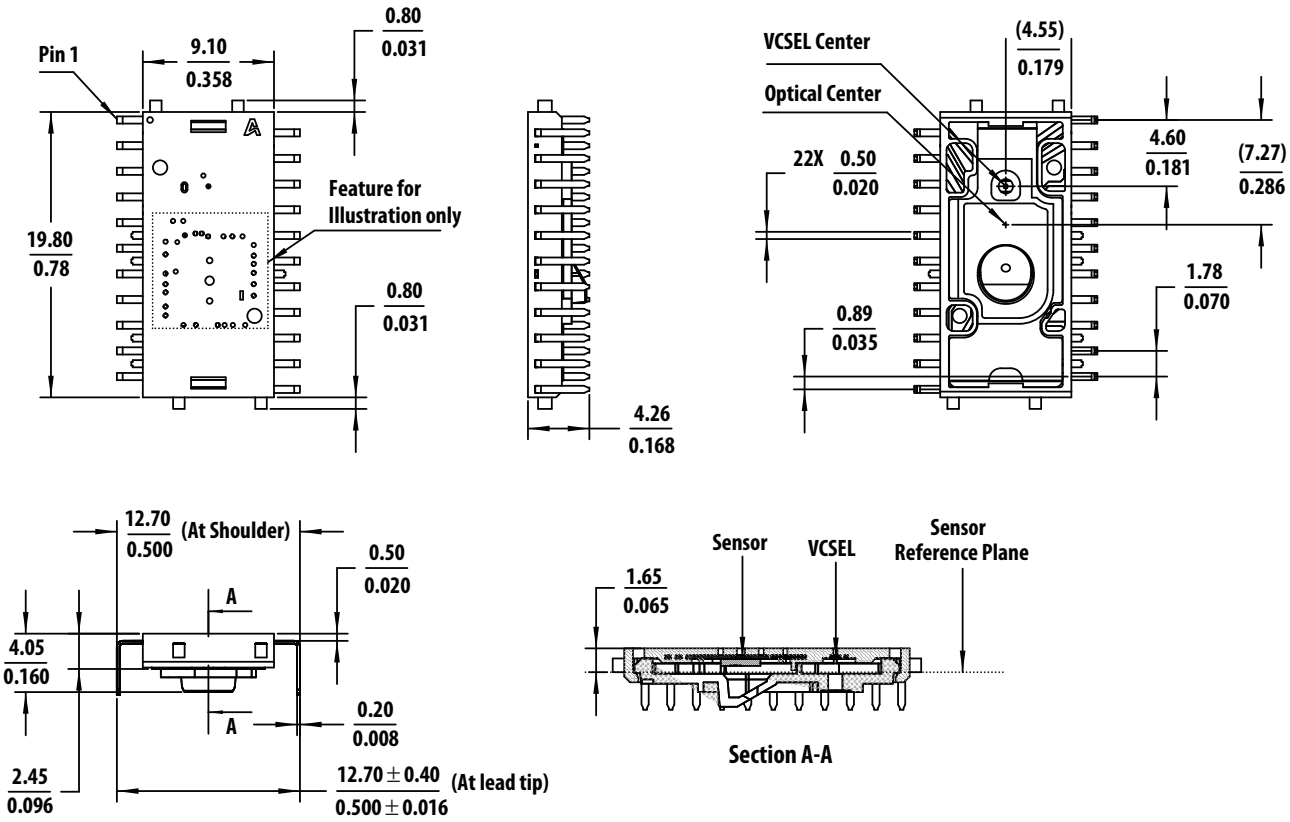
Table 2a. Device Pinout Configurations

	ADNS-7700-H4MY		ADNS-7700-HAMY				ADNS-7700-HCMY			
Pin No	**3B**	**3B + TW**	**3B**	**3B + TW**	**3B + OTF + 3LED**	**3B + TW + OTF**	**5B**	**5B + TW**	**5B + OTF**	**4B + TW + OTF**
1	+VCSEL	**+VCSEL**	+VCSEL	**+VCSEL**	+VCSEL	+VCSEL	+VCSEL	**+VCSEL**	+VCSEL	+VCSEL
2	NC	**TW2***	NC	**TW2***	LED0	TW2*	NC	**TW2***	OTF	TW2*
3	NC	**TW1***	NC	**TW1***	LED1	TW1*	NC	**TW1***	NC	TW1*
4	LASER_GND	**LASER_GND**	LASER_GND	**LASER_GND**	LASER_GND	LASER_GND	LASER_GND	**LASER_GND**	LASER_GND	LASER_GND
5	REFB	**REFB**	REFB	**REFB**	REFB	REFB	REFB	**REFB**	REFB	REFB
6	VDD5	**VDD5**	VDD5	**VDD5**	VDD5	VDD5	VDD5	**VDD5**	VDD5	VDD5
7	REFC	**REFC**	REFC	**REFC**	REFC	REFC	REFC	**REFC**	REFC	REFC
8	ZA	**ZA**	ZA	**ZA**	ZA	ZA	ZA	**ZA**	ZA	ZA
9	ZB	**ZB**	ZB	**ZB**	ZB	ZB	ZB	**ZB**	ZB	ZB
10	AGND	**AGND**	AGND	**AGND**	AGND	AGND	AGND	**AGND**	AGND	AGND
11	REFA	**REFA**	REFA	**REFA**	REFA	REFA	REFA	**REFA**	REFA	REFA
12	DGND	**DGND**	DGND	**DGND**	DGND	DGND	DGND	**DGND**	DGND	DGND
13	OSC_OUT	**OSC_OUT**	OSC_OUT	**OSC_OUT**	OSC_OUT	OSC_OUT	OSC_OUT	**OSC_OUT**	OSC_OUT	OSC_OUT
14	OSC_IN	**OSC_IN**	OSC_IN	**OSC_IN**	OSC_IN	OSC_IN	OSC_IN	**OSC_IN**	OSC_IN	OSC_IN
15	NC	**NC**	NC	**NC**	OTF	OTF	B5	**B5**	B5	OTF
16	NC	**NC**	NC	**NC**	LED2	NC	B4	**B4**	B4	B4
17	B3	**B3**	B3	**B3**	B3	B3	B3	**B3**	B3	B3
18	B2	**B2**	B2	**B2**	B2	B2	B2	**B2**	B2	B2
19	B1	**B1**	B1	**B1**	B1	B1	B1	**B1**	B1	B1
20	D-	**D-**	D-	**D-**	D-	D-	D-	**D-**	D-	D-
21	D+	**D+**	D+	**D+**	D+	D+	D+	**D+**	D+	D+
22	-VCSEL	**-VCSEL**	-VCSEL	**-VCSEL**	-VCSEL	-VCSEL	-VCSEL	**-VCSEL**	-VCSEL	-VCSEL

Table 2b. Device Pinout Configurations

	ADNS-7700-HMMY						
Pin No	**5B**	**5B + TW**	**5B + KM1/OTF_L**	**5B + KM1/OTF_L + KM2**	**4B + TW + KM1/ OTF_L**	**3B + TW + KM1/ OTF_L**	**3B + TW + KM1/ OTF_L + KM2**
1	+VCSEL	**+VCSEL**	+VCSEL	+VCSEL	+VCSEL	+VCSEL	+VCSEL
2	NC	**TW2***	KM1/OTF_L	KM1/OTF_L	TW2*	TW2*	TW2*
3	NC	**TW1***	NC	KM2	TW1*	TW1*	TW1*
4	LASER_GND	**LASER_GND**	LASER_GND	LASER_GND	LASER_GND	LASER_GND	LASER_GND
5	REFB	**REFB**	REFB	REFB	REFB	REFB	REFB
6	VDD5	**VDD5**	VDD5	VDD5	VDD5	VDD5	VDD5
7	REFC	**REFC**	REFC	REFC	REFC	REFC	REFC
8	ZA	**ZA**	ZA	ZA	ZA	ZA	ZA
9	ZB	**ZB**	ZB	ZB	ZB	ZB	ZB
10	AGND	**AGND**	AGND	AGND	AGND	AGND	AGND
11	REFA	**REFA**	REFA	REFA	REFA	REFA	REFA
12	DGND	**DGND**	DGND	DGND	DGND	DGND	DGND
13	OSC_OUT	**OSC_OUT**	OSC_OUT	OSC_OUT	OSC_OUT	OSC_OUT	OSC_OUT
14	OSC_IN	**OSC_IN**	OSC_IN	OSC_IN	OSC_IN	OSC_IN	OSC_IN
15	B5	**B5**	B5	B5	KM1/OTF_L	KM1/OTF_L	KM1/OTF_L
16	B4	**B4**	B4	B4	B4	NC	KM2
17	B3	**B3**	B3	B3	B3	B3	B3
18	B2	**B2**	B2	B2	B2	B2	B2
19	B1	**B1**	B1	B1	B1	B1	B1
20	D-	**D-**	D-	D-	D-	D-	D-
21	D+	**D+**	D+	D+	D+	D+	D+
22	-VCSEL	**-VCSEL**	-VCSEL	-VCSEL	-VCSEL	-VCSEL	-VCSEL

* Disclaimer: All designers and manufacturers of this design must assure that they have all necessary intellectual property rights.



NOTES: (Unless otherwise specified)

1. Dimensions in milimeter / inches.
2. Dimensional tolerance: ± 0.1mm.
3. Coplanarity of leads: 0.1mm.
4. Lead pitch tolerance: ± 0.15mm.
5. Non-cumulative pitch tolerance: ± 0.15mm.
6. Angular tolerance: ± 3°
7. Maximum flash: 0.2mm.
8. Chamfer (25° x 2) on the taper side of the lead.
9. Brackets () indicate reference dimension.
10. Document Number: LSR_SOC_INT_22A_Pkg_001

Figure 2. Package outline drawing

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Assembly Drawings

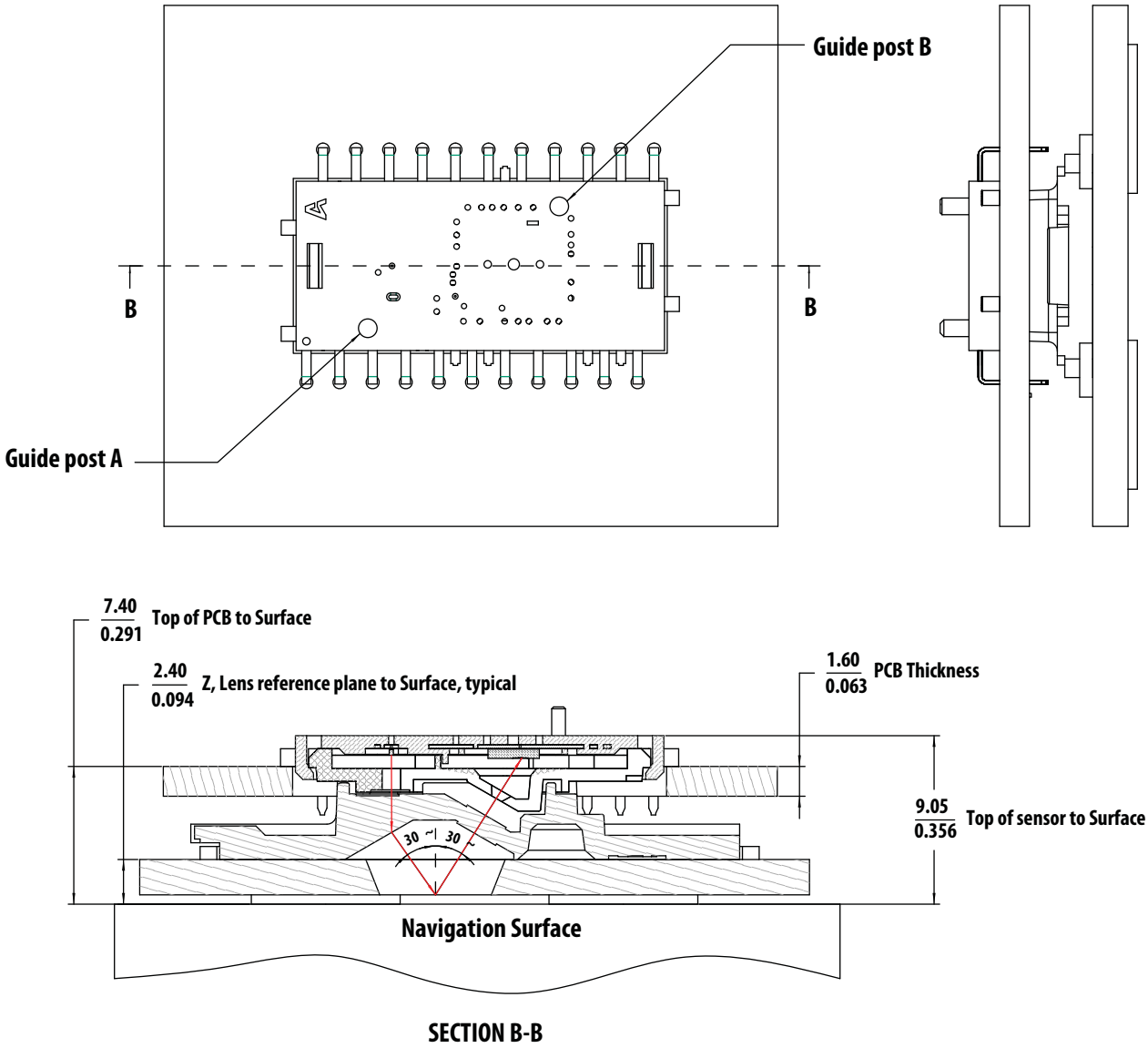
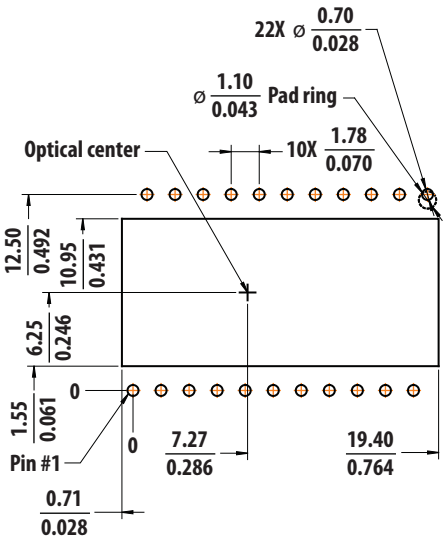


Figure 3. 2D assembly drawing of ADNS-7700 sensor coupled with ADNS-6180-002 lens, PCB & base plate

As shown in Figure 5, the components self align as they are mounted onto defined features on the base plate. The ADNS-7700 sensor is designed for mounting on a through-hole PCB, looking down. The guide holes in the sensor package mates and self-aligns with the guide posts in the ADNS-6180-001 or ADNS-6180-002 lens.

The integrated VCSEL is used for the illumination, provides a laser diode with a single longitudinal and a single transverse mode. Together with the VCSEL contained in the sensor package, the ADNS-6180-001 or ADNS-6180-002 lens provides directed illumination and optical imaging necessary for the operation of the sensor. The lens is a precision molded optical component and should be handled with care to avoid scratching and contamination on the optical surfaces.

3D drawing files in STEP or IGES format for the sensor, lens and base plate describing the components and base plate molding features for the lens and PCB alignment is available.



Dimensions in mm/inches

Figure 4. Recommended PCB mechanical cutouts and spacing

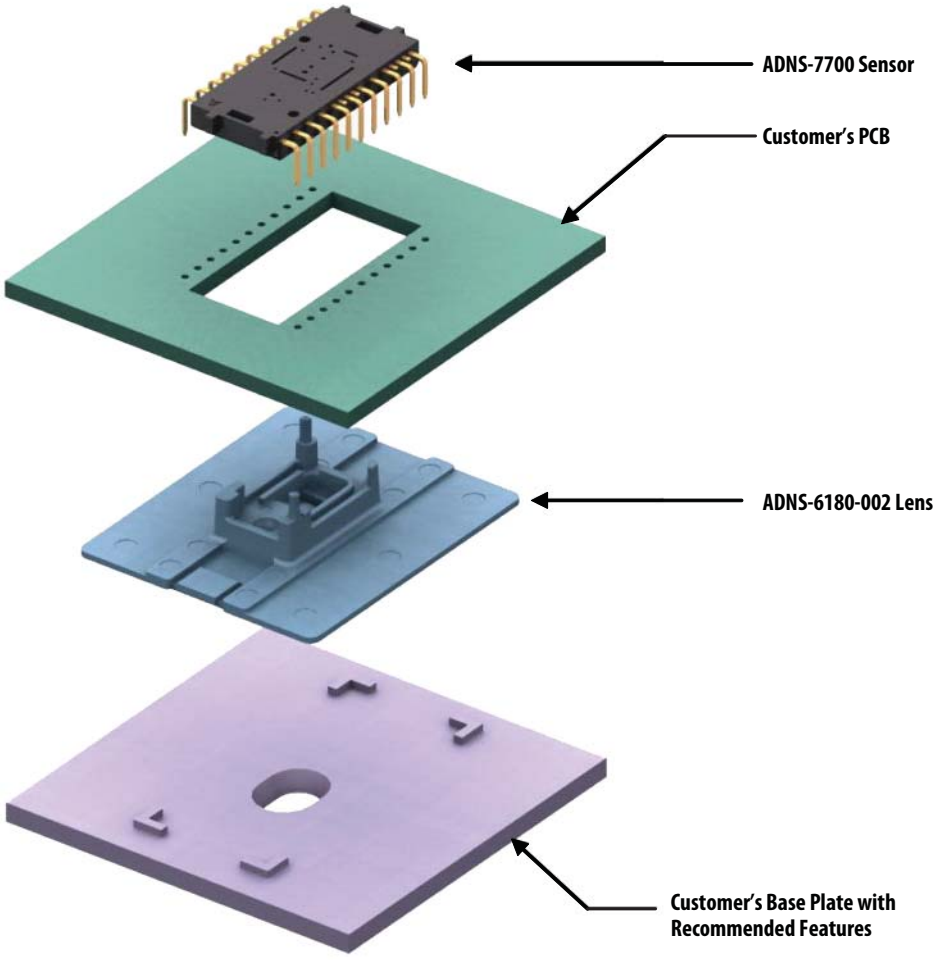


Figure 5. Exploded view drawing of ADNS-7700 sensor coupled with ADNS-6180-002 lens, PCB & base plate

Application Schematics

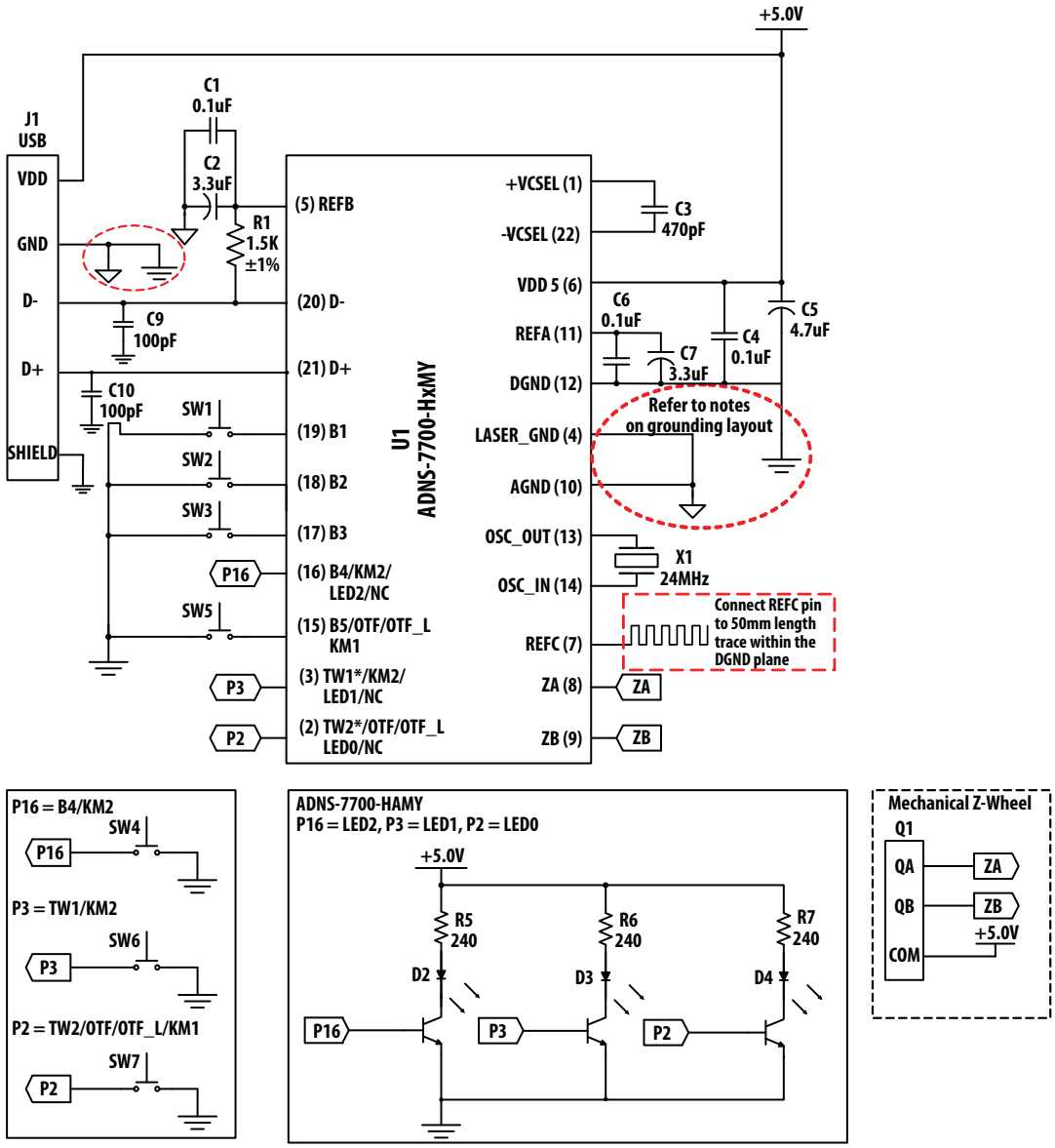


Figure 6. ADNS-7700 Sensor's Application Schematics

* DISCLAIMER: ALL DESIGNERS AND MANUFACTURERS OF THIS DESIGN MUST ASSURE THAT THEY HAVE ALL NECESSARY INTELLECTUAL PROPERTY RIGHTS.

PCB Layout Considerations:

1. The DGND and AGND paths *MUST* be layout as far as possible and connected together at the USB ground point with star topology. Ensure large grounding plane on the PCB layout for better performance on ESD and EFTB.
2. All caps *MUST* be as close to VDD5, REFA, REFB & +VCSEL sensor pins as possible and ground at the DGND and AGND plane that connected to USB GND, with trace length less than 5mm.
3. 1.5kΩ pullup resistor (R1) should be ± 1% tolerance and connected to REFB pin with shortest possible trace length.
4. Ceramic non-polarity caps and tantalum polarity caps are recommended.
5. Caps should have less than 5nH of self inductance.
6. Caps connected to VDD5 *MUST* have less than 0.2Ω ESR.
7. REFC pin requires an open ended trace of min 50 mm lengths within DGND plane for EFTB performance improvement. Refer to System Design Recommendations Application Note.
8. Do not use jumper on ground plane, D+ and D- paths.
9. Data lines (D+ and D-) should be as far as possible from resonator.

PCB Assembly Considerations

1. Insert the sensor package and all other electrical components into the application PCB. To maintain the Z alignment of sensor package, the sensor reference plane can be sit directly on the PCB.
2. This sensor package is only qualified for wave-solder process.
3. Wave solder the entire assembly in a non-wash solder process utilizing solder fixture. The solder fixture is needed to protect the sensor during the solder process shielding the optical aperture from direct solder contact.
4. Place the lens onto the base plate. Care must be taken to avoid contamination and scratches on the optical surfaces.
5. Hold the PCB vertically and remove the Kapton tape attached to the respective aperture of sensor and VCSEL. During the removal process of Kapton tape, care must be taken to prevent contaminants from entering through the apertures. Do NOT place the PCB facing upwards during the entire mouse assembly process.
6. Place the PCB over the lens onto base plate. The sensor package should be self-aligned and locked to the lens by the lens' alignment guide posts. The optical center reference for the PCB is set by base plate and lens. Note that the PCB movement due to button presses must be minimized to maintain good optical alignment.
7. Optional: The lens can be permanently locked to the sensor package by melting the lens' guide posts over the sensor with heat staking process.
8. Then, install the mouse top case. There MUST be feature in the top case (or other area) to press down onto the sensor or PCB assembly to ensure the sensor and lens are interlocked to correct vertical height.

Design Considerations for Improving ESD Performance

For improved electrostatic discharge performance, typical creepage and clearance distance are shown in the table below. Assumption: base plate construction as per the Avago supplied 3D model file when use with ADNS-6180-001 trim lens or ADNS-6180-002 wide trim lens. The lens flange can be sealed (i.e. glued) to the base plate. Note that the lens material is polycarbonate and therefore, cyanoacrylate based adhesives or other adhesives that may damage the lens should NOT be used.

Typical Distance (mm)	ADNS-6180-001 trim lens	ADNS-6180-002 wide trim lens
Creepage	5.5	17.5
Clearance	1.8	1.8

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with unshielded cable and following Avago Technologies recommendations.
- Passes EN 61000-4-4/IEC 801-4 EFT tests when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- Passes IEC-61000-4-2 Electrostatic Discharge Immunity Test (ESD) and provides sufficient ESD creepage/clearance distance to withstand up to 12 kV discharge when assembled into a mouse with ADNS-6180-001 trim lens and up to 15 kV discharge when assembled into a mouse with ADNS-6180-002 wide trim lens.
- Passes IEC/EN 60825-1 Class-1 Eye Safety when ADNS-7700 is driving the laser using ADNS-6180-001 or ADNS-6180-002 lens with recommended operating conditions.

Block Diagram

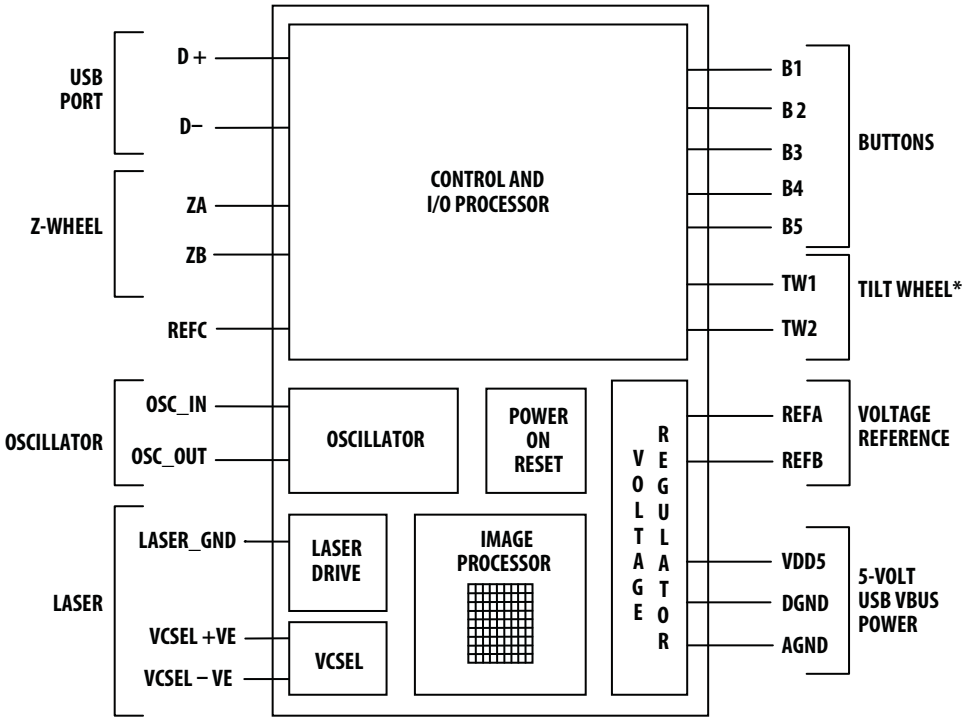


Figure 7. ADNS-7700 Block Diagram

Eye Safety

ADNS-7700 sensor and the associated components in the schematic of Figure 6 are intended to comply with Class 1 Eye Safety requirements of IEC/EN 60825-1. Avago Technologies calibrate sensor laser output power (LOP) to Class 1 eye safety level prior shipping out, thus no laser output power calibration is required at mouse manufacturer site.

ADNS-7700 sensor is designed to maintain the laser output power using ADNS-6180-002 lens within Class 1 requirements over components manufacturing tolerances under the recommended operating conditions and application circuit of Figure 6 as specified in this document. Under normal operating conditions, the sensor generates the drive current for the VCSEL. Increasing the LOP by other means on hardware and software can result in a violation of the Class 1 eye safety limit of 716 µW. For more information, please refer to Eye Safety Application Note.

Laser Output Power

The laser output power,LOP can be measured at the navigation surface plane. The sensor can drive the laser in continuous (CW) mode by writing to LSR_CTRL0 and LSR_CTRL1 registers via USB Set Vendor test command.

The pre-calibrated LOP value at typical operating supply voltage and temperature of 25 ± 5°C should not exceeding 506µW, otherwise the LOP_{max} limit in the Absolute Maximum Rating is applicable.

The following conditions apply:

1. The system is operated based on the recommended application circuit in Figure 6 and within the recommended operating conditions.
2. Measurement is taken at the optical center and illumination angle on navigation surface plane, Z.
3. No allowance for optical power meter accuracy is assumed.

Single Fault Detection

ADNS-7700 sensor is able to detect a short circuit or fault condition at the -VCSEL pin, which could lead to excessive laser power output. A path to ground on this pin will trigger the fault detection circuit, which will turn off the laser drive current source and set the LASER_NEN output high. The system will prevent excess laser power for a resistive path to ground at -VCSEL by shutting off the laser. In addition to the ground path fault detection described above, the fault detection circuit is continuously checking for proper operation by internally generating a path to ground with the laser turned off via LASER_NEN. If the -VCSEL pin is shorted internally to VDD3 or externally to REFB, this test will fail and will be reported as a fault.

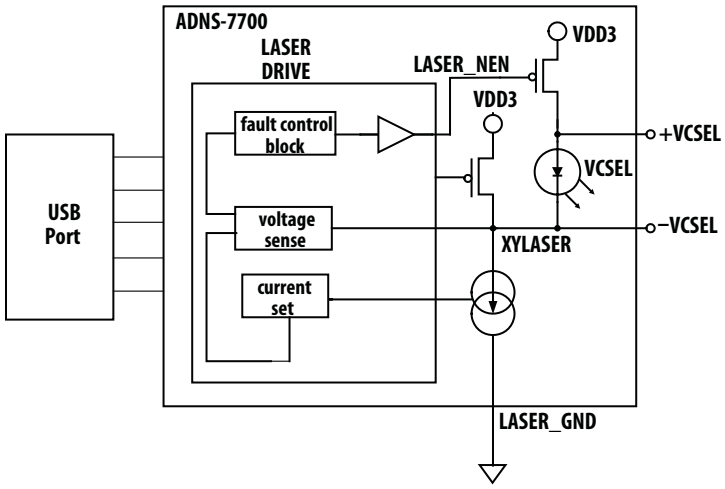


Figure 8. Single Fault Detection and Eye Safety Feature Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Lead Solder Temperature			260	°C	For 7 seconds, 1.6mm below seating plane. Refer to soldering reflow profile in PCB Assembly & Soldering Considerations Application Note AN 5023.
Supply Voltage	V_{DD}	-0.5	5.5	V	
ESD			2	kV	All pins, human body model
Input Voltage	V_{IN}	-0.5	V_{DD}+0.5	V	All I/O pins except OSC_IN and OSC_OUT, D+, D-
Input Voltage	V_{IN}	-1.0	4.6	V	D+, D-, AC waveform, see USB specification (7.1.1)
Input Voltage	V_{IN}	-0.5	3.6	V	OSC_IN and OSC_OUT
Input Short Circuit Voltage	V_{SC}	0	V_{DD}	V	D+, D-, see USB specification (7.1.1)
Laser Output Power	LOP_{max}		716	μW	Class 1 eye safety AEL with ADNS-6180-001 or ADNS-6180-002 lens

Comments:

1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are the stress ratings only and functional operation of the device at these or any other condition beyond those indicated for extended period of time may affect device reliability.
2. The inherent design of this component causes it to be sensitive to electrostatic discharge. The ESD threshold is listed above. To prevent ESD-induced damage, take adequate ESD precautions when handling this product.

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Operating Temperature	T_A	0		40	°C	
Power Supply Voltage	V_{DD}	4.4	5.0	5.25	Volts	For accurate navigation and proper USB operation
Power Supply Rise Time	V_{RT}	0.1		100	ms	
Power Supply Noise	V_N			100	mVp-p	Peak to peak within 50kHz-100MHz bandwidth
Velocity	Vel		45		ips	
Acceleration	Acc			20	g	In Run Mode only
Clock Frequency	f_{clk}	23.64	24.00	24.36	MHz	Due to USB timing constraints
Resonator Impedance	X_{RES}			55	Ω	
Distance from lens reference plane to surface	Z	2.18	2.40	2.62	mm	See Figure 9
Frame Rate			8000		fps	Internally adjusted by sensor
VCSEL's Peak Wavelength	λ	832		865	nm	

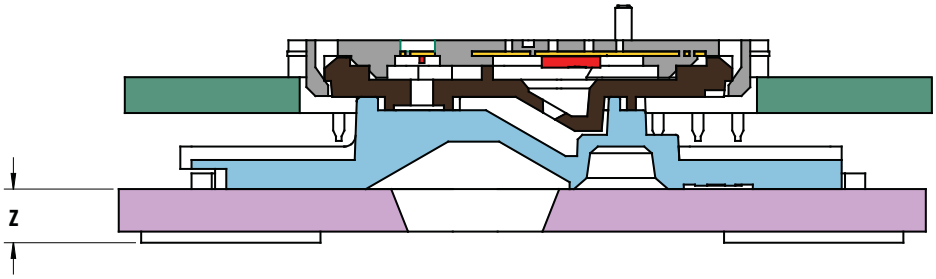


Figure 9. Distance from lens reference plane to object surface, Z

AC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25°C, V_{DD}=5.0 V.

Parameter	Symbol	Min.	Typical	Max.	Units	Notes
Wakeup delay from rest mode due to motion	T_{WUPP}			2	ms	
Power up delay	T_{PUP}			50	ms	Delay measured from VBUS=4.4V
Debounce delay on button inputs	T_{DBB}		6	9	ms	
Z-Wheel sampling period	T_{SW}	1.9	2.0	2.8	ms	ZA & ZB Pins
Transient Supply Current	I_{DDT}			75	mA	Max supply current during a V_{DD} ramp from 0 to 5.0 V with > 500µs rise time. Does not include charging currents for bypass capacitors.

DC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25°C, V_{DD}=5.0 V,

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Run Mode System Current (Mouse moving)	I_{DD5}			100	mA	Includes laser current on
Rest Mode System Current (Mouse not moving)	I_{DD5N}			100	mA	Includes laser current
USB Suspend Mode System Current (Remote Wakeup Enabled)	I_{DD5S}			500	µA	Includes D- pullup resistor
Input Low Voltage	V_{IL}			0.5	V	Pins: ZA, ZB
				0.2*V_{REFB}	V	Pins: B1-B5, TW1, TW2
Input High Voltage	V_{IH}	0.6*V_{DD}			V	Pins: ZA, ZB
		0.8* V_{REFB}			V	Pins: B1-B5, TW1, TW2
Input Hysteresis	V_{HYST}		230		mV	Pins: B1-B5, TW1, TW2
Button Pull Up Current	B_{IOUT}	100	300	500	µA	Pins: B1-B5, TW1, TW2
Regulator output, REFA	VREFA	1.55	1.8	2.05	V	Typical operation current load
Regulator output, REFB	VREFB	3.0	3.3	3.6	V	Typical operation current load

USB Electrical Specifications

Electrical Characteristics over recommended operating conditions.

Parameter	Symbol	Minimum	Maximum	Units	Notes
Output Signal Crossover Voltage	V_{CRS}	1.5	2.0	V	C_L = 200 to 600 pF (see Figure 10)
Input Signal Crossover Voltage	V_{ICRS}	1.2	2.1	V	C_L = 200 to 600 pF (see Figure 10)
Output High	V_{OH}	2.8	3.6	V	with 15kΩ to Ground and 1.5kΩ to V_{REFB} on D- (see Figure 10)
Output Low	V_{OL}	0.0	0.3	V	with 15kΩ to Ground and 1.5kΩ to V_{REFB} on D- (see Figure 10)
Single Ended Output	V_{SE0}		0.8	V	
Input High (Driven)	V_{IH}	2.0		V	
Input High (Floating)	V_{IHZ}	2.7	3.6	V	
Input Low	V_{IL}		0.8	V	1.5kΩ to V_{REFB} on D-
Differential Input Sensitivity	V_{DI}	0.2		V	|(D+)-(D-)| See Figure 12
Differential Input Common Mode Range	V_{CM}	0.8	2.5	V	Includes V_{DI}, See Figure 12
Single Ended Receiver Threshold	V_{SE}	0.8	2.0	V	
Transceiver Input Capacitance	C_{IN}		12	pF	D+ to V_{BUS}, D- to V_{BUS}

USB Timing Specifications

Timing Specifications over recommended operating conditions.

Parameter	Symbol	Minimum	Maximum	Units	Notes
D+/D- Transition rise time	T_{LR}	75		ns	C_L = 200 pF (10% to 90%), see Figure 10
D+/D- Transition rise time	T_{LR}		300	ns	C_L = 600 pF (10% to 90%), see Figure 10
D+/D- Transition fall time	T_{LF}	75		ns	C_L = 200 pF (90% to 10%), see Figure 10
D+/D- Transition fall time	T_{LF}		300	ns	C_L = 600 pF (90% to 10%), see Figure 10
Rise and Fall time matching	T_{LRFM}	80	125	%	T_R/T_F; C_L = 200 pF; Excluding the first transition from the Idle State
Wakeup delay from USB suspend mode due to buttons push	T_{WUPB}		17	ms	Delay from button push to USB operation Only required if remote wakeup enabled
Wakeup delay from USB suspend mode due to buttons push until accurate navigation	T_{WUPN}		50	ms	Delay from button push to navigation operation Only required if remote wakeup enabled
USB reset time	T_{reset}	18.7		µs	
Data Rate	t_{LDRATE}	1.4775	1.5225	Mb/s	Average bit rate, 1.5 Mb/s +/- 1.5%
Receiver Jitter Tolerance	t_{DJR1}	-75	75	ns	To next transition, see Figure 13
Receiver Jitter Tolerance	t_{DJR2}	-45	45	ns	For paired transitions, see Figure 13
Differential to EOP Transition Skew	t_{LDEOP}	-40	100	ns	See Figure 14
EOP Width at Receiver	t_{LEOPR}	670		ns	Accepts EOP, see Figure 14
Source EOP Width	t_{LEOPT}	1.25	1.50	µs	
Width of SE0 interval during Differential Transition	t_{LST}		210	ns	See Figure 11.
Differential Output Jitter	t_{UDJ1}	-95	95	ns	To next transition, see Figure 15
Differential Output Jitter	t_{UDJ2}	-150	150	ns	For paired transitions, see Figure 15

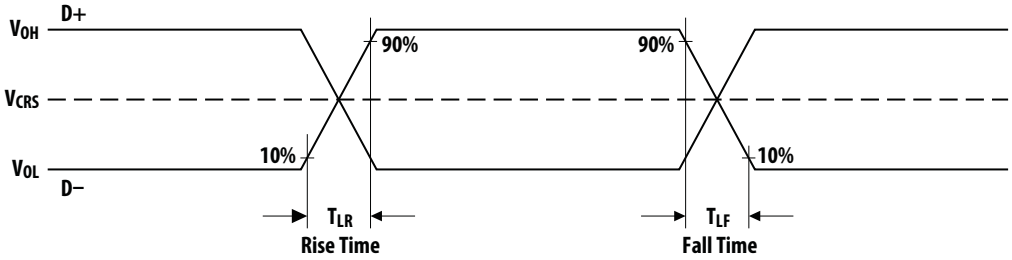


Figure 10. Data Signal Rise and Fall Times

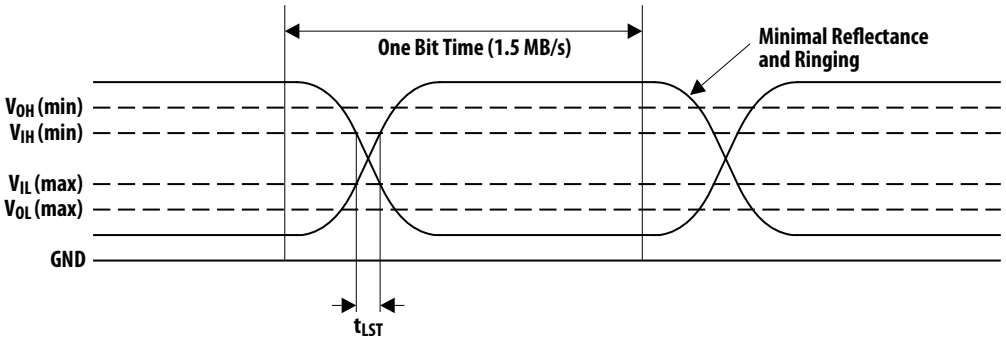


Figure 11. Data Signal Voltage Levels

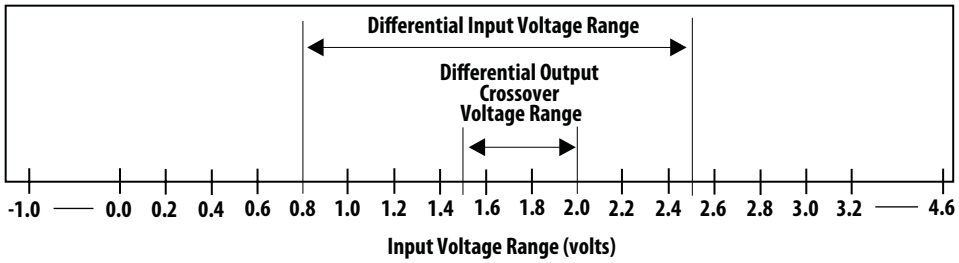


Figure 12. Differential Receiver Input Sensitivity vs. Common Mode Input Range

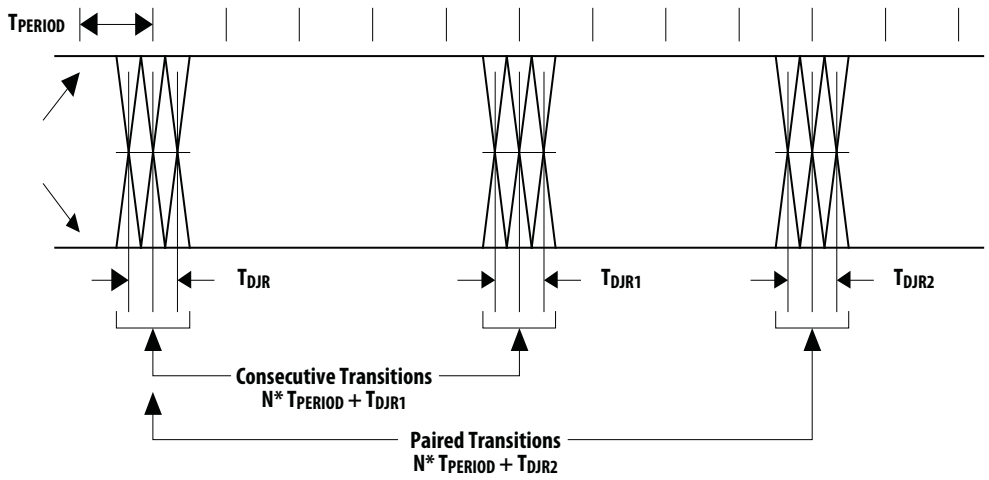


Figure 13. Receiver Jitter Tolerance

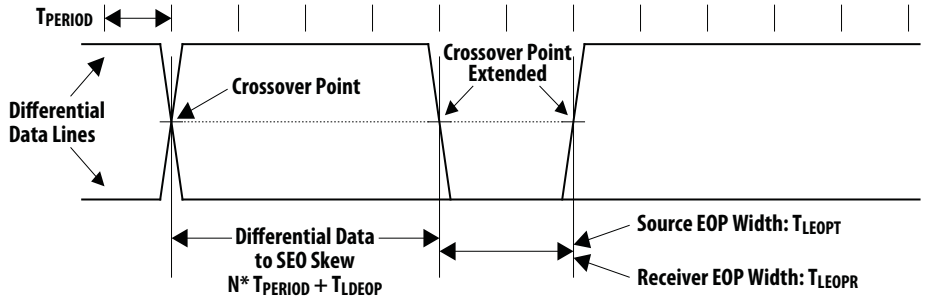


Figure 14. Differential to EOP Transition Skew and EOP Width

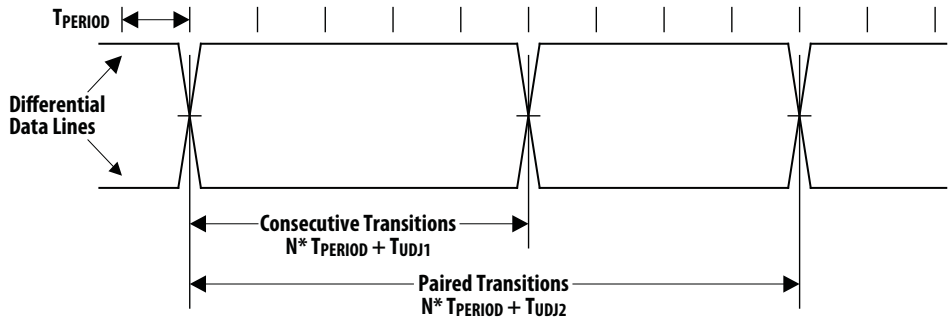


Figure 15. Differential Output Jitter

One-Time-Programmable (OTP) Memory

The on chip OTP memory allows device configuration flexibility to override the default setting of ADNS-7700 sensors without any external software driver. Once the OTP operation is enabled, all OTP registers must be programmed accordingly as the default values of un-program OTP registers are always zero when L2_USE_OTP register setting is not zero value. Tips: OTP write to the OTP register can be skipped if the setting is zero value (0x00) in order to save the OTP programming time.

OTP address space is from 0x80 to 0xFE. OTP can be programmed via USB interface using Set Vendor Test and Get Vendor Test commands.

OTP Byte Write Operation

OTP write operation flow chart is shown in Figure 16.

1. Set OTP enable bit in OTP_CONFIG register, 0x4C: OTP_EN = 1.
2. Write the OTP register address byte to OTP_ADDR register, 0x4D.
3. Write the OTP data byte to OTP_DATA register, 0x4E.
4. Set write enable bit in OTP_CTRL register, 0x4F to enable write command to OTP: WR = 1.
5. Read the write enable bit status in OTP_CTRL register, 0x4F. If WR = 1, repeat reading the bit status until it is clear.
6. Read the write status bit in OTP_CTRLSTAT register, 0x50.
   a. If WR_OK = 1, OTP write operation is completed. Repeat Step 2 for more OTP byte write operations.
   b. If WR_OK = 0, repeat Step 4.
7. If Step 6b is repeated up to 10 times, OTP write operation is failed and the chip is confirmed as defective unit.

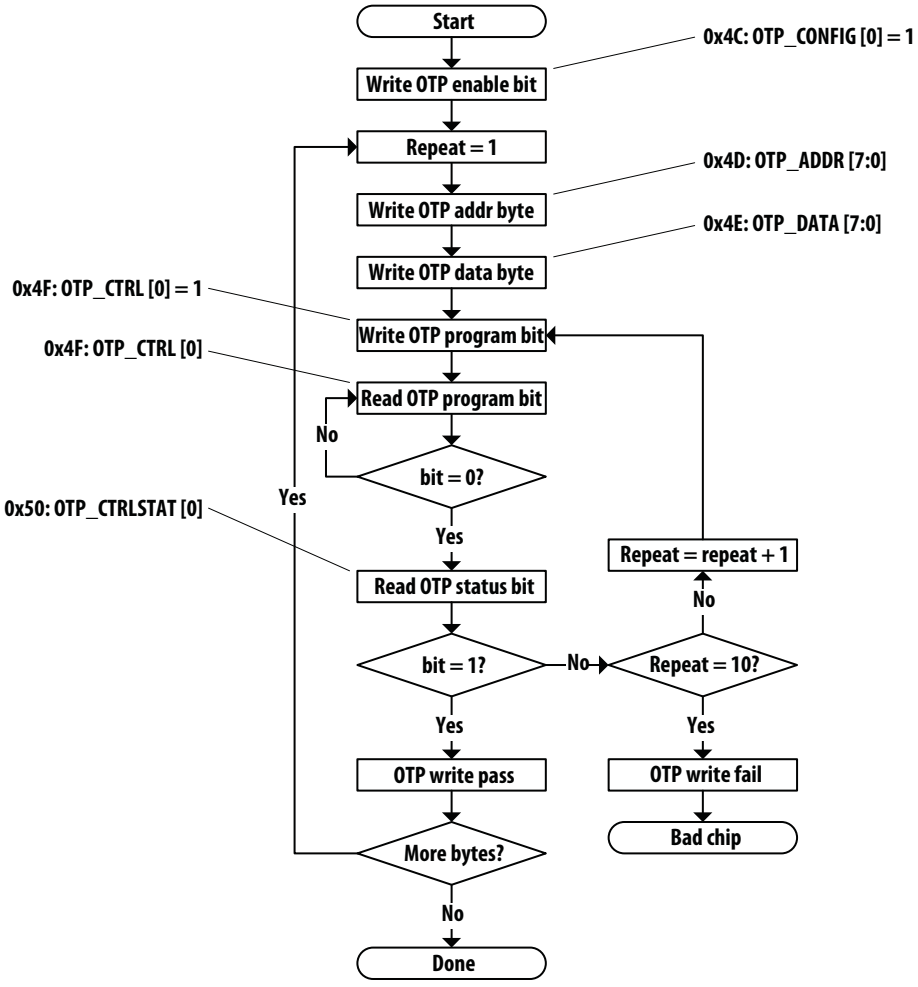


Figure 16. OTP Byte Write Flow Chart

OTP Byte Read Operation

OTP read operation flow chart is shown in Figure 17.

1. Set OTP enable bit in OTP_CONFIG register, 0x4C: OTP_EN = 1.
2. Write the OTP register address byte to OTP_ADDR register, 0x4D.
3. Set read enable bit in OTP_CTRL register, 0x4F to enable write command to OTP: RD = 1.
4. Read the read enable bit status in OTP_CTRL register, 0x4F. If RD = 1, repeat reading the bit status until it is clear.
5. Read the OTP data byte from OTP_DATA register, 0x4E to complete the OTP read operation.
6. Repeat Step 2 for more OTP read operations.

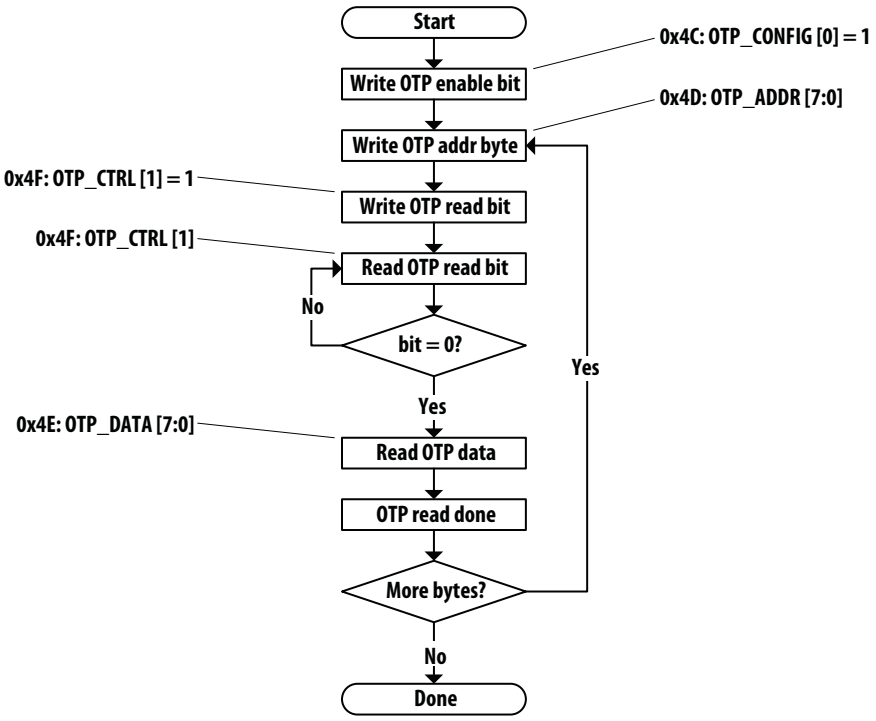


Figure 17. OTP Byte Read Flow Chart

OTP Lock Operation

OTP lock operation MUST be performed once OTP write to OTPLOCK2 register for the sensor to function. DO not reset or power up the chip right after OTP write to OTPLOCK2 register, otherwise the chip will be malfunction. The OTP lock operation flow chart is shown in Figure 18.

1. After OTP write to OTPLOCK2 register, set OTP enable bit in OTP_CONFIG register, 0x4C: OTP_EN = 1.
2. Set OTP lock bit in OTP_CTRL register, 0x4F to enable OTP lock command: LOCK_L2 = 1.
3. Read the OTP lock bit status in OTP_CTRL register, 0x4F. If LOCK_L2 = 1, repeat reading the bit status until it is clear.
4. Read the lock status and CRC bits in OTP_CTRLSTAT register, 0x50.
   a. If both L2_LOCK_OK and L2_CRC_OK = 1, OTP lock operation is completed.
   b. If either L2_LOCK_OK or L2_CRC_OK = 0, repeat Step 2 until both bits are set.
5. If Step 4b is repeated up to 10 times, OTP lock operation is failed and the chip is confirmed as defective unit.

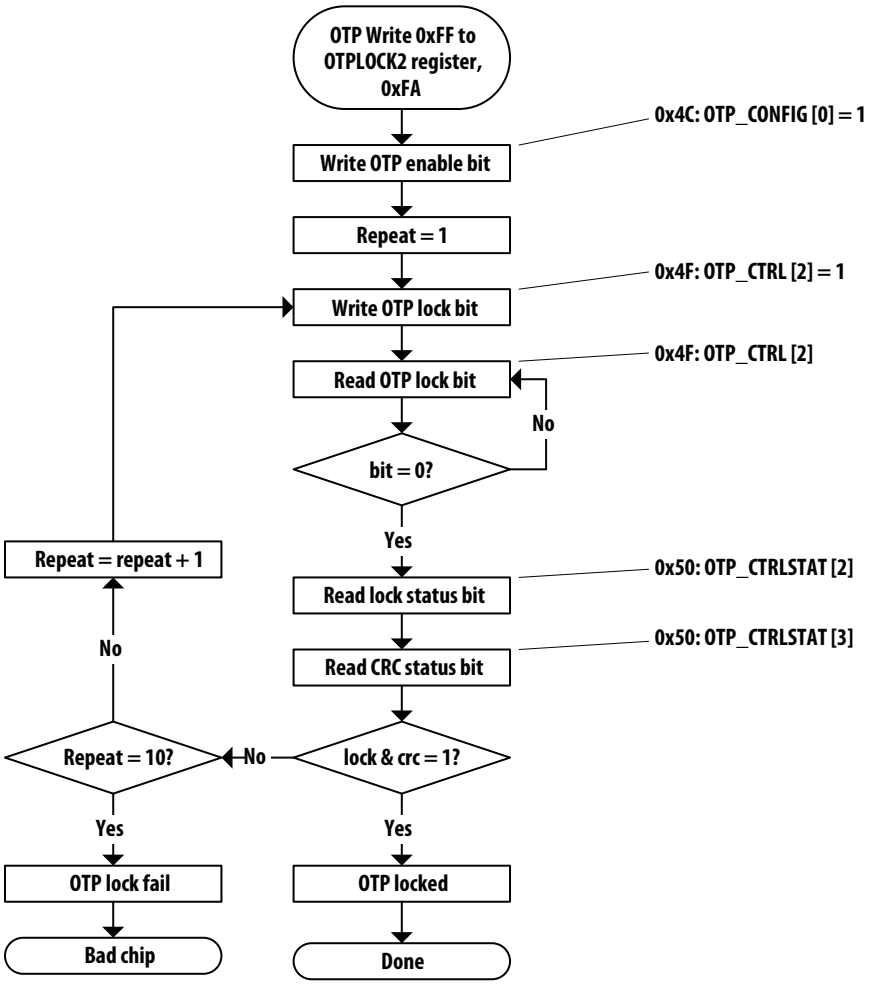


Figure 18. OTP Byte Lock Flow Chart

Buttons and Tilt Wheel

The minimum time between button presses is T_{DBB}. Buttons, B1 through B5 and Tilt Wheel are connected to a Schmidt trigger input with 100µA current sources pulling up to +5.0V during run, rest and USB suspend modes.

The tilt wheel feature can be enabled or disabled via OTP register. ***All designers and manufacturers of final product with tilt wheel enabled must assure that they have all necessary intellectual property rights.***

Debounce Algorithm

- Button inputs B1, B2, B3, B4, B5, TW1 and TW2 are sampled every 2ms.
- Three consecutive low values create a button press event.
- Three consecutive high values create a button release event.

Z-Wheel

ADNS-7700 is designed to be used with mechanical Z-Wheel for vertical scrolling. The Z-Wheel reporting format which determines the vertical scroll resolution is Z/2 as most of the commonly available mechanical Z-Wheel encoders come with lower sensitivity.

On-the-Fly (OTF) Resolution Mode

The ADNS-7700-HAMY, ADNS-7700-HCMY and ADNS-7700-HMMY sensors are enhanced with programmable On-the-Fly (OTF) resolution mode, which user is able to switch resolution setting anytime with OTF button click. OTF mode can be activated from OTP register 0xC1 by writing either 01 or 10 to OTF [1:0]. When OTF [1:0] = 00 or 11, the resolution setting is fixed as per CPI_SET0 register configuration. Refer to Table 4 on the configurable options.

Every OTF button click triggers the change of resolution setting from current state to next state. The OTF state machine as shown in Figure 19 implements in the sequence of S0: CPI_SET0, S1: CPI_SET1 and S2: CPI_SET2 in a cycle. The default state upon ADNS-7700 sensor power up is always at S0.

For ADNS-7700-HAMY sensor, the OTF state can be displayed with LED indication via LED0, LED1 and LED2 pins. LED0, LED1 and LED2 are active high output and can be connected to the base of a NPN bi-polar junction transistor (BJT) which when ON connects VDD to the LED.

The button click for OTF mode in ADNS-7700-HMMY requires long press. The long press timing is configurable via LONGPRESS register, 0xC6 with default timing of 0.256s.

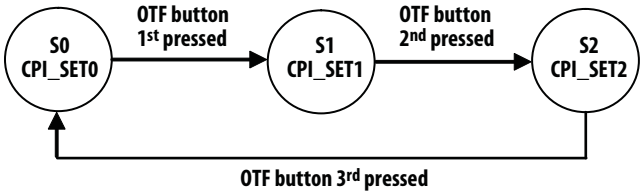


Figure 19. OTF Resolution Mode State Machine

Table 3. OTF LED Indication Status for ADNS-7700-HAMY

State Sequence		Current State Status		
Previous	**Current**	**LED0**	**LED1**	**LED2**
S2	S0	High	Low	Low
S0	S1	Low	High	Low
S1	S2	Low	Low	High

KeyMap (KM)

KeyMap mode enables B4, B5, TW1 or TW2 button to be assigned as keyboard shortcut key. Thus, the sensor can be customized to implement standard Microsoft keyboard shortcut keys or special shortcut keys used in different applications, eg. Office, CAD, PC Games, etc. Table 3 shows the configuration of KM1 and KM2 pins in KeyMap mode. KM [1:0] bits in DEVCONFIG register, 0xC1 must complement to each other in order to enable KeyMap modes.

KM1 will be implemented as per CodeA setting while KM2 will be implemented as per CodeB setting. CodeA and Code B allow configuration of two and above keys combination (eg. Alt+Tab, Alt+Ctrl+Del).

CodeA = CODEA_KEY1 register, 0xC2 + CODEA_KEY2 register, 0xC4

CodeB = CODEB_KEY1 register, 0xC3 + CODEB_KEY2 register, 0xC5

CODEA_KEY1 and CODEB_KEY1 registers consist of 8 predefined keyboard keys: Microsoft Logo GUI, Alt, Shift and Ctrl keys located at left and right sides. CODEA_KEY2 and CODEB_KEY2 registers can be programmed with a keyboard key scan code available from Windows Platform Design Notes on Keyboard Scan Code Specification, which can be downloaded from:

http://www.microsoft.com/whdc/archive/scancode.mspx

Table 4. Resolution and KeyMap Mode OTP Configurations

Part Number	Configuration Options	REG 0xC7	REG 0xC1	REG 0xC1	Pinout Configurations						
		TW_NEN	OTF1-0	KM1-0	B1	B2	B3	B4	B5	TW1	TW2
ADNS-7700-H4MY	3B	1	00	00	Left	Right	Middle	NA	NA	NA	NA
	3B + TW (Default)	**0**	**00**	**00**	**Left**	**Right**	**Middle**	**NA**	**NA**	**Tilt left**	**Tilt right**
ADNS-7700-HAMY	3B	1	00	00	Left	Right	Middle	NA	NA	NA	NA
	3B + TW (Default)	**0**	**00**	**00**	**Left**	**Right**	**Middle**	**NA**	**NA**	**Tilt left**	**Tilt right**
	3B + TW + OTF	0	01	00	Left	Right	Middle	NA	OTF	Tilt left	Tilt right
	3B + OTF + 3LED	1	01	00	Left	Right	Middle	LED2	OTF	LED1	LED0
ADNS-7700-HCMY	5B	1	00	00	Left	Right	Middle	Back	Forward	NA	NA
	5B + TW (Default)	**0**	**00**	**00**	**Left**	**Right**	**Middle**	**Back**	**Forward**	**Tilt left**	**Tilt right**
	5B + OTF	1	01	00	Left	Right	Middle	Back	Forward	NA	OTF
	4B + TW + OTF	0	01	00	Left	Right	Middle	Back	OTF	Tilt left	Tilt right
ADNS-7700-HMMY	5B	1	00	00	Left	Right	Middle	Back	Forward	NC	NC
	5B + TW (Default)	**0**	**00**	**00**	**Left**	**Right**	**Middle**	**Back**	**Forward**	**Tilt left**	**Tilt right**
	5B + KM1/OTF_L	1	01	01	Left	Right	Middle	Back	Forward	NC	KM1/ OTF_L
	5B + KM1/OTF_L + KM2	1	01	10	Left	Right	Middle	Back	Forward	KM2	KM1/ OTF_L
	4B + TW + KM1/ OTF_L	0	01	01	Left	Right	Middle	Back	KM1/ OTF_L	Tilt left	Tilt right
	3B + TW + KM1/ OTF_L	0	10	01	Left	Right	Middle	NC	KM1/ OTF_L	Tilt left	Tilt right
	3B + TW + KM1/ OTF_L + KM2	0	10	10	Left	Right	Middle	KM2	KM1/ OTF_L	Tilt left	Tilt right

Configuration after Power Up (Data Values)

Signal Function	State from Figure 9-1 of USB spec: Powered or Default Address or Configured	State from Figure 9-1 of USB spec: Suspended from any other states
B1	Pullup active for button use	Pullup active for button use
B2	Pullup active for button use	Pullup active for button use
B3	Pullup active for button use	Pullup active for button use
B4	Pullup active for button use	Pullup active for button use
B5	Pullup active for button use	Pullup active for button use
TW1	Pullup active for button use	Pullup active for button use
TW2	Pullup active for button use	Pullup active for button use
D+	USB I/O	Hi-Z input
D-	USB I/O	Hi-Z input
OSC_IN	24MHz	Drive Logic '1'
OSC_OUT	24MHz	Drive Logic '1'
-VCSEL	Pulsing	Pulled high (off)
ZA	Hi-Z input	Hi-Z input
ZB	Hi-Z input	Hi-Z input

Typical Performance Characteristics

The following graphs are the typical performance of the ADNS-7700 sensor, assembled as shown in the 2D assembly drawing with the ADNS-6180-001 or ADNS-6180-002 lens.

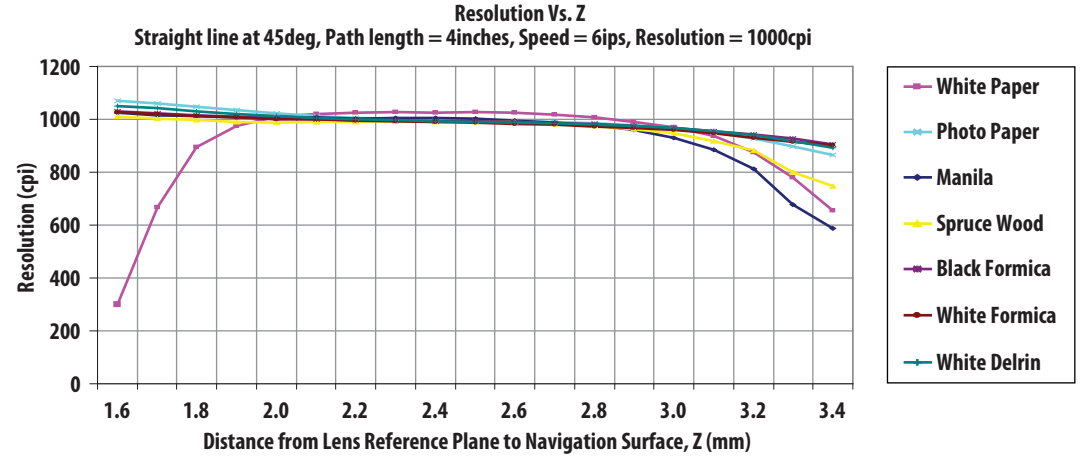


Figure 20. Mean Resolution vs. Z

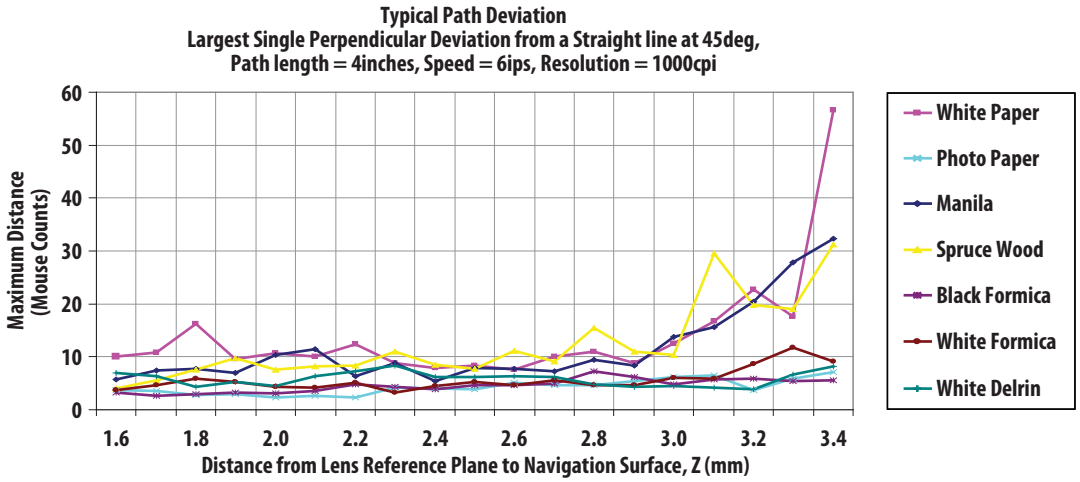


Figure 21. Average Error vs. Z

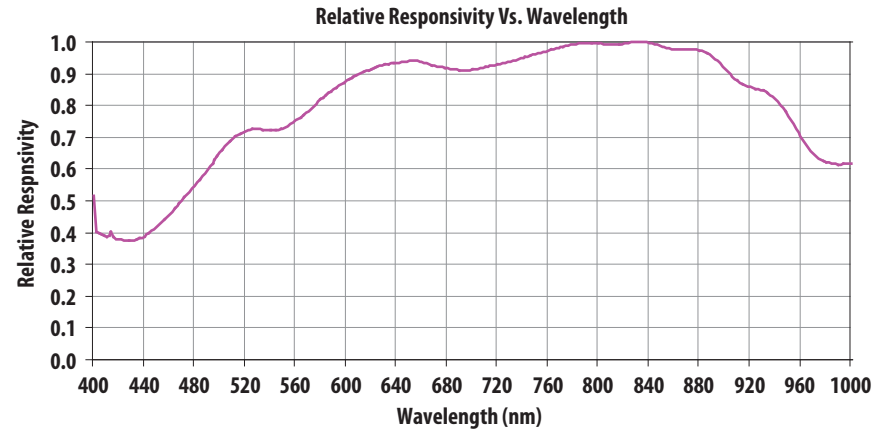


Figure 22. Wavelength Responsivity

USB Commands

Mnemonic	Command	Notes
USB_RESET	D+/D- low > 18.7us	Device Resets; Address = 0
USB_SUSPEND	Idle state > 3mS	Device enters USB low-power mode
USB_RESUME	Non-idle state	Device exits USB low-power mode
Get_Status_Device	80 00 00 00 00 00 02 00	Normally returns 00 00, Self powered 00 00, Remote wakeup 02 00
Get_Status_Interface	81 00 00 00 00 00 02 00	Normally returns 00 00
Get_Status_Endpt0	82 00 00 00 xx 00 02 00	OUT: xx = 00, IN: xx = 80 Normally returns 00 00
Get_Status_Endpt1	82 00 00 00 81 00 02 00	Normally returns 00 00, Halt 00 01
Get_Configuration	80 08 00 00 00 00 01 00	Return: 00 = not config., 01 = configured
Get_Interface	81 0A 00 00 00 00 01 00	Normally returns 00
Get_Protocol	A1 03 00 00 00 00 01 00	Normally returns 01, Boot protocol 00
Get_Desc_Device	80 06 00 01 00 00 nn 00	See USB Command Details Application Note
Get_Desc_Config	80 06 00 02 00 00 nn 00	See USB Command Details Application Note
Get_Desc_String	80 06 xx 03 00 00 nn 00	See USB Command Details Application Note
Get_Desc_HID	81 06 00 21 00 00 09 00	See USB Command Details Application Note
Get_Desc_HID_Report	81 06 00 22 00 00 nn 00	See USB Command Details Application Note
Get_HID_Input	A1 01 00 01 00 00 nn 00	Return depends on motion & config
Get_Idle	A1 02 00 00 00 00 01 00	Returns rate in multiples of 4ms
Get_Vendor_Test	C0 01 00 00 xx 00 01 00	xx = address of register to read
Set_Address	00 05 xx 00 00 00 00 00	xx = address
Set_Configuration	00 09 xx 00 00 00 00 00	Not configured: xx = 00 Configured: xx = 01
Set_Interface	01 0B 00 00 00 00 00 00	Only one interface supported
Set_Protocol	21 0B xx 00 00 00 00 00	Boot: xx=00, Report: xx=01
Set_Feature_Device	00 03 01 00 00 00 00 00	Enable remote wakeup
Set_Feature_Endpt0	02 03 00 00 xx 00 00 00	Halt. OUT: xx = 00, IN: xx = 80
Set_Feature_Endpt1	02 03 00 00 81 00 00 00	Halt
Clear_Feature_Device	00 01 01 00 00 00 00 00	Disable Remote wakeup
Clear_Feature_Endpt0	02 01 00 00 xx 00 00 00	Clear Halt; OUT: xx = 00, IN: xx = 80
Clear_Feature_Endpt1	02 01 00 00 81 00 00 00	Clear Halt
Set_Idle	21 0A 00 rr 00 00 00 00	rr = report rate in multiples of 4ms
Set_Vendor_Test	40 01 00 00 xx yy 00 00	Write yy to address xx
Poll_Endpt1		Read buttons, motion, & Z-wheel

Note: The last two bytes in a command shown as "nn 00" specify the 16-bit data size in the order of "LowByte HighByte." For example a two-byte data size would be specified as "02 00." ADNS-7700 will not provide more bytes than the number requested in the command, but it will only supply up to a maximum of 8bytes at a time. The ADNS-7700 will re-send the last packet if the transfer is not acknowledged properly.

USB Data Packet Format

Sensor		ADNS-7700-H4MY, ADNS-7700-HAMY						
Configuration		3B, 3B+OTF+3LED						
Button		3						
Motion Format		8-Bit						
Z-Wheel		Mechanical						
Tilt-Wheel		Disabled						
OTF		Disabled/ Enabled						
KM		Disabled/						
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Byte 1	0	0	0	0	0	MB	RB	LB
Byte 2	X[7]	X[6]	X[5]	X[4]	X[3]	X[2]	X[1]	X[0]
Byte 3	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]
Byte 4	Z[7]	Z[6]	Z[5]	Z[4]	Z[3]	Z[2]	Z[1]	Z[0]

Sensor		ADNS-7700-H4MY, ADNS-7700-HAMY						
Configuration		3B+TW, 3B+TW+OTF						
Button		3						
Motion Format		8-Bit						
Z-Wheel		Mechanical						
Tilt-Wheel		Enabled						
OTF		Disabled/ Enabled						
KM		Disabled						
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Byte 1	0	0	0	0	0	MB	RB	LB
Byte 2	X[7]	X[6]	X[5]	X[4]	X[3]	X[2]	X[1]	X[0]
Byte 3	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]
Byte 4	Z[7]	Z[6]	Z[5]	Z[4]	Z[3]	Z[2]	Z[1]	Z[0]
Byte 5	TW[7]	TW[6]	TW[5]	TW[4]	TW[3]	TW[2]	TW[1]	TW[0]

Sensor		ADNS-7700-HCMY, ADNS-7700-HMMY						
Configuration		5B, 5B+OTF						
Button		5						
Motion Format		8-Bit						
Z-Wheel		Mechanical						
Tilt-Wheel		Disabled						
OTF		Disabled/Enabled						
KM		Disabled						
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Byte 1	0	0	0	FB	BB	MB	RB	LB
Byte 2	X[7]	X[6]	X[5]	X[4]	X[3]	X[2]	X[1]	X[0]
Byte 3	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]
Byte 4	Z[7]	Z[6]	Z[5]	Z[4]	Z[3]	Z[2]	Z[1]	Z[0]

Sensor		ADNS-7700-HCMY						
Configuration		5B+TW						
Button		5						
Motion Format		8-Bit						
Z-Wheel		Mechanical						
Tilt-Wheel		Enabled						
OTF		Disabled						
KM		Disabled						
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Byte 1	0	0	0	FB	BB	MB	RB	LB
Byte 2	X[7]	X[6]	X[5]	X[4]	X[3]	X[2]	X[1]	X[0]
Byte 3	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]
Byte 4	Z[7]	Z[6]	Z[5]	Z[4]	Z[3]	Z[2]	Z[1]	Z[0]
Byte 5	TW[7]	TW[6]	TW[5]	TW[4]	TW[3]	TW[2]	TW[1]	TW[0]