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Digital Controller for Isolated Power Supply Applications

ADP1043A

FEATURES

- **Integrates all typical controller functions**
  - **Digital control loop**
  - **Remote and local voltage sense**
  - **Primary and secondary side current sense**
  - **PWM control**
  - **Synchronous rectifier control**
  - **Current sharing**
  - **Integrated programmable loop filter**
- **I²C interface**
- **Extensive fault detection and protection**
- **Extensive programming**
- **Fast calibration**
- **EEPROM**
- **Standalone or microcontroller control**

APPLICATIONS

- **AC-to-DC power supplies**
- **Isolated dc-to-dc power supplies**
- **Redundant power supplies**
- **Parallel power supplies**
- **Server, storage, network, and communications infrastructure**

GENERAL DESCRIPTION

The ADP1043A is a secondary side power supply controller IC designed to provide all the functions that are typically needed in an ac-to-dc or isolated dc-to-dc control application.

The ADP1043A is optimized for minimal component count, maximum flexibility, and minimum design time. Features include remote voltage sense, local voltage sense, primary and secondary side current sense, pulse-width modulation (PWM) generation, and hot-swap sense and control. The control loop is digital with an integrated programmable digital filter. Protection features include current limiting, ac sense, undervoltage lockout (UVLO), and overvoltage protection (OVP).

The built-in EEPROM provides extensive programming of the integrated loop filter, PWM signal timing, inrush current, and soft start timing and sequencing. Reliability is improved through a built-in checksum and redundancy of critical circuits.

A comprehensive GUI is provided for easy design of loop filter characteristics and programming of the safety features. The industry-standard I²C bus provides access to the many monitoring and system test functions.

The ADP1043A is available in a 32-lead LFCSP and operates from a single 3.3 V supply.

TYPICAL APPLICATION CIRCUIT

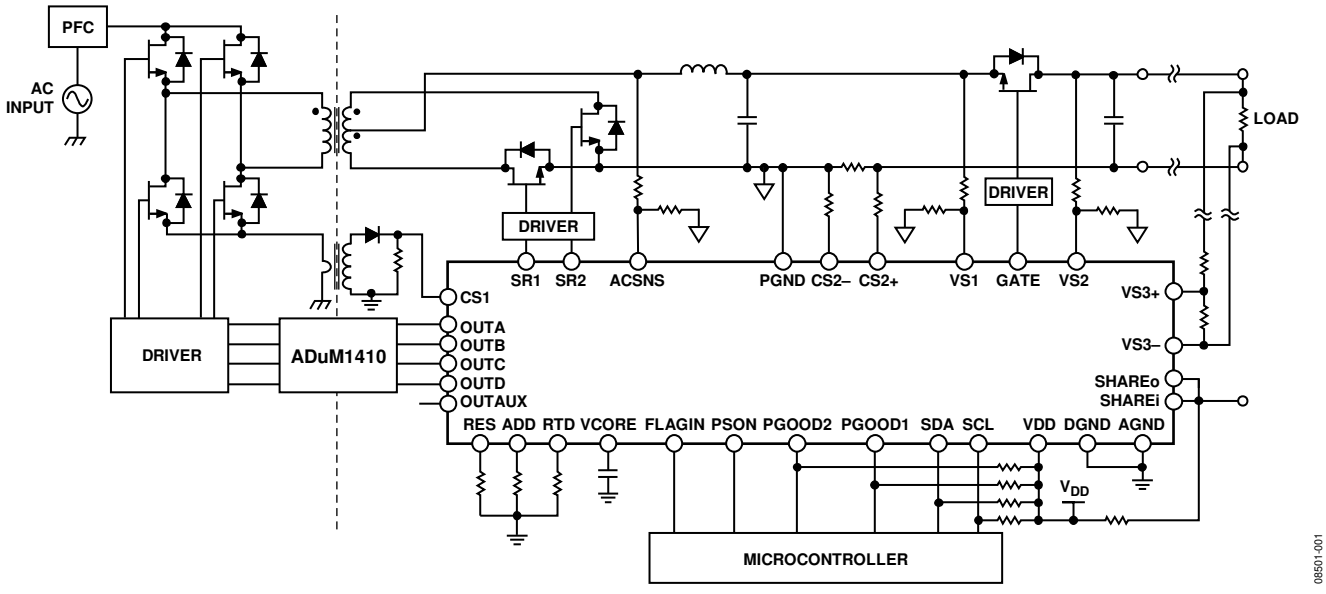

Figure 1.

Rev. 0

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- ADP1043A 100W Full-Bridge Evaluation Board
- USB to I2C Interface Connector

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Data Sheet

- ADP1043A: Digital Controller for Isolated Power Supply Applications

User Guides

- ADP1043A GUI Reference Guide VB.NET

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADP1043A Software

DESIGN RESOURCES

- ADP1043A Material Declaration
- PCN-PDN Information
- Quality And Reliability
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TABLE OF CONTENTS

REVISION HISTORY

10/09—Revision 0: Initial Version

The ADP1043A is a secondary side controller for switch mode power supplies (SMPS). It is designed for use in isolated redundant applications. The ADP1043A integrates the typical functions that are needed to control a power supply. These include

- Output voltage sense and feedback
- Digital loop filter compensation
- PWM generation
- Current sharing
- Current, voltage, and temperature sense
- OrFET control
- Housekeeping and I²C interface
- Calibration and trimming

The main function of controlling the output voltage is performed using the feedback ADCs, the digital loop filter, and the PWM block. The feedback ADCs use a multipath approach (patent pending). The ADP1043A combines a high speed, low resolution (fast and coarse) ADC and a low speed, high resolution (slow and accurate) ADC. Loop compensation is implemented using the digital filter. This PID (proportional, integral, derivative) filter is implemented in the digital domain to allow easy programming of filter characteristics, which is of great value in customizing and debugging designs.

The PWM block generates up to seven programmable PWM outputs for control of FET drivers and synchronous rectification FET drivers. This programmability allows many traditional and unique switching topologies to be realized.

A current share bus interface provides for parallel power supplies. The part also has hot-swap OrFET sense and control for N + 1 redundant power supplies.

Conventional power supply housekeeping features, such as remote and local voltage sense and primary and secondary side current sense, are included. An extensive set of protections is offered, including overvoltage protection (OVP), overcurrent protection (OCP), overtemperature protection (OTP), undervoltage protection (UVP), ground continuity monitoring, and ac sense.

All these features are programmable through the I²C bus interface. This bus interface is also used to calibrate the power supply. Other information, such as input current, output current, and fault flags, is also available through the I²C bus interface.

The internal EEPROM can store all programmed values and allows standalone control without a microcontroller. A free, downloadable GUI is available that provides all the necessary software to program the ADP1043A. For more information about the GUI, contact Analog Devices, Inc., for the latest software and a user guide.

The ADP1043A operates from a single 3.3 V supply and is specified from −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

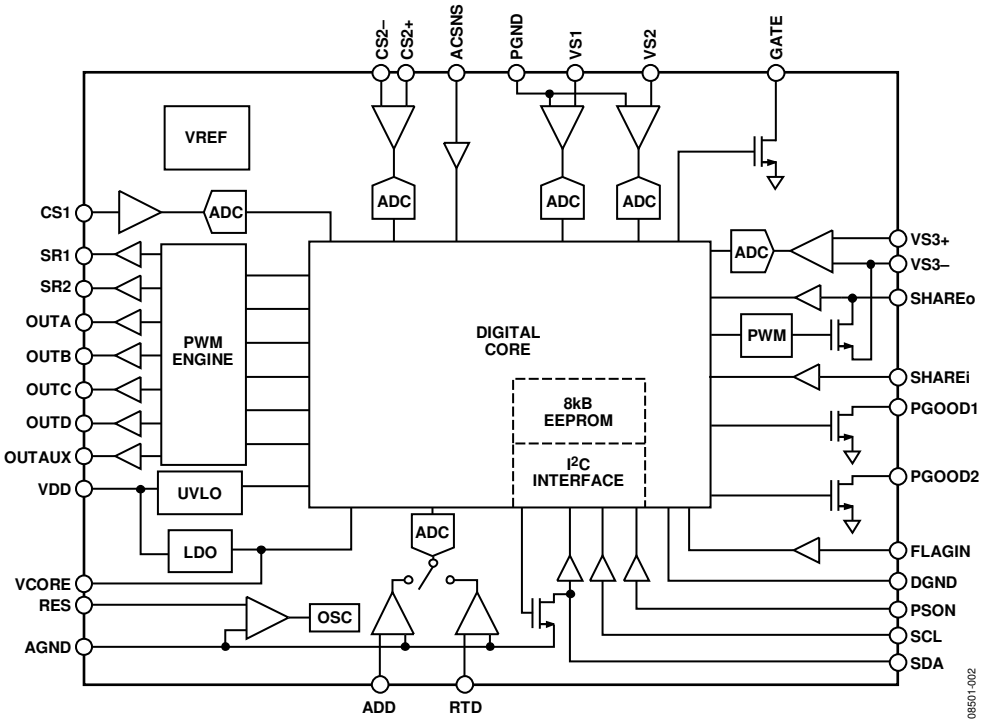

Figure 2.

SPECIFICATIONS

V_{DD} = 3.3 V, T_A = −40°C to +85°C, unless otherwise noted. FSR = full-scale range.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
V_{DD}	V_{DD}		3.1	3.3	3.6	V
I_{DD}	I_{DD}	Normal operation (PSON is high)		20		mA
		Power supply off (PSON is low)		15		mA
		During EEPROM programming (40 ms)		I_{DD} + 8		mA
POWER-ON RESET						
Power-On Reset		V_{DD} rising	3.05			V
UVLO		V_{DD} falling	2.75	2.85	2.95	V
UVLO Hysteresis				35		mV
OVLO			3.7	3.9	4.1	V
VCORE PIN						
Output Voltage		T_A = 25°C	2.3	2.5	2.7	V
OSCILLATOR AND PLL						
PLL Frequency		RES = 49.9 kΩ	190	200	210	MHz
OUTA, OUTB, OUTC, OUTD, OUTAUX, SR1, SR2 PINS						
Output Low Voltage	V_{OL}	Source current = 10 mA			0.4	V
Output High Voltage	V_{OH}	Source current = 10 mA	V_{DD} − 0.4			V
Rise Time		C_{LOAD} = 50 pF		3.5		ns
Fall Time		C_{LOAD} = 50 pF		1.5		ns
AC SENSE		PWM and resonant mode				
Input Voltage Threshold			0.3	0.45	0.65	V
Propagation Delay		From ACSNS threshold to SR start; resonant mode only		160		ns
VS1, VS2, VS3 LOW SPEED ADC						
Input Voltage Range	V_{IN}	Differential voltage from VS1, VS2 to PGND, and from VS3+ to VS3−	0	1	1.55	V
Sampling Frequency	f_{SAMP}			100		Hz
Voltage Sense Measurement Accuracy		From 0% to 100% of input voltage range	−10		+10	% FSR
			−155		+155	mV
		From 10% to 90% of input voltage range	−2.5		+2.5	% FSR
			−38.75		+38.75	mV
		From 900 mV to 1.1 V	−1.5		+1.5	% FSR
			−23.25		+23.25	mV
Voltage Sense Measurement Resolution				12		Bits
Voltage Differential from VS3− to PGND			−200		+200	mV
VS1 OVP Comparator Speed		Register 0x2C[2] = 0		300		µs
VS1 OVP Threshold Accuracy		Relative to nominal voltage (1 V) on VS1		2.5		%
VS2 and VS3 OVP Comparator Speed		Register 0x2C[2] = 0		300		µs
VS2 and VS3 OVP Threshold Accuracy		Relative to nominal voltage (1 V) on VS2 and VS3		2.5		%
VS1 HIGH SPEED ADC						
Sampling Frequency	f_{SAMP}			400		kHz
Resolution				6		Bits
Dynamic Range				±18		mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENT SENSE 1 (CS1 PIN)						
Input Voltage Range	V_{IN}		0	1	1.38	V
Sampling Frequency	f_{SAMP}			100		Hz
Current Sense Measurement Accuracy		From 10% to 90% of input voltage range	−3.0		+3.0	% FSR
			−41.4		+41.4	mV
		From 0% to 100% of input voltage range	−10		+10	% FSR
			−138		+138	mV
Current Sense Measurement Resolution				12		Bits
CS1 Fast OCP Threshold			1.1	1.2	1.3	V
CS1 Fast OCP Speed				80	100	ns
CS1 Accurate OCP DC Accuracy		From 10% to 90% of input voltage range	−3.0		+3.0	% FSR
			−41.4		+41.4	mV
CS1 Accurate OCP Speed				10		ms
Leakage Current				4.0		µA
CURRENT SENSE 2 (CS2+, CS2− PINS)						
Input Voltage Range	V_{IN}	Differential voltage from CS2+ to CS2−	−100		+225	mV
ADC Input Voltage Range		LSB = 61.04 µV	0		225	mV
Sampling Frequency	f_{SAMP}			100		Hz
Current Sense Measurement Accuracy		From 0 mV to 200 mV	−4		+4	mV
		From 200 mV to 225 mV	−15		+15	mV
			−7.5		+7.5	% FSR
Current Sense Measurement Resolution				12		Bits
CS2 Accurate OCP Accuracy		From 0 mV to 200 mV	−4		+4	mV
		From 200 mV to 225 mV	−15		+15	mV
			−7.5		+7.5	% FSR
CS2 Accurate OCP Speed				10		ms
Current Sink (High Side)				100		µA
Current Source (Low Side)				100		µA
Common-Mode Voltage at the CS2+ and CS2− Pins		To achieve CS2 measurement accuracy	0.8	1	1.3	V
GATE PIN (OPEN DRAIN)						
Output Low Voltage	V_{OL}				0.4	V
OrFET PROTECTION (CS2+, CS2−)		Low-side current sensing only				
Accurate OrFET Threshold Accuracy			−1.2	0	+1	mV
Accurate OrFET Speed				10		ms
Fast OrFET Accuracy		−25 mV setting	−40	−25	−10	mV
		−50 mV setting	−70	−50	−30	mV
		−75 mV setting	−100	−75	−50	mV
		−100 mV setting	−125	−100	−75	mV
Fast OrFET Speed		Debounce = 40 ns		110	150	ns
RTD PIN						
Input Voltage Range	V_{IN}		0	1	1.55	V
Current Source		RTD resistor = 100 kΩ	9.5	10.8	12	µA
RTD ADC Measurement Accuracy		From 2% to 20% of input voltage range	−1		+1	% FSR
		From 32 mV to 320 mV	−15.5		+15.5	mV
		From 0% to 100% of input voltage range	−10		+10	% FSR
		From 0 V to 1.55 V	−155		+155	mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OTP Threshold Accuracy		When RTD = 10 kΩ	−0.5		+0.5	% FSR
			−7.75		+7.75	mV
		When RTD = 100 kΩ	−5		+5	% FSR
			−77.5		+77.5	mV
OTP Speed				10		ms
OTP Threshold Hysteresis		When RTD = 10 kΩ		16		mV
PGOOD1, PGOOD2, SHAREo PINS (OPEN DRAIN)						
Output Low Voltage	V_{OL}				0.4	V
PSON, FLAGIN, SHAREi PINS (DIGITAL INPUTS)						
Input Low Voltage	V_{IL}				0.4	V
Input High Voltage	V_{IH}		V_{DD} − 0.8			V
SDA/SCL PINS		V_{DD} = 3.3 V				
Input Low Voltage	V_{IL}				0.4	V
Input High Voltage	V_{IH}		V_{DD} − 0.8			V
Output Low Voltage	V_{OL}				0.4	V
Leakage Current			−5		+5	µA
SERIAL BUS TIMING						
Clock Frequency				100	400	kHz
Glitch Immunity	t_{SW}				50	ns
Bus-Free Time	t_{BUF}		4.7			µs
Start Setup Time	$t_{SU;STA}$		4.7			µs
Start Hold Time	$t_{HD;STA}$		4			µs
SCL Low Time	t_{LOW}		4.7			µs
SCL High Time	t_{HIGH}		4			µs
SCL, SDA Rise Time	t_R				1000	ns
SCL, SDA Fall Time	t_F				300	ns
Data Setup Time	$t_{SU;DAT}$		250			ns
Data Hold Time	$t_{HD;DAT}$		300			ns
EEPROM RELIABILITY						
Endurance[1]			10,000			Cycles
Data Retention[2]		T_J = 85°C	20			Years

[1] Endurance is qualified as per JEDEC Standard 22, Method A117, and is measured at −40°C, +25°C, +85°C, and +125°C.
[2] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22, Method A117. Retention lifetime derates with junction temperature.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (Continuous) VDD	4.2 V
Digital Pins	−0.3 V to V_{DD} + 0.3 V
VS3− to PGND, AGND, DGND	−0.3 V to +0.3 V
RTD, VS1 to AGND	2.5 V
VS2, VS3+, ADD to AGND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS-Compliant Assemblies (20 sec to 40 sec)	260°C
ESD Charged Device Model	1.5 kV
ESD Human Body Model	3.5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP	44.4	6.4	°C/W

SOLDERING

It is important to follow the correct guidelines when laying out the PCB footprint for the ADP1043A and when soldering the part onto the PCB. The AN-772 Application Note discusses this topic in detail (see www.analog.com).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

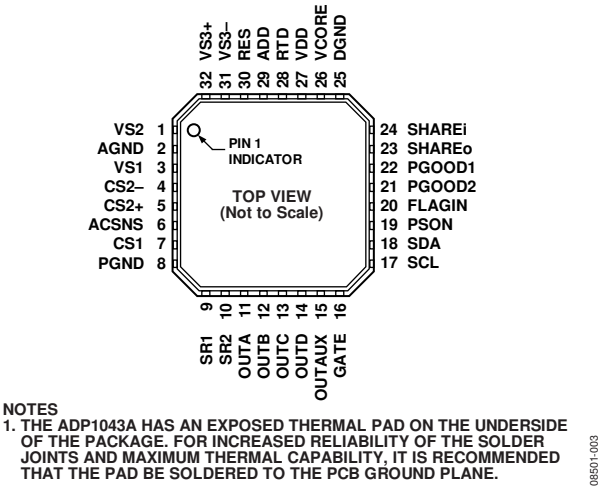

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VS2	Power Supply Output Sense Input. This signal is referred to PGND. Input to a low frequency Σ-Δ ADC. Nominal voltage at this pin should be 1 V. The resistor divider on this input must have a tolerance specification of 0.5% or better to allow for trimming.
2	AGND	Analog Ground. This pin is the ground for the analog circuitry of the ADP1043A. Star connect to DGND.
3	VS1	Local Voltage Sense Input. This signal is referred to PGND. Input to a high frequency Σ-Δ ADC. Nominal voltage at this pin should be 1 V. The resistor divider on this input must have a tolerance specification of 0.5% or better to allow for trimming.
4	CS2–	Inverting Differential Current Sense Input. Nominal voltage at this pin should be 1 V for best operation. When using high-side current sensing in a 12 V application, place a 110 kΩ resistor between the sense resistor and this pin. When using low-side current sensing, place a 10 kΩ resistor between the sense resistor and this pin. When using high-side current sensing, use the formula R = ($V_{COMMONMODE}$ − 1)/100 µA. A 0.1% resistor must be used to connect this circuit.
5	CS2+	Noninverting Differential Current Sense Input. Nominal voltage at this pin should be 1 V for best operation. When using high-side current sensing in a 12 V application, place a 110 kΩ resistor between the sense resistor and this pin. When using low-side current sensing, place a 10 kΩ resistor between the sense resistor and this pin. When using high-side current sensing, use the formula R = ($V_{COMMONMODE}$ − 1)/100 µA. A 0.1% resistor must be used to connect this circuit.
6	ACSNS	AC Sense Input. This input is connected upstream of the main inductor through a resistor divider network. The nominal voltage for this circuit is 0.45 V. This signal is referred to PGND.
7	CS1	Primary Side Current Sense Input. This pin is the current transformer input to measure and control the primary side current. This signal is referred to PGND. The resistors on this input must have a tolerance specification of 0.5% or better to allow for trimming.
8	PGND	Power Ground. This pin is the ground connection for the main power rail of the power supply. Star connect to AGND.
9	SR1	Synchronous Rectifier Output. This PWM output connects to the input of a FET driver. This pin can be disabled when not in use. This signal is referred to AGND.
10	SR2	Synchronous Rectifier Output. This PWM output connects to the input of a FET driver. This pin can be disabled when not in use. This signal is referred to AGND.
11	OUTA	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referred to AGND.
12	OUTB	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referred to AGND.
13	OUTC	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referred to AGND.
14	OUTD	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referred to AGND.
15	OUTAUX	Auxiliary PWM Output. This pin can be disabled when not in use. This signal is referred to AGND.
16	GATE	OrFET Gate Drive Output (Open Drain). This signal is referred to AGND.
17	SCL	I^2C Serial Clock Input. This signal is referred to AGND.
18	SDA	I^2C Serial Data Input and Output (Open Drain). This signal is referred to AGND.

Pin No.	Mnemonic	Description
19	PSON	Power Supply On Input. This signal is referred to DGND. This is the hardware PSON control signal. It is recommended that a 1 nF capacitor be included from the PSON pin to DGND for noise debounce and decoupling.
20	FLAGIN	Flag Input. An external signal can be input at this pin to generate a flag condition.
21	PGOOD2	Power-Good Output (Open Drain). This signal is referred to AGND. This pin is controlled by the PGOOD2 flag. This pin is set if any flag is set.
22	PGOOD1	Power-Good Output (Open Drain). This signal is referred to AGND. This pin is controlled by the PGOOD1 flag. This pin is set if any of the following are out of range: power supply, CS1 fast OCP, CS1 accurate OCP, CS2 accurate OCP, UVP, local OVP, or load OVP.
23	SHAREo	Share Bus Output Voltage Pin. Connect this pin to 3.3 V through a 2.2 kΩ resistor. When configured as a digital share bus, this pin is a digital output. This signal is referred to AGND.
24	SHAREi	Share Bus Feedback Pin. Connect this pin to the SHAREo pin. This signal is referred to AGND.
25	DGND	Digital Ground. This pin is the ground for the digital circuitry of the ADP1043A. Star connect to AGND.
26	VCORE	Output of 2.5 V Regulator. Connect a 100 nF capacitor from this pin to DGND.
27	VDD	Positive Supply Input. Range is from 3.1 V to 3.6 V. This signal is referred to AGND.
28	RTD	Thermistor Input. A 100 kΩ thermistor is placed from this pin to AGND. This signal is referred to AGND.
29	ADD	Address Select Input. Connect a resistor from ADD to AGND. This signal is referred to AGND.
30	RES	Resistor Input. This pin sets up the internal voltage reference for the ADP1043A. Connect a 49.9 kΩ resistor (±0.1%) from RES to AGND. This signal is referred to AGND.
31	VS3−	Inverting Remote Voltage Sense Input. There should be a low ohmic connection to AGND. The resistor divider on this input must have a tolerance specification of 0.5% or better to allow for trimming.
32	VS3+	Noninverting Remote Voltage Sense Input. This signal is referred to VS3−. Use 0.1% resistors as the resistor divider to connect this circuit. The resistor divider on this input must have a tolerance specification of 0.5% or better to allow for trimming.
Exposed Pad	EP	The ADP1043A has an exposed thermal pad on the underside of the package. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the PCB ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

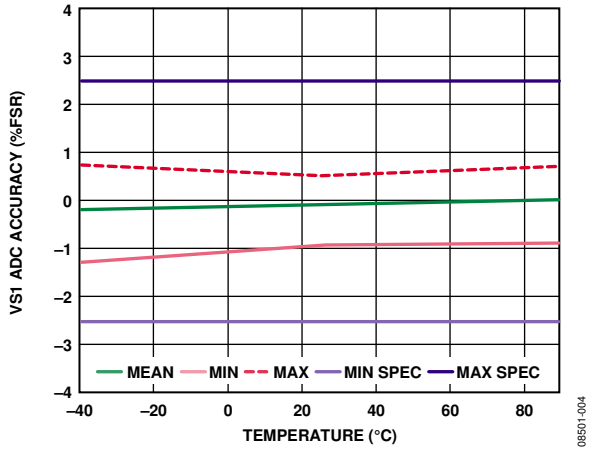

Figure 4. VS1 ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

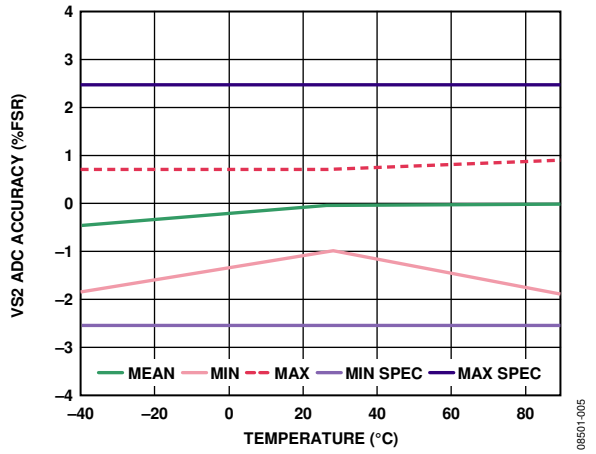

Figure 5. VS2 ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

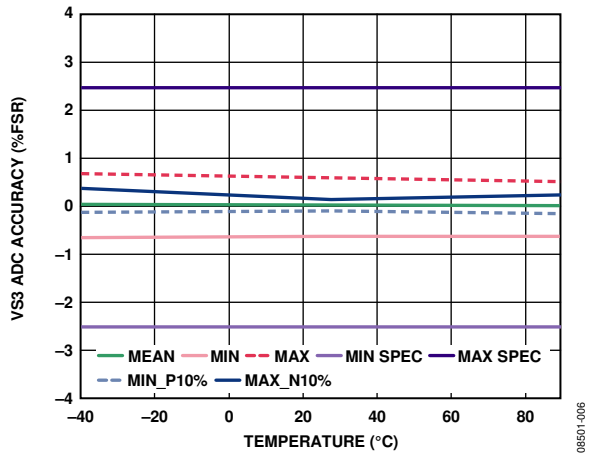

Figure 6. VS3 ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

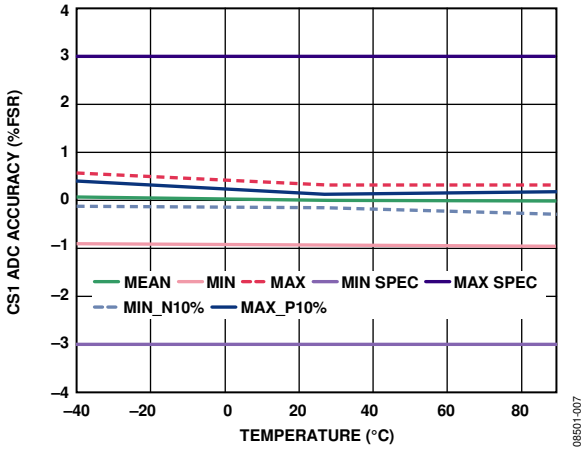

Figure 7. CS1 ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

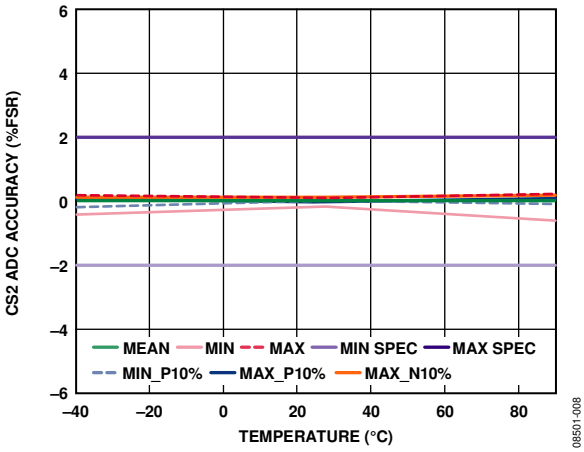

Figure 8. CS2 ADC Accuracy vs. Temperature (from 0 mV to 200 mV)

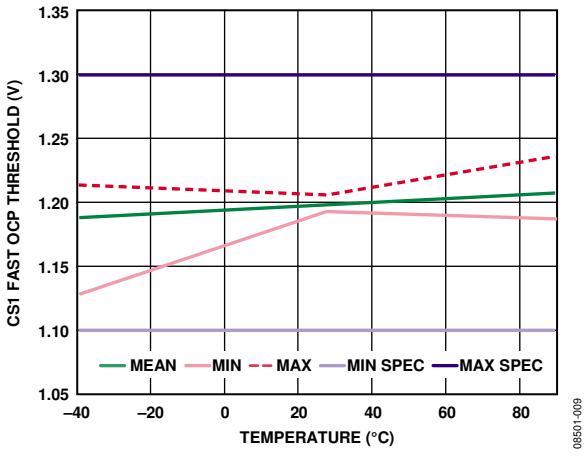

Figure 9. CS1 Fast OCP Threshold vs. Temperature

THEORY OF OPERATION

CURRENT SENSE

The ADP1043A has two individual current sense inputs: CS1 and CS2±. These inputs sense, protect, and control the output current and the share bus information. They can be calibrated to remove any errors due to external components.

CS1 Operation (CS1)

CS1 is typically used for the monitoring and protection of the primary side current. This is commonly known as the current transformer (CT) method of current sensing. The input signal at the CS1 pin is fed into an ADC for current monitoring. The range of the ADC is 0 V to 1.38 V. The input signal is also fed into a comparator for fast OCP protection. The typical configuration for the current sense is shown in Figure 10.

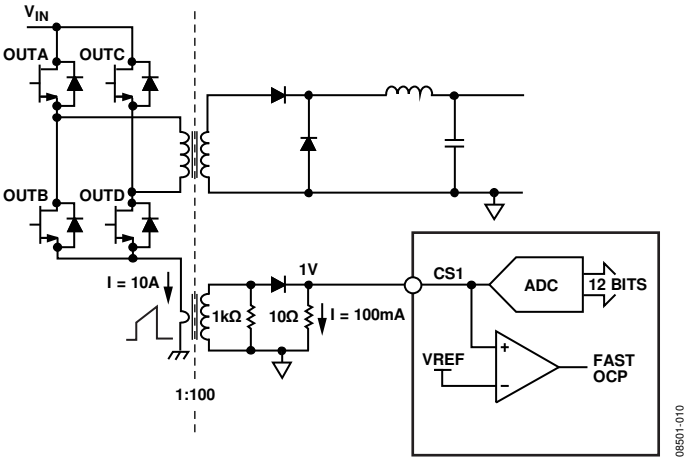

Figure 10. Current Sense 1 (CS1) Operation

The comparator effectively measures peak current, and the ADC effectively measures the average current information. This information is available through the I²C interface. Various thresholds and limits can be set for CS1, such as OCP. These thresholds and limits are described in the Current Sense and Current Limit Registers section.

CS2 Operation (CS2+, CS2–)

CS2± is used for the monitoring and protection of the secondary side current. The full-scale range of the CS2 ADC is 225 mV. The nominal full load voltage drop can be configured for 37.5 mV, 75 mV, or 150 mV. The differential inputs are fed into an ADC through a pair of external resistors. When using low-side current sensing, a 10 kΩ resistor is required. When using high-side current sensing, a 110 kΩ resistor is required (for a 12 V application).

Low-side current sensing is recommended because it provides improved performance compared with high-side current sensing. High-side current sensing is not supported for applications where the output voltage is above 20 V common mode. (There is not enough offset trim range above 20 V common mode.)

Typical configurations are shown in Figure 11 and Figure 12. Various thresholds and limits can be set for CS2, such as OCP. These thresholds and limits are described in the Current Sense and Current Limit Registers section.

When not in use, both CS2 inputs should be connected through 10 kΩ resistors to PGND.

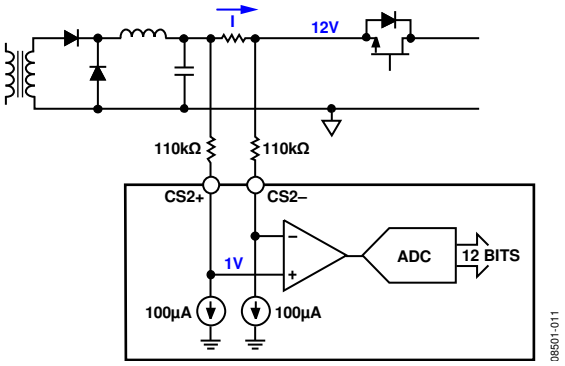

Figure 11. High-Side Resistive Current Sense

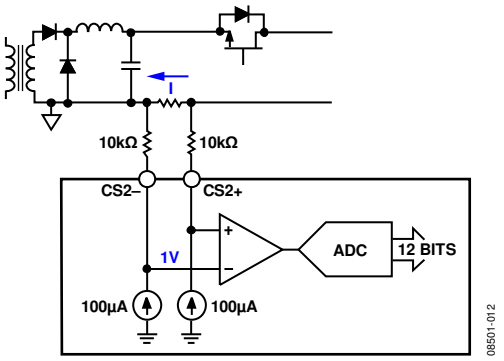

Figure 12. Low-Side Resistive Current Sense (Recommended)

VOLTAGE SENSE AND CONTROL LOOP

Multiple voltage sense inputs on the ADP1043A are used for the monitoring, control, and protection of the power supply output. The voltage information is available through the I²C interface. All voltage sense points can be calibrated digitally to remove any errors due to external components. This calibration can be performed in the production environment, and the settings can be stored in the EEPROM of the ADP1043A (see the Power Supply Calibration and Trim section for more information).

The update rate of the ADC from a control loop standpoint is set to the switching frequency. Therefore, if the switching frequency is set to 100 kHz, the ADC outputs a signal every 100 kHz to the control loop. Because the Σ-Δ modulators of the ADC sample at 1.6 MHz, the output of the ADC is the average of the 16 readings taken during the 1.6 MHz time frame.

For voltage monitoring, the VS1, VS2, and VS3 voltage value registers are updated every 10 ms. The ADP1043A stores every ADC sample for 10 ms and then outputs the average value at the end of the 10 ms period. Therefore, if these registers are read at least every 10 ms, a true average value is read. The same applies to the CS1 and CS2 current readings.

For the control loop, the high speed signal always comes from the VS1 high speed ADC. The low speed signal normally comes from the VS3 low speed ADC. However, during soft start or in response to a load OVP or other fault condition, the ADP1043A can switch its low speed regulating point from VS3 to VS1.

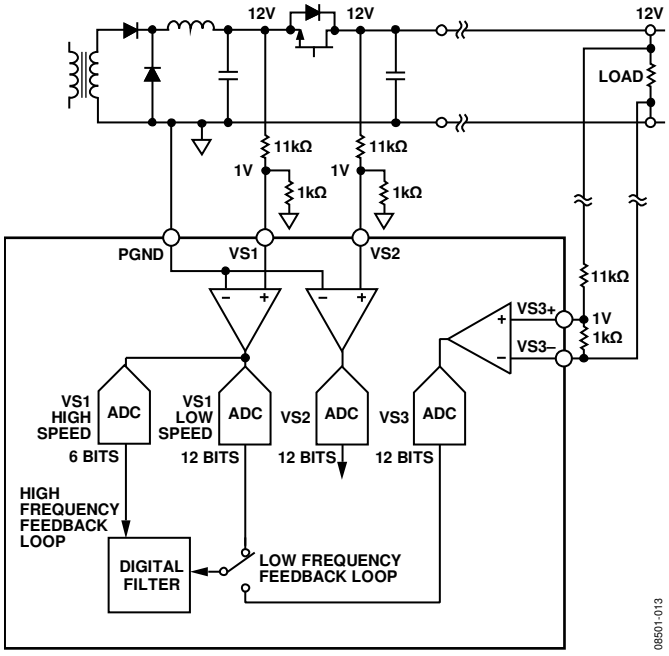

Figure 13. Voltage Sense Configuration

VS1 Operation (VS1)

VS1 is used for the monitoring and protection of the power supply voltage at the output of the LC stage, upstream of the OrFET. This is also the high frequency feedback loop for the power supply. The VS1 sense point on the power rail needs an external resistor divider to bring the nominal common-mode signal to 1 V at the VS1 pin (see Figure 13). The resistor divider is necessary because the ADP1043A VS1 ADC input range is 0 V to 1.55 V. This divided-down signal is internally fed into a high speed and a low speed Σ-Δ ADC. The output of the VS1 ADCs goes to the digital filter.

The high speed ADC has a 2 MHz bandwidth and is run from a 25 MHz clock. It has a range of ±18 mV. When the sampling rate is 200 kHz, there is 0.6 mV (two LSBs) of quantization noise. Increasing the sampling rate to 400 kHz increases the quantization noise to 1.2 mV.

In the event of a load overvoltage condition, the power supply is regulated from the VS1 sense point, rather than from the VS3 sense point.

VS2 Operation (VS2)

VS2 is typically used for the monitoring and protection of the output of the power supply, downstream of the OrFET. It is used with VS1 to control the OrFET gate drive turn-on. The VS2 sense point on the power rail needs an external resistor divider to bring the nominal common-mode signal to 1 V at the VS2 pin (see Figure 13). The resistor divider is necessary because the ADP1043A VS2 ADC input range is 0 V to 1.55 V. This divided-down signal is internally fed into an ADC. The output of the VS2 ADC goes to the VS2 voltage value register (Register 0x16).

VS3 Operation (VS3+, VS3–)

VS3± is used for the monitoring and protection of the remote load voltage. It is a fully differential input. This is the main feedback sense point for the power supply control loop. The VS3 sense point on the power rail needs an external resistor divider to bring the nominal common-mode signal to 1 V at the VS3± pins (see Figure 13). The resistor divider is necessary because the ADP1043A VS3 ADC input range is 0 V to 1.55 V. This divided-down signal is internally fed into an ADC. The output of the VS3 ADC goes to the digital filter.

ADCs

The ADP1043A includes several ADCs. The high speed ADC is described in the VS1 Operation (VS1) section. The other ADCs are low speed, high resolution. They have a 1 kHz bandwidth and 12-bit resolution. Each ADC has its own voltage reference for added protection from potential failure. The digital output of each ADC is readable through the appropriate value register.

DIGITAL FILTER

The loop response of the power supply can be changed using the internal programmable digital filter. A Type 3 filter architecture has been implemented. To tailor the loop response to the specific application, the low frequency gain, zero location, pole location, and high frequency gain can all be set individually (see the Digital Filter Programming Registers section). It is recommended that the Analog Devices software GUI be used to program the filter. The software GUI displays the filter response in Bode plot format and can be used to calculate all stability criteria for the power supply.

From the sensed voltage to the duty cycle, the transfer function of the filter in z-domain is as follows:

$$H(z)=\left(\frac{d}{202.24\times m}\times\frac{z}{z-1}\right)+\left(\frac{c}{7.68}\times\frac{z-b}{z-a}\right) \quad (1)$$

where:
a = filter_pole_register_value/256.
b = filter_zero_register_value/256.
c = high_frequency_gain_register_value.
d = low_frequency_gain_register_value.
m = 1 when 48.8 kHz ≤ f_{SW} < 97.7 kHz.
m = 2 when 97.7 kHz ≤ f_{SW} < 195.3 kHz.
m = 4 when 195.3 kHz ≤ f_{SW} < 390.6 kHz.
m = 8 when 390.6 kHz ≤ f_{SW}.

To go from z-domain to s-domain, plug the following equation into the H(z) equation:

$$z(s)=\frac{2f_{SW}+s}{2f_{SW}-s}$$

where f_{SW} is the switching frequency.

The digital filter introduces an extra phase delay element into the control loop. The digital filter circuit sends the duty cycle information to the PWM circuit at the beginning of each switching cycle (unlike an analog controller, which makes decisions on the duty cycle information continuously). Therefore, the extra phase delay for phase margin, Φ, introduced by the filter block is

$$\Phi = 180\times(f_C/f_{SW})$$

where:
f_C is the crossover frequency.
f_{SW} is the switching frequency.

At one tenth of the switching frequency, the phase delay is 18°. The GUI incorporates this phase delay into its calculations.

Two sets of registers allow for two distinct filter responses. The main filter, called the normal mode filter, is controlled by programming Register 0x60 to Register 0x63. The other filter, called the light load mode filter, is controlled by programming Register 0x64 to Register 0x67. The ADP1043A uses the light load mode filter only when the modulation is below the load current threshold (programmed through Register 0x3B).

The Analog Devices software GUI allows the user to program the light load mode filter in the same manner as the normal mode filter. It is recommended that the GUI be used for this purpose.

In addition, during the soft start process, a different set of digital filters is used. The soft start filter value for a, b, and c in Equation 1 is 0, and the d value is programmed through the soft start filter gain setting (Register 0x5F[1:0]).

PWM AND SYNC RECT OUTPUTS (OUTA, OUTB, OUTC, OUTD, OUTAUX, SR1, SR2)

The PWM and SR outputs are used for control of the primary side drivers and the synchronous rectifier drivers. These outputs can be used for several control topologies, including full-bridge, phase-shifted ZVS, and interleaved two switch forward converter configurations. Delays between rising and falling edges can be individually programmed. Special care must be taken to avoid shoot-through and cross-conduction. It is recommended that the Analog Devices software GUI be used to program these outputs. Figure 14 shows an example configuration to drive a full-bridge, phase shift topology with synchronous rectification.

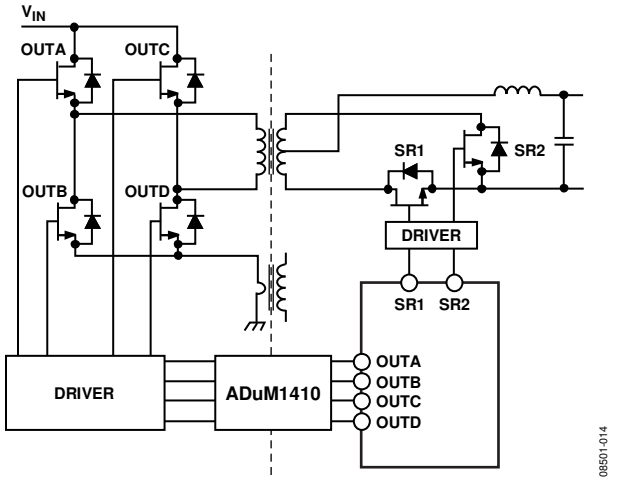

Figure 14. PWM Pin Assignment

The PWM and SR outputs all work together. Therefore, when reprogramming more than one of these outputs, it is important to first update all the registers, and then latch the information into the ADP1043A at one time. During reprogramming, the outputs are temporarily disabled. A special instruction is sent to the ADP1043A to ensure that new timing information is programmed simultaneously. This is done by setting Register 0x5D[0] to 1. It is recommended that PWM outputs be disabled when not in use.

OUTAUX is an additional PWM output pin; OUTAUX allows an extra PWM signal to be generated at a different frequency from the other six PWM outputs. This signal can be used to drive an extra power converter stage, such as a buck controller located in front of a full-bridge converter. OUTAUX can also be used as a clock reference signal.

SYNCHRONOUS RECTIFICATION

SR1 and SR2 are recommended for use as the PWM control signals when using synchronous rectification. These PWM signals can be set up similarly to the other PWM outputs. The turn-on of these signals can be programmed in two ways. They can either be turned on to their full PWM value immediately, or they can be turned on in a soft start fashion. When turned on in a soft start, the signals ramp up from zero duty cycle to the desired duty cycle. The advantage of ramping the SR signals is to minimize a voltage step that would occur by turning the SR FETs on completely. The advantage of turning the SR signals completely on immediately is that they can help to minimize the voltage transient caused by a load step.

Using Register 0x54[1], the SR soft start can be programmed to occur just once, the first time that the SR signals are enabled, or every time that the SR signals are enabled.

When programming the ADP1043A to use SR soft start, ensure correct operation of this function by setting the falling edge of SR1 (t_{10}) to a lower value than the rising edge of SR1 (t_9) and by setting the falling edge of SR2 (t_{12}) to a lower value than the rising edge of SR2 (t_{11}).

The speed of the SR enable is approximately 200 µs. This ensures that in case of a load step, the SR signals (and any other PWM outputs that are temporarily disabled) can be turned on quickly enough to prevent damage to the FETs that they are controlling.

ADAPTIVE DEAD TIME CONTROL

A set of registers called the adaptive dead time (ADT) registers (Register 0x68 to Register 0x6F) allows the dead time between PWM edges to be adapted on-the-fly. The ADP1043A uses the ADT only when the modulation is below the dead time (load current) threshold (programmed in Register 0x68). The Analog Devices software GUI allows the user to easily program the dead time values, and it is recommended that the software be used for that purpose.

Each individual PWM rising and falling edge (t_1 to t_{14}) can then be programmed to have a specific dead time offset. This offset can be positive or negative. The offset is relative to the nominal edge position. For example, if t_1 has a nominal rising edge of 100 ns and the ADT setting for t_1 is −15 ns, t_1 moves to 85 ns when it falls below the adaptive dead time threshold. The dead times are programmed using Register 0x69 to Register 0x6F.

LIGHT LOAD MODE

Register 0x3B allows the ADP1043A to shut down PWM outputs under light load conditions. The light load current threshold can be programmed. Below this current threshold, the SR outputs are disabled. The user can also program any of the other PWM outputs to shut down below this current threshold. This allows the ADP1043A to be used with an interleaved two transistor forward topology, incorporating phase shedding at light load. The light load mode digital filter is also used during light load mode.

MODULATION LIMIT

Using the modulation limit register (Register 0x2E), it is possible to apply a maximum modulation limit and a minimum modulation limit to any PWM signal, thus limiting the modulation range of any PWM. These limits are a percentage of the switching period. If the modulation required is lower than the minimum setting, pulse skipping can be enabled.

Following is an example of how to use the modulation limit settings. In this example, the switching cycle period is 4 µs and modulation on the t_2 edge (falling edge) is enabled. The nominal position of t_2 is set to 1.6 µs, which is 40% of the 4 µs period. The modulation high limit is set to (nominal + 50%). Therefore, the modulation high limit is (40% + 50%) = 90% of the switching cycle period; 90% of 4 µs = 3.6 µs. The modulation low limit is set to (nominal − 35%). Therefore, the modulation low limit is (40% − 35%) = 5% of the switching cycle period; 5% of 4 µs = 0.2 µs.

The GUI provided with the ADP1043A is recommended for evaluating this feature of the ADP1043A (see Figure 15).

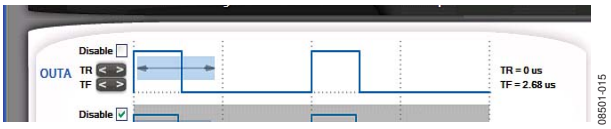

Figure 15. Setting Modulation Limits (Modulation Range Shown by Arrows)

OrFET CONTROL (GATE)

The GATE control signal drives an external OrFET. The OrFET gate control is used to protect against power flow into the power supply from another supply. This ensures that power flows only out of the power supply and that the unit can be hot-swapped. The OrFET circuit can be used only when the ADP1043A is connected to a sense resistor on the low side. The OrFET circuit is not guaranteed for operation with high-side current sensing.

The GATE pin is an open-drain, N-channel MOSFET. An external 2.2 kΩ pull-up resistor is recommended. Its output is normally high to keep the OrFET turned off. When the start-up criteria have been achieved, the GATE output is pulled low, allowing the OrFET to turn on. The OrFET turn-on and turn-off thresholds can be individually programmed. The GATE outputs are CMOS levels (0 V to 3.3 V). An external driver is required to turn the OrFET on or off.

The OrFET can be turned off by three methods:

- Fault flag (any fault flag can be programmed to turn off the OrFET)
- Fast OrFET control circuit
- Accurate OrFET control circuit

Fast OrFET control looks at the reverse voltage across CS2+ and CS2− and is implemented using an analog comparator (see Figure 16). If the voltage difference between CS2+ and CS2− is greater than the fast OrFET threshold programmed in Register 0x30, the OrFET is turned off.

Accurate OrFET control also uses the reverse voltage across the CS2+ and CS2− pins to disable the OrFET (see Figure 16). If the voltage difference between CS2+ and CS2− is greater than 0 mV, the OrFET is disabled. The accurate OrFET circuit is more accurate, but it is slower than the fast OrFET circuit.

The OrFET turn-on circuit looks at the voltage difference between VS1 and VS2 (see Figure 16). When the forward voltage drop from VS1 to VS2 is greater than the programmable OrFET enable threshold (Register 0x30[5:4]), the OrFET is enabled. The OrFET enable threshold can be set to −0.5%, 0%, 1%, or 2% of the nominal output voltage (12 V).

Recommended Setup

In a 12 V application, while in normal operating mode

- When 12 V < V_{OUT} < OVP, use the accurate OrFET control circuit to turn off the OrFET.
- When V_{OUT} > OVP, use load OVP to turn off the OrFET.

In a 12 V application, while in light load mode

- When 12 V < V_{OUT} < OVP, use ACSNS to turn off the OrFET.
- When V_{OUT} > OVP, use load OVP to turn off the OrFET.

In a 12 V application, when an internal short circuit occurs, follow this procedure:

1. Use fast OrFET to turn off the OrFET.
2. Use CS1 OCP or VS1 UVP to shut down the unit and restart it.

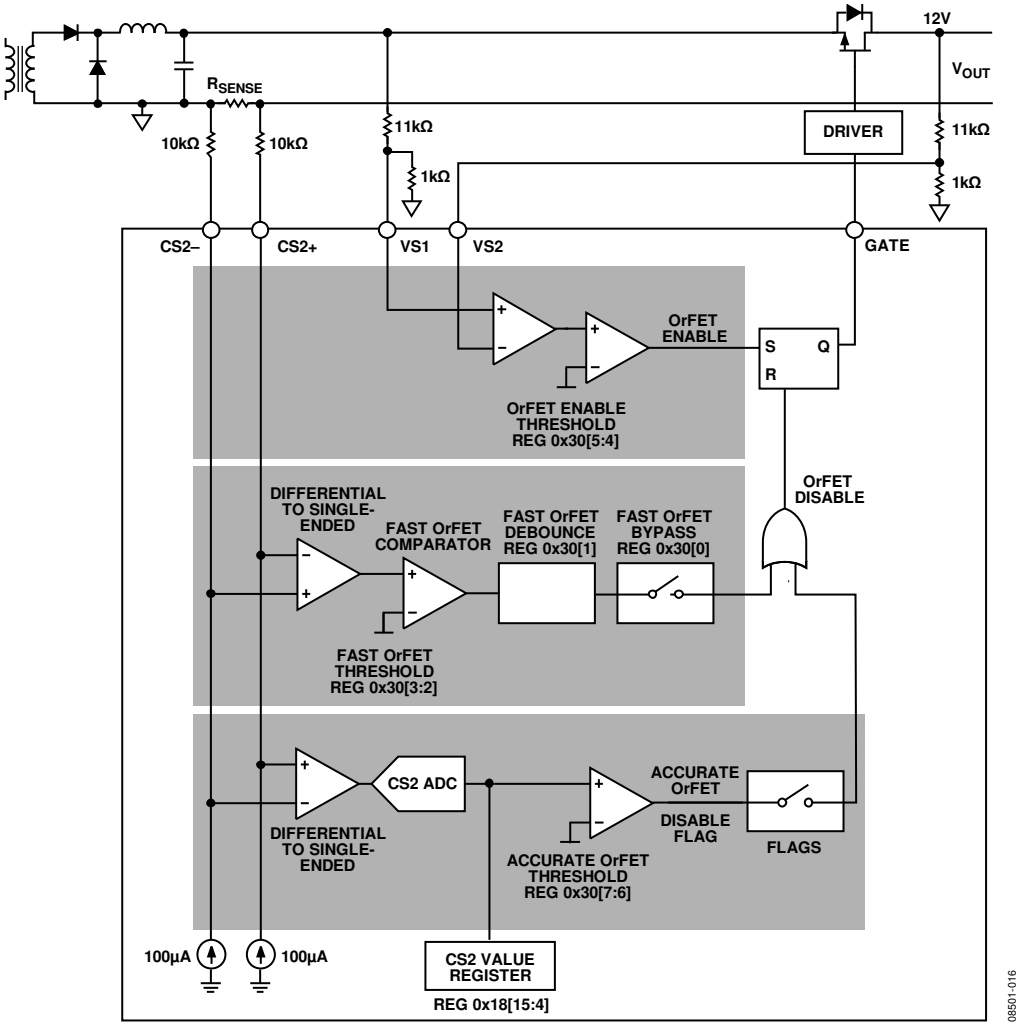

Figure 16. OrFET Control Circuit Internal Detailed Diagram

OrFET Operation Examples

Hot Plug into a Live Bus

A new PSU is plugged into a live 12 V bus (yellow). The internal voltage VS1 (red) is ramped up before the OrFET is turned on. After the OrFET is turned on (green), current in the new PSU begins to flow to the load (blue). The turn-on voltage threshold between the new PSU and the bus is programmable.

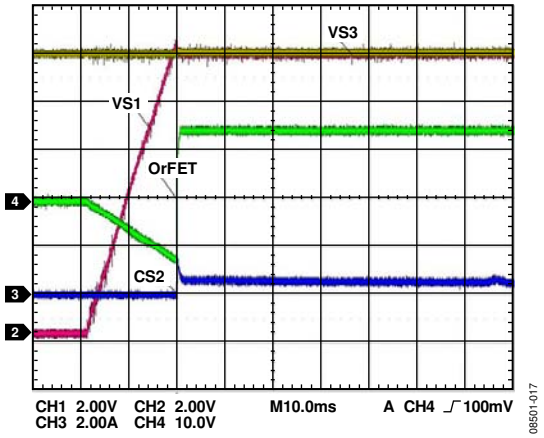

Figure 17. Hot Plug into a Live Bus (Yellow Is Bus Voltage; Red Is VS1 Voltage; Green Is OrFET Control Signal; Blue Is Load Current)

Runaway Master

A rogue PSU on the bus (yellow) has a fault condition, and the result is that the bus voltage increases above the OVP threshold. The good PSU turns off the OrFET (green) and regulates its internal voltage VS1 (red). When the rogue power supply fault condition is removed, the bus voltage decreases. The OrFET of the good PSU is immediately turned on and the good PSU resumes regulating from VS3.

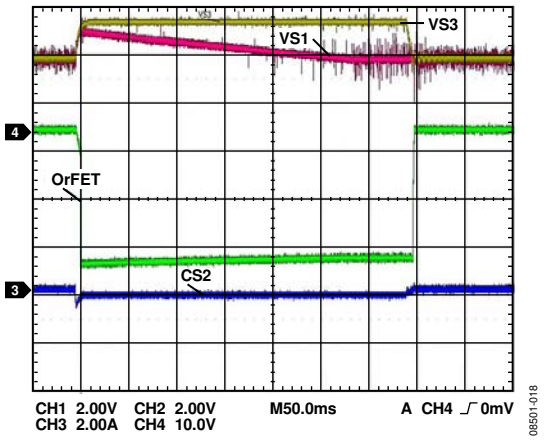

Figure 18. Runaway Master (Yellow Is Bus Voltage; Red Is VS1 Voltage; Green Is OrFET Control Signal; Blue Is Load Current)

Short Circuit

When one of the output rectifiers fails, the bus voltage can collapse if the OrFET is not promptly turned off. The fast OrFET comparator is used to protect the system from this fault event. Figure 19 shows a short circuit applied to the output capacitors, before the OrFET. After the fast OrFET threshold for CS2 (blue) is triggered, the OrFET (green) is turned off. In this case, the gate driver is not very fast and takes about 500 ns. (A larger buffer to drive the OrFET would turn it off quicker.) Figure 19 also shows the operation when the short circuit is removed. The internal regulation point, VS1 (red), returns to 12 V, and the OrFET (green) is reenabled. The PSU again begins to contribute current to the load (blue).

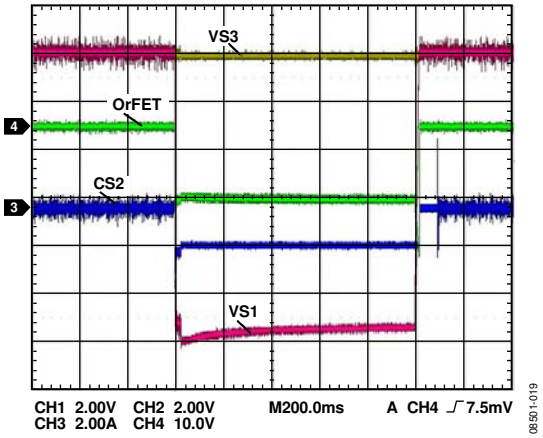

Figure 19. Internal Short Circuit (Yellow Is Bus Voltage; Red Is VS1 Voltage; Green Is OrFET Control Signal; Blue Is Load Current)

Light Load Mode Operation

PSU 1 increases its voltage at light load from 12 V to 12.1 V (yellow). Both PSU 1 and PSU 2 are CCM, so PSU 1 sources current and PSU 2 sinks current (blue). In PSU 2, after 10 ms the accurate OrFET control turns off the OrFET to prevent reverse current from flowing. Note that the OrFET voltage (green) is solid during this transition because PSU 1 and PSU 2 are in CCM mode.

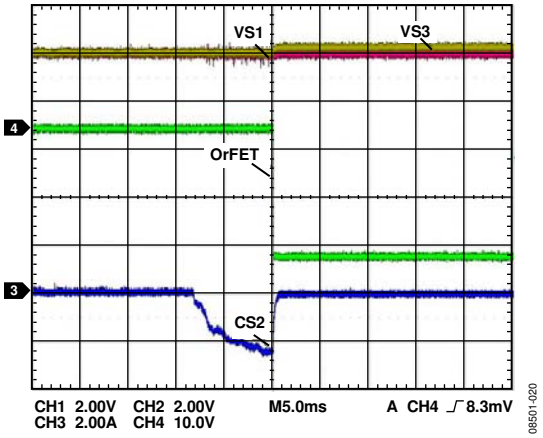

Figure 20. Light Load Mode (Yellow Is Bus Voltage; Red Is VS1 Voltage; Green Is OrFET Control Signal; Blue Is Load Current)

VDD

When VDD is applied, a certain time elapses before the part is capable of regulating the power supply. When the VDD rises above the power-on reset and UVLO levels, it takes approximately 20 µs for VCORE to reach its operational point of 2.5 V. The EEPROM contents are then downloaded to the registers. The download takes an additional 25 µs (approximately). After the EEPROM download, the ADP1043A is ready for operation. If the ADP1043A is programmed to power up at this time, the soft start ramp begins.

VDD/VCORE OVLO

The ADP1043A has built-in overvoltage protection (OVP) on its supply rails. When the VDD or VCORE voltage rises above the OVLO threshold, the response can be programmed. This circuit can be set to be ignored, but it is recommended that the user not program the OVP circuit to be ignored.

POWER GOOD

The ADP1043A has two power-good pins. The PGOOD1 pin and fault flag are set when any of the following conditions are out of range: power supply, CS1 fast OCP, CS1 accurate OCP, CS2 accurate OCP, UVP, local OVP, or load OVP.

The PGOOD2 pin and fault flag are set when any flag is set: power supply, OrFET, CS1 fast OCP, CS1 accurate OCP, CS2 accurate OCP, voltage continuity, UVP, accurate OrFET disable, ACSNS, external flag (FLAGIN), VCORE OV, VDD OV, local OVP, load OVP, OTP, CRC fault, and EEPROM unlocked.

If Register 0x2D[3] is set, PGOOD2 looks only at the flags that are not programmed to be ignored.

The PGOOD2 pin can also be used as an interrupt pin to notify a host controller that a flag has been set. The polarity of the PGOOD1 and PGOOD2 pins is configured as active low.

SOFT START

A dedicated filter is used during soft start. The filter is disabled at the end of the soft start routine, and the voltage loop digital filter is used.

Fault Condition During Soft Start

If a CS1 fast OCP fault condition occurs during soft start, the entire soft start routine is reset, and the ADP1043A begins another soft start routine. All other fault flags are ignored during soft start.

Soft Start Routine

When the user turns on the power supply (enables PSON), the following soft start procedure occurs:

1. The PSON signal is enabled at Time t_0. The ADP1043A checks that initial flags are OK. These flags include VDD OK and GND OK.
2. The ADP1043A waits for Time t_1 before it begins soft start. The length of t_1 is set in Register 0x2C, Bits[4:3].
3. The soft start begins to ramp up the power supply voltage at the start of Time t_2.
4. The ADP1043A keeps the OrFET gate signal turned off. The voltage differential across the OrFET increases (VS1 − VS2) due to the diode conduction of the OrFET. When the voltage differential reaches the OrFET enable threshold (Register 0x30, Bits[5:4]), the OrFET gate signal is enabled at Time t_3. The ADP1043A begins to regulate voltage from VS3 instead of VS1.
5. After the power supply voltage increases above the VS1 UVP undervoltage limit (Register 0x34, Bits[6:0]), at the end of Time t_4, the UVP flag is reset.
6. After the UVP flag is reset and if all other PGOOD1 fault conditions are OK, the PGOOD1 signal waits for Time t_5 before it is enabled. The length of t_5 is programmable in Register 0x2D, Bits[7:4].

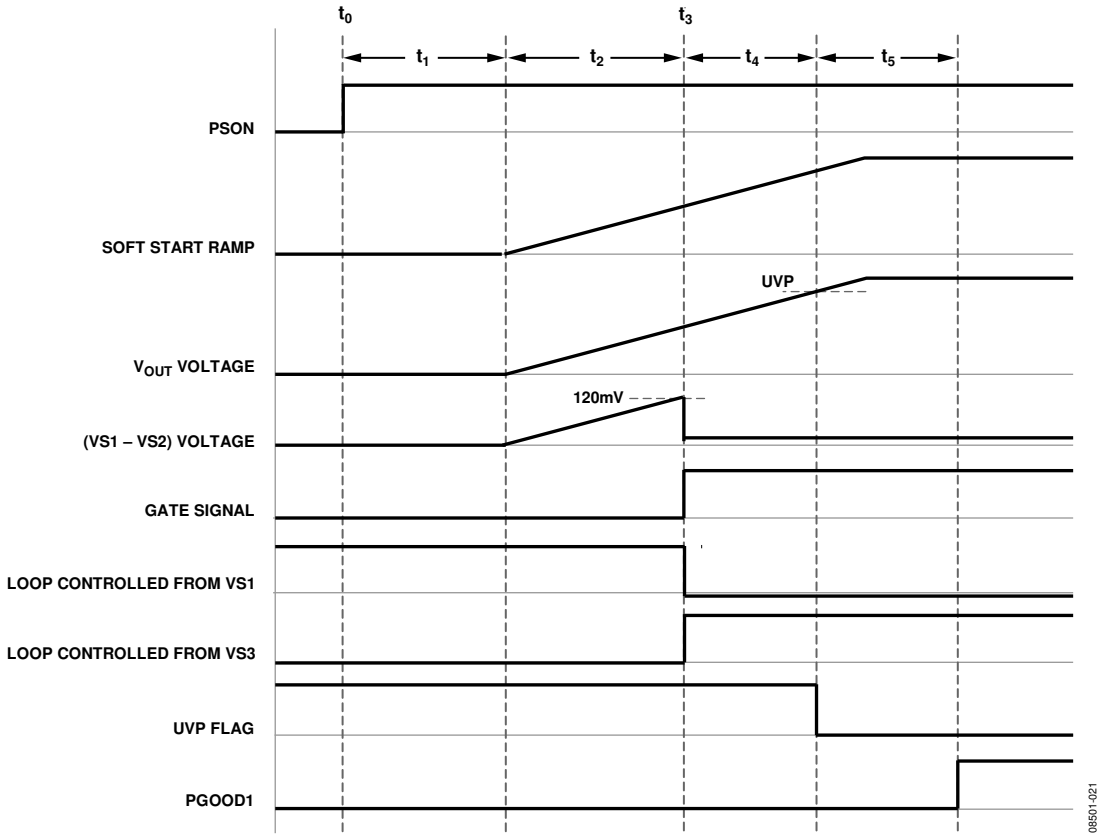

Figure 21. Soft Start Timing Diagram

CURRENT SHARING (SHARE)

The ADP1043A supports both analog current sharing and digital current sharing. It is recommended that analog current sharing be used because it offers improved performance over digital current sharing. Digital current sharing requires a load line of >15 mΩ to prevent oscillation between units. The analog current sharing scheme has no such issues.

Using Register 0x29, Bit 3, it is possible to program the ADP1043A to use the CS1 current information or the CS2 current information for current sharing.

Analog Current Sharing

The ADP1043A supports analog current sharing. The current reading from CS1 or CS2 can be output to the SHAREo pin in the form of a digital bit stream, which is the output of the current sense ADC (see Figure 23). The bit stream is proportional to the current being delivered by this unit to the load. By filtering this digital bit stream using an external RC filter, the current information is turned into an analog voltage. This means that there is now an analog voltage that is proportional to the current being delivered by this unit to the load. This voltage can be compared to the share bus. If the unit is not supplying enough current, an error signal can be applied to the VS3 feedback point. This signal causes the unit to increase its output voltage and, therefore, its current contribution to the load.

For more information about the analog current share functionality, including schematics and measurements in different fault and setup conditions, see the product page for the ADP1043A.

Digital Share Bus

The digital share bus scheme is similar in principle to the traditional analog share bus scheme. The difference is that instead of using a voltage on the share bus to represent current, a digital word is used.

The ADP1043A outputs a digital word onto the share bus. The digital word is a function of the current that the power supply is providing (the higher the current, the larger the digital word).

The power supply with the highest current controls the bus (master). A power supply that is putting out less current (slave) sees that another supply is providing more power to the load than it is. During the next cycle, the slave increases its current output contribution by increasing its output voltage. This cycle continues until the slave outputs the same current as the master, within a programmable tolerance range. Figure 22 shows the configuration of the digital share bus.

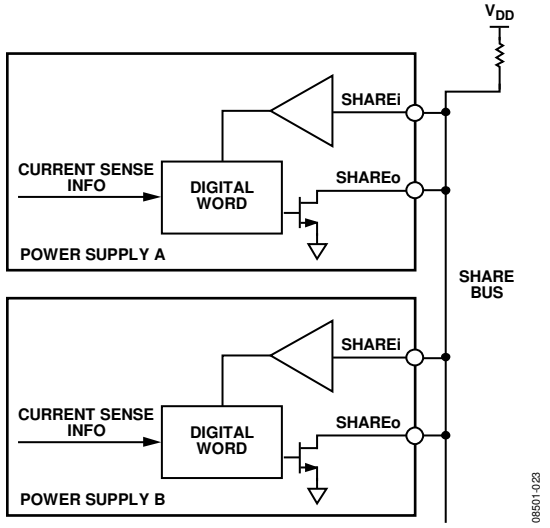

Figure 22. Digital Current Share Configuration

The digital share bus is based on a single-wire communication bus principle; that is, the clock and data signals are contained together.

When two or more ADP1043A devices are connected, they synchronize their share bus timing. This synchronization is performed by the start bit at the beginning of a communications frame. If a new ADP1043A is hot-swapped onto an existing digital share bus, it waits to begin sharing until the next frame. The new ADP1043A monitors the share bus until it sees a stop bit, which designates the end of a share frame. It then performs synchronization with the other ADP1043A devices during the next start bit. The digital share bus frame is shown in Figure 24.

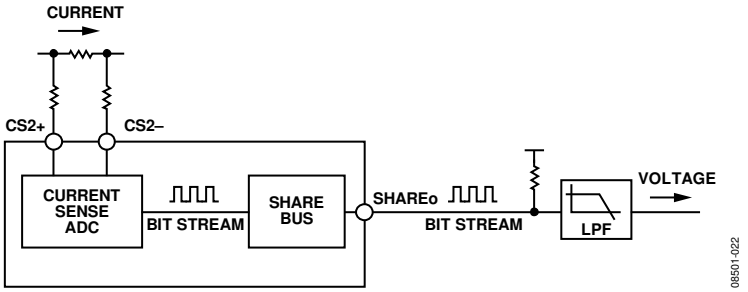

Figure 23. Analog Current Share Configuration

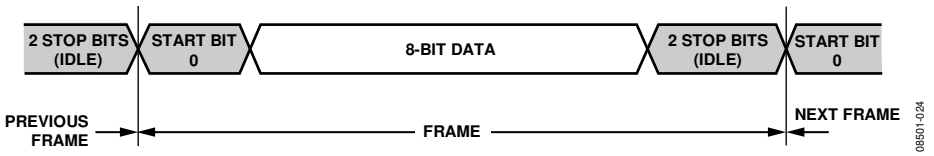

Figure 24. Digital Current Share Frame Timing Diagram

Figure 25 shows the possible signals on the share bus.

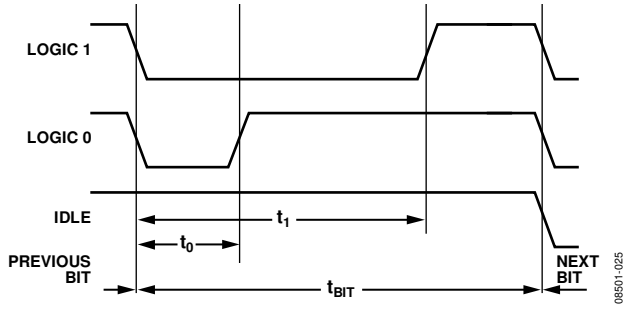

Figure 25. Share Bus High, Low, and Idle Bits

The length of a bit (t_{BIT}) is fixed at 10 µs. A Logic 1 is defined as a high-to-low transition at the start of the bit and a low-to-high transition at 75% of t_{BIT}. A Logic 0 is defined as a high-to-low transition at the start of the bit and a low-to-high transition at 25% of t_{BIT}.

The bus is idle when it is high during the whole period of t_{BIT}. All other activity on the bus is illegal. Glitches up to t_{GLITCH} (200 ns) are ignored.

The digital word that represents the current information is eight bits long. The ADP1043A takes the eight MSBs of the CS1 or CS2 reading (whichever the user chooses as the current share signal) and uses this reading as the digital word. When read, the share bus value at any given time is equal to the CS1 or CS2 current reading (see Figure 26).

Digital Share Bus Scheme

Each power supply compares the digital word that it is outputting with the digital words of all the other supplies on the bus.

Round 1

In Round 1, every supply first places its MSB on the bus. If a supply senses that its MSB is the same as the value on the bus, it continues to Round 2. If a supply senses that its MSB is less than the value on the bus, it means that this supply must be a slave.

When a supply becomes a slave, it stops communicating on the share bus because it knows that it is not the master. The supply then increases its output voltage in an attempt to share more current.

If two units have the same MSB, they both continue to Round 2, because either of them could be the master.

Round 2

In Round 2, all supplies that are still communicating on the bus place their second MSB on the share bus. If a supply senses that its MSB is less than the value on the bus, it means that this supply must be a slave and it stops communicating.

Round 3 to Round 8

The same algorithm is repeated for up to eight rounds to allow supplies to compare their digital words and, in this way, to determine whether each unit is the master or a slave.

Digital Share Bus Configuration

The digital share bus can be configured in various ways. The bandwidth of the share bus loop is programmable in Register 0x29[2:0]. The extent to which a slave tries to match the current of the master can be selected by programming Register 0x2A[3:0]. The primary side or the secondary side can be used as the current share signal by programming Register 0x29[3].

A load line may be required between PSUs when using a digital share bus. A minimum impedance of 15 mΩ is recommended between the remote voltage sense node and the load.

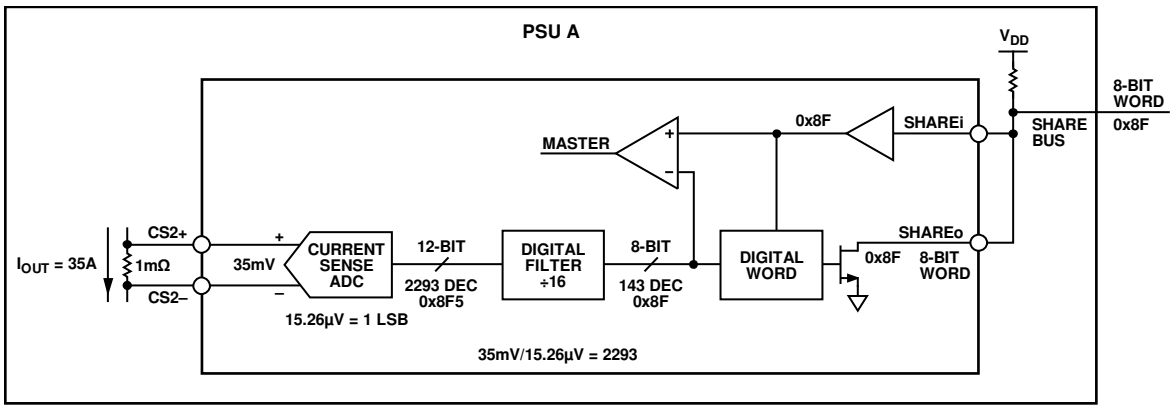

Figure 26. How the Share Bus Generates the Digital Word to Place on the Digital Share Bus

POWER SUPPLY SYSTEM AND FAULT MONITORING

The ADP1043A has extensive system and fault monitoring capabilities. The system monitoring functions include voltage, current, power, and temperature readings. The fault conditions include out-of-limit values for current, voltage, power, and temperature. The limits for the fault conditions are programmable. The ADP1043A has an extensive set of flags that are set when certain thresholds or limits are exceeded. These thresholds and limits are described in the Fault Registers section.

FLAGS

The ADP1043A has an extensive set of flags that are set when certain limits, conditions, and thresholds are exceeded. The real-time status of these flags can be read in Register 0x00 to Register 0x03. The response to these flags is individually programmable. Flags can be ignored or used to trigger tasks such as turning off certain PWM outputs or the OrFET GATE output. Flags can also be used to turn off the power supply. The ADP1043A can be programmed to respond when these flags are reset. For more information, see Register 0x08 to Register 0x0D.

The ADP1043A also has a set of latched fault registers (Register 0x04 to Register 0x07). The latched fault registers have the same flags as Register 0x00 to Register 0x03, but the flags in the latched registers remain set so that intermittent faults can be detected. Reading a latched register resets all the flags in that register.

MONITORING FUNCTIONS

The ADP1043A monitors and reports several signals, including voltages, currents, power, and temperature. All these values are stored in individual registers and can be read through the I²C interface. See the Value Registers section for more details.

VOLTAGE READINGS

The VS1, VS2, and VS3 ADCs have an input range of 1.55 V. The outputs of the ADCs are 12-bit values, which means that the LSB size is 1.55 V/4096 = 378.4 µV. The user is limited to an input range of 1.5 V, which means that the ADC output code is limited to 1.5 V/378.4 µV = 3964.

The equation to calculate the ADC code at a certain voltage (Vx) is given by the following formula:

$$ADC\ Code = Vx/378.4\ \mu V$$

For example, when there is 1 V on the input of the ADC

$$ADC\ Code = 1\ V/378.4\ \mu V$$

$$ADC\ Code = 2643$$

In a 12 V application, the 12 V reading is divided down using a resistor divider network to provide 1 V at the sense pin. Therefore, to convert the register value to a real voltage, use the following formula:

$$V_{OUT} = (VSx\_Voltage\_Value/2643) \times ((R1 + R2)/R2)$$

In a 12 V system, this equates to

$$V_{OUT} = (VSx\_Voltage\_Value/2643) \times 12\ V$$

CURRENT READINGS

CS1 Pin

DC Input Voltage

The CS1 ADC is identical in design to the VS1, VS2, and VS3 ADCs. Therefore, the description in the Voltage Readings section also applies to the CS1 ADC. When there is exactly 1 V on the CS1 pin, the value in the CS1 value register (Register 0x13) reads 2968.

CS1 has an input range of 1.38 V. The ADC performs a 12-bit reading conversion on this value, which means that the LSB size is 1.38 V/4096 = 337 µV.

The equation to calculate the ADC code at a certain CS1 input voltage (Vx) is given by the following formula:

$$ADC\ Code = Vx/337\ \mu V$$

For example, when there is 1 V on the CS1 input pin

$$ADC\ Code = 1\ V/337\ \mu V$$

$$ADC\ Code = 2968$$

AC Input Voltage

CS1 often receives a rectified ac signal through a current transformer. In this case, the ADC has a frequency response (see Figure 27).

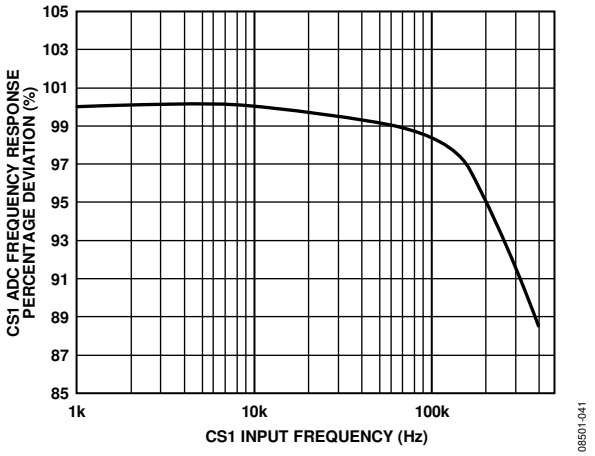

Figure 27. CS1 ADC Frequency Response

To compensate for this frequency response, the multiplication factor (M) should be used, as shown in the following equation:

$$M = (-2 \times 10^{-18} \times f_{SW}^3) + (2 \times 10^{-12} \times f_{SW}^2) + (2 \times 10^{-8} \times f_{SW}) + 0.9998$$

where f_{SW} is the switching frequency of the power supply.

Using the multiplication factor (M) results in a more accurate reading. This formula can be used by an MCU or other system monitoring device. The ADP1043A GUI has the option to use this formula.

CS2 Pin

The user sets the full-scale (FS) voltage drop—37.5 mV, 75 mV, or 150 mV—that is present across the R_{SENSE} resistor by programming Register 0x23, Bits[7:6].

The CS2 ADC has an input range of 250 mV. The resolution is 12 bits, which means that the LSB size is 250 mV/4096 = 61.04 µV. The user is limited to an input range of 215 mV.

The equation to calculate the ADC code at a certain voltage (V_X) is given by the following formula:

$$ADC\ Code = V_X/250\ mV \times 4096$$

For example, when there is 150 mV on the input of the ADC

$$ADC\ Code = 150\ mV/250\ mV \times 4096$$

$$ADC\ Code = 2457$$

Therefore, to convert the CS2 value reading to a real current, use the following formula:

$$I_{OUT} = (CS2\_Value/2457) \times (FS/R_{SENSE})$$

where:
FS is the full-scale voltage drop (37.5 mV, 75 mV, or 150 mV).
R_{SENSE} is the sense resistor value.

For example, if CS2_Value = 1520, R_{SENSE} = 20 mΩ, and FS = 150 mV, the real current is calculated as follows:

$$I_{OUT} = (1520/2457) \times (150\ mV/20\ m\Omega)$$
$$I_{OUT} = 4.64\ A$$

POWER READINGS

The output power value register (Register 0x19) is the product of the VS3 voltage value and the CS2 current value. Therefore, a combination of the formulas in the Voltage Readings section and the CS2 Pin section is used to calculate the power reading in watts. This register is a 16-bit word. It multiplies two 12-bit numbers and discards the eight LSBs.

$$P_{OUT} = (V_{OUT}) \times (I_{OUT})$$

For example,

$$P_{OUT} = (12\ V) \times (4.64\ A) = 55.68\ W$$

POWER MONITORING ACCURACY

The ADP1043A power monitoring accuracy is specified relative to the full-scale range of the signal that it is measuring.

FIRST FLAG FAULT ID AND VALUE REGISTERS

When the ADP1043A registers several fault conditions, it stores the value of the first fault in a dedicated register. For example, if the overtemperature (OTP) fault is registered, followed by an OVP fault, the OTP flag is stored in the first flag ID register (Register 0x10). This register gives the user more information for fault diagnosis than a simple flag. The contents of this register are latched, meaning that they are stored until read by the user. The contents are also reset by a PSON signal.

If a flag is set to be ignored, it does not appear in the first flag register.

EXTERNAL FLAG INPUT (FLAGIN PIN)

The FLAGIN pin can be used to send an external fault signal into the ADP1043A. The reaction to this flag can be programmed in the same way as the internal flags.

TEMPERATURE READINGS (RTD PIN)

The RTD pin is set up for use with an external 100 kΩ negative temperature coefficient (NTC) thermistor. The RTD pin has an internal 10.8 µA current source. Therefore, with a 100 kΩ thermistor, the voltage on the RTD pin is 1 V at 25°C. An ADC on the ADP1043A monitors the voltage on the RTD pin.

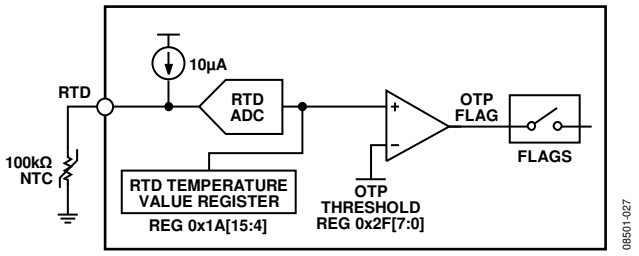

Figure 28. RTD Pin Internal Details

The output of the RTD ADC is linearly proportional to the voltage on the RTD pin. However, thermistors exhibit a nonlinear function of resistance vs. temperature. Therefore, it is necessary to perform some postprocessing on the RTD ADC reading to accurately read the temperature. This postprocessing can be in the form of a lookup table or polynomial equation to match the specific NTC being used.

OVERTEMPERATURE PROTECTION (OTP)

If the temperature sensed at the RTD pin exceeds the programmable threshold, the OTP flag is set. The hysteresis on this flag is 16 mV (see Register 0x2F in Table 43 for details). The response to the OTP flag is programmable.

The RTD trim is required to make accurate temperature readings at the lower end of the RTD ADC range. This results in a more accurate measurement for determining the OTP threshold (see the RTD/OTP Trim section).

OVERCURRENT PROTECTION (OCP)

The ADP1043A has several OCP functions. CS1 and CS2 have individual OCP circuits to provide both primary and secondary side protection.

CS1 has two protection circuits: CS1 fast OCP and CS1 accurate OCP (see Figure 29). CS1 fast OCP is an analog comparator. When the voltage at the CS1 pin exceeds the (fixed) 1.2 V threshold, the CS1 fast OCP flag is set. A blanking time can be set to ignore the current spike at the beginning of the current signal. A debounce time can be programmed to improve the noise immunity of the OCP circuit. When the CS1 fast OCP comparator is set, all PWM outputs are immediately disabled for the remainder of the switching cycle. They are reenabled at the start of the next switching cycle. This function can be bypassed if not needed.

CS1 accurate OCP is used for more precise control of overcurrent protection. With CS1 accurate OCP, the reading at the output of the CS1 ADC (Register 0x13) is compared to a programmable OCP value. The CS1 accurate OCP value can be programmed from 0 to 31 decimal using Register 0x22, Bits[4:0]. If the CS1 reading exceeds the CS1 accurate OCP value, the CS1 accurate OCP flag is set. The speed of this decision is 10 ms. The response to the flag is programmable.

CS2 has one OCP protection circuit: CS2 accurate OCP. The reading at the output of the CS2 ADC (Register 0x18) is compared to a programmable OCP threshold. The CS2 OCP threshold can be programmed from 0 to 254 decimal using Register 0x26, Bits[7:0]. If the CS2 reading exceeds the CS2 OCP threshold, the CS2 accurate OCP flag is set. The speed of this decision is 10 ms. The response to the flag is programmable.

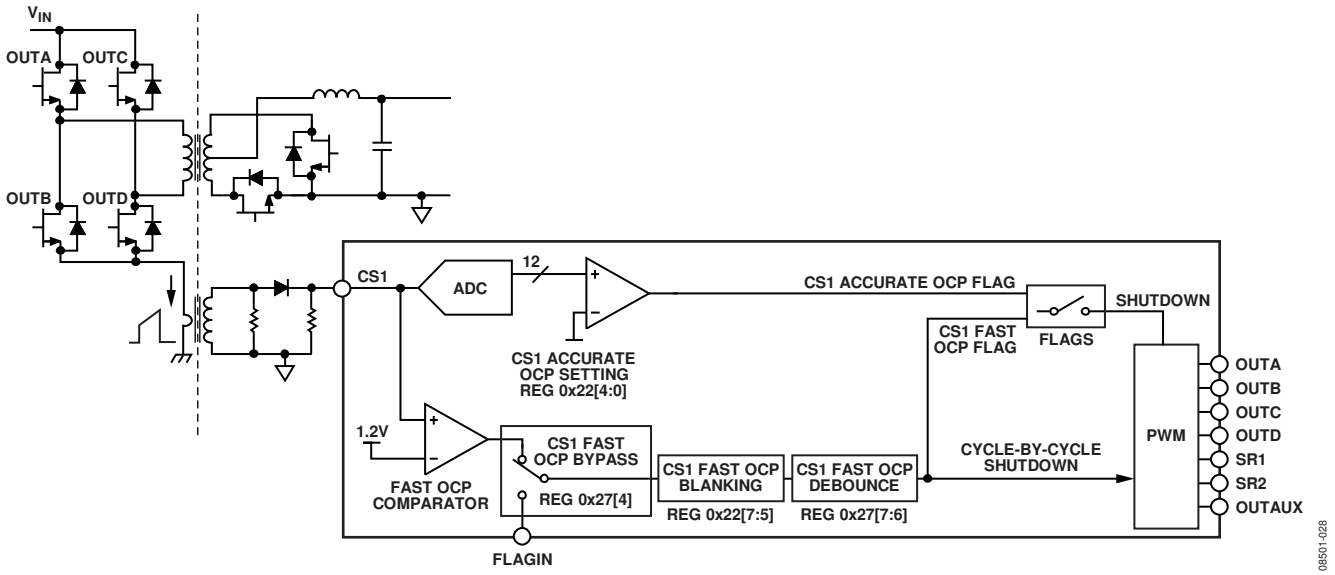

Figure 29. CS1 OCP Detailed Internal Schematic