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Digital Controller for Isolated Power Supply Applications

Data Sheet

ADP1046AW

FEATURES

- **Qualified for automotive applications**
- **Integrates all typical PWM controller functions**
  - **7 PWM control signals**
  - **Digital control loop**
  - **Integrated programmable loop filters**
  - **Programmable voltage line feedforward**
  - **Dedicated soft start filter**
  - **Remote and local voltage sense**
  - **Primary and secondary side current sense**
  - **Synchronous rectifier control**
  - **Current sharing**
  - **OrFET control**
- **I²C interface**
- **Extensive fault detection and protection**
- **Extensive programming and telemetry**
- **Fast digital calibration**
- **User accessible EEPROM**

APPLICATIONS

- **AC-to-DC power supplies**
- **Isolated dc-to-dc power supplies**
- **Redundant power supply systems**
- **Server, storage, network, and communications infrastructure**

GENERAL DESCRIPTION

The ADP1046AW is a flexible, digital secondary side controller designed for ac-to-dc and isolated dc-to-dc secondary side applications. The ADP1046AW is pin-compatible with the ADP1043A and offers several enhancements and new features, including voltage feedforward and improved loop response to maximize efficiency.

The ADP1046AW is optimized for minimal component count, maximum flexibility, and minimum design time. Features include local and remote voltage sense, primary and secondary side current sense, digital pulse-width modulation (PWM) generation, current sharing, and redundant OrFET control. The control loop digital filter and compensation terms are integrated and can be programmed over the I²C interface. Programmable protection features include overcurrent protection (OCP), overvoltage protection (OVP), undervoltage lockout (UVLO), and overtemperature protection (OTP).

The built-in EEPROM provides extensive programming of the integrated loop filter, PWM signal timing, inrush current, and soft start timing and sequencing. Reliability is improved through a built-in checksum and programmable protection circuits.

A comprehensive GUI is provided for easy design of loop filter characteristics and programming of the safety features. The industry-standard I²C bus provides access to the many monitoring and system test functions.

The ADP1046AW is available in a 32-lead LFCSP and operates from a single 3.3 V supply.

TYPICAL APPLICATION CIRCUIT

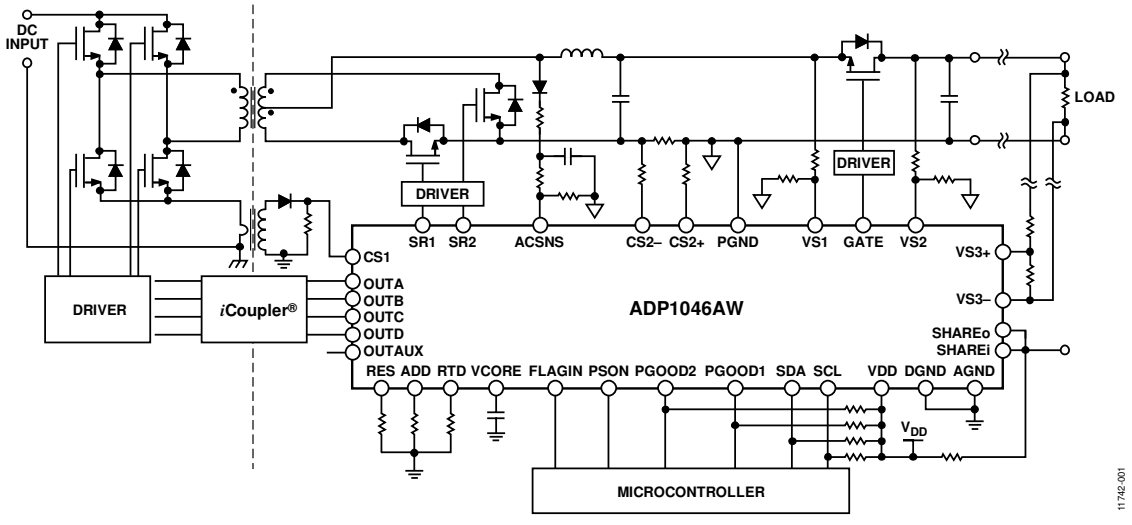

Figure 1.

Rev. 0 **Document Feedback**

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REVISION HISTORY

12/13—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.0 V to 3.6 V, T_A = −40°C to +125°C, unless otherwise noted. FSR = full-scale range.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
Supply Voltage	V_{DD}	4.7 µF capacitor connected to AGND	3.05	3.3	3.6	V
Supply Current	I_{DD}	Normal operation (PSON is high or low)		20		mA
		During EEPROM programming (40 ms)		I_{DD} + 8		mA
		Shutdown (V_{DD} below UVLO)		100		µA
POWER-ON RESET						
Power-On Reset		V_{DD} rising			3.02	V
UVLO		V_{DD} falling	2.75	2.85	2.97	V
UVLO Hysteresis				40		mV
OVLO			3.75	4.0	4.13	V
OVLO Debounce		When set to 2 µs		2.0		µs
		When set to 500 µs		500		µs
VCORE PIN		0.33 µF capacitor connected to DGND				
Output Voltage		T_A = 25°C	2.4	2.5	2.7	V
OSCILLATOR AND PLL						
PLL Frequency		RES = 10 kΩ (±0.1%)	190	200	210	MHz
OUTA, OUTB, OUTC, OUTD, OUTAUX, SR1, SR2, GATE PINS						
Output Low Voltage	V_{OL}	Source current = 10 mA			0.4	V
Output High Voltage	V_{OH}	Source current = 10 mA	V_{DD} − 0.4			V
Rise Time		C_{LOAD} = 50 pF		3.5		ns
Fall Time		C_{LOAD} = 50 pF		1.5		ns
VS1, VS2, VS3 LOW SPEED ADCs						
Input Voltage Range	V_{IN}	Differential voltage from VS1, VS2 to PGND, and from VS3+ to VS3−	0	1	1.6	V
Usable Input Voltage Range			0		1.4	V
ADC Clock Frequency				1.56		MHz
Register Update Rate				10		ms
Voltage Sense Measurement Accuracy		Factory trimmed at 1.0 V				
		0% to 100% of usable input voltage range	−3.0		+3.0	% FSR
			−48		+48	mV
		10% to 90% of usable input voltage range	−2.0		+2.0	% FSR
			−32		+32	mV
		900 mV to 1.1 V	−1.2		+1.2	% FSR
			−16		+16	mV
Temperature Coefficient					65	ppm/°C
Leakage Current					1.0	µA
Voltage Sense Measurement Resolution				12		Bits
Common-Mode Voltage Offset			−0.25		+0.25	% FSR
Voltage Differential from VS3− to PGND			−200		+200	mV
VS1 Accurate OVP Speed		Register 0x32[1:0] = 00; equivalent resolution is 7 bits		80		µs
VS1 OVP Threshold Accuracy		Relative to nominal voltage (1 V) on VS1	−2.0		+2.0	% FSR
VS2 and VS3 OVP Speed		Register 0x33[1:0] = 00; equivalent resolution is 7 bits		80		µs
VS2 and VS3 OVP Threshold Accuracy		Relative to nominal voltage (1 V) on VS2 and VS3	−2.0		+2.0	% FSR

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
VS3 HIGH SPEED ADC						
Equivalent Sampling Frequency	f_{SAMP}			f_{SW}		kHz
Equivalent Resolution		f_{SW} = 390.6 kHz		6		Bits
Dynamic Range				±30		mV
VS1 FAST OVP COMPARATOR						
Threshold Accuracy		At factory trim of 1.2 V		1	1.60	%
		At other thresholds (0.8 V to 1.6 V)	−2.06		+2.06	%
Propagation Delay		Does not include debounce time (Register 0x0A[7] = 1)		40		ns
VS1 UVP DIGITAL COMPARATOR						
VS1 UVP Accuracy			−3.0		+3.0	% FSR
Propagation Delay		Does not include debounce time (Register 0x0B[3] = 1)		80		µs
AC SENSE COMPARATOR		PWM and resonant mode				
Input Voltage Threshold			0.4	0.45	0.5	V
Propagation Delay		From ACSNS threshold to SRx rising edge (resonant mode only)		160		ns
ADC Clock Frequency				1.56		MHz
Input Voltage Range	V_{ACSNS}		0	1	1.6	V
Usable Input Voltage Range			0		1.4	V
Sampling Frequency for I^2C Reporting				100		Hz
Sampling Period for Feedforward		Equivalent resolution is 11 bits		10		µs
Measurement Accuracy		Factory trimmed at 1.0 V				
		0% to 100% of usable input voltage range	−5.0		+3.0	% FSR
		10% to 90% of usable input voltage range	−2.0		+2.0	% FSR
		900 mV to 1.1 V	−1.2		+1.2	% FSR
			−16		+16	mV
Leakage Current					1.0	µA
CURRENT SENSE 1 (CS1 PIN)						
Input Voltage Range	V_{IN}		0	1	1.4	V
Usable Input Voltage Range			0		1.3	V
ADC Clock Frequency				1.56		MHz
Register Update Rate				10		ms
Current Sense Measurement Accuracy		Factory trimmed at 0.7 V; tested under dc input conditions				
		10% to 50% of usable input voltage range	−3.0		+3.0	% FSR
			−41.4		+41.4	mV
		0% to 100% of usable input voltage range	−6.0		+3.0	% FSR
			−84		+42	mV
		40% to 60% of usable input voltage range	−1.0		+1.0	% FSR
Current Sense Measurement Resolution				12		Bits
CS1 Fast OCP Threshold			1.175	1.2	1.216	V
CS1 Fast OCP Speed				80	100	ns
CS1 Accurate OCP DC Accuracy		10% to 90% of usable input voltage range	−2.0		+2.0	% FSR
			−28		+28	mV
CS1 Accurate OCP Speed				2.62	5.24	ms
Leakage Current				0.8	1.1	µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENT SENSE 2 (CS2+, CS2− PINS)						
Input Voltage Range	V_{IN}	Differential voltage from CS2+ to CS2−, LSB = 29.297 µV	0		120	mV
Usable Input Voltage Range			0		110	mV
ADC Clock Frequency				1.56		MHz
Temperature Coefficient						
120 mV Range		0 mV to 100 mV			78	ppm/°C
		0 mV to 50 mV			70	ppm/°C
60 mV Range		0 mV to 50 mV			156	ppm/°C
		0 mV to 25 mV			140	ppm/°C
Current Sense Measurement						
120 mV Setting		0 mV to 110 mV	−2.1		+2.1	% FSR
			−2.52		+2.52	mV
60 mV Setting		0 mV to 55 mV	−4.2		+4.2	% FSR
			−5.04		+5.04	mV
Current Sense Measurement Accuracy		With 0.01% level shifting resistors				
120 mV Setting		0 mV to 100 mV, V_{DD} = 3.3 V	−1.3		+1.3	% FSR
			−1.08		+1.08	mV
60 mV Setting		0 mV to 55 mV, V_{DD} = 3.3 V	−1.8		+1.8	% FSR
			−2.16		+2.16	mV
Current Sense Measurement Resolution				12		Bits
CS2 Accurate OCP Speed				2.62	5.24	ms
Current Sink (High Side)				2		mA
Current Source (Low Side)				200		µA
Common-Mode Voltage at the CS2+ and CS2− Pins		To achieve CS2 measurement accuracy	0.8	1.0	1.4	V
OrFET PROTECTION (CS2+, CS2−)		Low-side and high-side current sensing				
Fast OrFET Accuracy		−3 mV setting	+4.2	−2.6	−9.5	mV
		−6 mV setting	+1.2	−5.9	−12.7	mV
		−9 mV setting	−2.0	−9	−16.2	mV
		−12 mV setting	−5.3	−12.5	−19.4	mV
		−15 mV setting	−8	−15.5	−22	mV
		−18 mV setting	−11.7	−19	−25.9	mV
		−21 mV setting	−14.8	−22.1	−29.2	mV
		−24 mV setting	−17.5	−25.3	−31.5	mV
Fast OrFET Speed		Debounce = 40 ns		110	150	ns
RTD TEMPERATURE SENSE						
ADC Clock Frequency				1.56		MHz
Input Voltage Range		RTD to AGND	0		1.6	V
Usable Input Voltage Range			0		1.3	V
Source Current		Factory trimmed to 46 µA (Register 0x11 set to 0xE6)	44.35	46	47.65	µA
		Current source set to 10 µA	9.25	10.1	10.85	µA
		Current source set to 20 µA	18.35	20.1	21.85	µA
		Current source set to 30 µA	28.45	30.2	31.95	µA
		Current source set to 40 µA	38.45	40.3	41.95	µA
Source Current Fine Setting		See Register 0x11[5:0]		160		nA
RTD ADC						
Register Update Rate				10		ms
Resolution				12		Bits

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Measurement Accuracy		Factory trimmed at 1 V				
		10 mV to 160 mV	−0.5		+0.5	% FSR
			−8		+8	mV
		0% to 100% of usable input voltage range	−3.0		+3.0	% FSR
			−42		+42	mV
Temperature Readings Using Internal Linearization Scheme		RTD source set to 46 µA (Register 0x11 set to 0xE6); NTC R0 = 100 kΩ, 1%; beta = 4250, 1%; R_{EXT} = 16.5 kΩ, 1%				
		25°C to 100°C			7	°C
		100°C to 125°C			5	°C
OTP						
Threshold Accuracy		T = 85°C with 100 kΩ||16.5 kΩ	−0.25		+0.9	% FSR
			−4		+14.4	mV
		T = 100°C with 100 kΩ||16.5 kΩ	−0.5		+1.1	% FSR
			−8		+17.6	mV
Comparator Speed				10.5		ms
OTP Threshold Hysteresis				16		mV
PGOOD1, PGOOD2, SHAREo PINS		Open-drain outputs				
Output Low Voltage	V_{OL}				0.4	V
PSON, SHAREi PINS		Digital inputs				
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		V_{DD} − 0.8			V
Leakage Current					1.0	µA
FLAGIN PIN		Digital input				
Input Low Voltage	V_{IL}				0.4	V
Input High Voltage	V_{IH}		V_{DD} − 0.8			V
Propagation Delay		Does not include debounce time (Register 0x0A[3] = 1); flag action set to disable PSU		200		ns
Leakage Current					1.0	µA
GATE PIN						
Output Low Voltage	V_{OL}				0.4	V
Output High Voltage	V_{OH}		V_{DD} − 0.4			V
SDA/SCL PINS		V_{DD} = 3.3 V				
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		V_{DD} − 0.8			V
Output Low Voltage	V_{OL}				0.4	V
Leakage Current					1.0	µA
SERIAL BUS TIMING		See Figure 2				
Clock Operating Frequency			10	100	400	kHz
Bus-Free Time	t_{BUF}	Between stop and start conditions	1.3			µs
Start Hold Time	$t_{HD;STA}$	Hold time after (repeated) start condition; after this period, the first clock is generated	0.6			µs
Start Setup Time	$t_{SU;STA}$	Repeated start condition setup time	0.6			µs
Stop Setup Time	$t_{SU;STO}$		0.6			µs
SDA Setup Time	$t_{SU;DAT}$		100			ns
SDA Hold Time	$t_{HD;DAT}$	For readback	125			ns
		For write	300			ns
SCL Low Timeout	$t_{TIMEOUT}$		25		35	ms
SCL Low Period	t_{LOW}		1.3			µs
SCL High Period	t_{HIGH}		0.6			µs
Clock Low Extend Time	$t_{LO;SEXT}$				25	ms
SCL, SDA Fall Time	t_F		20		300	ns
SCL, SDA Rise Time	t_R		20		300	ns

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
EEPROM RELIABILITY						
Endurance[1]		T_J = 85°C	10,000			Cycles
		T_J = 125°C	1000			Cycles
Data Retention[2]		T_J = 85°C	20			Years
		T_J = 125°C	10			Years

[1] Endurance is qualified as per JEDEC Standard 22, Method A117, and is measured at −40°C, +25°C, +85°C, and +125°C. Endurance conditions are subject to change pending EEPROM qualification.
[2] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22, Method A117. The derated retention lifetime equivalent at junction temperature T_J = 125°C is 2.87 years and is subject to change pending EEPROM qualification.

Timing Diagram

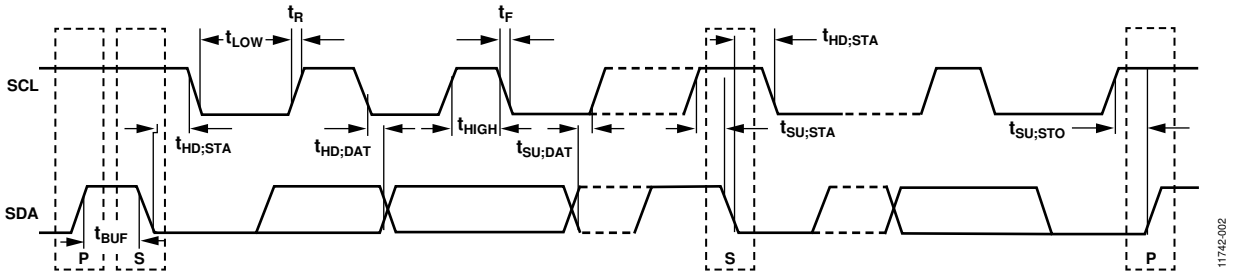

Figure 2. Serial Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (Continuous), V_{DD}	4.2 V
Digital Pins: OUTA, OUTB, OUTC, OUTD, OUTAUX, SR1, SR2, GATE, PGOOD1, PGOOD2	−0.3 V to V_{DD} + 0.3 V
VS3− to PGND, AGND, DGND	−0.3 V to +0.3 V
VS1, VS2, VS3+, ACSNS	−0.3 V to V_{DD} + 0.3 V
RTD, ADD	−0.3 V to V_{DD} + 0.3 V
CS1, CS2+, CS2−	−0.3 V to V_{DD} + 0.3 V
FLAGIN, PSON	−0.3 V to V_{DD} + 0.3 V
SDA, SCL	−0.3 V to V_{DD} + 0.3 V
SHAREo, SHAREi	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS-Compliant Assemblies (20 sec to 40 sec)	260°C
ESD Charged Device Model	1.5 kV
ESD Human Body Model	3.5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP	44.4	6.4	°C/W

SOLDERING

It is important to follow the correct guidelines when laying out the PCB footprint for the ADP1046AW and when soldering the part onto the PCB. For detailed information about these guidelines, see the AN-772 Application Note.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

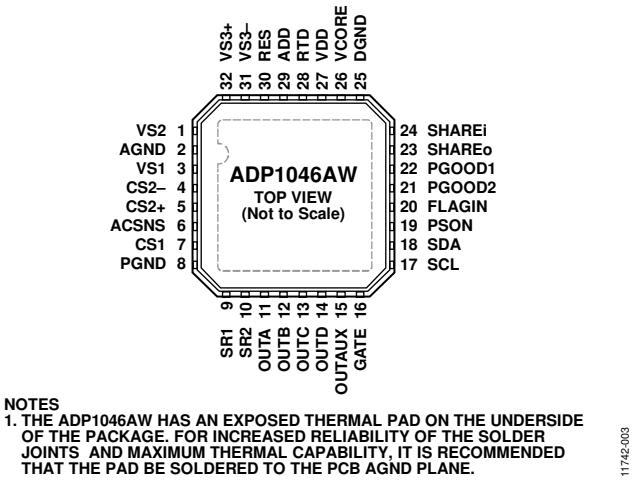

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VS2	Power Supply Output Voltage Sense Input. This signal is referenced to PGND and is the input to a low frequency Σ-Δ ADC. Nominal voltage at this pin should be 1 V. The resistor divider on this input must have a tolerance specification of 0.5% or better to allow for trimming.
2	AGND	Analog Ground. This pin is the ground for the analog circuitry and the return for the VDD pin of the ADP1046AW.
3	VS1	Local Output Voltage Sense Input. This signal is referenced to PGND. Nominal voltage at this pin should be 1 V. The resistor divider on this input must have a tolerance specification of 0.5% or better to allow for trimming.
4	CS2–	Inverting Differential Current Sense Input. Nominal voltage at this pin should be 1 V for best operation. When using low-side current sensing, place a 5 kΩ resistor between the sense resistor and this pin. When using high-side current sensing in a 12 V application, place a 5.5 kΩ resistor between the sense resistor and this pin. When using high-side current sensing with a voltage other than 12 V, use the following formula to calculate the resistor value: $R = (V_{OUT} - 1)/2$ mA. A 0.1% resistor must be used to connect this circuit. If this pin is not used, connect it to PGND and set CS2± to high-side current sense mode (set Bit 2 of Register 0x27). It is recommended that a 500 pF to 1000 pF capacitor be connected either across the resistor or from this pin to AGND.
5	CS2+	Noninverting Differential Current Sense Input. Nominal voltage at this pin should be 1 V for best operation. When using low-side current sensing, place a 5 kΩ resistor between the sense resistor and this pin. When using high-side current sensing in a 12 V application, place a 5.5 kΩ resistor between the sense resistor and this pin. When using high-side current sensing with a voltage other than 12 V, use the following formula to calculate the resistor value: $R = (V_{OUT} - 1)/2$ mA. A 0.1% resistor must be used to connect this circuit. If this pin is not used, connect it to PGND and set CS2± to high-side current sense mode (set Bit 2 of Register 0x27). It is recommended that a 500 pF to 1000 pF capacitor be connected either across the resistor or from this pin to AGND.
6	ACSNS	AC Sense Input. This input is connected upstream of the main output inductor through a resistor divider network. The nominal voltage for this circuit is 0.45 V. This pin is also connected to the voltage feedforward ADC (nominal voltage 1 V). This signal is referenced to PGND.
7	CS1	Primary Side Current Sense Input. This pin is connected to the primary side current sensing ADC and to the fast OCP comparator. This signal is referenced to PGND. The resistors on this input must have a tolerance specification of 0.5% or better to allow for trimming. If this pin is not used, connect it to PGND.
8	PGND	Power Ground. This pin is the ground connection for the main power rail of the power supply and is the reference for all voltage and current sensing other than CS2± and VS3±. Star connect to AGND.
9	SR1	Synchronous Rectifier Output. This PWM output connects to the input of a FET driver. This signal is referenced to AGND. This pin can be disabled when not in use.
10	SR2	Synchronous Rectifier Output. This PWM output connects to the input of a FET driver. This signal is referenced to AGND. This pin can be disabled when not in use.
11	OUTA	PWM Output for Primary Side Switch. This signal is referenced to AGND. This pin can be disabled when not in use.
12	OUTB	PWM Output for Primary Side Switch. This signal is referenced to AGND. This pin can be disabled when not in use.
13	OUTC	PWM Output for Primary Side Switch. This signal is referenced to AGND. This pin can be disabled when not in use.

Pin No.	Mnemonic	Description
14	OUTD	PWM Output for Primary Side Switch. This signal is referenced to AGND. This pin can be disabled when not in use.
15	OUTAUX	Auxiliary PWM Output. This signal is referenced to AGND. This pin can be disabled when not in use.
16	GATE	OrFET Gate Drive Output. This signal is referenced to AGND. If this pin is not used, leave it floating.
17	SCL	I^2C Serial Clock Input. This signal is referenced to AGND.
18	SDA	I^2C Serial Data Input and Output (Open Drain). This signal is referenced to AGND.
19	PSON	Power Supply On Input. This signal is referenced to AGND. This pin is the hardware PSON control signal. It is recommended that a 1 nF capacitor be connected from the PSON pin to AGND for noise debouncing and decoupling.
20	FLAGIN	Flag Input. An external signal can be input at this pin to generate a flag condition.
21	PGOOD2	Power-Good Output (Open Drain). This signal is referenced to AGND. This pin is controlled by the PGOOD2 flag. This pin is set by a programmable combination of internal flags. If this pin is not used, connect it to AGND.
22	PGOOD1	Power-Good Output (Open Drain). This signal is referenced to AGND. This pin is controlled by the PGOOD1 flag. This pin is set by a programmable combination of internal flags. If this pin is not used, connect it to AGND.
23	SHAREo	Share Bus Output Voltage Pin. Connect this pin to 3.3 V through a pull-up resistor (typically 2.2 kΩ). When configured for a digital share bus, this pin is a digital output. This signal is referenced to AGND. If this pin is not used, connect it to AGND.
24	SHAREi	Share Bus Feedback Pin. Connect this pin to the SHAREo pin. This signal is referenced to AGND. If this pin is not used, connect it to AGND.
25	DGND	Digital Ground. This pin is the ground reference for the digital circuitry of the ADP1046AW. Star connect to AGND.
26	VCORE	Output of the 2.5 V Regulator. Connect a decoupling capacitor of at least 330 nF (1 µF maximum) from this pin to DGND as close to the IC as possible to minimize PCB trace length. It is recommended that the VCORE pin not be used as a reference or to generate other logic levels using resistive dividers.
27	VDD	Positive Supply Input. This signal is referenced to AGND. Connect a 4.7 µF decoupling capacitor from this pin to AGND as close to the IC as possible to minimize PCB trace length.
28	RTD	Thermistor Input. Place a thermistor (100 kΩ, 1%; beta = 4250, 1%) in parallel with a 16.5 kΩ, 1% resistor. This pin is referenced to AGND. If this pin is not used, connect it to AGND.
29	ADD	Address Select Input. This pin is used to program the I^2C address. Connect a resistor from ADD to AGND. This signal is referenced to AGND.
30	RES	Resistor Input. This pin sets up the internal voltage reference for the ADP1046AW. Connect a 10 kΩ, ±0.1% resistor from RES to AGND. This signal is referenced to AGND.
31	VS3−	Inverting Remote Voltage Sense Input. There should be a low ohmic connection to AGND. The resistor divider on this input must have a tolerance specification of 0.5% or better to allow for trimming. Connect a 0.1 µF capacitor from VS3− to AGND.
32	VS3+	Noninverting Remote Voltage Sense Input. This signal is referenced to VS3−, and the nominal input voltage at this pin is 1 V. The resistor divider on this input must have a tolerance specification of 0.5% or better to allow for trimming. This pin is the input to the high frequency Δ-Σ ADC.
	EP	Exposed Pad. The ADP1046AW has an exposed thermal pad on the underside of the package. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the PCB AGND plane.

TYPICAL PERFORMANCE CHARACTERISTICS

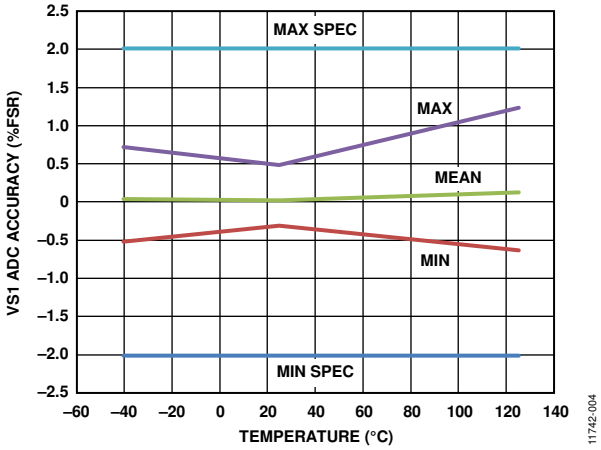

Figure 4. VS1 ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

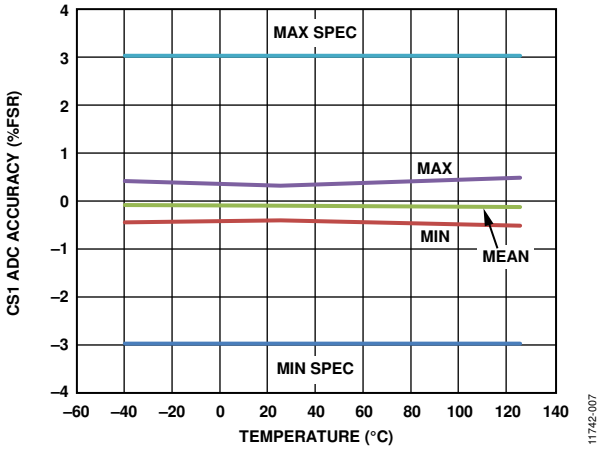

Figure 7. CS1 ADC Accuracy vs. Temperature (from 10% to 50% of FSR)

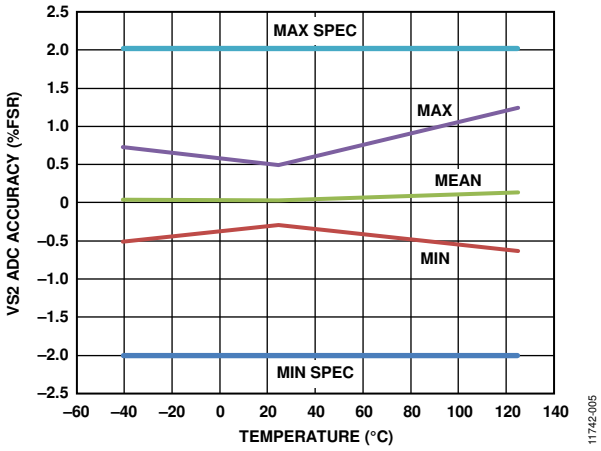

Figure 5. VS2 ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

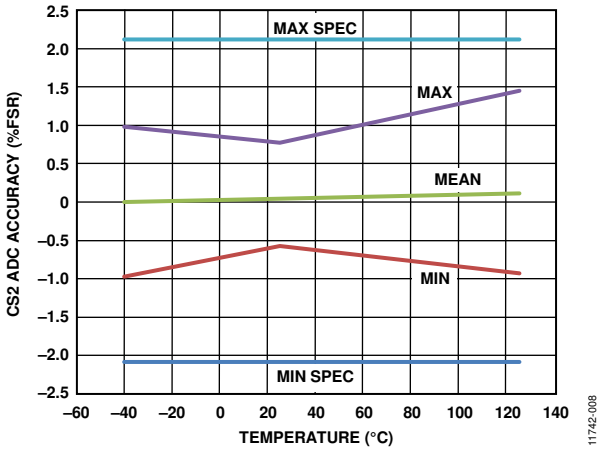

Figure 8. CS2 ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

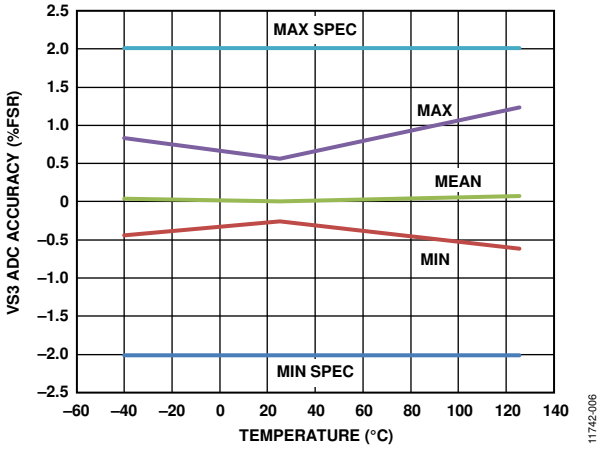

Figure 6. VS3 ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

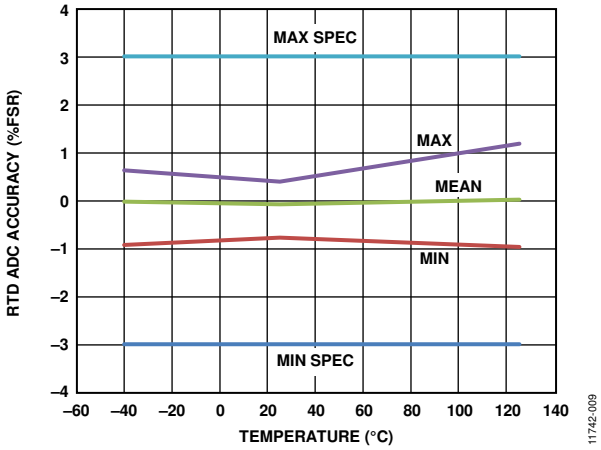

Figure 9. RTD ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

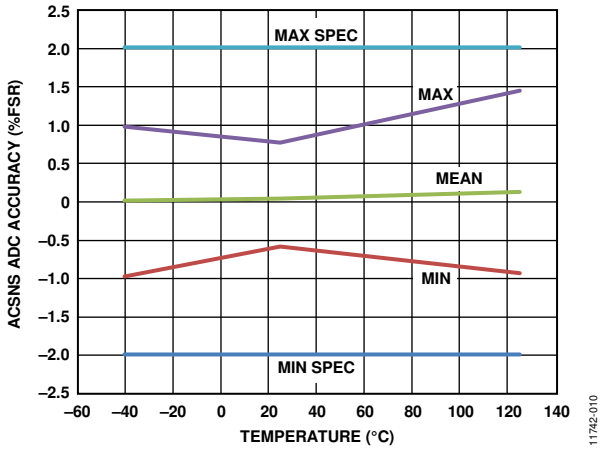

Figure 10. ACSNS ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

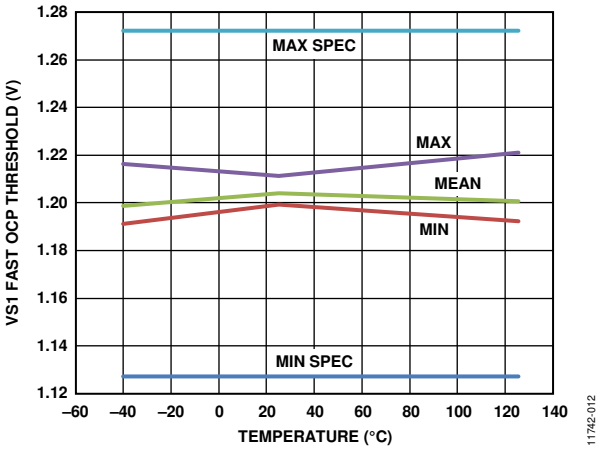

Figure 12. VS1 Fast OCP Threshold vs. Temperature

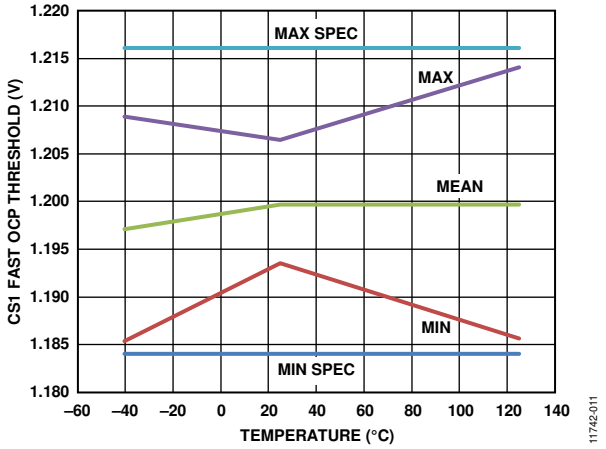

Figure 11. CS1 Fast OCP Threshold vs. Temperature

THEORY OF OPERATION

The ADP1046AW is a secondary side controller for switch mode power supplies. It is designed for use in isolated redundant applications. The ADP1046AW integrates the typical functions that are needed to control a power supply, such as

- Output voltage sense and feedback
- Voltage line feedforward control
- Digital loop filter compensation
- PWM generation
- Current sharing
- Current, voltage, and temperature sense
- OrFET control
- Housekeeping and I²C interface
- Calibration and trimming

The main function of controlling the output voltage is performed using the feedback ADCs, the digital loop filter, and the PWM block.

The feedback ADCs use a multipath approach (patent pending). The ADP1046AW combines a high speed, low resolution (fast and coarse) ADC with a low speed, high resolution (slow and accurate) ADC. Loop compensation is implemented using the digital filter. This proportional, integral, derivative (PID) filter is implemented in the digital domain to allow easy programming of filter characteristics, which is of great value in customizing and debugging designs.

The PWM block generates up to seven programmable PWM outputs for control of FET drivers and synchronous rectification FET drivers. This programmability allows many traditional and unique switching topologies to be realized.

A current share bus interface is provided for paralleling multiple power supplies. The ADP1046AW also has hot-swap OrFET sense and control for N + 1 redundant power supplies.

Conventional power supply housekeeping features, such as remote and local voltage sense and primary and secondary side current sense, are included. An extensive set of protections is offered, including overvoltage protection (OVP), overcurrent protection (OCP), overtemperature protection (OTP), undervoltage protection (UVP), ground continuity monitoring (voltage continuity), and ac sense.

All these features are programmable through the I²C bus interface. This bus interface is also used to calibrate the power supply. Other information that is useful for power monitoring, such as input current, output current, and fault flags, is also available through the I²C bus interface.

The internal EEPROM can store all programmed values and allows standalone control without a microcontroller. A free, downloadable GUI is available and provides all the necessary software to program the ADP1046AW. To obtain the latest software and a user guide, visit http://www.analog.com/digitalpower.

The ADP1046AW operates from a single 3.3 V supply and is specified from −40°C to +125°C.

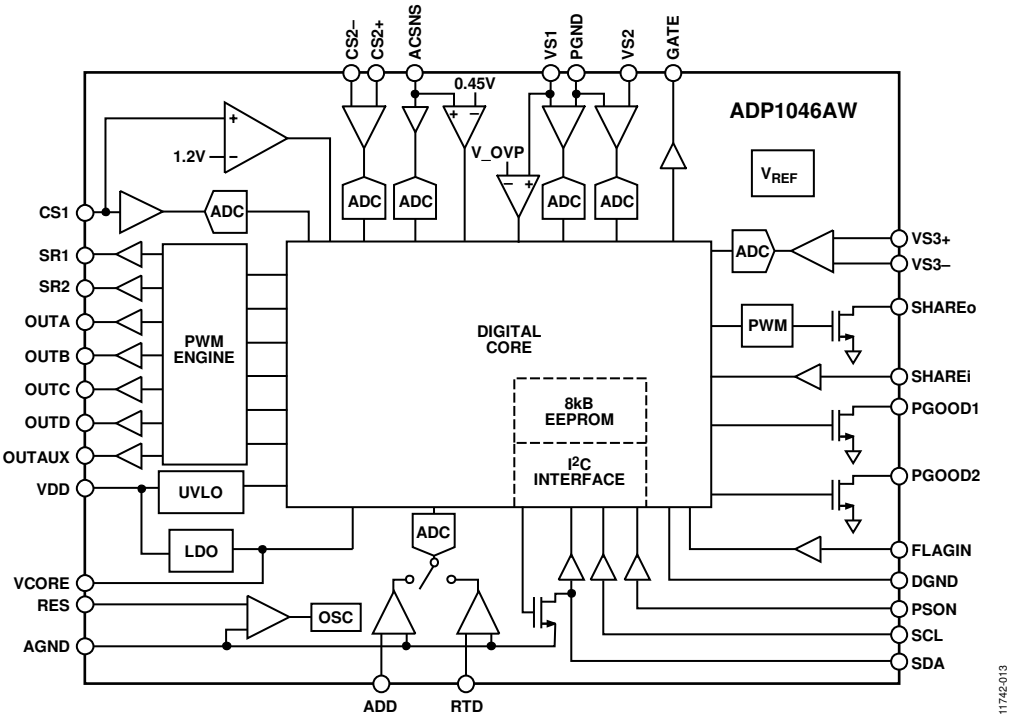

Figure 13. Simplified Block Diagram

CURRENT SENSE

The ADP1046AW has two current sense inputs: CS1 and CS2±. These inputs sense, protect, and control the primary input current, secondary output current, and the share bus information. They can be calibrated to reduce errors due to external components.

CS1 Operation (CS1)

CS1 is typically used for the monitoring and protection of the primary side current, which is commonly sensed using a current transformer (CT). The input signal at the CS1 pin is fed into an ADC for current monitoring. The range of the ADC is 0 V to 1.4 V. The input signal is also fed into a comparator for pulse-by-pulse OCP protection. The typical configuration for the CS1 current sense is shown in Figure 14.

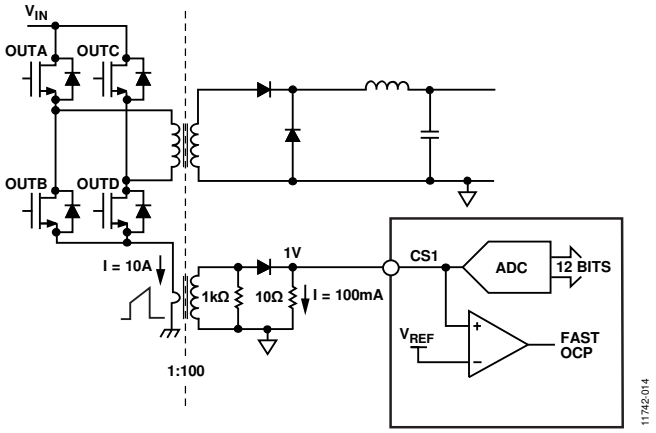

Figure 14. Current Sense 1 (CS1) Operation

The CS1 ADC is used to measure the average value of the primary current; the reading is averaged every 2.62 ms in an asynchronous fashion to make fault decisions. The ADP1046AW also writes the 12-bit CS1 reading every 10 ms to Register 0x13.

The fast OCP comparator is used to limit the instantaneous primary current within each switching cycle and has a nominal threshold of 1.2 V.

Various thresholds and limits can be set for CS1, as described in the Current Sense and Current Limit Registers section.

CS2 Operation (CS2+, CS2–)

CS2+ and CS2– are differential inputs used for the monitoring and protection of the secondary side current. The full-scale range of the CS2 ADC is programmable to 60 mV or 120 mV. The differential inputs are fed into an ADC through a pair of external resistors that provide the necessary level shifting. The device pins, CS2+ and CS2–, are internally regulated to approximately 1 V by internal current sources.

When using low-side current sensing, the current sources are 200 µA; therefore, the required resistor value is 1 V/200 µA = 5 kΩ. When using high-side current sensing, the current sources are 2 mA; therefore, the resistor value required is (V_{OUT} – 1 V)/2 mA. In the case of V_{OUT} = 12 V, the required resistor value is 5.5 kΩ.

Typical configurations are shown in Figure 15 and Figure 16. Various thresholds and limits can be set for CS2±, such as OCP. These thresholds and limits are described in the Current Sense and Current Limit Registers section.

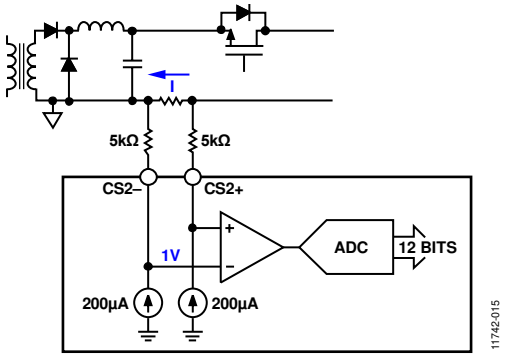

Figure 15. Low-Side Resistive Current Sense (Recommended)

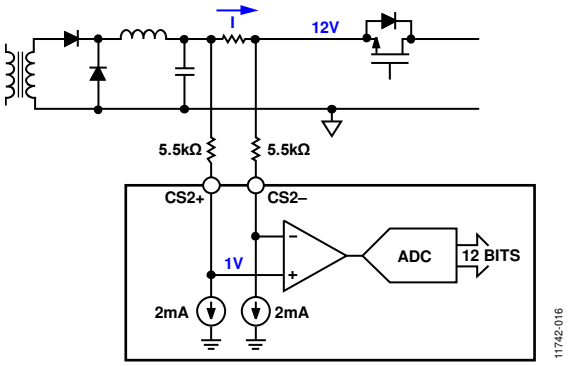

Figure 16. High-Side Resistive Current Sense

When the CS2+ and CS2– inputs are not in use, connect them directly to PGND, and set CS2± to high-side current sense mode (Register 0x27[2] = 1).

The CS2 ADC is used to measure the CS2 current; the reading is averaged every 2.62 ms in an asynchronous fashion. This averaged reading is used to make fault decisions, such as the CS2 OCP fault. The ADP1046AW also writes the 12-bit CS2 reading every 10 ms to Register 0x18.

VOLTAGE SENSE AND CONTROL LOOP

Multiple voltage sense inputs on the ADP1046AW are used for the monitoring, control, and protection of the power supply output. This information is available through the I²C interface. All voltage sense points can be calibrated digitally to minimize errors due to external components. This calibration can be performed in the production environment, and the settings can be stored in the EEPROM of the ADP1046AW (see the Power Supply Calibration and Trim section for more information).

For voltage monitoring, the VS1, VS2, and VS3 voltage value registers (Register 0x15, Register 0x16, and Register 0x17, respectively) are updated every 10 ms. The ADP1046AW stores every ADC sample for 10 ms and then outputs the average value at the end of the 10 ms period. Therefore, if these registers are read at least every 10 ms, a true average value is read.

The ADP1046AW uses two separate sensing points: VS1 and VS3±, depending on the condition of the OrFET. When the OrFET is turned off, the control loop is regulated via VS1; when the OrFET is turned on, the control loop is regulated via the differential sensing on VS3±. This sensing mechanism effectively performs a local and remote voltage sense.

The control loop of the ADP1046AW features a patented multipath architecture. The output voltage is converted simultaneously by two ADCs: a high accuracy ADC and a high speed ADC. The complete signal is reconstructed and processed in the digital filter to provide a high performance, cost competitive solution.

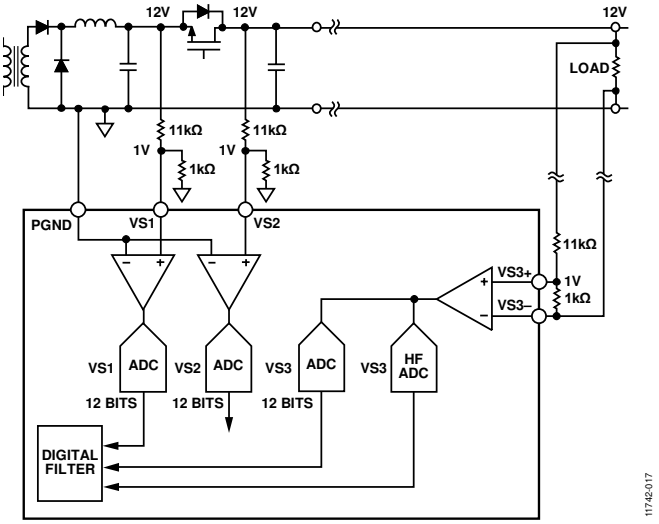

Figure 17. Voltage Sense Configuration

ADCs

Two kinds of Σ-Δ ADCs are used in the feedback loop of the ADP1046AW: a low frequency (LF) ADC that runs at 1.56 MHz and a high frequency (HF) ADC that runs at 25 MHz.

Σ-Δ ADCs have a resolution of one bit and operate differently from traditional flash ADCs. The equivalent resolution that can be obtained depends on how long the output bit stream of the Σ-Δ ADC is sampled.

Σ-Δ ADCs also differ from Nyquist rate ADCs in that the quantization noise is not uniform across the frequency spectrum. At lower frequencies, the noise is lower, and at higher frequencies, the noise is higher (see Figure 18).

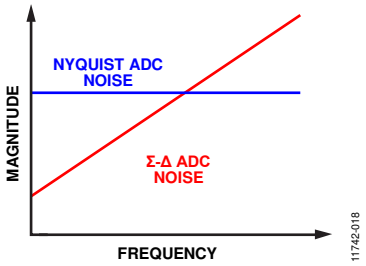

Figure 18. Noise Performance for Nyquist Rate and Σ-Δ ADCs

The low frequency ADC runs at approximately 1.56 MHz. For a specified bandwidth, the equivalent resolution can be calculated as follows:

$$\ln(1.56\ \text{MHz}/BW)/\ln(2) = N\ \text{bits}$$

For example, at a bandwidth of 95 Hz, the equivalent resolution/noise is

$$\ln(1.56\ \text{MHz}/95)/\ln(2) = 14\ \text{bits}$$

At a bandwidth of 1.5 kHz, the equivalent resolution/noise is

$$\ln(1.56\ \text{MHz}/1.5\ \text{kHz})/\ln(2) = 10\ \text{bits}$$

The high frequency ADC has a clock of 25 MHz. It is comb filtered and outputs at the switching frequency (f_{SW}) into the digital filter. The equivalent resolution at some sample frequencies is listed in Table 5.

Table 5. Equivalent Resolutions for High Frequency ADC at Various Switching Frequencies

f_{SW} (kHz)	High Frequency ADC Resolution
48.8	9 bits
97.7	8 bits
195.3	7 bits
390.6	6 bits

The HF ADC has a range of ±30 mV. Using a base switching frequency (f_{SW}) of 100 kHz (8-bit HF ADC resolution), when f_{SW} increases to 200 kHz (7-bit HF ADC resolution), the quantization noise is 0.9375 mV (1 LSB). Increasing f_{SW} to 400 kHz increases the quantization noise to 3.75 mV (1 LSB = 2 × 30 mV/2^6 = 0.9375 mV).

VS1 OPERATION (VS1)

VS1 is used for the monitoring and protection of the power supply voltage at the output of the LC stage, upstream of the OrFET. The VS1 sense point on the power rail needs an external resistor divider to bring the nominal input voltage to 1 V at the VS1 pin (see Figure 17). The resistor divider is necessary because the VS1 ADC input range is 0 V to 1.6 V (12-bit reading). This divided-down signal is internally fed into a low speed Σ-Δ ADC. The output of the VS1 ADC goes to the digital filter and is also updated in Register 0x15 every 10 ms. The VS1 signal is referenced to PGND. When the OrFET is turned off, the power supply is regulated from the VS1 sense point instead of the VS3± sense point.

VS2 OPERATION (VS2)

VS2 is used in conjunction with VS1 to control the OrFET gate drive turn-on. The VS2 sense point on the power rail needs an external resistor divider to bring the nominal common-mode signal to 1 V at the VS2 pin (see Figure 17).

The resistor divider is necessary because the VS2 ADC input range is 0 V to 1.6 V. This divided-down signal is internally fed into the VS2 ADC. The output of the VS2 ADC goes to the VS2 voltage value register (Register 0x16). The VS2 signal is never used for the control loop but is used to control the turn-on and turn-off of the OrFET (see the OrFET Control (GATE Pin) section) as well as the voltage continuity flag. If the OrFET function of the ADP1046AW is not used, it is recommended that the VS2 input be connected directly to PGND. The VS2 value is updated in Register 0x16 every 10 ms.

VS3 OPERATION (VS3+, VS3–)

VS3± is used for the monitoring and protection of the remote load voltage. VS3± is a fully differential input that is the main feedback sense point for the power supply control loop. The VS3± sense point on the power rail needs an external resistor divider to bring the nominal common-mode signal to 1 V at the VS3± pins (see Figure 17). The resistor divider is necessary because the VS3 ADC input range is 0 V to 1.6 V. This divided-down signal is internally fed into a high frequency (HF) ADC. The output of the VS3 ADC goes to the digital filter and is also updated in Register 0x17 every 10 ms. The HF ADC is also the high frequency feedback loop for the power supply.

VOLTAGE LINE FEEDFORWARD AND ACSNS

The ADP1046AW supports voltage line feedforward control to improve line transient performance. The ACSNS value is used to divide the output of the digital filter, and the result is fed into the PWM engine. The input voltage signal can be sensed at the secondary winding of the isolation transformer and must be filtered by an RCD network to eliminate the voltage spike at the switch node (see Figure 19).

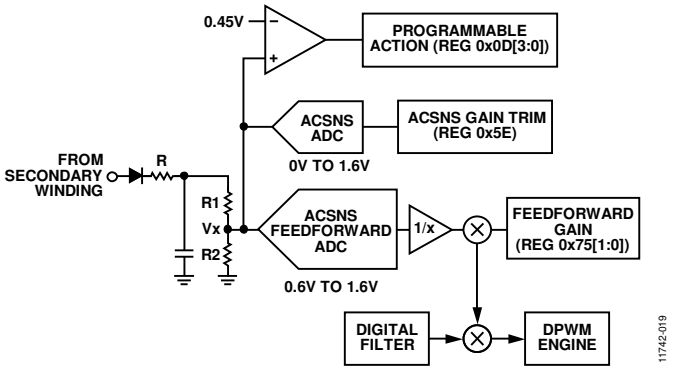

Figure 19. Feedforward Configuration

The ACSNS voltage must be set to 1 V when the nominal input voltage is applied. The ACSNS ADC sampling period is 10 µs; therefore, the decision to modify the PWM outputs based on input voltage is performed at this rate.

The feedforward scheme modifies the modulation value based on the ACSNS voltage. When the ACSNS input is 1 V, the line feedforward has no effect. For example, if the digital filter output remains unchanged and the ACSNS voltage changes to 50% of its original value (still higher than 0.5 V), the modulation of the falling edge of OUTx doubles and vice versa (see Figure 20). The voltage line feedforward function is optional and is programmable using Register 0x75.

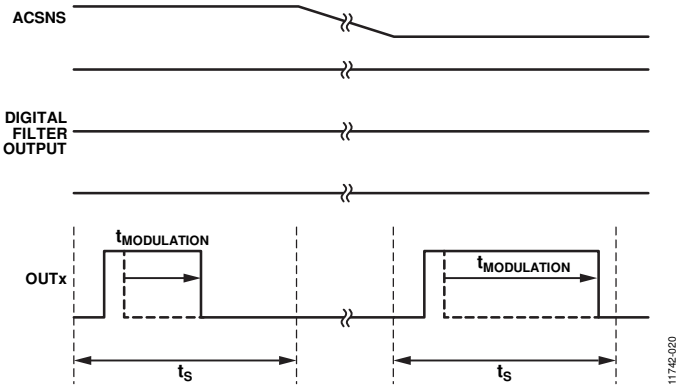

Figure 20. Feedforward Control on Modulation

The ACSNS level comparator is also connected on the same pin and flags an ACSNS fault when the voltage on the pin is below 0.45 V within each switching period. The ACSNS level comparator is used to detect whether the node is switching.

DIGITAL FILTER

The loop response of the power supply can be changed using the internal programmable digital filter. A Type 3 filter architecture has been implemented. To tailor the loop response to the specific application, the low frequency gain, zero location, pole location, and high frequency gain can all be set individually (see the Digital Filter Programming Registers section). It is recommended that the Analog Devices, Inc., software GUI be used to program the filter. The software GUI displays the filter response in Bode plot format and can be used to calculate all stability criteria for the power supply.

From the sensed voltage to the duty cycle, the transfer function of the filter in z-domain is as follows:

$$H(z) = \left(\frac{d}{202.24 \times m} \times \frac{z}{z-1} \right) + \left(\frac{c}{7.68} \times \frac{z-b}{z-a} \right)$$

where:

a = filter_pole_register_value/256.
b = filter_zero_register_value/256.
c = high_frequency_gain_register_value.
d = low_frequency_gain_register_value.
m = 1 when 48.8 kHz ≤ f_{SW} < 97.7 kHz.
m = 2 when 97.7 kHz ≤ f_{SW} < 195.3 kHz.
m = 4 when 195.3 kHz ≤ f_{SW} < 390.6 kHz.
m = 8 when 390.6 kHz ≤ f_{SW}.

f_{SW} is the switching frequency.

To transfer the z-domain value to the s-domain, plug the following bilinear transformation equation into the H(z) equation:

$$z(s) = \frac{2f_{SW} + s}{2f_{SW} - s}$$

The digital filter introduces an extra phase delay element into the control loop. The digital filter circuit sends the duty cycle information to the PWM circuit at the beginning of each switching cycle (unlike an analog controller, which makes decisions on the duty cycle information continuously). Therefore, the extra phase delay for phase margin, Φ, introduced by the filter block is

$$\Phi = 360 \times (f_C/f_{SW})$$

where:
f_C is the crossover frequency.
f_{SW} is the switching frequency.

At one-tenth the switching frequency, the phase delay is 36°. The GUI incorporates this phase delay into its calculations. Note that the GUI does not account for other delays such as gate driver and propagation delays.

Two sets of registers allow for two distinct filter responses. The main filter, called the normal mode filter, is controlled by programming Register 0x60 to Register 0x63. The light load mode filter is controlled by programming Register 0x64 to Register 0x67. The ADP1046AW uses the light load mode filter only when the output current measured on CS2± is below the load current threshold (programmed using Register 0x3B[2:0]).

The Analog Devices software GUI allows the user to program the light load mode filter in the same manner as the normal mode filter. It is recommended that the GUI be used for this purpose.

In addition, during the soft start process, a soft start filter can be used in combination with the normal mode filter and the light load mode filter. The soft start filter is programmed using Register 0x71 to Register 0x74. For more information, see the Soft Start section.

Filter Transitions

To avoid output voltage glitches and provide a seamless transition from one filter to another, the ADP1046AW supports programmable filter transitions. This feature allows a gradual transition from one filter to another. Filter transitions are programmed using Register 0x7A[2:0].

PWM AND SYNCHRONOUS RECTIFIER OUTPUTS (OUTA, OUTB, OUTC, OUTD, OUTAUX, SR1, SR2)

The PWM and SR outputs are used for control of the primary side drivers and the synchronous rectifier drivers. These outputs can be used for several control topologies such as full-bridge, phase-shifted ZVS configurations and interleaved, two switch forward converter configurations. Delays between rising and falling edges can be individually programmed. Special care must be taken to avoid shoot-through and cross-conduction. It is recommended that the Analog Devices software GUI be used to program these outputs. Figure 21 shows an example configuration to drive a full-bridge, phase-shifted topology with synchronous rectification.

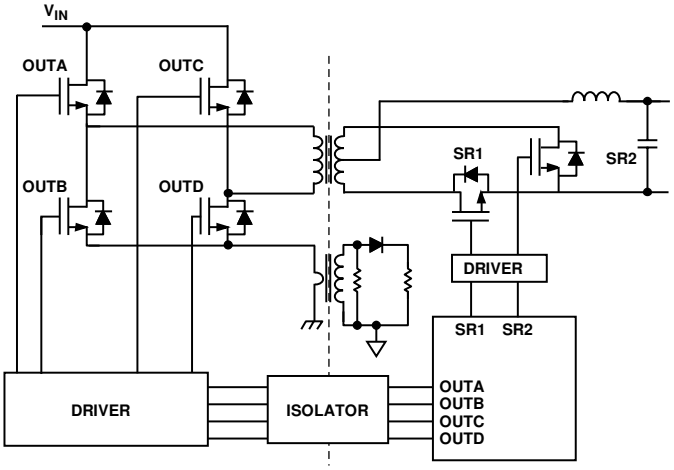

Figure 21. PWM Pin Assignment for Full-Bridge, Phase-Shifted Topology with Synchronous Rectification

The PWM and SR outputs are all synchronized with each other. Therefore, when reprogramming more than one of these outputs, it is important to first update all the registers and then latch the information into the ADP1046AW at the same time. During reprogramming, the outputs are temporarily disabled. A special instruction is sent to the ADP1046AW to ensure that new timing information is programmed simultaneously. This is done by setting Bit 1 in Register 0x7F. It is recommended that PWM outputs be disabled when not in use.

OUTAUX is an additional PWM output pin. OUTAUX allows an extra PWM signal to be generated at a different frequency from the other six PWM outputs. This signal can be used to drive an extra power converter stage, such as a buck controller located in front of a full-bridge converter. OUTAUX can also be used as a clock reference signal.

For more information about the various programmable switching frequencies and PWM timings, see the PWM and Synchronous Rectifier Timing Registers section (Register 0x3F to Register 0x5C).

SYNCHRONOUS RECTIFICATION

SR1 and SR2 are recommended for use as the PWM control signals when using synchronous rectification. These PWM signals can be configured much like the other PWM outputs.

An optional soft start can be applied to the synchronous rectifier PWM outputs. The SR soft start can be programmed using Register 0x54[1:0].

- When SR soft start is disabled (Register 0x54[0] = 0), the SR signals are turned on to their full PWM duty cycle values immediately.
- When SR soft start is enabled (Register 0x54[0] = 1), the SR signals ramp up from zero duty cycle to the desired duty cycle in steps of 40 ns per switching cycle.

The advantage of ramping the SR signals is to minimize the output voltage step that occurs when the SR FETs are turned on without a soft start. The advantage of turning the SR signals completely on immediately is that they can help to minimize the voltage transient caused by a load step.

Using Register 0x54[1], the SR soft start can be programmed to occur only once (the first time that the SR signals are enabled) or every time that the SR signals are enabled, for example, when the system enters or exits light load mode.

When programming the ADP1046AW to use SR soft start, ensure correct operation of this function by setting the falling edge of SR1 (t_{10}) to a lower value than the rising edge of SR1 (t_9) and by setting the falling edge of SR2 (t_{12}) to a lower value than the rising edge of SR2 (t_{11}). SR soft start can also be disabled by setting Register 0x0F[7] = 1.

SYNCHRONOUS RECTIFIER (SR) DELAY

The ADP1046AW is well suited for dc-to-dc converters in isolated topologies. Every time a PWM signal crosses the isolation barrier an additional propagation delay is added due to the isolating components. The ADP1046AW allows programming of an adjustable delay (0 ns to 315 ns in steps of 5 ns) using Register 0x79[5:0]. This delay moves both SR1 and SR2 later in time to compensate for the added delay due to the isolating components (see Figure 57). In this way, the edges of all PWM outputs can be aligned, and the SR delay can be applied separately as a constant dead time.

LIGHT LOAD MODE

The ADP1046AW can be configured to disable PWM outputs under light load conditions based on the value of CS2. Register 0x3B and Register 0x7D are used to program the light load mode thresholds for turn-off and turn-on of SR1, SR2, and other PWM outputs. Below the light load threshold programmed in Register 0x3B, the SR outputs are disabled; the user can also program any of the other PWM outputs to shut down below this threshold. Light load mode allows the ADP1046AW to be used with interleaved topologies that incorporate automatic phase shedding at light load.

To prevent the system from oscillating between light load and normal modes due to the thresholds being programmed too close to each other, a programmable debounce is provided in Register 0x7D[5:4]. This debounce prevents the part from changing state within the programmed interval.

The speed of the SR enable is programmable from 37.5 µs to 300 µs in four discrete steps using Register 0x7D[3:2]. This ensures that, in case of a load step, the SR signals (and any other PWM outputs that are temporarily disabled) can be turned on quickly enough to prevent damage to the FETs that they are controlling.

The light load mode digital filter is also used during light load mode.

MODULATION LIMIT

The modulation limit register (Register 0x2E) can be programmed to apply a maximum duty cycle modulation limit to any PWM signal, thus limiting the modulation range of any PWM output. When modulation is enabled, the maximum modulation limit is applied to all PWM outputs collectively. As shown in Figure 22, this limit is the maximum time variation for the modulated edges from the default timing, following the configured modulation direction. There is no minimum duty cycle limit setting. Therefore, the user must set the rising edges and falling edges based on the case with the least modulation.

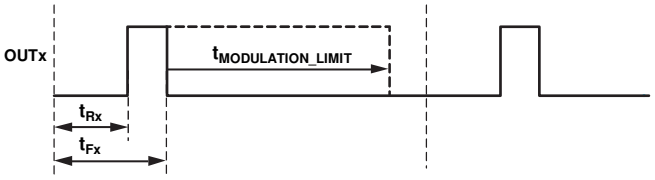

Figure 22. Modulation Limit Settings

Each LSB in Register 0x2E corresponds to a different time step size, depending on the switching frequency (see Table 46). The modulated edges cannot extend beyond one switching cycle.

The GUI provided with the ADP1046AW is recommended for programming this feature (see Figure 23).

Figure 23. Setting Modulation Limits (Modulation Range Shown by Arrows)

SOFT START

The turning on and off of the ADP1046AW is controlled by the hardware PSON pin and/or the software PSON register, depending on the configured settings in Register 0x2C. When the user turns on the power supply (enables PSON), the following soft start procedure occurs (see Figure 24).

1. The PSON signal is enabled at Time t_0. If the part is programmed to be always on (Register 0x2C[7:6] = 00), PSON is enabled as soon as VCORE is above UVLO.
2. The ADP1046AW waits for the programmed PS_ON delay (set in Register 0x2C[4:3]).
3. The soft start begins to ramp up the internal digital reference. The total duration of the soft start ramp is programmable from 5 ms to 100 ms using Register 0x5F[7:5].
4. If the soft start from precharge function is enabled (Register 0x5F[4] = 1), the soft start ramp starts from the value of the output voltage sensed on VS1 or VS3± (depending on the OrFET status), and the soft start ramp time is reduced proportionally. If the soft start from precharge function is disabled, the soft start ramp time is the programmed value in Register 0x5F[7:5].
5. When the power supply voltage exceeds the VS1 undervoltage protection (UVP) limit (set in Register 0x34[6:0]), the UVP flag is reset.
6. The OrFET is turned on as soon as the OrFET enable threshold is met. (The OrFET enable threshold is programmed in Register 0x30[6:5].) The regulation point is switched from VS1 to VS3±.
7. If no other fault conditions are present, the PGOODx signals wait for the programmed debounce time (set in Register 0x2D[7:4]) and are then enabled. The soft start flag must be unmasked in Register 0x7B and Register 0x7C (Bit 7 must be set to 0).
8. If no OrFET is used, the power supply must be configured to regulate using VS3 at all times (Register 0x33[2] = 1). VS2 can be used as a secondary OVP mechanism.

Fault Condition During Soft Start

If a fault condition occurs during soft start, the controller responds as programmed unless the flag is blanked. Flag blanking during soft start is programmed in Register 0x0F. The ACSNS flag is always blanked during soft start. The OTP, FLAGIN, OVP, and OCP fault flags can be blanked during soft start by setting the appropriate bits in Register 0x0F.

The UVP fault is blanked only for the debounce time during soft start. Therefore, if the soft start period exceeds the debounce time, the UVP fault is triggered and stored in the first flag ID register (Register 0x10). A read of the latched fault registers and the first flag ID register clears the falsely triggered UVP condition.

Digital Compensation Filters During Soft Start

The ADP1046AW has a dedicated soft start filter (SSF) that can be used to fine-tune and optimize the dynamic response during the output voltage ramp-up.

Before it ramps up the internal reference after the PSON signal is enabled, the ADP1046AW evaluates whether the OrFET should be turned on or off by looking at the difference between VS1 and VS2. This step is done to determine whether the regulation point should be VS1 or VS3± (see Figure 24).

- If the regulation point is VS1, the soft start filter is used by default during the ramp-up. At the end of the soft start ramp, the part switches to the normal mode filter (NMF).
- If the regulation point is VS3±, the part starts the ramp using the normal mode filter (NMF).

In both cases, after the voltage reaches 12.5% of the nominal output voltage value, the load current is evaluated.

- If the load current is below the light load mode threshold, the part switches to the light load mode filter (LLF).
- If the load current is above the light load mode threshold, the normal mode filter is used until the end of the soft start ramp, even if the system subsequently enters light load mode based on a change to the load current.

Register 0x2C can be programmed to configure the use of the different filters during soft start as follows:

- Force soft start filter (Bit 0). This option forces the part to use the soft start filter even when the regulation point is VS3. In some cases, this option allows better fine-tuning of the ramp-up voltage. This option can also be selected when an OrFET is not used.
- Disable light load mode during soft start (Bit 1). This option prevents the use of the light load mode filter during soft start, even if the light load condition is met. The light load mode filter is available for use after the end of the soft start ramp.

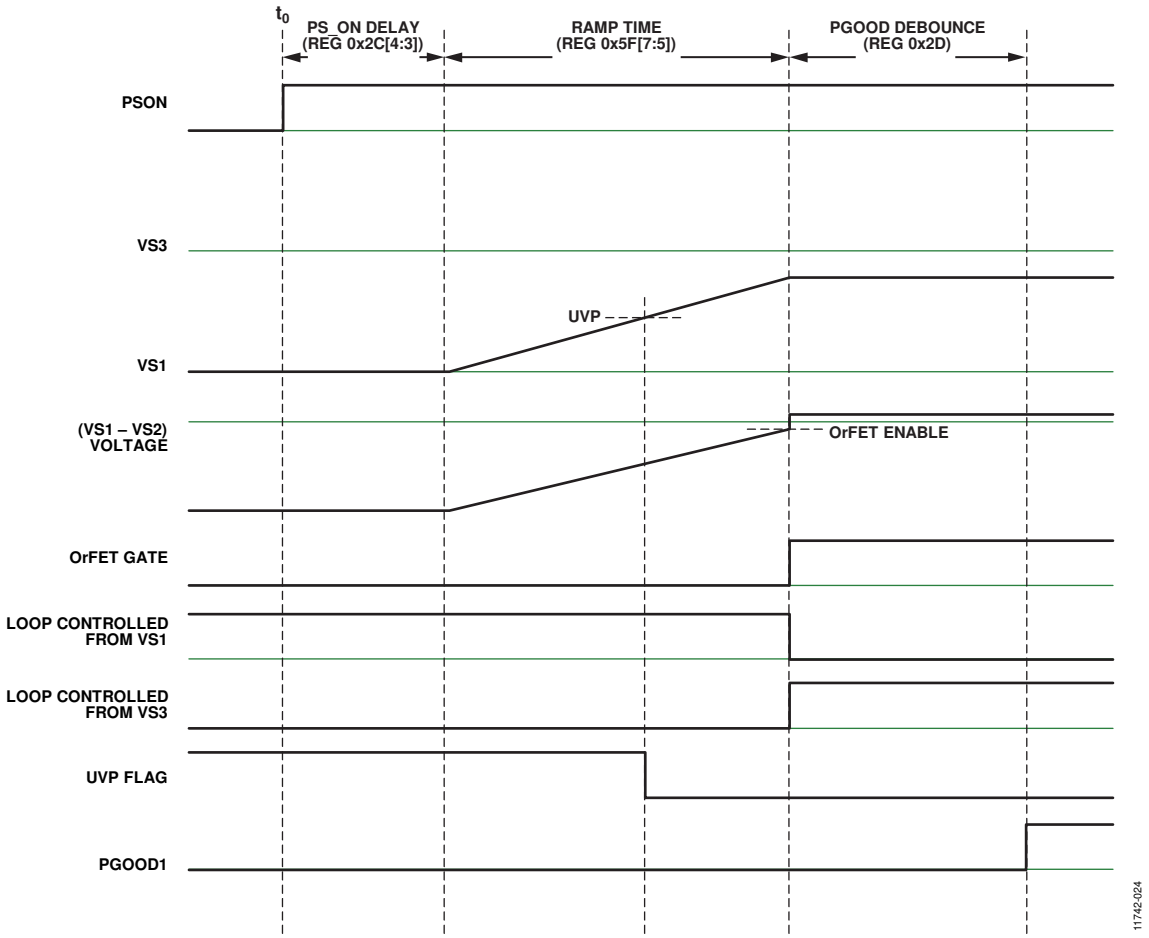

Figure 24. Soft Start Timing Diagram

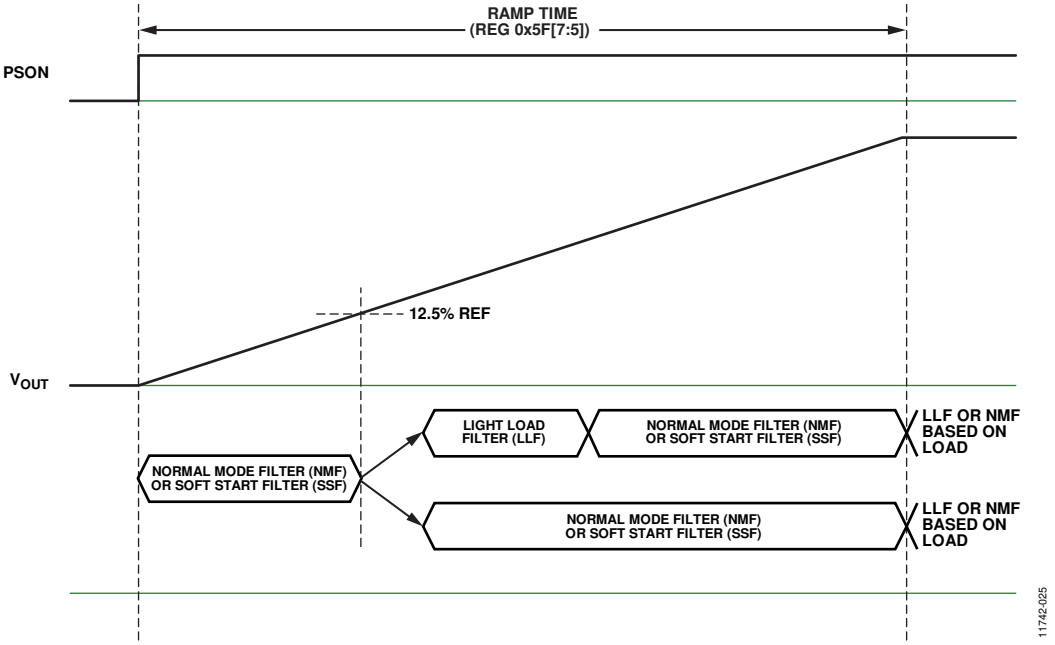

Figure 25. Filter Sequencing at Startup

OrFET CONTROL (GATE PIN)

The GATE control signal drives an external OrFET. The OrFET is used in redundant systems to protect against power flow into the power supply from the output terminals of another supply. This ensures that power flows only out of the power supply and that the unit can be hot-swapped.

The GATE pin is a totem-pole output and does not require a pull-up resistor. The GATE pin polarity can be programmed via Register 0x2D[1] to be active high or active low. The GATE output is CMOS level (0 V to 3.3 V). An external driver is required to turn the OrFET on or off.

OrFET Turn-On

The turn-on process for the OrFET is controlled by the voltage difference between VS1 and VS2. For this reason, the VS1 and VS2 readings must be correctly calibrated for the OrFET function to perform properly.

The OrFET turn-on circuit detects the voltage difference between VS1 and VS2 (see Figure 26). When the forward voltage drop from VS1 to VS2 is greater than the programmable OrFET enable threshold set in Register 0x30[6:5], the OrFET is enabled. The OrFET enable threshold can be set to 0%, −0.5%, −1%, or −2% of the nominal output voltage.

OrFET Turn-Off

The OrFET can be turned off by three methods:

- Fault flag. Any flag in a fault configuration register (Register 0x08 to Register 0x0D) can be programmed with an action to turn off the OrFET. The OrFET is kept off for as long as the flag is set.
- OrFET programmable comparator. If the reverse voltage present on CS2± exceeds the analog comparator threshold programmed in Register 0x30[4:2], the OrFET is turned off. This comparator can be disabled using Register 0x30[0].
- GATE signal disable. When Register 0x5D[0] = 1, the GATE signal is disabled and has no effect on the VSx feedback point.

OrFET GATE Control and Regulation Points

The GATE signal is enabled when the threshold configured in Register 0x30[6:5]) is met. The GATE signal controls a very important function of output voltage regulation: the control loop sensing point.

- When the GATE signal is disabled, the OrFET is turned off and the voltage regulation sensing point is VS1.
- When the GATE signal is enabled, the OrFET is turned on and the voltage regulation sensing point is VS3±.

Recommended Setup for a 12 V Application

In normal operating mode, follow this procedure:

- When 12 V < V_{OUT} < OVP, use the fast OrFET control circuit to turn off the OrFET.
- When V_{OUT} > OVP, use load OVP to turn off the OrFET.

In light load mode, follow this procedure:

- When 12 V < V_{OUT} < OVP, use ACSNS to turn off the OrFET.
- When V_{OUT} > OVP, use load OVP to turn off the OrFET.

In a 12 V application, when an internal short circuit occurs, use CS1 OCP or VS1 UVP to shut down the unit and restart it.

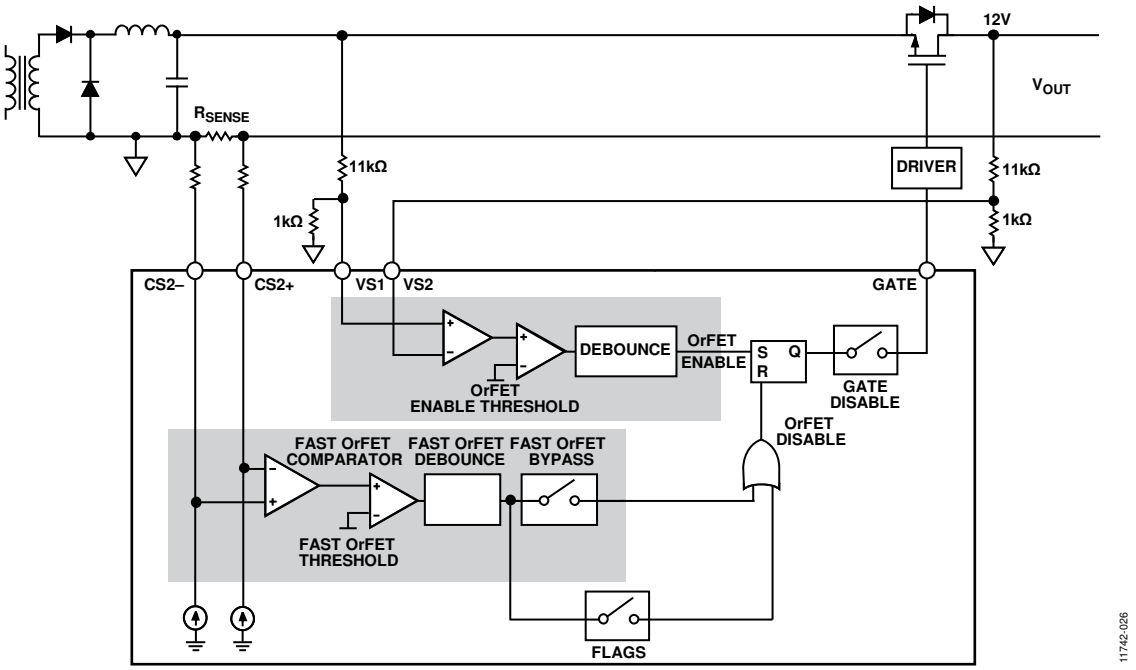

Figure 26. OrFET Control Circuit Detailed Internal Diagram

OrFET Operation Examples

Hot Plug into a Live Bus

A new PSU is plugged into a live 12 V bus (yellow). The internal voltage, VS1 (red), is ramped up before the OrFET is turned on. After the OrFET is turned on (green), current in the new PSU begins to flow to the load (blue). The turn-on voltage threshold between the new PSU and the bus is programmable.

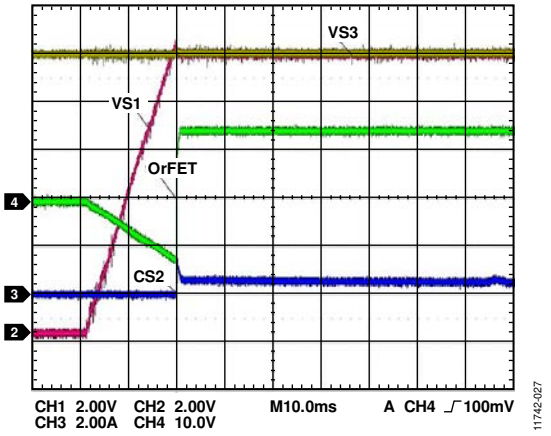

Figure 27. Hot Plug into a Live Bus (Yellow Is Bus Voltage; Red Is VS1 Voltage; Green Is OrFET Control Signal; Blue Is Load Current)

Runaway Master

A rogue PSU on the bus (yellow) has a fault condition, causing the bus voltage to increase above the OVP threshold. The good PSU turns off the OrFET (green) and regulates its internal voltage, VS1 (red). When the rogue power supply fault condition is removed, the bus voltage decreases. The OrFET of the good PSU is immediately turned on, and the good PSU resumes regulating from VS3±.

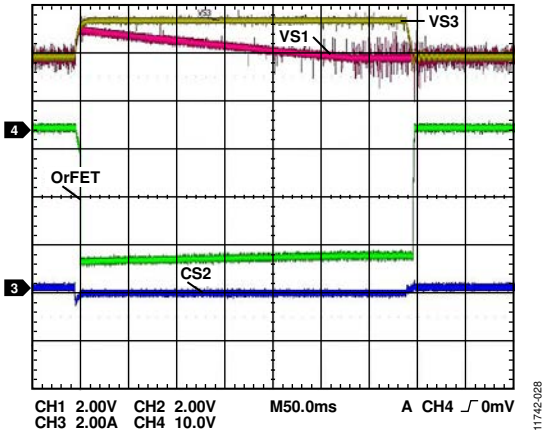

Figure 28. Runaway Master (Yellow Is Bus Voltage; Red Is VS1 Voltage; Green Is OrFET Control Signal; Blue Is Load Current)

Short Circuit

When one of the output rectifiers fails, the bus voltage can collapse if the OrFET is not promptly turned off. The fast OrFET comparator is used to protect the system from this fault event. Figure 29 shows a short circuit applied to the output capacitors before the OrFET. After the fast OrFET threshold for CS2± (blue) is triggered, the OrFET (green) is turned off. Figure 29 also shows the operation when the short circuit is removed. The internal regulation point, VS1 (red), returns to 12 V, and the OrFET (green) is reenabled. The PSU again begins to contribute current to the load (blue).

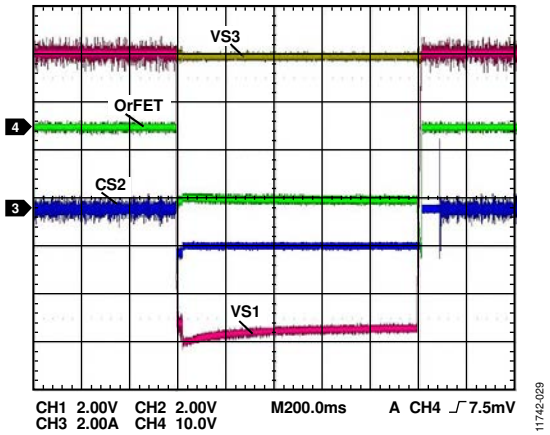

Figure 29. Internal Short Circuit (Yellow Is Bus Voltage; Red Is VS1 Voltage; Green Is OrFET Control Signal; Blue Is Load Current)

Light Load Mode Operation

PSU 1 increases its voltage at light load from 12 V to 12.1 V (yellow). Both PSU 1 and PSU 2 are CCM; therefore PSU 1 sources current and PSU 2 sinks current (blue). In PSU 2, the OrFET control turns off the OrFET to prevent reverse current from flowing. Note that the OrFET voltage (green) is solid during this transition because PSU 1 and PSU 2 are in CCM mode.

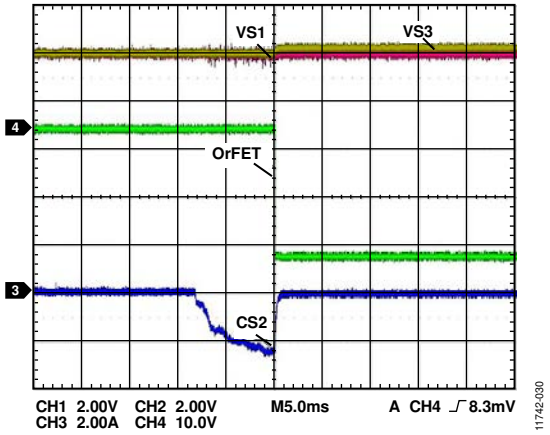

Figure 30. Light Load Mode (Yellow Is Bus Voltage; Red Is VS1 Voltage; Green Is OrFET Control Signal; Blue Is Load Current)

VDD

When VDD is applied, a certain time elapses before the part is capable of regulating the power supply. When VDD rises above the power-on reset and UVLO levels, it takes approximately 20 µs for VCORE to reach its operational point of 2.5 V. The EEPROM contents are then downloaded to the registers. The download takes an additional 25 µs (approximately). After the EEPROM download, the ADP1046AW is ready for operation.

If the ADP1046AW is programmed to power up at this time (PSON is enabled), the soft start ramp begins. Otherwise, the part waits for the PSON signal.

The proper amount of decoupling capacitance must be placed between VDD and AGND, as close as possible to the device to minimize the trace length. It is recommended that the VCORE pin not be used as a reference or to generate other logic levels using resistive dividers.

VDD/VCORE OVLO

The ADP1046AW has built-in overvoltage protection (OVP) on its supply rails. When the VDD or VCORE voltage rises above the OVLO threshold, the response can be programmed using Register 0x0E[7:5]. It is recommended that when a VDD/VCORE OVP fault occurs, the response be set to download the EEPROM before restarting the part (set Register 0x0E[6] = 1).

POWER GOOD

The ADP1046AW has two open-drain power-good pins. The PGOOD1 pin is driven low when a PGOOD1 fault condition is present; the PGOOD2 pin is driven low when a PGOOD2 fault condition is present.

The PGOOD1 and PGOOD2 pins and flags can be programmed to respond to the following flags:

- Soft start
- CS1 fast OCP
- CS1 accurate OCP
- CS2 accurate OCP
- UVP
- Local OVP (fast and accurate)
- Load OVP
- OrFET (GATE pin)

The masking of these flags is programmed in Register 0x7B (for PGOOD1) and Register 0x7C (for PGOOD2). When a flag is masked, it does not set PGOOD1 or PGOOD2.

The following additional flags can also set the PGOOD2 pin either unconditionally or based on the flag response, as programmed in Register 0x2D[3] (see Figure 31 and Table 45).

- Voltage continuity
- OrFET disable
- ACSNS
- External flag (FLAGIN pin)
- OTP

These additional flags can be programmed in Register 0x2D[3] to always set PGOOD2 or to set PGOOD2 only if the flag action is not set to "ignore" in the fault configuration register for that flag (see Table 12 and Table 13).

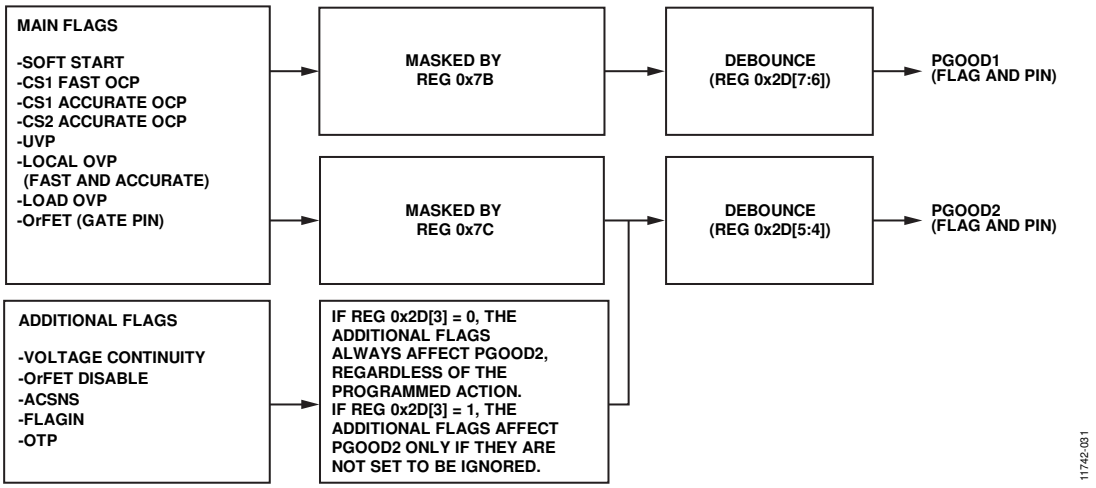

Figure 31. PGOOD1, PGOOD2 Programming

CURRENT SHARING

The ADP1046AW supports both analog current sharing and digital current sharing. The ADP1046AW uses the CS2 current information for current sharing (this setting is programmed in Register 0x29[3]).

Analog Current Sharing

Analog current sharing uses the internal current sensing circuitry to provide a current reading to an external current error amplifier. Therefore, an additional differential current amplifier is not necessary.

The current reading from CS2 can be output to the SHAREo pin in the form of a digital bit stream, which is the output of the current sense ADC (see Figure 33). The bit stream from the Σ-Δ ADC is proportional to the current delivered by this unit to the load. By filtering this digital bit stream using an external RC filter, the current information is turned into an analog voltage that is proportional to the current delivered by this unit to the load. This voltage can be compared to the share bus voltage. If the unit is not supplying enough current, an error signal can be applied to the VS3± feedback point. This signal causes the unit to increase its output voltage and, in turn, its current contribution to the load.

Digital Share Bus

The digital share bus scheme is similar in principle to the traditional analog share bus scheme. The difference is that instead of using a voltage on the share bus to represent current, a digital word is used.

The ADP1046AW outputs a digital word onto the share bus. The digital word is a function of the current that the power supply is providing (the higher the current, the larger the digital word).

The power supply with the highest current controls the bus (master). A power supply that is putting out less current (slave) sees that another supply is providing more power to the load than it is.

During the next cycle, the slave increases its current output contribution by increasing its output voltage. This cycle continues until the slave outputs the same current as the master, within a programmable tolerance range. Figure 32 shows the configuration of the digital share bus.

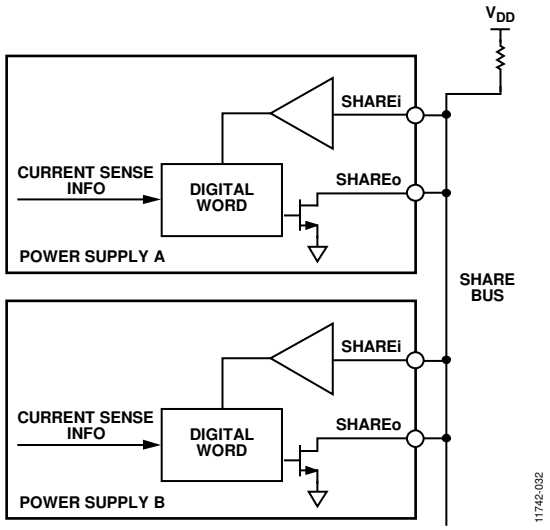

Figure 32. Digital Current Share Configuration

The digital share bus is based on a single-wire communication bus principle; that is, the clock and data signals are contained together.

When two or more ADP1046AW devices are connected, they synchronize their share bus timing. This synchronization is performed by the start bit at the beginning of a communications frame. If a new ADP1046AW is hot-swapped onto an existing digital share bus, the device waits to begin sharing until the next frame. The new ADP1046AW monitors the share bus until it sees a stop bit, which designates the end of a share frame. It then performs synchronization with the other ADP1046AW devices during the next start bit. The digital share bus frame is shown in Figure 34.

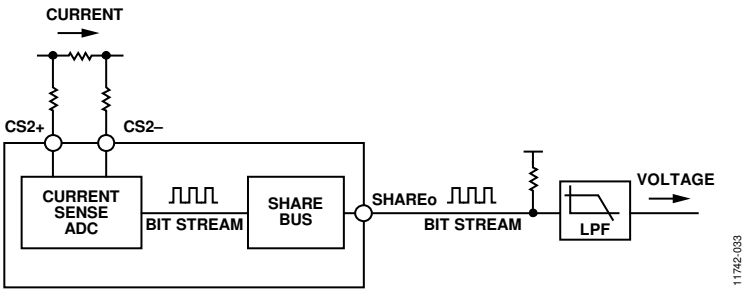

Figure 33. Analog Current Share Configuration

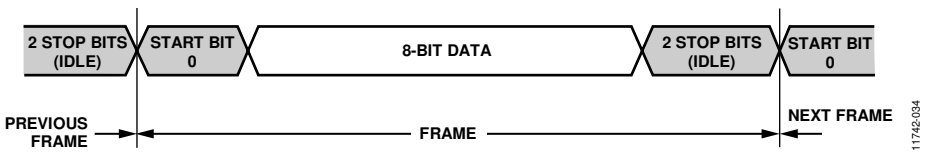

Figure 34. Digital Current Share Frame Timing Diagram