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Digital Controller for Isolated Power Supply with PMBus Interface

Data Sheet

ADP1050

FEATURES

- Versatile digital voltage mode controller
- High speed input voltage feedforward control
- 4 pulse-width modulation (PWM) logic outputs with 625 ps resolution
- Switching frequency: 49 kHz to 625 kHz
- Frequency synchronization as slave device
- Pulse skipping power saving mode
- Prebias startup
- Conditional overvoltage protection
- Extensive fault detection and protection
- PMBus compliant
- Graphical user interface (GUI) for ease of programming
- On-board EEPROM for programming and data storage
- Available in a 20-lead, 4 mm × 4 mm LFCSP
- −40°C to +125°C operating temperature

APPLICATIONS

- High density, isolated dc-to-dc power supplies
  - Intermediate bus converters
  - High availability parallel power systems
- Server, storage, industrial, networking, and communications infrastructure

GENERAL DESCRIPTION

The ADP1050 is an advanced digital controller with a PMBus™ interface targeting high density, high efficiency dc-to-dc power conversion. This controller implements voltage mode control with high speed, input voltage feedforward operation for enhanced transient and noise performance. The ADP1050 has four programmable pulse-width modulation (PWM) outputs capable of controlling most high efficiency power supply topologies, with the added control of synchronous rectification (SR).

The ADP1050 implements several features to enable a robust system of parallel and redundant operation for customers who require high availability. The device provides synchronization, prebias startup, and conditional overvoltage techniques to identify and safely shut down an erroneous power supply in parallel operation mode.

The ADP1050 is based on flexible state machine architecture and is programmed using an intuitive graphical user interface (GUI). The easy to use GUI reduces design cycle time and results in a robust, hardware coded system loaded into the built-in EEPROM. The small size (4 mm × 4 mm) of the LFCSP package makes the ADP1050 ideal for ultracompact, isolated dc-to-dc power module or embedded power designs.

TYPICAL APPLICATIONS CIRCUIT

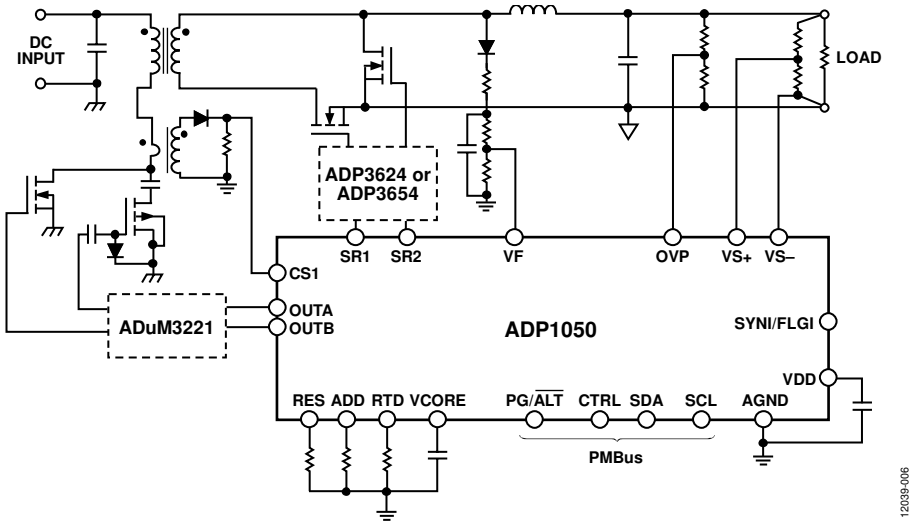

Figure 1.

Rev. A

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- ADP1050 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1306: ADP1050 and ADP1051 EEPROM Programming and Calibration in the Power Supply Manufacturing Environment

Data Sheet

- ADP1050: Digital Controller for Isolated Power Supply with PMBus Interface Data Sheet

User Guides

- UG-664: 240 W Evaluation Board Kit for the ADP1050, Digital Controller for Isolated Power Supply with PMBus Interface
- UG-691: 150 W Eighth Brick Module for the ADP1050, Digital Controller for Isolated Power Supply with PMBus Interface

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADP1050/ADP1051/ADP1052 Software

REFERENCE MATERIALS

Technical Articles

- Designing Digital Power Supplies With A State Machine

DESIGN RESOURCES

- ADP1050 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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TABLE OF CONTENTS

REVISION HISTORY

6/14—Rev. 0 to Rev. A

Changes to Table 2 8
Changes to Pin 1, Table 4 9
Changes to VOUT_COMMAND Section 53
Change to Bit 7, Table 164 89

1/14—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.0 V to 3.6 V, T_J = −40°C to +125°C, unless otherwise noted. FSR = full-scale range.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	2.2 µF capacitor connected to AGND
Supply Current	I_{DD}		28.5	33	mA	Normal operation; PWM pins unloaded
			I_{DD} + 6		mA	During EEPROM programming
			50	100	µA	Shutdown; V_{DD} below undervoltage lockout (UVLO) threshold
POWER-ON RESET						
Power-On Reset				3.0	V	V_{DD} rising
UVLO Threshold		2.75	2.85	2.97	V	V_{DD} falling
UVLO Hysteresis			35		mV	
OVLO Threshold		3.7	3.9	4.1	V	
OVLO Debounce			2		µs	VDD_OV flag debounce set to 2 µs
			500		µs	VDD_OV flag debounce set to 500 µs
VCORE PIN						
Output Voltage	V_{CORE}	2.45	2.6	2.75	V	330 nF capacitor connected to AGND
OSCILLATOR AND PLL						
PLL Frequency		190	200	210	MHz	RES input = 10 kΩ (±0.1%)
Digital PWM Resolution			625		ps	
OUTA, OUTB, SR1, SR2 PINS						
Output Low Voltage	V_{OL}			0.4	V	I_{OH} = 10 mA
Output High Voltage	V_{OH}	V_{DD} − 0.4			V	I_{OL} = −10 mA
Rise Time	t_R		3.5		ns	C_{LOAD} = 50 pF
Fall Time	t_F		1.5		ns	C_{LOAD} = 50 pF
Output Source Current	I_{OL}	−10			mA	
Output Sink Current	I_{OH}			10	mA	
VS+, VS− VOLTAGE SENSE PINS						
Input Voltage Range	V_{IN}	0	1	1.6	V	Differential voltage from VS+ to VS−
Leakage Current				1.0	µA	
VS Accurate ADC						
Valid Input Voltage Range		0		1.6	V	
ADC Clock Frequency			1.56		MHz	
Register Update Rate			10		ms	
Measurement Resolution			12		Bits	
Measurement Accuracy						Factory trimmed at 1.0 V
		−5		+5	% FSR	0% to 100% of input voltage range
		−80		+80	mV	
		−2		+2	% FSR	10% to 90% of input voltage range
		−32		+32	mV	
		−1.0		+1.0	% FSR	900 mV to 1.1 V
		−16		+16	mV	
Temperature Coefficient				70	ppm/°C	
Voltage Differential from VS− to AGND		−200		+200	mV	
VS High Speed ADC						
Equivalent Sampling Frequency	f_{SAMP}		f_{SW}		kHz	
Equivalent Resolution			6		Bits	f_{SW} = 390.5 kHz
Dynamic Range			±25		mV	Regulation voltage = 0 mV to 1.6 V
VS UVP Digital Comparator						Triggers VOUT_UV_FAULT flag
Threshold Accuracy		−2		+2	% FSR	10% to 90% of input voltage range
Comparator Update Speed			82		µs	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OVP PIN						Triggers VOUT_OV_FAULT flag
Leakage Current				1.0	µA	
OVP Comparator						
Voltage Range		0.75		1.5	V	Differential voltage from OVP to VS−
Threshold Accuracy		−1.6	+1	+1.6	%	0.75 V to 1.5 V voltage range
Propagation Delay (Latency)			61	85	ns	Debounce time not included
VF VOLTAGE SENSE PIN						
Input Voltage Range	V_{IN}	0	1	1.6	V	Voltage from VF to AGND
Leakage Current				1.0	µA	
General ADC						
Valid Input Voltage Range		0		1.6	V	
ADC Clock Frequency			1.56		MHz	
Register Update Rate			1.31		ms	
Measurement Resolution			11		Bits	
Measurement Accuracy		−2		+2	% FSR	10% to 90% of input voltage range
		−32		+32	mV	
		−5		+5	% FSR	0% to 100% of input voltage range
		−80		+80	mV	
VF UVP Digital Comparator						Triggers VIN_LOW or VIN_UV_FAULT flag
Threshold Accuracy						Based on VF general ADC parameter values
Comparator Update Speed			1.31		ms	
Feedforward ADC						
Input Voltage Range	V_{IN}	0.5	1	1.6	V	
Resolution			11		Bits	
Sampling Period			10		µs	
CS1 CURRENT SENSE PIN						
Input Voltage Range	V_{IN}	0	1	1.6	V	Voltage from CS1 to AGND
Source Current		−1.2		−0.35	µA	
CS1 ADC						
Valid Input Voltage Range		0		1.6	V	
ADC Clock Frequency			1.56		MHz	
Register Update Rate			10		ms	
Measurement Resolution			12		Bits	
Measurement Accuracy		−2		+2	% FSR	10% to 90% of input voltage range
		−32		+32	mV	
		−5		+5	% FSR	0% to 100% of input voltage range
		−80		+80	mV	
CS1 OCP Comparator						Triggers internal CS1_OCP flag
Reference Accuracy		1.185	1.2	1.215	V	When set to 1.2 V
		0.235	0.25	0.265	V	When set to 0.25 V
Propagation Delay (Latency)			65	105	ns	Debounce/blanking time not included
CS3[1] Measurement and Digital Comparator						Triggers CS3_OC_FAULT flag
Register Update Rate			10		ms	
Comparator Speed			10		ms	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RTD TEMPERATURE SENSE PIN						
Input Voltage Range	V_{IN}	0		1.6	V	Voltage from RTD to AGND
Source Current						Factory default setting
Register 0xFE2D = 0xE6		44.6	46	47.3	µA	
Register 0xFE2D = 0xB0		38.6	40	42	µA	
Register 0xFE2D = 0x80		28.6	30	31.8	µA	
Register 0xFE2D = 0x40		18.6	20	21.6	µA	
Register 0xFE2D = 0x00		9.1	10	11	µA	
RTD ADC						
Valid Input Voltage Range	V_{IN}	0		1.6	V	
ADC Clock Frequency			1.56		MHz	
Register Update Rate			10		ms	
Measurement Resolution			12		Bits	
Measurement Accuracy		−0.3		+0.45	% FSR	2% to 20% of the input voltage range
		−4.8		+7.2	mV	
		−2		+2	% FSR	0% to 100% of the input voltage range
		−80		+80	mV	
OTP Digital Comparator						Triggers OT_FAULT flag
Threshold Accuracy		−0.9		+0.25	% FSR	T = 85°C with 100 kΩ||16.5 kΩ
		−14.4		+4	mV	
		−0.5		+1.1	% FSR	T = 100°C with 100 kΩ||16.5 kΩ
		−8		+17.6	mV	
Comparator Update Speed			10		ms	
Temperature Readings According to Internal Linearization Scheme						Source current is set to 46 µA (Register 0xFE2D = 0xE6); NTC R25 = 100 kΩ (1%); beta = 4250 (1%); R_{EXT} = 16.5 kΩ (1%)
				7	°C	25°C to 100°C
				5	°C	100°C to 125°C
PG/$\overline{\text{ALT}}$ (OPEN-DRAIN) PIN						
Output Low Level	V_{OL}			0.4	V	Sink current = 10 mA
CTRL PIN						
Input Low Level	V_{IL}			0.4	V	
Input High Level	V_{IH}	V_{DD} − 0.8			V	
Leakage Current				1.0	µA	
SYNI/FLGI PIN						
Input Low Level	V_{IL}			0.4	V	
Input High Level	V_{IH}	V_{DD} − 0.8			V	
Synchronization Range % of Internal Clock Period	t_{SYNC}	90		110	%	
SYNI Positive Pulse Width		360			ns	External clock applied on the SYNI/FLGI pin
SYNI Negative Pulse Width		360			ns	External clock applied on the SYNI/FLGI pin
SYNI Period Drift				280	ns	Period drift between two consecutive external clocks
Leakage Current				1.0	µA	
SDA AND SCL PINS						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	V_{DD} − 0.8			V	
Output Low Voltage	V_{OL}			0.4	V	Sink current = 3 mA
Leakage Current		−5		+5	µA	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL BUS TIMING						See Figure 2
Clock Operating Frequency		10	100	400	kHz	
Glitch Immunity				50	ns	
Bus Free Time	t_{BUF}	1.3			µs	Between stop and start conditions
Start Setup Time	$t_{SU;STA}$	0.6			µs	Repeated start condition setup time
Start Hold Time	$t_{HD;STA}$	0.6			µs	Hold time after repeated start condition; after this period, the first clock is generated
Stop Setup Time	$t_{SU;STO}$	0.6			µs	
SDA Setup Time	$t_{SU;DAT}$	100			ns	
SDA Hold Time	$t_{HD;DAT}$	125			ns	For readback
		300			ns	For write
SCL Low Timeout	$t_{TIMEOUT}$	25		35	ms	
SCL Low Time	t_{LOW}	0.6			µs	
SCL High Time	t_{HIGH}	0.6			µs	
SCL Low Extended Time	$t_{LOW;SEXT}$			25	ms	
SCL, SDA Rise Time	t_R	20		300	ns	
SCL, SDA Fall Time	t_F	20		300	ns	
EEPROM						
EEPROM Update Time				40	ms	Time from the update command to completion of the EEPROM update
Reliability						
Endurance[2]		10,000			Cycles	T_J = 85°C
		1000			Cycles	T_J = 125°C
Data Retention[3]		20			Years	T_J = 85°C
		15			Years	T_J = 125°C

[1] CS3 is an alternative output current reading that is calculated by the CS1 reading (representing input current), duty cycle, and the main transformer turns ratio.
[2] Endurance is qualified as per JEDEC Standard 22, Method A117, and is measured at −40°C, +25°C, +85°C, and +125°C.
[3] Retention lifetime equivalent at junction temperature as per JEDEC Standard 22, Method A117.

TIMING DIAGRAM

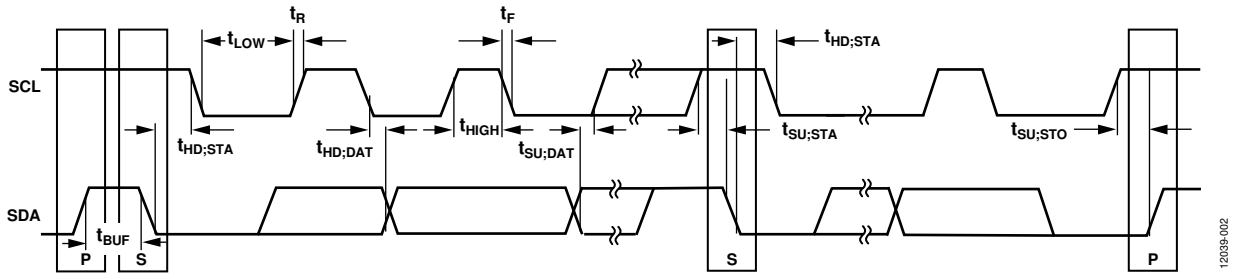


Figure 2. Serial Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (Continuous) V_{DD}	4.2 V
Digital Pins (OUTA, OUTB, SR1, SR2, PG/$\overline{ALT}$, SDA, SCL) to AGND	−0.3 V to V_{DD} + 0.3 V
VS−, VS+, VF, OVP, RTD, ADD, CS1 to AGND	−0.3 V to V_{DD} + 0.3 V
SYNI/FLGI, CTRL	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (T_A)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS-Compliant Assemblies (20 sec to 40 sec)	260°C
ESD Charged Device Model	1.25 kV
ESD Human Body Model	5.0 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead LFCSP	37.05	1.53	°C/W

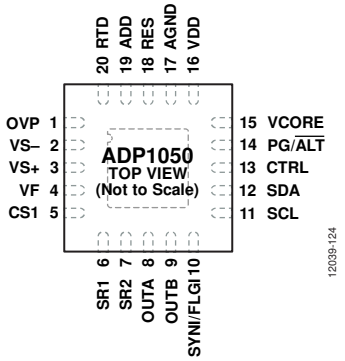
SOLDERING

It is important to follow the correct guidelines when laying out the printed circuit board (PCB) footprint for the ADP1050 and for soldering the device onto the PCB. For detailed information about these guidelines, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE ADP1050 HAS AN EXPOSED THERMAL PAD ON THE UNDERSIDE OF THE PACKAGE. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE EXPOSED PAD BE SOLDERED TO THE PCB AGND PLANE.

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OVP	Overvoltage Protection. This signal is used as redundant overvoltage protection. This signal is referred to AGND.
2	VS–	Inverting Voltage Sense Input. This pin is the connection for the ground line of the power rail. Provide a low ohmic connection to AGND. To allow trimming, it is recommended that the resistor divider on this input have a tolerance specification of ≤0.5%.
3	VS+	Noninverting Voltage Sense Input. This signal is referred to VS–. To allow trimming, it is recommended that the resistor divider on this input have a tolerance specification of ≤0.5%.
4	VF	Voltage Feedforward. Three optional functions can be implemented with this pin: feedforward, primary side input voltage sensing, and input voltage UVLO protection. The pin is connected upstream of the output inductor through a resistor divider network. The nominal voltage at this pin is 1 V. This signal is referred to AGND.
5	CS1	Primary Side Current Sense Input. This pin is connected to the primary side current sensing ADC and to the cycle-by-cycle current-limit comparator. This signal is referred to AGND. To allow trimming, it is recommended that the resistors on this input have a tolerance specification of ≤0.5%. If this pin is not used, connect it to AGND.
6	SR1	PWM Logic Output Drive. This pin can be disabled when not in use. This signal is referred to AGND.
7	SR2	PWM Logic Output Drive. This pin can be disabled when not in use. This signal is referred to AGND.
8	OUTA	PWM Logic Output Drive. This pin can be disabled when not in use. This signal is referred to AGND.
9	OUTB	PWM Logic Output Drive. This pin can be disabled when not in use. This signal is referred to AGND.
10	SYNI/FLGI	Synchronization Signal Input (SYNI)/External Signal Input to Generate a Flag Condition (FLGI). If this pin is not used, connect it to AGND.
11	SCL	I²C/PMBus Serial Clock Input and Output (Open Drain). This signal is referred to AGND.
12	SDA	I²C/PMBus Serial Data Input and Output (Open Drain). This signal is referred to AGND.
13	CTRL	PMBus Control Signal. It is recommended that a 1 nF capacitor be connected from the CTRL pin to AGND for noise debounce and decoupling. This signal is referred to AGND.
14	PG/$\overline{\text{ALT}}$	Power-Good Output (Open Drain)(PG)/Active Low SMBus $\overline{\text{ALERT}}$ Signal ($\overline{\text{ALT}}$). Connect this pin to VDD using a pull-up resistor (typically 2.2 kΩ). The power-good signal is referred to AGND. For information about the SMBus specification, see the PMBus Features section.
15	VCORE	Output of the 2.6 V Regulator. Connect a decoupling capacitor of at least 330 nF from this pin to AGND, as close as possible to the ADP1050 to minimize the PCB trace length. It is recommended that this pin not be used as a reference or to generate other logic levels using resistive dividers.
16	VDD	Positive Supply Input. Voltage of 3.0 V to 3.6 V. This signal is referred to AGND. Connect a 2.2 µF decoupling capacitor from this pin to AGND, as close as possible to the ADP1050 to minimize the PCB trace length.
17	AGND	Common Analog Ground. The internal analog circuitry ground and the digital circuitry ground are star connected to this pin through bonding wires.
18	RES	Resistor Input. This pin sets the internal reference for the internal PLL frequency. Connect a 10 kΩ resistor (±0.1%) from this pin to AGND. This signal is referred to AGND.
19	ADD	Address Select Input. This pin is used to program the I²C/PMBus address. Connect a resistor from ADD to AGND. This signal is referred to AGND.

Pin No.	Mnemonic	Description
20	RTD	Thermistor Input. Place a thermistor (R25 = 100 kΩ (1%), beta = 4250 (1%)) in parallel with a 16.5 kΩ (1%) resistor and a 1 nF filtering capacitor. This pin is referred to AGND. If this pin is not used, connect it to AGND.
	EP	Exposed Pad. The ADP1050 has an exposed thermal pad on the underside of the package. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the exposed pad be soldered to the PCB AGND plane.

TYPICAL PERFORMANCE CHARACTERISTICS

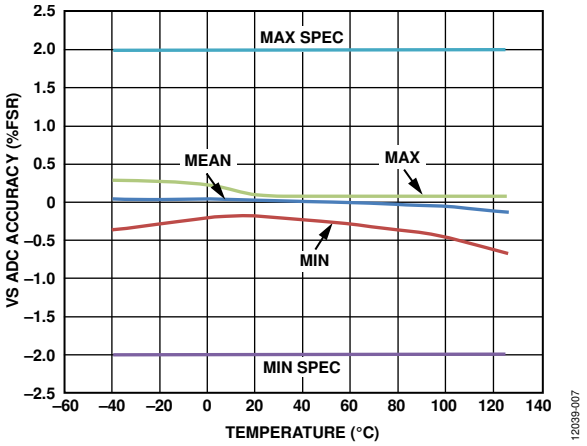


Figure 4. VS ADC Accuracy vs. Temperature (From 10% to 90% of FSR)

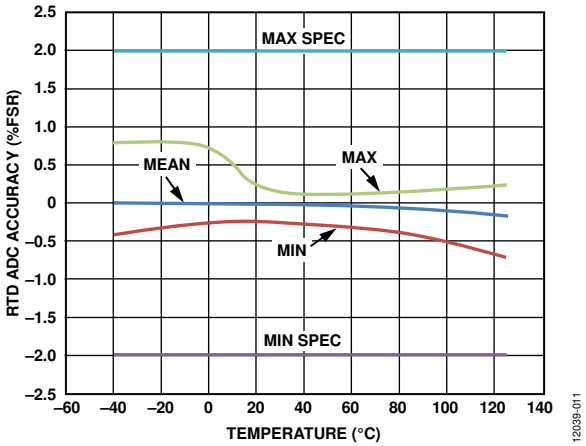


Figure 7. RTD ADC Accuracy vs. Temperature (From 10% to 90% of FSR)

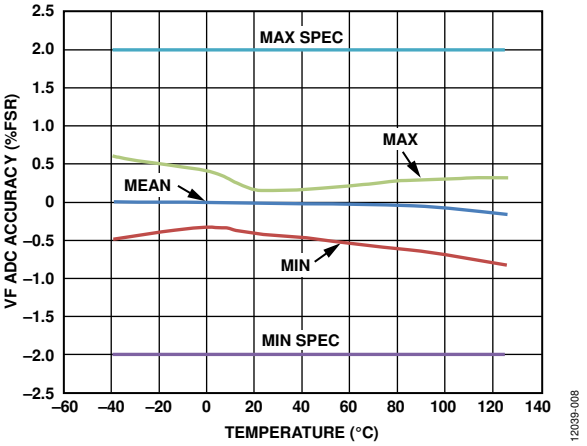


Figure 5. VF ADC Accuracy vs. Temperature (From 10% to 90% of FSR)

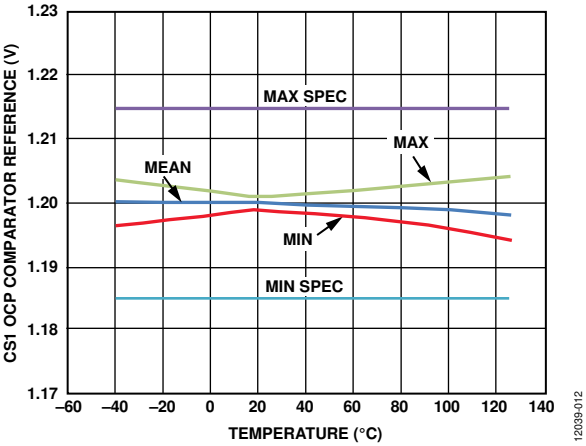


Figure 8. CS1 OCP Comparator Reference vs. Temperature (1.2 V Reference)

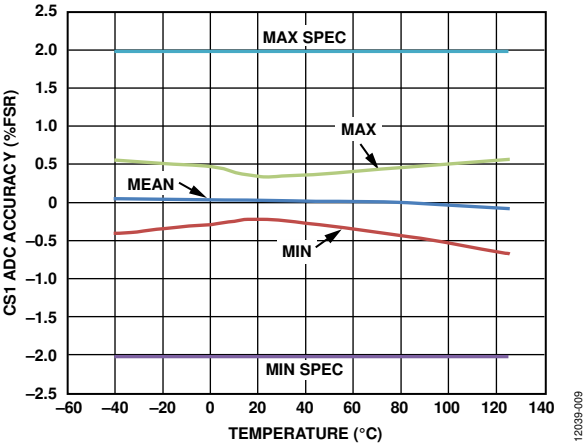


Figure 6. CS1 ADC Accuracy vs. Temperature (From 10% to 90% of FSR)

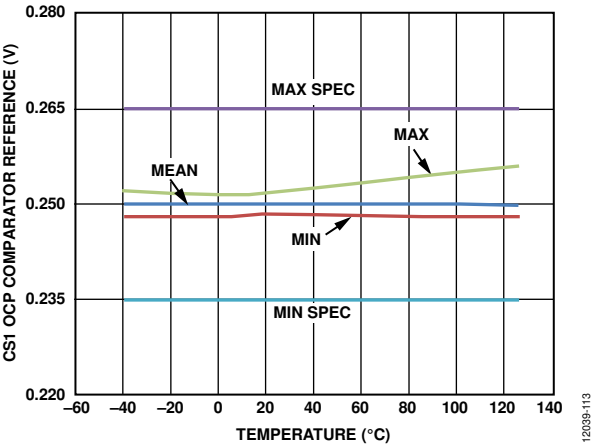


Figure 9. CS1 OCP Comparator Reference vs. Temperature (0.25 V Reference)

THEORY OF OPERATION

The ADP1050 is designed as a flexible, easy to use, digital power supply controller. The ADP1050 integrates the typical functions that are needed to control a power supply, such as

- Output voltage sense and feedback
- Voltage feedforward control
- Digital loop filter compensation
- PWM generation
- Current, voltage, and temperature sense
- Housekeeping and I²C/PMBus interface
- Calibration and trimming

The main function of controlling the output voltage is performed by the feedback ADCs, the digital loop compensator, and the digital PWM engine.

The feedback ADCs feature a patented multipath architecture, with a high speed, low resolution (fast and coarse) ADC and a low speed, high resolution (slow and accurate) ADC. The ADC outputs are combined to form a high speed and high resolution feedback path. Loop compensation is implemented using the digital compensator. This proportional, integral, derivative (PID) compensator is implemented in the digital domain to allow easy programming of filter characteristics, which is of great value in customizing and debugging designs. The PWM engine generates up to four programmable PWM outputs for control of primary side FET drivers and synchronous rectification FET drivers. This programmability allows many generic and specific switching power supply topologies to be realized.

Conventional power supply housekeeping features, such as input voltage sense, output voltage sense, primary side current sense, and secondary side current sense, are included. An extensive set of protections is included, such as overvoltage protection (OVP), overcurrent protection (OCP), overtemperature protection (OTP), and undervoltage protection (UVP).

These features are programmable through the I²C/PMBus digital bus interface. This interface is also used for calibrations. Other information, such as input current, output current, and fault flags, is also available through this digital bus interface.

The internal EEPROM can store all programmed values and allows standalone control without a microcontroller. A free, downloadable GUI is available that provides all the necessary software to program the ADP1050. To obtain the latest GUI software and a user guide, visit http://www.analog.com/digitalpower.

The ADP1050 operates from a single 3.3 V power supply and is specified from −40°C to +125°C.

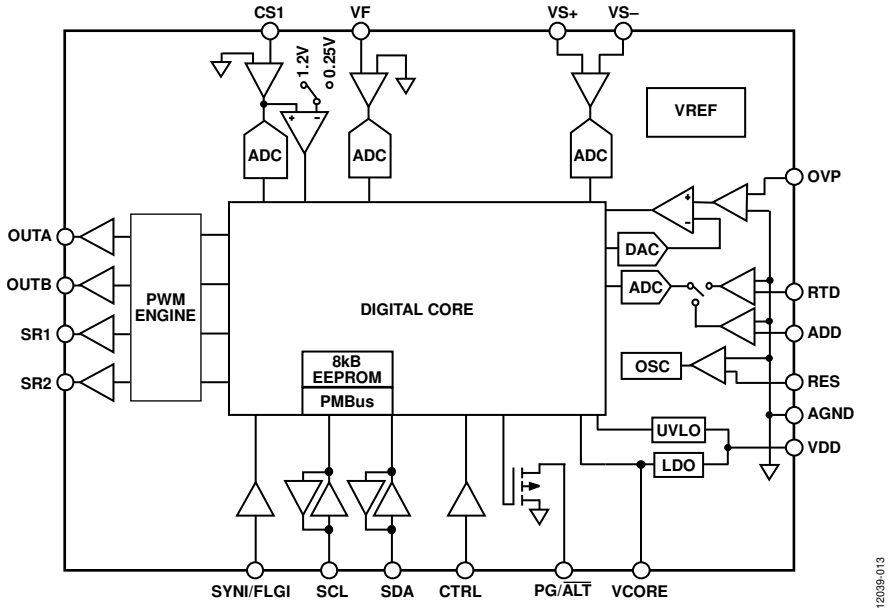


Figure 10. Functional Block Diagram

PWM OUTPUTS (OUTA, OUTB, SR1, AND SR2)

The PWM outputs are used for control of the primary side drivers and the synchronous rectifier drivers. They can be used for several topologies, including hard-switched full bridge, half bridge, push pull, two-switch forward, active clamp forward, and interleaved buck. Delays between rising and falling edges can be individually programmed. Special care must be taken to avoid shoothrough and cross conduction. It is recommended that the ADP1050 GUI software be used to program these outputs.

Figure 11 shows an example configuration to drive an active clamp forward topology with synchronous rectification. The QA, QB, QSR1, and QSR2 switches are driven separately by the PWM outputs (OUTA, OUTB, SR1, and SR2). Figure 12 shows an example of the PWM settings in the GUI for the power stage shown in Figure 11.

The PWM outputs are all synchronized with each other. Therefore, when reprogramming more than one of these outputs, it is important to first update all of the registers and then latch the information into the shadow registers at one time. During the reprogramming operation, the outputs are temporarily disabled. To ensure that the new PWM timings and the switching frequency setting are programmed simultaneously, a special instruction is sent to the ADP1050 by setting Register 0xFE61[2:1] (the go commands). It is recommended that the PWM outputs not in use be disabled via Register 0xFE53[5:4] and Register 0xFE53[1:0].

See the PWM Outputs Timing Registers section for additional information about the PWM timings.

SYNCHRONOUS RECTIFICATION

SR1 and SR2 are recommended for use as the PWM control signals when synchronous rectification is in use. These PWM signals can be configured much like the other PWM outputs.

An optional soft start can be applied to the synchronous rectifier (SR) PWM outputs. The SR soft start can be programmed using Register 0xFE08[4:0].

- When the SR soft start is disabled (Register 0xFE08[1:0] = 00), the SR signals are immediately turned on to their modulated PWM duty cycle values.
- When the SR soft start is enabled (Register 0xFE08[1:0] = 11), the SR1 and SR2 rising edges move left from the t_{RX} + t_{MODU_LIMIT} position to the t_{RX} + $t_{MODULATION}$ position in steps that are set in Register 0xFE08[3:2]. t_{RX} represents the rising edge timing of SR1 (t_{R5}) and the rising edge timing of SR2 (t_{R6}) (see Figure 58); t_{MODU_LIMIT} represents the modulation limit defined in Register 0xFE3C (see Figure 57); $t_{MODULATION}$ represents the real-time modulation value.
- The SR soft start is still applicable even if the SR1 and SR2 outputs are not programmed to be modulated. When the SR soft start is enabled, the SR1 and SR2 rising edges move left from the t_{RX} + t_{MODU_LIMIT} position to the t_{RX} position in steps that are set in Register 0xFE08[3:2].

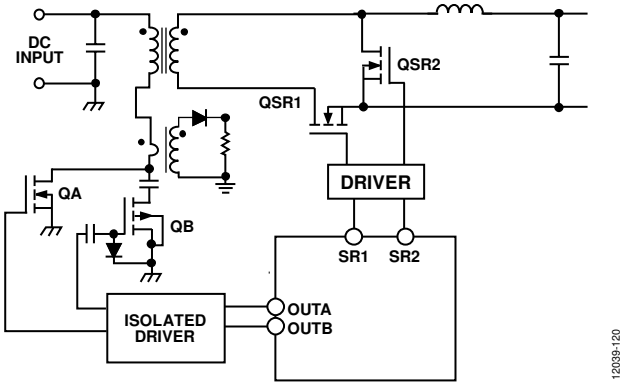


Figure 11. PWM Assignment for Active Clamp Forward Topology with Synchronous Rectification

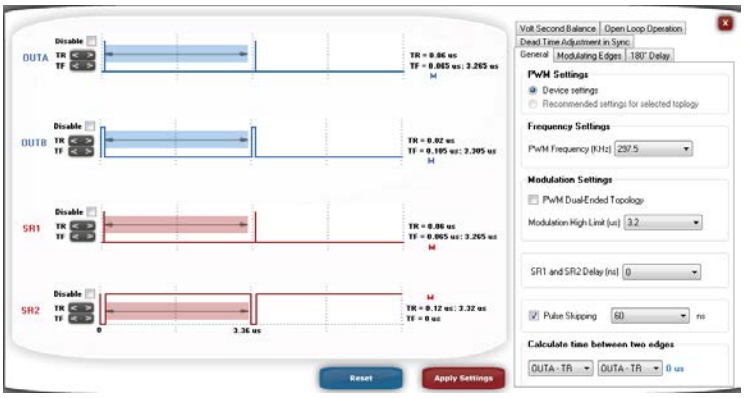


Figure 12. PWM Settings for Active Clamp Forward Topology with Synchronous Rectification Using the ADP1050 GUI

The advantage of the SR soft start is that it minimizes the output voltage undershoot that occurs when the SR FETs are turned on without a soft start. The advantage of turning the SRx signals completely on immediately is that they can help minimize the voltage transient caused during a load step.

Using Register 0xFE08[4], the SR soft start can be programmed to occur only once (the first time that the SRx signals are enabled) or every time that the SRx signals are enabled.

When programming the ADP1050 to use the SR soft start, ensure the correct operation of this function by setting the falling edge of SR1 (t_{F5}) to a lower value than the rising edge of SR1 (t_{R5}) and setting the falling edge of SR2 (t_{F6}) to a lower value than the rising edge of SR2 (t_{R6}). During the SR soft start, the rising edges of SRx move gradually from the right side (the t_{RX} + t_{MODU_LIMIT} position) to the left side to increase the duty cycle.

The ADP1050 is well suited for dc-to-dc converters in isolated topologies. Every time a PWM signal crosses the isolation barrier, a propagation delay is added because of the isolating components. Using Register 0xFE3A[5:0], an adjustable delay (0 ns to 315 ns in steps of 5 ns) can be programmed to move both SR1 and SR2 later in time to compensate for the added propagation delay. In this way, all the PWM edges can be aligned (see Figure 58).

PWM MODULATION LIMIT AND 180° PHASE SHIFT

The modulation limit register (Register 0xFE3C) can be programmed to apply a maximum modulation limit to any PWM signal, thus limiting the modulation range of any PWM output. If modulation is enabled, the maximum modulation limit is applied to all PWM outputs collectively. This limit, t_{MODU_LIMIT}, is the maximum time variation for the modulated edges from the default timing, following the configured modulation direction (see Figure 13). There is no setting for the minimum duty cycle limit. Therefore, the user must set the rising edges and falling edges based on the case with the least modulation.

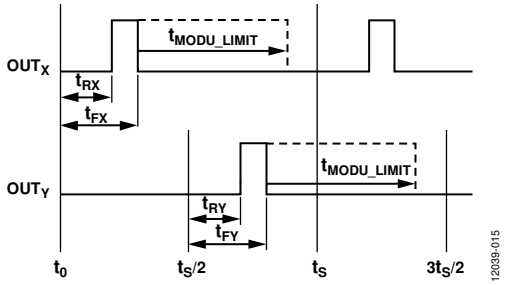


Figure 13. Setting Modulation Limits

Each least significant bit (LSB) in Register 0xFE3C corresponds to a different time step size, depending on the switching frequency (see Table 137). If the ADP1050 is to control a dual-ended topology (such as full bridge, half bridge, or push pull), enable the dual-ended topology mode using Register 0xFE13[6]. When dual-ended topology mode is enabled, the modulation limit in each half cycle is half of the modulation value programmed by Register 0xFE3C.

The modulated edges cannot go beyond one switching cycle. To extend the modulation range for some applications, the 180° phase shift can be enabled, using Register 0xFE3B[5:4] and Register 0xFE3B[1:0]. When the 180° phase shift is disabled, the rising edge timing and the falling edge timing are referred to the start of the switching cycle (see t_{RX} and t_{FX} in Figure 13). When the 180° phase shift is enabled, the rising edge timing and the falling edge timing are referred to half of the switching cycle (see t_{RY} and t_{FY} in Figure 13, which are referred to $t_S/2$). Therefore, when the 180° phase shift is disabled, the edges are always located between t_0 and t_S. When the 180° phase shift is enabled, the edges are located between $t_S/2$ and $3t_S/2$.

The 180° phase shift function can be used to extend the maximum duty cycle in a multiphase, interleaved converter. Figure 14 shows a dual phase, interleaved buck converter. The OUTB and SR1 PWM outputs can be programmed with a 180° phase shift with the OUTA and SR2 PWM outputs.

The ADP1050 GUI is recommended for evaluating this feature.

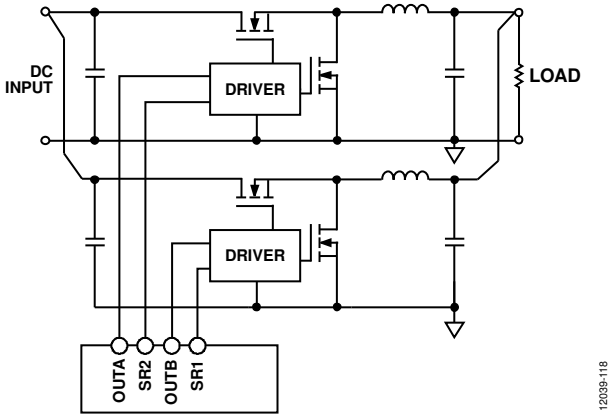


Figure 14. Dual Phase, Interleaved Buck Converter Controlled by the ADP1050

FREQUENCY SYNCHRONIZATION

The ADP1050 can be programmed as a slave device to use the SYNI/FLGI pin signal as the reference to synchronize the internal programmed PWM clock with an external clock.

The period of the external clock that is applied at the SYNI/FLGI pin must be in the range of 90% to 110% of the period of the internal programmed PWM clock. The minimum pulse width of the SYNI signal is 360 ns. From the rising edge of the SYNI signal to the start of the internal clock cycle, there is a 760 ns propagation delay. To realize interleaving control with different controllers, additional delay time can be programmed using Register 0xFE11.

To achieve a smooth synchronization transition between asynchronous operation and synchronous operation, there is a phase capture range bit for synchronization in Register 0xFE12[6] for capturing the phase of the external clock signal. The ADP1050 detects the phase shift between the external clock signal and the internal clock signal when synchronization is enabled. When the phase shift falls within the phase capture range, synchronization begins.

The ADP1050 synchronizes to the external clock frequency as follows:

1. After the synchronization function is enabled by Register 0xFE12[3] and Register 0xFE12[0], the ADP1050 starts to detect the period of the external clock signal applied at the SYNI/FLGI pin.
2. If all periods of the most recent 64 consecutive cycles of the external clocks fall within 90% to 110% of the internal switching clock period, the ADP1050 uses the latest current cycle as the synchronization reference, and the period of the external clock is identified. This interval is t_2 or t_4, as shown in Figure 15. Otherwise, the ADP1050 discards this cycle and looks for the next cycle (frequency capture mode).
3. After the external clock period is determined, the ADP1050 detects the phase shift between the external clock (plus the delay time set by Register 0xFE11) and the internal PWM signal. If the phase shift is within the phase capture range, the internal and external clocks are synchronized (phase capture mode).
4. The PWM clock is synchronized with the external clock. Cycle-by-cycle synchronization starts.
5. If the external clock signal is lost at any time, or if the period exceeds the minimum limit (89% of the internal programmed frequency) or the maximum limit (114% of the internal programmed frequency), the ADP1050 takes the last valid external clock signal as the synchronization reference source. At the same time, the phase shift between the synchronization reference and the internal clock is detected. When the phase shift falls within the phase capture range, the PWM clock returns to the internal clock set by the internal oscillator. This interval is t_1 or t_3, as shown in Figure 15.
   This is the first synchronization unlock condition, called Synchronization Unlocked Mode 1, in which the switching frequency is out of range (range is 89% to approximately 114% of the internal programmed frequency).
6. If the period of the external SYNI signal changes significantly (for example, if the period difference between contiguous cycles exceeds 280 ns), the ADP1050 takes the last valid external clock signal as the synchronization reference source. At the same time, the phase shift between the synchronization reference and the internal clock is detected. When the phase shift falls within the phase capture range, the PWM clock returns to the internal clock set by the internal oscillator.
   This is the second synchronization unlock condition, called Synchronization Unlocked Mode 2, in which the phase shift exceeds 280 ns.

Figure 15 shows the synchronization operation diagram. The internal frequency, f_{SW_INT}, is the internal free-running frequency of the ADP1050. Before the synchronization is locked, the ADP1050 runs at f_{SW_INT}. The external frequency, f_{SW_EXT}, is the frequency of the external clock to which the ADP1050 must synchronize. After synchronization is locked, the ADP1050 runs at f_{SW_EXT}.

The ADP1050 does not allow the switching frequency to cross the boundaries of 97.5 kHz, 195.5 kHz, or 390.5 kHz on-the-fly. Ensure that the external clock does not cross these boundaries. Otherwise, the internal switching frequency cannot be set within ±10% of these boundaries.

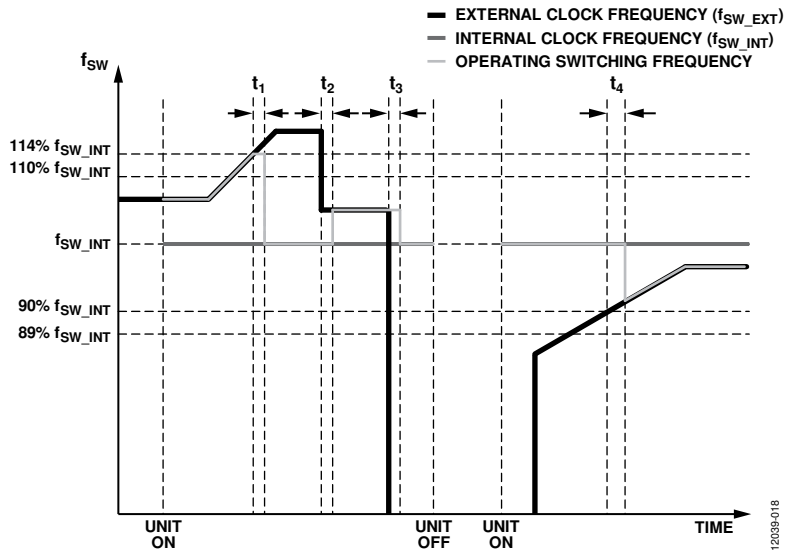


Figure 15. Synchronization Operation

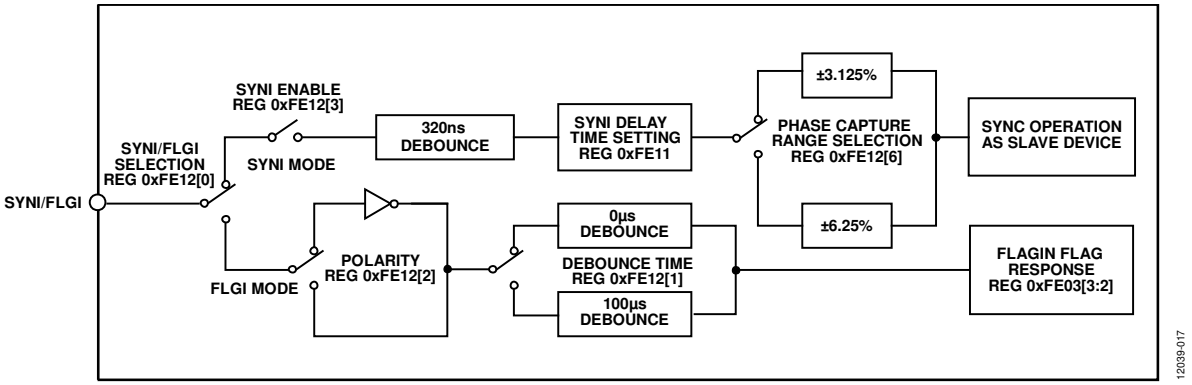


Figure 16. Synchronization Configuration

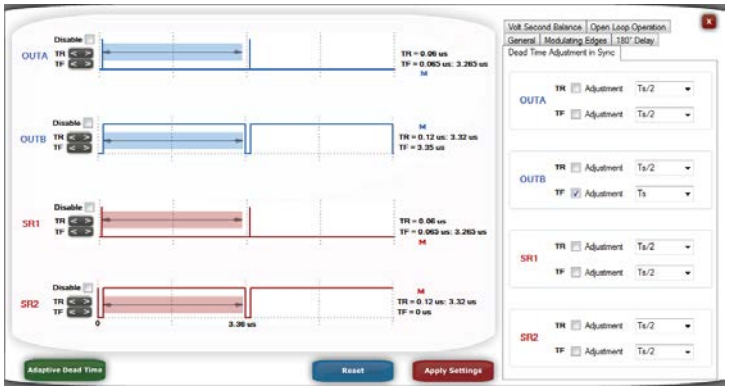


Figure 17. Edge Adjustment Reference During Synchronization

To ensure a constant dead time before and after synchronization, Register 0xFE6D and Register 0xFE6F can be set for edge adjustment referred to $t_S/2$ or t_S. For example, the falling edge of OUTA (t_{F1}) is referred to the ½ × t_S position, which means that the time difference between t_{F1} and ½ × t_S is a constant during the synchronization transition. Figure 17 shows an example of the edge adjustment reference settings in a full bridge topology.

OUTPUT VOLTAGE SENSE AND ADJUSTMENT

The output voltage sense and adjustment function is used for control, monitoring, and undervoltage protection of the remote output voltage. VS– (Pin 2) and VS+ (Pin 3) are fully differential inputs. The voltage sense point can be calibrated digitally to remove any errors due to external components. This calibration can be performed in the production environment, and the settings can be stored in the EEPROM of the ADP1050 (see the Power Supply Calibration and Trim section for more information).

For voltage monitoring, the READ_VOUT output voltage command (Register 0x8B) is updated every 10 ms. The ADP1050 stores every ADC sample for 10 ms and then calculates the average value at the end of the 10 ms period. Therefore, if Register 0x8B is read at least every 10 ms, a true average value is obtained. The voltage information is available through the I²C/PMBus interface.

The control loop of the ADP1050 features a patented multipath architecture. The output voltage is converted simultaneously by two ADCs: a high accuracy ADC and a high speed ADC. The complete signal is reconstructed and processed in the digital compensator to provide a high performance and cost competitive solution.

Voltage Feedback Sensing (VS+ and VS– Pins)

The voltage sense point on the power rail requires an external resistor divider (R1 and R2 in Figure 18) to bring the nominal differential mode signal to 1 V between the VS+ and VS– pins (see Figure 18). This external resistor divider is necessary because the VS ADC input range of the ADP1050 is 0 V to 1.6 V. When R1 and R2 are known, the VOUT_SCALE_LOOP parameter can be calculated using the following equation:

$$VOUT\_SCALE\_LOOP = R2/(R1 + R2)$$

In a 12 V system with resistor dividers of 11 kΩ and 1 kΩ, VOUT_SCALE_LOOP can be calculated as follows:

$$VOUT\_SCALE\_LOOP = 1\ k\Omega/(11\ k\Omega + 1\ k\Omega) = 0.08333$$

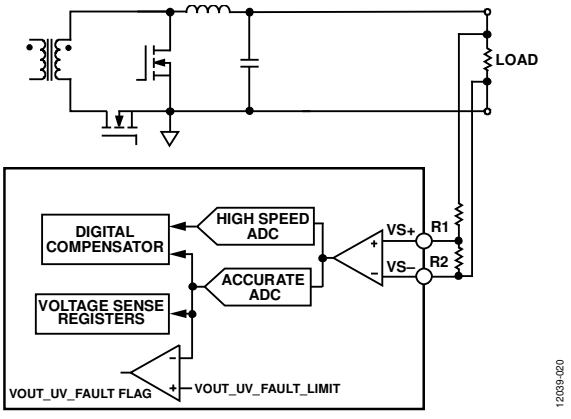


Figure 18. Voltage Sense Configuration

Voltage Sense ADCs

Two kinds of Σ-Δ ADCs are used in the ADP1050 feedback loop, as follows:

- Low frequency (LF) ADC, running at 1.56 MHz
- High frequency (HF) ADC, running at 25 MHz

The Σ-Δ ADCs have a resolution of one bit and operate differently from traditional flash ADCs. The equivalent resolution that is obtained depends on how long the output bit stream of the Σ-Δ ADC is filtered.

The Σ-Δ ADCs also differ from Nyquist rate ADCs in that the quantization noise is not uniform across the frequency spectrum. At lower frequencies, the noise decreases. At higher frequencies, the noise increases (see Figure 19).

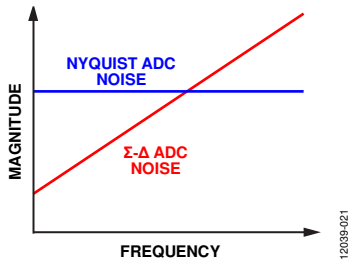


Figure 19. ADC Noise Performance

The low frequency ADC runs at approximately 1.56 MHz. For a specified bandwidth, the equivalent resolution is calculated as

$$\ln(1.56\ \text{MHz}/BW)/\ln(2) = N\ \text{bits}$$

For example, at a bandwidth of 95 Hz, the equivalent resolution/noise is

$$\ln(1.56\ \text{MHz}/95\ \text{Hz})/\ln(2) = 14\ \text{bits}$$

At a bandwidth of 1.5 kHz, the equivalent resolution/noise is

$$\ln(1.56\ \text{MHz}/1.5\ \text{kHz})/\ln(2) = 10\ \text{bits}$$

The high frequency ADC has a 25 MHz clock. It is comb filtered and outputs at the switching frequency into the digital compensator. See Table 5 for equivalent resolutions at selected sampling frequencies.

Table 5. Equivalent Resolutions for High Frequency ADC at Selected Switching Frequencies

f_{SW} (kHz)	High Frequency ADC Resolution (Bits)
49 to 87	9
97.5 to 184	8
195.5 to 379	7
390.5 to 625	6

The high frequency ADC has a range of ±25 mV. Using a base switching frequency of 97.5 kHz at an 8-bit HF ADC resolution, the quantization noise is 0.195 mV (1 LSB = 2 × 25 mV/2^8 = 0.195 mV). When the switching frequency increases to 195.5 kHz at a 7-bit HF ADC resolution, the quantization noise is 0.391 mV (1 LSB = 2 × 25 mV/2^7 = 0.391 mV). Increasing the switching frequency to 390.5 kHz increases the quantization noise to 0.781 mV (1 LSB = 2 × 25 mV/2^6 = 0.781 mV).

Output Voltage Adjustment Commands

In the ADP1050, the voltage data for commanding or reading the output voltage or related parameters is in linear data format. The linear format exponent is fixed at −10 decimal (see the VOUT_MODE command, Register 0x20, in Table 21).

The following three basic commands are used for setting the output voltage:

- VOUT_COMMAND command (Register 0x21, Table 22)
- VOUT_MARGIN_HIGH command (Register 0x25, Table 26)
- VOUT_MARGIN_LOW command (Register 0x26, Table 27)

One of these three values is selected by the OPERATION command (Register 0x01, Table 13).

The VOUT_MAX command (Register 0x24, Table 25) sets an upper limit on the output voltage that the ADP1050 can command, regardless of any other commands or combinations.

During output voltage adjustment, use the VOUT_TRANSITION_RATE command (Register 0x27, Table 28) to set the rate (in mV/µs) at which the VS± pins change voltage.

DIGITAL COMPENSATOR

Use the internal programmable digital compensator to change the control loop of the power supply. A Type III digital compensator architecture has been implemented. This Type III compensator is reconstructed by a low frequency filter, with input from the low frequency ADC, and a high frequency filter, with input from the high frequency ADC. From the voltage sense ADC outputs to the digital compensator output, the transfer function of the digital compensator in z-domain is as follows:

$$H(z) = \frac{d}{204.8 \times m} \times \frac{z}{z-1} + \frac{c}{12.8} \times \frac{z-b}{z-a}$$

where:
a = HF filter pole register value/256 (Register 0xFE32/256).
b = HF filter zero registers value/256 (Register 0xFE31/256).
c = HF filter gain register value (Register 0xFE33).
d = LF filter gain register value (Register 0xFE30).
m is the scale factor, as follows:

m = 1 when 49 kHz ≤ f_{SW} < 97.5 kHz
m = 2 when 97.5 kHz ≤ f_{SW} < 195.5 kHz
m = 4 when 195.5 kHz ≤ f_{SW} < 390.5 kHz
m = 8 when 390.5 kHz ≤ f_{SW}

To tailor the loop response to the specific application, the low frequency gain (represented by d), the zero location of the HF filter (represented by b), the pole location of the HF filter (represented by a), and the high frequency gain (represented by c) can all be set up individually (see the Digital Compensator and Modulation Setting Registers section).

It is recommended that the ADP1050 GUI be used to program the compensator. The GUI displays the filter response, using a Bode plot in the s-domain, and calculates all stability criteria for the power supply.

To transfer the z-domain value to the s-domain, plug the following bilinear transformation equation into the H(z) equation:

$$z(s) = \frac{2f_{SW} + s}{2f_{SW} - s}$$

where s is the s-domain value.

The filter introduces an extra phase delay element into the control loop. The digital compensator circuit sends the information about the duty cycle to the digital PWM engine at the beginning of each switching cycle (unlike an analog controller, which makes decisions on the duty cycle information continuously). There is an additional delay for ADC sampling and decimation filtering. This extra phase delay for phase margin (Φ) is expressed as follows:

$$\Phi = 360 \times f_C/f_{SW}$$

where
f_C is the crossover frequency.
f_{SW} is the switching frequency.

At one-tenth the switching frequency, the phase delay is 36°. The GUI incorporates this phase delay into its calculations. Note that the ADP1050 GUI does not account for other delays, such as gate driver and propagation delay.

The main compensator, called the normal mode compensator, is programmed using Register 0xFE30 to Register 0xFE33. In addition, a dedicated filter is used during soft start. The filter is disabled at the end of the soft start routine, after which the voltage loop digital compensator is used. The soft start filter gain is a programmable value of 1, 2, 4, or 8, using Register 0xFE3D[1:0].

CLOSED-LOOP INPUT VOLTAGE FEEDFORWARD CONTROL AND VF SENSE

The ADP1050 supports closed-loop input voltage feedforward control to improve input transient performance. The VF value is sensed by the feedforward ADC and is used to divide the output of the digital compensator. The result is fed into the digital PWM engine. The input voltage signal can be sensed at the center tap in the secondary windings of the isolation transformer and must be filtered by a residual current device (RCD) circuit network to eliminate the voltage spike at the switching node. Alternatively, the input voltage signal can be sensed from a winding of the auxiliary power transformer.

The VF pin (Pin 4) voltage must be set to 1 V when the nominal input voltage is applied. The feedforward ADC sampling period is 10 µs. Therefore, the decision to modify the PWM outputs, based on the input voltage, is performed at this rate.

As shown in Figure 20, the feedforward scheme modifies the modulation value, based on the VF voltage. When the VF input is 1 V, the line voltage feedforward has no effect. For example, if the digital compensator output remains unchanged and the VF voltage changes to 50% of its original value (still greater than 0.5 V), the modulation of the OUTx edges that are configured for modulation doubles.

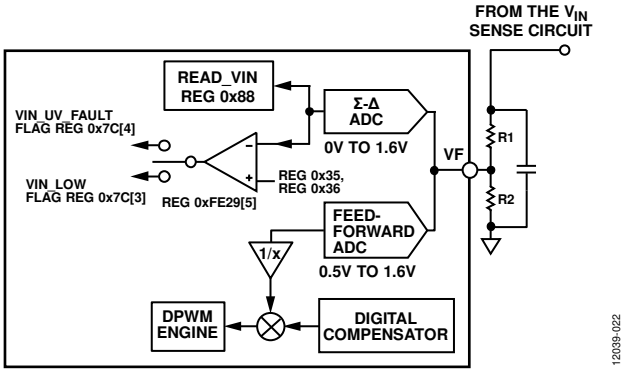


Figure 20. Closed-Loop Input Voltage Feedforward Configuration

If the digital compensator output remains unchanged and the VF voltage changes to 200% of its original value (still less than 1.6 V), the modulation of the OUTx edges that are configured for modulation is divided by 2 (see Figure 21). Register 0xFE3D[3:2] is used to program the optional input voltage feedforward function.

The VF pin also has a low speed, high resolution Σ-Δ ADC. The ADC has an update rate of 800 Hz with 11-bit resolution. The ADC output value is stored in Register 0xFEAC and converted to the READ_VIN command (Register 0x88). This value provides information for the input voltage monitoring and flag functions.

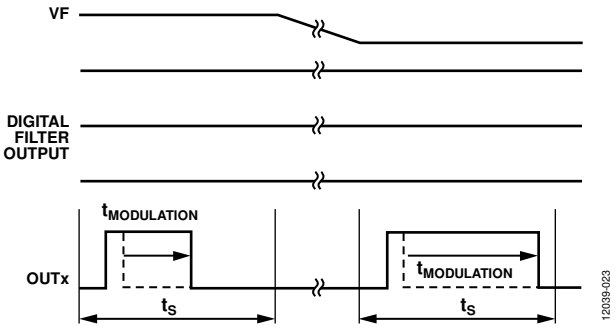


Figure 21. Closed-Loop Input Voltage Feedforward Changes Modulation Values

OPEN-LOOP INPUT VOLTAGE FEEDFORWARD OPERATION

The ADP1050 can run in open-loop input voltage feedforward operation mode. In this mode, the input voltage is sensed as the feedforward signal for the generation of the PWM outputs.

As shown in Figure 22, the digital compensator output is modified by a programmable modulation reference. The VF value, which represents the input voltage, is fed into the feedforward ADC to divide the modulation reference. The result of this division is then fed into the PWM engine. The duty cycle value is in inverse proportion to the input voltage.

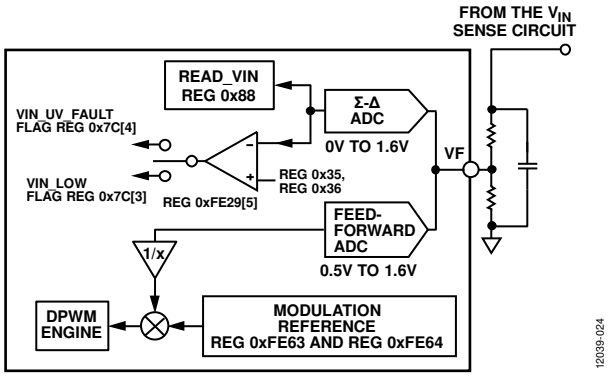


Figure 22. Open-Loop Feedforward Operation

Use the following equations to derive the output voltage equation:

$$D = \frac{V_{IN\_NOM}}{V_{IN}} \times (t_{REF} \times f_{SW})$$

and

$$V_{OUT} = \frac{V_{IN} \times D}{n}$$

The output voltage can then be derived by

$$V_{OUT} = \frac{V_{IN\_NOM} \times (t_{REF} \times f_{SW})}{n}$$

where:
D is the duty cycle value.
V_{IN_NOM} is the nominal input voltage.
V_{IN} is the input voltage.
V_{OUT} is the output voltage.
n is the turns ratio of the main transformer.
t_{REF} is the modulation reference, which is set by Register 0xFE63 and Register 0xFE64.
f_{SW} is the switching frequency.

In the equation to derive V_{OUT}, the input voltage, V_{IN}, is cancelled out. Therefore, the output voltage does not change when the input voltage changes.

Register 0xFE63 and Register 0xFE64 set the modulation reference, based on the target output voltage and the nominal input voltage at which the VF pin voltage is 1 V (see Figure 22).

The PWM settings for open-loop input voltage feedforward operation are similar to those of general closed-loop operation. The falling edge timings, rising edge timings, and modulation are set in the same manner as for closed-loop operation, by using Register 0xFE3E to Register 0xFE52. Register 0xFE09[4:3] sets the soft start speed of the modulation edges. Register 0xFE3D[6] enables open-loop feedforward operation. Register 0xFE3D[7] is used to enable the soft start procedure for open-loop feedforward operation.

The flag settings for open-loop feedforward operation are also similar to those of general closed-loop operation.

Because the output voltage is not regulated in the same manner as in closed-loop operation, some settings, such as the V_{OUT} setting, the digital compensator settings, and the constant current mode setting, are not functional. Other settings can be programmed in a manner that is similar to general closed-loop operation.

OPEN-LOOP OPERATION

The ADP1050 can also run in open-loop operation mode. In this mode, the rising edges and falling edges of the PWM outputs are fixed during normal operation. Therefore, the output voltage varies with the input voltage. The topologies include full bridge, half bridge, and push pull converters.

The PWM settings for open-loop operation are different from those of general closed-loop operation.

1. Set the rising edge timings and falling edge timings using Register 0xFE3E to Register 0xFE4F. Typically, a duty cycle setting of ~50% is recommended for ease of zero voltage switching operation. A phase shift function of 180° is recommended to guarantee balanced PWM outputs.
2. Program Register 0xFE3C to a value of 0x00, which sets the modulation limit to 0 µs.
3. For soft start, apply negative modulation to the falling edges of the OUTA and OUTB outputs. The soft start of SR1 and SR2 is not recommended.
4. Write 111111 to Register 0xFE67[5:4] and Register 0xFE67[1:0] to set all PWM channels to follow open-loop operation. Set Register 0xFE09[7] to enable the soft start procedure. The soft start speed is specified by Register 0xFE09[4:3].
5. Always set Register 0xFE09[2] = 1. The soft start ramp time is determined by $t_{F2} - t_{R2}$.

Because the output voltage is not regulated, some of the settings, such as the V_{OUT} setting, digital compensator settings, and constant current control, are not functional. Other settings can be programmed to be similar to those of general closed-loop operation.

CS1 CURRENT SENSE (CS1 PIN)

The CS1 current sense input (Pin 5) senses, protects, and controls the primary side input. CS1 can be calibrated to reduce errors due to the external components.

Current Sense 1 (CS1) is typically used for the monitoring and protection of the primary side current, which is commonly sensed using a current transformer (CT). The input signal at the CS1 pin is fed into an ADC for current monitoring. The range of the ADC is 0 V to 1.60 V. The input signal is also fed into an analog comparator for cycle-by-cycle current limiting and I_{IN} overcurrent fast protection, with a reference of 0.25 V or 1.2 V set by Register 0xFE1B[6]. The typical configuration for the CS1 current sense is shown in Figure 23.

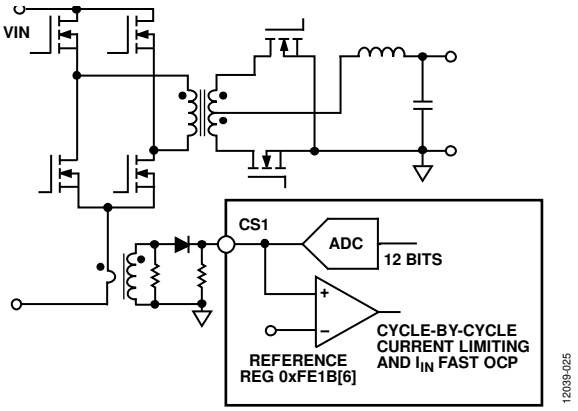


Figure 23. Current Sense 1 (CS1) Operation

The CS1 ADC is used to measure the average value of the primary side current. The ADC samples at a frequency of 1.56 MHz and reports a CS1 reading (12 bits) in the READ_IIN command (Register 0x89), with an asynchronously averaged rate of 10 ms, 52 ms, 105 ms, or 210 ms set by Register 0xFE65[1:0].

Various I_{IN} overcurrent fast fault limits and response actions can be set for CS1. These are described in the Current Sense and Limit Setting Registers section.

SOFT START AND SHUTDOWN

On/Off Control

The OPERATION command (Register 0x01) and the ON_OFF_CONFIG command (Register 0x02) control the power-on and power-off behavior of the ADP1050. The OPERATION command turns the ADP1050 on and off in conjunction with input from the CTRL pin (Pin 13). The combination of the CTRL pin input and the serial bus commands required to turn the ADP1050 on and off is configured by the ON_OFF_CONFIG command. When the ADP1050 is commanded to turn on, the power supply on (PSON) signal is enabled, and the ADP1050 follows the soft start procedure to begin the power conversion.

Soft Start

After VDD power-up and initialization, the PSON signal is enabled when the ADP1050 is commanded to turn on. The controller waits for a user specified turn-on delay (TON_DELAY, Register 0x60) before initiating output voltage soft start ramp. The soft start is then performed by actively regulating the output voltage and digitally ramping up the target voltage to the commanded voltage setpoint. The rise time of the voltage ramp is programmed, using the TON_RISE command (Register 0x61) to minimize the inrush currents associated with the start-up voltage ramp. A nonzero prebiased voltage results in a longer turn-on delay and shorter rise time.

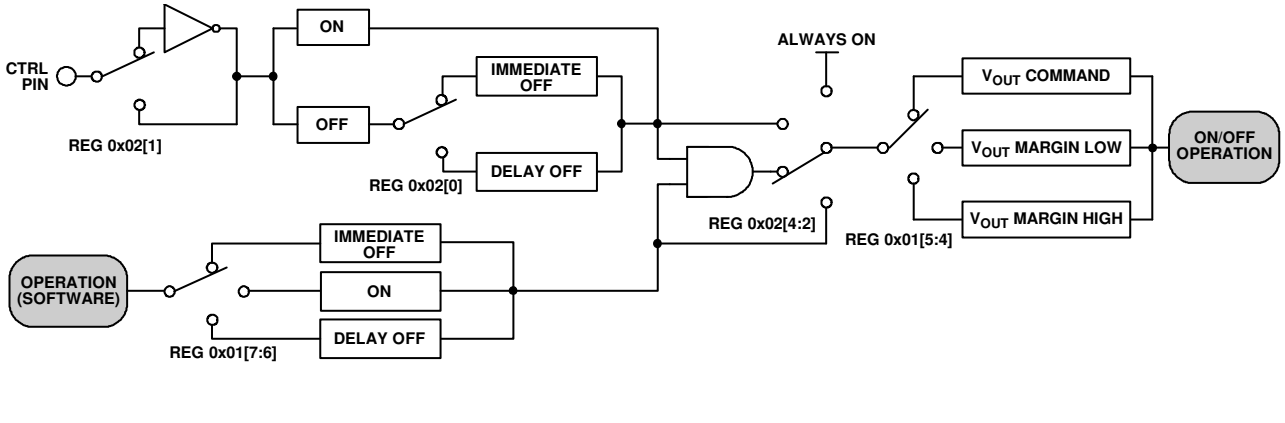


Figure 24. On/Off Control Diagram

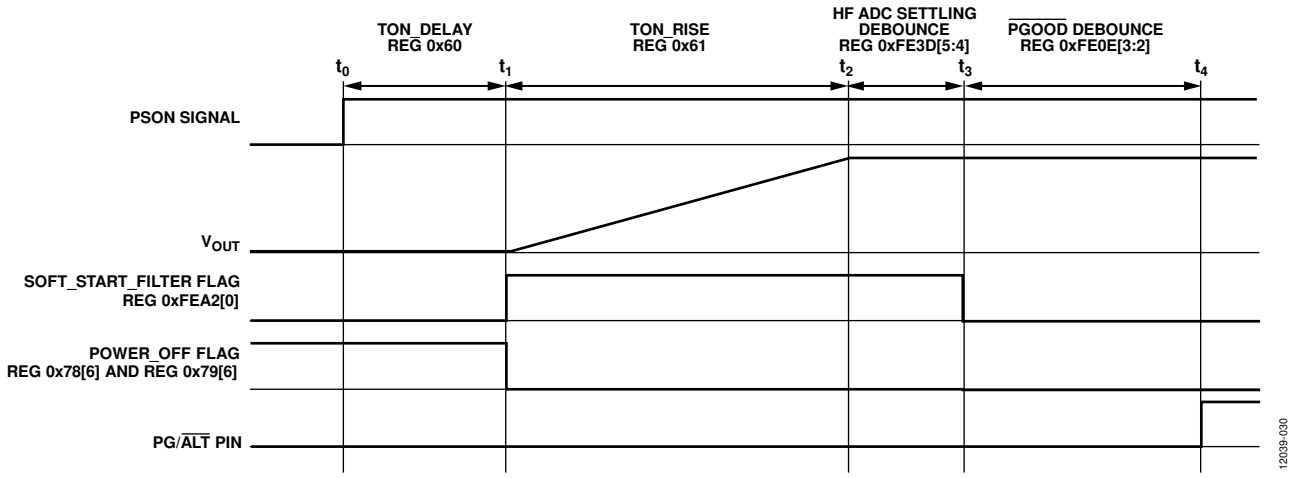


Figure 25. Soft Start Timing Diagram

When the user turns on the power supply, the following soft start procedure is initiated (see Figure 25):

1. At t_0, the PSON signal is enabled by using the OPERATION command, the ON_OFF_CONFIG command, and/or the CTRL pin. The ADP1050 verifies that the initial flags indicate no abnormalities.
2. The ADP1050 waits for the programmed TON_DELAY time to ramp up the power stage voltage at t_1. The soft start filter gain (set by Register 0xFE3D[1:0]) is used for closed-loop control.
3. The soft start begins to ramp up the internal reference. The soft start ramp time is programmed using the TON_RISE command.
4. At t_2, the soft start ramp reaches the output voltage setpoint. The high frequency ADC starts to settle.
5. Additional high frequency ADC settling debounce time can be programmed using Register 0xFE3D[5:4]. If the debounce time is used, the high frequency ADC is activated at t_3. The period between t_2 and t_3 is the high frequency ADC settling debounce time. At t_3, the control loop is switched from the soft start filter to the normal filter.

If no faults are present, the $\overline{\text{PGOOD}}$ signal waits for the programmed clearing debounce time (Register 0xFE0E[3:2]) before the PG/$\overline{\text{ALT}}$ pin is pulled high at t_4.

If a fault condition occurs during the soft start ramp (the time set by the TON_RISE command, t_1 to t_2), the ADP1050 responds as programmed, unless the flag is blanked during soft start. The user can program which flags are active during the soft start. All flags are active at the end of the soft start ramp (t_2). See the Flag Blanking During Soft Start section for more information.

The SR1 and SR2 outputs and the volt-second balance functions can also be disabled during the soft start ramp. For more information, see the Synchronous Rectification section and the Volt-Second Balance Control section, respectively.

Digital Filters During Soft Start

A dedicated soft start filter is used during soft start. The soft start filter is a pure low frequency filter with a programmable gain. The filter is disabled at the end of the soft start routine (t_2), and then the general digital compensator is used. The soft start filter gain is programmed using Register 0xFE3D[1:0]. The soft start filter is used during the ramp time of the voltage reference, until the VS high frequency ADC is settled. The user can program (using Register 0xFE3D[4]) whether a high frequency ADC debounce time is added. The high frequency ADC debounce time is the interval from when the high frequency ADC is settled to when the frequency filter takes action. The debounce time can be programmed at 5 ms or 10 ms using Register 0xFE3D[5]. During the time when the soft start filter is in use, the SOFT_START_FILTER flag is set. It is recommended that a high frequency ADC debounce time not be used if the fast load transient occurs during soft start.

Software Reset

The software reset command allows the user to perform a software reset of the ADP1050. When a 1 is written to Register 0xFE06[0], the power supply is immediately turned off and then restarted with a soft start following a restart delay. The restart delay time can be programmed as 0 ms, 500 ms, 1 sec, or 2 sec (Register 0xFE07[1:0]). If both TON_DELAY and the restart delay are programmed with 0 ms, a write to Register 0xFE06[0] does nothing.

Shutdown

When the ADP1050 is commanded to turn off, the PSON signal is cleared. Depending on the setting of the OPERATION command, the ADP1050 shuts down immediately or waits for a user specified turn-off delay (TOFF_DELAY) prior to the shutdown action.

If the ADP1050 is turned off because a fault condition occurs, the shutdown actions are programmed by the specific fault flag responses. See the Power Monitoring, Flags, and Fault Responses section for more information. The $\overline{\text{PGOOD}}$ flag setting debounce time can be programmed in Register 0xFE0E[1:0]). This debounce time is from when the $\overline{\text{PGOOD}}$ setting condition is met to when the $\overline{\text{PGOOD}}$ flag is set and the PG/$\overline{\text{ALT}}$ pin is pulled low.

Power-Good Signals

The ADP1050 has an open-drain, power-good pin, PG (PG/$\overline{\text{ALT}}$, Pin 14). When the pin is logic high, the power is good. The ADP1050 also has a power-good flag, $\overline{\text{PGOOD}}$, which is a negation of power good. When this flag is set, it indicates that the power is not good. The PG/$\overline{\text{ALT}}$ pin and the $\overline{\text{PGOOD}}$ flag can be programmed to respond to the flags from the following list:

- VIN_UV_FAULT
- IIN_OC_FAST_FAULT
- VOUT_OV_FAULT
- VOUT_UV_FAULT
- OT_FAULT
- OT_WARNING

Register 0xFE0D is used to program the masking of these flags, which prevents them from setting the $\overline{\text{PGOOD}}$ flag and driving the PG/$\overline{\text{ALT}}$ pin low. Register 0xFE0E[1:0] is used to set the debounce time to drive the PG/$\overline{\text{ALT}}$ pin low and set the $\overline{\text{PGOOD}}$ flag (see Figure 26).

The POWER_GOOD_ON command (Register 0x5E) sets the voltage limit that the output voltage must exceed before the $\overline{\text{POWER\_GOOD}}$ flag (Register 0x79[11]) can be cleared. Similarly, the output voltage must fall below the POWER_GOOD_OFF limit (Register 0x5F) for the $\overline{\text{POWER\_GOOD}}$ flag to be set.

The PG/$\overline{\text{ALT}}$ pin is always driven low and the $\overline{\text{PGOOD}}$ flag is always set when one of the POWER_OFF, SOFT_START_FILTER, CRC_FAULT, or $\overline{\text{POWER\_GOOD}}$ flags is set.

The debounce timings for setting and clearing the $\overline{\text{PGOOD}}$ flag can be programmed to 0 ms, 200 ms, 320 ms, or 600 ms in Register 0xFE0E[3:0].

VOLT-SECOND BALANCE CONTROL

The ADP1050 has a dedicated circuit to maintain volt-second balance in the main transformer when operating in full bridge topology. This circuit eliminates the need for a dc blocking capacitor. In interleaved topologies, volt-second balance can also be used for current balancing to ensure that each interleaved phase contributes equal power.

The circuit monitors the current flowing in both legs of the full bridge topology and stores this information. It compensates the selected PWM signals to ensure equal current flow in the two legs of the full bridge topology. The CS1 pin is used as the input for this function.

Several switching cycles are required for the circuit to operate effectively. The maximum amount of modulation applied to each edge of the selected PWM outputs is programmable to ±80 ns or ±160 ns, using Register 0xFE54[2]. The balance control gains are programmable via Register 0xFE54[1:0].

The compensation of the PWM drive signals is performed on the edges of two selected outputs, using Register 0xFE55 and Register 0xFE57. The direction of the modulation is also programmable in these registers.

The volt-second balance control can be disabled during soft start using Register 0xFE0C[1].

There are also leading edge blanking functions at the sensed CS1 signal for more accurate control results. The blanking time follows the CS1 cycle-by-cycle current-limit blanking time (see the CS1 Current Sense section).

To avoid the wrong compensation in light load condition, there is a CS1 threshold in Register 0xFE38 to enable volt-second balance. Below this threshold, volt-second balance is not enabled.

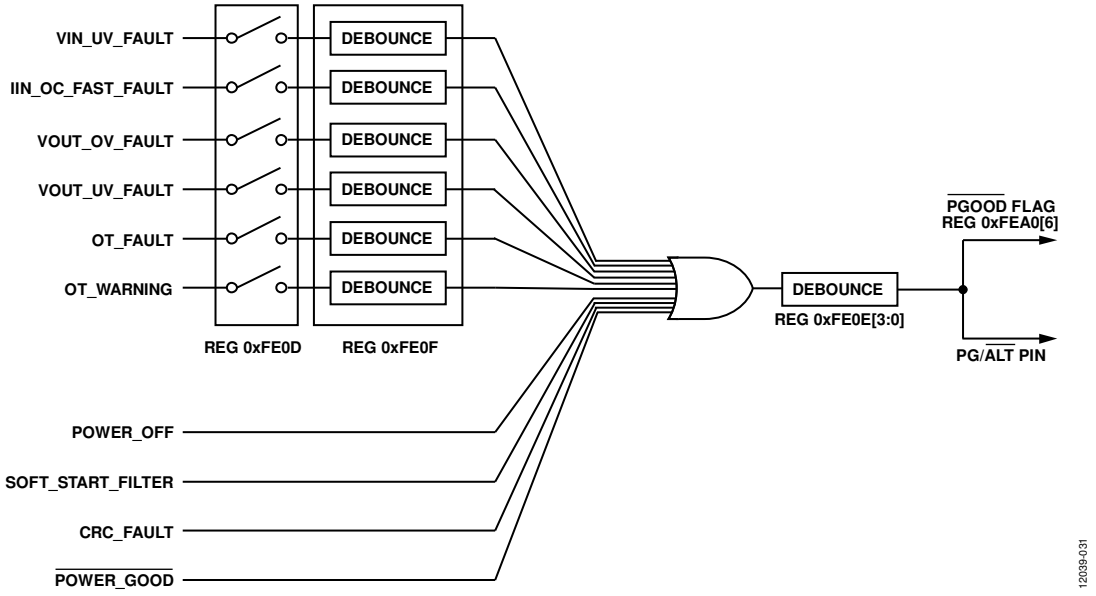


Figure 26. $\overline{\text{PGOOD}}$ Programming

PULSE SKIPPING

The pulse skipping function can reduce the switching loss under very light load current conditions while keeping the output voltage stable. Register 0xFE67[6] can be set to activate this function.

As the output current falls, the supply enters discontinuous conduction mode (DCM). In DCM, the modulation value is a function of the load current. If a very light load current requires a modulation value (duty cycle) of less than the threshold set by Register 0xFE69, pulse skipping mode is enabled. In pulse skipping mode, the PWM output appears intermittently. If the digital compensator signals an error requiring a modulation value that is less than the threshold set by Register 0xFE69, no PWM pulses are generated. If the digital compensator signals an error requiring a modulation value that is greater than the threshold that is set by Register 0xFE69, PWM pulses are generated. Pulse skipping mode is always blanked during soft start.

PREBIAS STARTUP

The prebias start-up function provides the capability to start up the ADP1050 with a prebiased voltage on the output. It protects the power supply against existing external voltage on the output during startup and ensures a monotonic startup before the power supply reaches full regulation (see Figure 27).

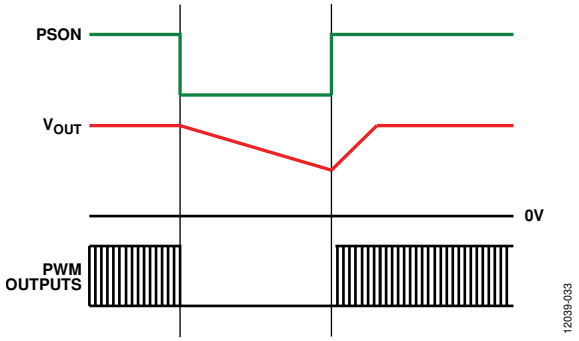


Figure 27. Prebias Startup

The prebias start-up function is enabled by Register 0xFE25[7]. During prebias startup, the ADP1050 soft start ramp starts at the existing voltage value sensed on the VS± pins, and the soft start ramp time is reduced proportionally. The initial PWM modulation value does not begin with zero but, instead, with a value that builds a balanced relationship between the input voltage and the output voltage. This balance avoids the sudden charging or discharging of the output capacitor and achieves a monotonic and smooth startup. The initial modulation value is calculated by the following equation:

$$t_{MODU\_INI} = t_{MODU\_NOM} \times \frac{V_{OUT}}{V_{OUT\_NOM}} \times \frac{V_{IN\_NOM}}{V_{IN}}$$

where:
t_{MODU_INI} is the initial modulation value when the controller begins to generate PWM pulses during startup.
t_{MODU_NOM} is the modulation value set by Register 0xFE39. This value emulates the modulation value when the input voltage and the output voltage are in the nominal condition.
V_{OUT} is the output voltage sensed on the VS± pins.
V_{OUT_NOM} is the nominal output voltage set by VOUT_COMMAND (Register 0x21).
V_{IN_NOM} is the nominal input voltage when the VF pin voltage = 1 V.
V_{IN} is the sensed input voltage.

In addition, Register 0xFE6C[1] is set for correct operation. To sense the input voltage (represented by VF) when the power supply is off, use additional circuitry, such as an auxiliary power circuit, to sense the input voltage.

If the input voltage signal is not available when the power is off, the t_{MODU_INI} value is calculated based on the t_{MODU_NOM} and the output voltage information. In this case, Register 0xFE6C[1] is cleared to 0.

The initial modulation value is calculated as follows:

$$t_{MODU\_INI} = t_{MODU\_NOM} \times \frac{V_{OUT}}{V_{OUT\_NOM}}$$

where:
t_{MODU_INI} is the initial modulation value when the controller begins to generate PWM pulses during startup.
t_{MODU_NOM} is the modulation value set by Register 0xFE39. This value emulates the modulation value when the input voltage and the output voltage are in the nominal condition.
V_{OUT} is the output voltage sensed on the VS± pins.
V_{OUT_NOM} is the nominal output voltage set by VOUT_COMMAND (Register 0x21).

If the closed-loop line voltage feedforward function is selected, the input voltage is introduced from the feedforward loop, and the V_{IN} value is always included for calculation of the initial modulation value.

SR soft start can also be enabled in this mode to achieve a smooth transition. See the Synchronous Rectification section for more information.

VDD AND VCORE

When the voltage of the VDD pin (V_{DD}) is applied, there is a delay before the ADP1050 can regulate the power supply. When V_{DD} rises above the power-on reset and UVLO levels, it takes ~20 µs for the VCORE pin (Pin 15) to reach its operational point of 2.6 V. The EEPROM contents are then downloaded to the registers. The download takes approximately 120 µs. After the EEPROM contents are downloaded, the ADP1050 is ready for operation; however, it takes a maximum of 52 ms for the ADP1050 to complete initialization of the address after a power-on reset. Therefore, it is recommended that the master device access the ADP1050 at least 52 ms after a power-on reset.

If the ADP1050 is programmed to power up at this time, the soft start ramp begins. Otherwise, the device waits for a PSON signal, as programmed in Register 0x01 and Register 0x02.

To minimize trace length, the proper amount of decoupling capacitance must be placed between the VDD pin (Pin 16) and the AGND pin (Pin 17), as close as possible to the device. The same requirement applies to the VCORE pin (Pin 15). It is recommended that the VCORE pin not be used as a reference or to generate other logic levels using resistive dividers.

CHIP PASSWORD

On power-up, some registers in the ADP1050 are locked and protected from being written to or read from. When the chip is locked, the following commands and all read only registers are accessible:

- Operation
- ON_OFF_CONFIG
- CLEAR_FAULTS
- WRITE_PROTECT
- RESTORE_DEFAULT_ALL
- VOUT_COMMAND
- VOUT_TRIM
- VOUT_CAL_OFFSET

Unlock the Chip Password

To unlock the chip password, perform two consecutive writes with the correct password (default value = 0xFFFF) using the CHIP_PASSWORD command (Register 0xD7). Between the two write actions, any read or write action to another register in this device interrupts the unlocking of the chip password. The CHIP_PASSWORD_UNLOCKED flag (Register 0xFEA0[7]) is set to indicate that the chip password is unlocked for access.

Lock the Chip Password

To lock the chip password, use the CHIP_PASSWORD command (Register 0xD7) to write any value other than the correct password. The CHIP_PASSWORD_UNLOCKED flag (Register 0xFEA0[7]) is then cleared to indicate that the chip password is locked from access.

Change the Chip Password

To change the chip password, first write the old password using the CHIP_PASSWORD command (Register 0xD7). Next, write the new password using the same command. The chip password is changed to the new password. If the chip password is to be changed permanently, the register contents must be saved in the EEPROM after the chip password is changed. If the correct chip password is lost, the RESTORE_DEFAULT_ALL command (Register 0x12) restores the factory default settings. In this case, all the user settings are reset.