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Digital Controller for Isolated Power Supply with PMBus Interface

Data Sheet

ADP1052

FEATURES

- Peak data telemetry recording
- High speed input voltage feedforward control
- 6 pulse-width modulation (PWM) logic outputs with 625 ps resolution
- Switching frequency: 49 kHz to 625 kHz
- Frequency synchronization as master and slave device
- Multiple energy saving modes
- Adaptive dead time compensation for efficiency optimization
- Low power consumption: 100 mW typical
- Direct parallel control for power supplies without OR'ing devices
  - Accurate droop current share
  - Prebias startup
  - Reverse current protection
  - Conditional overvoltage protection
- Extensive fault detection and protection
- PMBus compliant
- Graphical user interface (GUI) for ease of programming
- On-board EEPROM for programming and data storage
- Available in a 24-lead, 4 mm × 4 mm LFCSP
- −40°C to +125°C operating temperature

APPLICATIONS

- High density isolated dc-to-dc power supplies
  - Intermediate bus converters
  - High availability parallel power systems
- Server, storage, industrial, networking, and communications infrastructure

GENERAL DESCRIPTION

The ADP1052 is an advanced digital controller with a PMBus™ interface targeting high density, high efficiency, dc-to-dc power conversion. This controller implements voltage mode control with high speed, input line feedforward for enhanced transient and improved noise performance. The ADP1052 has six programmable pulse-width modulation (PWM) outputs capable of controlling most high efficiency power supply topologies, with added control of synchronous rectification (SR). The device includes adaptive dead time compensation to improve efficiency over the load range, and programmable light load mode operation, combined with low power consumption, to reduce system standby power losses.

The ADP1052 implements several features to enable a robust system of parallel and redundant operation for customers that require high availability or parallel connection. The device provides synchronization, reverse current protection, prebias startup, accurate current sharing between power supplies, and conditional overvoltage techniques to identify and safely shut down an erroneous power supply in parallel operation mode.

The ADP1052 is based on flexible state machine architecture and is programmed using an intuitive GUI. The easy to use interface reduces design cycle time and results in a robust, hardware coded system loaded into the built-in EEPROM. The small size (4 mm × 4 mm) LFCSP package makes the ADP1052 ideal for ultracompact, isolated dc-to-dc power module or embedded power designs.

TYPICAL APPLICATIONS CIRCUIT

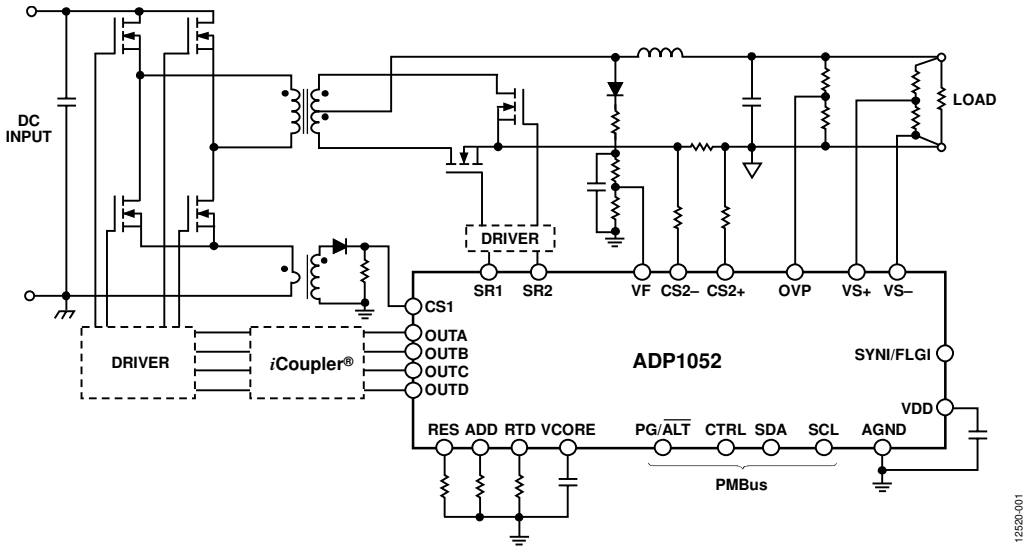

Figure 1.

Rev. A Document Feedback

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- ADP1052: Digital Controller for Isolated Power Supply with PMBus Interface Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADP1050/ADP1051/ADP1052 Software

DESIGN RESOURCES

- ADP1052 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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REVISION HISTORY

4/15—Rev. 0 to Rev. A

Changes to Ordering Guide 113

1/15—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.0 V to 3.6 V, T_J = −40°C to +125°C, unless otherwise noted; FSR = full-scale range.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	2.2 µF capacitor connected to AGND
Supply Current	I_{DD}		33		mA	Normal operation; PWM pins unloaded
			I_{DD} + 6		mA	During EEPROM programming
			50	100	µA	Shutdown; V_{DD} below undervoltage lockout (UVLO)
POWER-ON RESET						
Power-On Reset				3.0	V	V_{DD} rising
UVLO Threshold	UVLO	2.75	2.85	2.97	V	V_{DD} falling
UVLO Hysteresis			35		mV	
Overvoltage Lockout (OVLO) Threshold	OVLO	3.7	3.9	4.1	V	
OVLO Debounce			2		µs	VDD_OV flag debounce set to 2 µs
			500		µs	VDD_OV flag debounce set to 500 µs
VCORE PIN						
Output Voltage	V_{CORE}	2.45	2.6	2.75	V	330 nF capacitor connected to AGND
OSCILLATOR AND PLL						
PLL Frequency		190	200	210	MHz	RES input = 10 kΩ (±0.1%)
Digital PWM Resolution			625		ps	
OUTA, OUTB, OUTC, OUTD, SR1, SR2 PINS						
Output Voltage						
Low	V_{OL}			0.4	V	I_{OH} = 10 mA
High	V_{OH}	V_{DD} − 0.4			V	I_{OL} = −10 mA
Rise Time	t_R		3.5		ns	C_{LOAD} = 50 pF
Fall Time	t_F		1.5		ns	C_{LOAD} = 50 pF
Output Current						
Source	I_{OL}	−10			mA	
Sink	I_{OH}			10	mA	
Synchronization Signal Output (SYNO) Positive Pulse Width		600	640	680	ns	OUTC or OUTD programmed as SYNO
VS+, VS− VOLTAGE SENSE PINS						
Input Voltage Range	V_{IN}	0	1	1.6	V	Differential voltage from VS+ to VS−
Leakage Current				1.0	µA	
Voltage Sense (VS) Accurate Analog-to-Digital Converter (ADC)						
Valid Input Voltage Range		0		1.6	V	
ADC Clock Frequency			1.56		MHz	
Register Update Rate			10		ms	
Measurement						
Resolution			12		Bits	
Accuracy						Factory trimmed at 1.0 V
		−5		+5	% FSR	0% to 100% of input voltage range
		−80		+80	mV	
		−2		+2	% FSR	10% to 90% of input voltage range
		−32		+32	mV	
		−1.0		+1.0	% FSR	900 mV to 1.1 V
		−16		+16	mV	
Temperature Coefficient				70	ppm/°C	
Voltage Differential from VS− to AGND		−200		+200	mV	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
VS High Speed ADC						
Equivalent Sampling Frequency	f_{SAMP}		f_{SW}		kHz	
Equivalent Resolution			6		Bits	f_{SW} = 390.5 kHz
Dynamic Range			±25		mV	Regulation voltage = 0 mV to 1.6 V
VS Undervoltage Protection (UVP) Digital Comparator						Triggers VOUT_UV_FAULT flag
Threshold Accuracy		−2		+2	% FSR	10% to 90% of input voltage range
Comparator Update Speed			82		µs	
OVP PIN						Triggers VOUT_OV_FAULT flag
Leakage Current				1.0	µA	
Overvoltage Protection (OVP) Comparator						
Voltage Range		0.75		1.5	V	Differential voltage from OVP to VS−
Threshold Accuracy		−1.6	1	+1.6	%	0.75 V to 1.5 V voltage range
Propagation Delay (Latency)			61	85	ns	Debounce time not included
VF VOLTAGE SENSE PIN						
Input Voltage Range	V_{IN}	0	1	1.6	V	Voltage from VF to AGND
Leakage Current				1.0	µA	
General ADC						
Valid Input Voltage Range		0		1.6	V	
ADC Clock Frequency			1.56		MHz	
Register Update Rate			1.31		ms	
Measurement						
Resolution			11		Bits	
Accuracy		−2		+2	% FSR	10% to 90% of input voltage range
		−32		+32	mV	
		−5		+5	% FSR	0% to 100% of input voltage range
		−80		+80	mV	
Feedforward Voltage (VF) UVP Digital Comparator						Triggers VIN_LOW or VIN_UV_FAULT flag
Threshold Accuracy						Based on VF general ADC parameter values
Comparator Update Speed			1.31		ms	
Feedforward ADC						
Input Voltage Range	V_{IN}	0.5	1	1.6	V	
Resolution			11		Bits	
Sampling Period			10		µs	
CS1 CURRENT SENSE PIN						
Input Voltage Range	V_{IN}	0	1	1.6	V	Voltage from CS1 to AGND
Source Current		−1.2		−0.35	µA	
CS1 ADC						
Valid Input Voltage Range		0		1.6	V	
ADC Clock Frequency			1.56		MHz	
Register Update Rate			10		ms	
Measurement						
Resolution			12		Bits	
Accuracy		−2		+2	% FSR	10% to 90% of input voltage range
		−32		+32	mV	
		−5		+5	% FSR	0% to 100% of input voltage range
		−80		+80	mV	
CS1 Overcurrent Protection (OCP) Comparator						Triggers internal CS1_OCP flag
Reference Accuracy		1.185	1.2	1.215	V	When set to 1.2 V
		0.235	0.25	0.265	V	When set to 0.25 V
Propagation Delay (Latency)			65	105	ns	Debounce/blanking time not included

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CS3[1] Measurement and Digital Comparator						Triggers CS3_OC_FAULT flag
Register Update Rate			10		ms	
Comparator Speed			10		ms	
CS2+, CS2− CURRENT SENSE PINS						
Input Voltage Range	V_{IN}	0		120	mV	Differential voltage from CS2+ to CS2−
Common-Mode Voltage at CS2+ and CS2−		0.8	1.15	1.4	V	To achieve CS2 current measurement accuracy
Current						
Sink (High-Side Mode)		1.87	1.915	1.96	mA	
Source (Low-Side Mode)		195	225	255	µA	
Temperature Coefficient				95	ppm/°C	
CS2 ADC						
Valid Input Voltage Range		0		120	mV	
ADC Clock Frequency			1.56		MHz	
Measurement Resolution			12		Bits	
Current Measurement Sense Accuracy						
Low-Side Mode						4.99 kΩ (0.01%) level shift resistors
		−1.9		+1.9	% FSR	From 0 mV to 110 mV
		−2.28		+2.28	mV	
		−6.1		+1.4	% FSR	From 110 mV to 120 mV
		−7.32		+1.68	mV	
High-Side Mode						With CS2 high-side factory trim values loaded; 4.99 kΩ (0.01%) level shift resistors; V_{OUT} = 11 V
		−1.6		+2.3	% FSR	From 0 mV to 110 mV
		−1.92		+2.76	mV	
		−5.3		+0.7	% FSR	From 110 mV to 120 mV
		−6.36		+0.84	mV	
CS2 OCP Digital Comparator						Triggers IOUT_OC_FAULT flag
Threshold Accuracy						Same as CS2 ADC low-side and high-side mode current measurement sense accuracy values
Comparator Update Speed			82		µs	When set to the 7-bit averaging speed
			328		µs	When set to the 9-bit averaging speed
CS2 Reverse Current Comparator						Triggers SR_RC_FAULT flag
Threshold Accuracy		−8.5	−3	+3	mV	SR_RC_FAULT_LIMIT set to −3 mV
		−11.5	−6	0	mV	SR_RC_FAULT_LIMIT set to −6 mV
		−14	−9	−3	mV	SR_RC_FAULT_LIMIT set to −9 mV
		−17	−12	−6	mV	SR_RC_FAULT_LIMIT set to −12 mV
		−21	−15	−9	mV	SR_RC_FAULT_LIMIT set to −15 mV
		−24	−18	−12	mV	SR_RC_FAULT_LIMIT set to −18 mV
		−27	−21	−15	mV	SR_RC_FAULT_LIMIT set to −21 mV
		−30	−24	−18	mV	SR_RC_FAULT_LIMIT set to −24 mV
Propagation Delay			110	150	ns	Debounce time = 40 ns
RTD TEMPERATURE SENSE PIN						
Input Voltage Range	V_{IN}	0		1.6	V	Voltage from RTD to AGND
Source Current		44.6	46	47.3	µA	Register 0xFE2D = 0xE6, factory default setting
		38.6	40	42	µA	Register 0xFE2D = 0xB0
		28.6	30	31.8	µA	Register 0xFE2D = 0x80
		18.6	20	21.6	µA	Register 0xFE2D = 0x40
		9.1	10	11	µA	Register 0xFE2D = 0x00

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RTD ADC						
Valid Input Voltage Range		0		1.6	V	
ADC Clock Frequency			1.56		MHz	
Register Update Rate			10		ms	
Measurement						
Resolution			12		Bits	
Accuracy		−0.3		+0.45	% FSR	2% to 20% of the input voltage range
		−4.8		+7.2	mV	
		−2		+2	% FSR	0% to 100% of the input voltage range
		−80		+80	mV	
OTP Digital Comparator						Triggers OT_FAULT flag
Threshold Accuracy		−0.9		+0.25	% FSR	T = 85°C with 100 kΩ||16.5 kΩ
		−14.4		+4	mV	
		−0.5		+1.1	% FSR	T = 100°C with 100 kΩ||16.5 kΩ
		−8		+17.6	mV	
Comparator Update Speed			10		ms	
Temperature Readings According to Internal Linearization Scheme						Current source set to 46 µA (Register 0xFE2D = 0xE6); NTC R25 = 100 kΩ (1%); beta = 4250 (1%); R_{EXT} = 16.5 kΩ (1%)
				7	°C	25°C to 100°C
				5	°C	100°C to 125°C
PG/$\overline{\text{ALT}}$ (OPEN-DRAIN) PIN						
Output Low Level	V_{OL}			0.4	V	Sink current = 10 mA
CTRL PIN						
Input Level						
Low	V_{IL}			0.4	V	
High	V_{IH}	V_{DD} − 0.8			V	
Leakage Current				1.0	µA	
SYNI/FLGI PINS						
Input Level						
Low	V_{IL}			0.4	V	
High	V_{IH}	V_{DD} − 0.8			V	
Synchronization Range, Percent of Internal Clock Period	t_{SYNC}	90		110	%	
SYNI Pulse Width						
Positive		360			ns	External clock applied on the SYNI/FLGI pin
Negative		360			ns	External clock applied on the SYNI/FLGI pin
SYNI Period Drift				280	ns	Period drift between two consecutive external clocks
Leakage Current				1.0	µA	
SDA, SCL PINS						
Input Voltage						
Low	V_{IL}			0.8	V	
High	V_{IH}	V_{DD} − 0.8			V	
Output Voltage Low	V_{OL}			0.4	V	Sink current = 3 mA
Leakage Current		−5		+5	µA	
SERIAL BUS TIMING						See Figure 2
Clock Operating Frequency		10	100	400	kHz	
Glitch Immunity				50	ns	
Bus Free Time	t_{BUF}	1.3			µs	Between stop and start conditions

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Start Setup Time	$t_{SU;STA}$	0.6			µs	Repeated start condition setup time
Start Hold Time	$t_{HD;STA}$	0.6			µs	Hold time after (repeated) start condition; after this period, the first clock is generated
Stop Setup Time	$t_{SU;STO}$	0.6			µs	
SDA Setup Time	$t_{SU;DAT}$	100			ns	
SDA Hold Time	$t_{HD;DAT}$	125			ns	For readback
		300			ns	For write
SCL Low Timeout	$t_{TIMEOUT}$	25		35	ms	
SCL Low Time	t_{LOW}	0.6			µs	
SCL High Time	t_{HIGH}	0.6			µs	
SCL Low Extend Time	$t_{LOW;SEXT}$			25	ms	
SCL, SDA Rise Time	t_R	20		300	ns	
SCL, SDA Fall Time	t_F	20		300	ns	
EEPROM						
EEPROM Update Time				40	ms	Time from the update command to completion of the EEPROM update
Reliability						
Endurance[2]		10,000			Cycles	T_J = 85°C
		1000			Cycles	T_J = 125°C
Data Retention[3]		20			Years	T_J = 85°C
		15			Years	T_J = 125°C

[1] CS3 is an alternative output current reading that is calculated by the CS1 reading (representing input current), duty cycle, and main transformer turn ratio.
[2] Endurance is qualified per JEDEC Standard 22, Method A117, measured at −40°C, +25°C, +85°C, and +125°C.
[3] Retention lifetime equivalent at junction temperature per JEDEC Standard 22, Method A117.

Timing Diagram

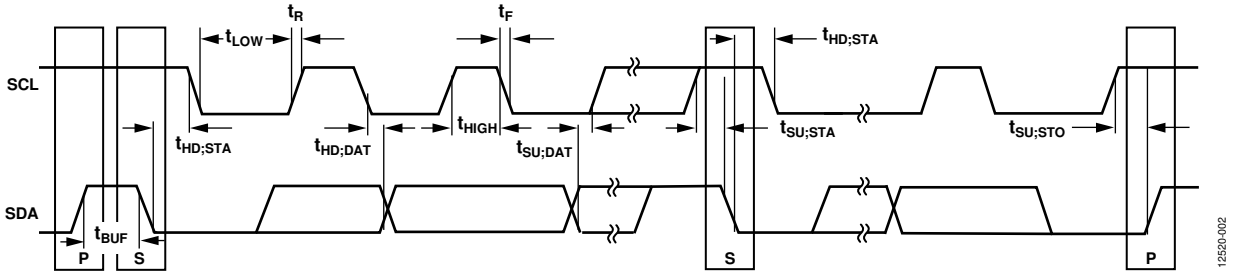

Figure 2. Serial Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (Continuous) V_{DD} to AGND	4.2 V
Digital Pins (OUTA, OUTB, OUTC, OUTD, SR1, SR2) to AGND	−0.3 V to V_{DD} + 0.3 V
PG/$\overline{\text{ALT}}$, SDA, SCL to AGND	−0.3 V to +3.9 V
VS−, VS+, VF, OVP, RTD, ADD, CS1, CS2+, CS2− to AGND	−0.3 V to V_{DD} + 0.3 V
SYNI/FLGI, CTRL to AGND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (T_A)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS-Compliant Assemblies (20 sec to 40 sec)	260°C
ESD Models	
ESD Charged Device Model	1.25 kV
ESD Human Body Model	5.0 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
24-Lead LFCSP	36.26	1.51	°C/W

SOLDERING

It is important to follow the correct guidelines when laying out the printed circuit board (PCB) footprint for the ADP1052 and for soldering the device onto the PCB. For detailed information about these guidelines, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

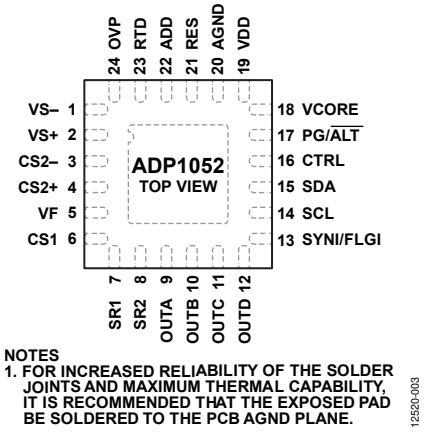

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VS–	Inverting Voltage Sense Input. This pin is the connection for the ground line of the power rail. Provide a low ohmic connection to AGND. To allow for trimming, it is recommended that the resistor divider on this input have a tolerance specification of ≤0.5%.
2	VS+	Noninverting Voltage Sense Input. This pin signal is referred to VS–. To allow for trimming, it is recommended that the resistor divider on this input have a tolerance specification of ≤0.5%.
3	CS2–	Inverting Differential Current Sense Input. For best operation, use a nominal voltage of 1.12 V with this pin. When using low-side current sensing, place a 4.99 kΩ level shifting resistor between the sense resistor and this pin. When using high-side current sensing in a 12 V application, place a 5.62 kΩ resistor between the sense resistor and this pin. When using high-side current sensing, apply the formula R = (V_{OUT} − 1.12 V)/1.915 mA. A 0.1% resistor must be used to connect this circuit. If this pin is not used, connect it to AGND and set the CS2 current sense to high-side current sense mode (Register 0xFE19[7] = 1 binary).
4	CS2+	Noninverting Differential Current Sense Input. For best operation, use a nominal voltage of 1.12 V with this pin. When using low-side current sensing, place a 4.99 kΩ level shifting resistor between the sense resistor and this pin. When using high-side current sensing in a 12 V application, place a 5.62 kΩ resistor between the sense resistor and this pin. When using high-side current sensing, apply the formula R = (V_{OUT} − 1.12 V)/1.915 mA. A 0.1% resistor must be used to connect this circuit. If this pin is not used, connect it to AGND and set the CS2 current sense to high-side current sense mode (Register 0xFE19[7] = 1 binary).
5	VF	Feedforward/Voltage Sense/UVLO Protection. Three optional functions can be implemented with this pin: feedforward, primary side input voltage sensing, and input voltage UVLO protection. This pin is connected upstream of the output inductor through a resistor divider network. The nominal voltage at this pin should be 1 V. This signal is referred to AGND.
6	CS1	Primary Side Current Sense Input. This pin is connected to the primary side current sensing ADC and to the cycle-by-cycle current-limit comparator. This signal is referred to AGND. The resistors on this input must have a tolerance specification of ≤0.5% to allow for trimming. When not in use, connect this pin to AGND.
7	SR1	PWM Logic Output Drive. This signal is referred to AGND. When not in use, disable this pin.
8	SR2	PWM Logic Output Drive. This signal is referred to AGND. When not in use, disable this pin.
9	OUTA	PWM Logic Output Drive. This signal is referred to AGND. When not in use, disable this pin.
10	OUTB	PWM Logic Output Drive. This signal is referred to AGND. When not in use, disable this pin.
11	OUTC	PWM Logic Output Drive. This signal is referred to AGND. This pin can also be programmed as a synchronization signal output (SYNO). When not in use, disable this pin.
12	OUTD	PWM Logic Output Drive. This signal is referred to AGND. This pin can also be programmed as a synchronization signal output (SYNO). When not in use, disable this pin.
13	SYNI/FLGI	Synchronization Signal Input/External Signal Input to Generate a Flag Condition. When not in use, connect this pin to AGND.
14	SCL	I^2C/PMBus Serial Clock Input and Output (Open-Drain). This signal is referred to AGND.
15	SDA	I^2C/PMBus Serial Data Input and Output (Open-Drain). This signal is referred to AGND.
16	CTRL	PMBus Control Signal. It is recommended that a 1 nF capacitor be connected from the CTRL pin to AGND for noise debounce and decoupling. This signal is referred to AGND.

Pin No.	Mnemonic	Description
17	PG/$\overline{\text{ALT}}$	Power-Good Output (Open-Drain). Connect this pin to VDD through a pull-up resistor (typically 2.2 kΩ). This signal is referred to AGND. This pin is also used as an SMBus $\overline{\text{ALERT}}$ signal. (For information about the SMBus specification, see the PMBus Features section.)
18	VCORE	Output of the 2.6 V Regulator. Connect a decoupling capacitor of at least 330 nF from this pin to AGND, as close as possible to the ADP1052, minimizing the printed circuit board (PCB) trace length. It is recommended that this pin not be used as a reference or to generate other logic levels using resistive dividers.
19	VDD	Positive Supply Input. Voltage of 3.0 V to 3.6 V. This signal is referred to AGND. Connect a 2.2 µF decoupling capacitor from this pin to AGND, as close as possible to the ADP1052, minimizing the PCB trace length.
20	AGND	Common Analog Ground. The internal analog circuitry ground and digital circuitry ground are star connected to this pin through bonding wires.
21	RES	Resistor Input. This pin sets up the internal reference for the internal PLL frequency. Connect a 10 kΩ resistor (±0.1%) from this pin to AGND. This signal is referred to AGND.
22	ADD	Address Select Input. This pin programs the I^2C/PMBus address. Connect a resistor from ADD to AGND. This signal is referred to AGND.
23	RTD	Thermistor Input. Place a thermistor (R25 = 100 kΩ (1%), beta = 4250 (1%)) in parallel with a 16.5 kΩ (1%) resistor and a 1 nF filtering capacitor. This pin is referred to AGND. When not in use, connect this pin to AGND.
24	OVP	Overvoltage Protection. Use this signal for redundant overvoltage protection. This signal is referred to AGND.
	EP	Exposed Pad. The ADP1052 has an exposed thermal pad on the underside of the package. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the exposed pad be soldered to the PCB AGND plane.

TYPICAL PERFORMANCE CHARACTERISTICS

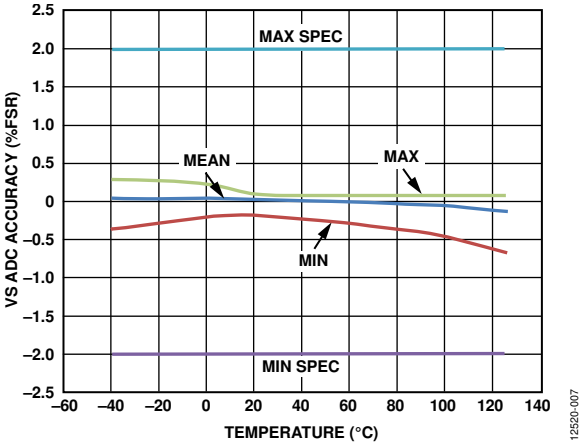

Figure 4. VS ADC Accuracy vs. Temperature (From 10% to 90% of FSR)

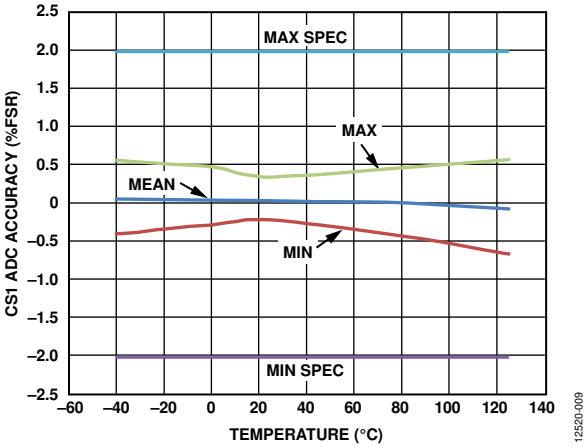

Figure 6. CS1 ADC Accuracy vs. Temperature (From 10%to 90% of FSR)

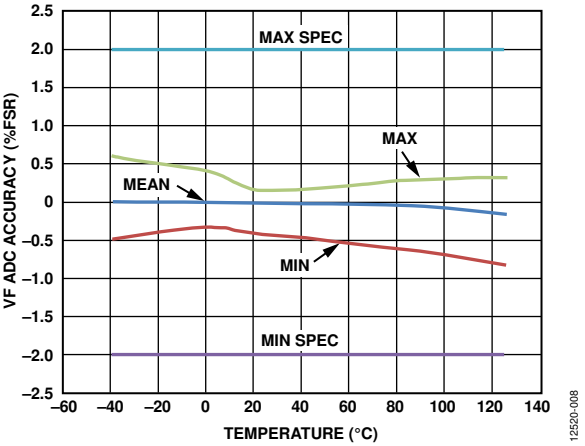

Figure 5. VF ADC Accuracy vs. Temperature (From 10% to 90% of FSR)

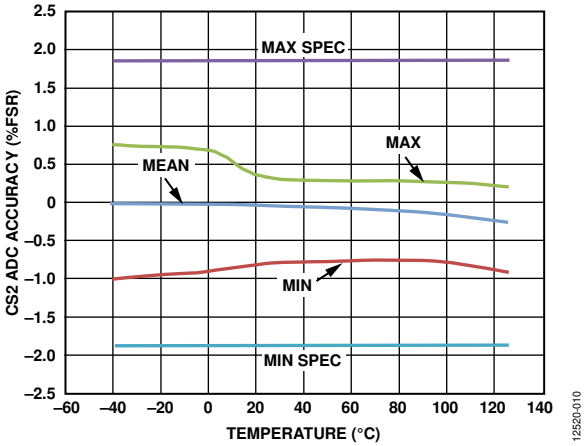

Figure 7. CS2 ADC Accuracy vs. Temperature (From 0 mV to 120 mV)

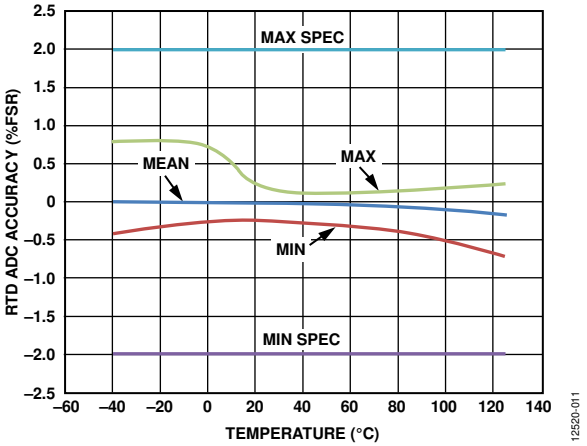

Figure 8. Resistance Temperature Detection (RTD) ADC Accuracy vs. Temperature (From 10% to 90% of FSR)

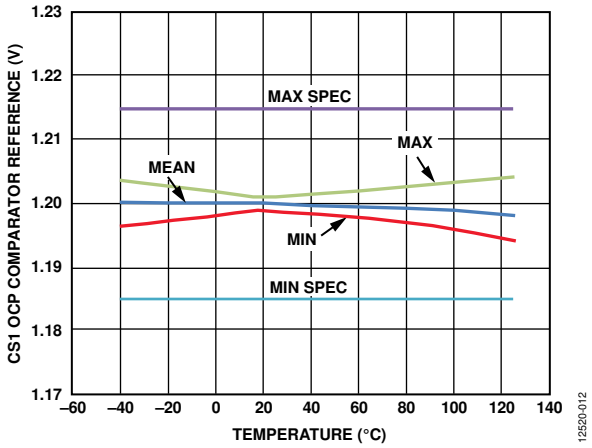

Figure 9. CS1 OCP Comparator Reference vs. Temperature (1.2 V Reference)

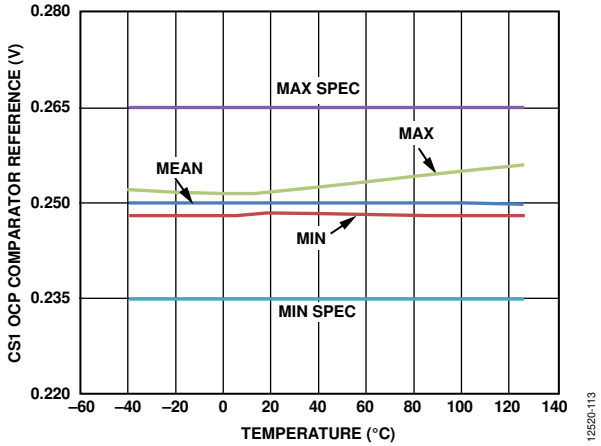

Figure 10. CS1 OCP Comparator Reference vs. Temperature (0.25 V Reference)

THEORY OF OPERATION

The ADP1052 is designed as a flexible, easy to use, digital power supply controller. The ADP1052 integrates the typical functions that control power supply, such as

- Output voltage sense and feedback
- Voltage feedforward control
- Digital loop filter compensation
- PWM generation
- Current, voltage, and temperature sense
- Housekeeping and I²C/PMBus interface
- Calibration and trimming

The main function of controlling the output voltage is through the feedback ADCs, the digital loop compensator, and the digital PWM engine.

The feedback ADCs feature a patented multipath architecture, with a high speed, low resolution (fast and coarse) ADC and a low speed, high resolution (slow and accurate) ADC. The ADC outputs are combined to form a high speed and high resolution feedback path. Loop compensation is implemented using the digital compensator. This proportional, integral, derivative (PID) compensator is implemented in the digital domain to allow easy programming of filter characteristics, which is of great value in customizing and debugging designs. The PWM engine generates up to six programmable PWM outputs for control of primary side FET drivers and synchronous rectification FET drivers. This programmability allows many generic and specific switching power supply topologies to be realized.

Conventional power supply housekeeping features, such as input voltage sense, output voltage sense, primary side current sense, and secondary side current sense, are included. The device offers an extensive set of protections, including overvoltage protection (OVP), overcurrent protection (OCP), overtemperature protection (OTP), undervoltage protection (UVP), and synchronous rectifier (SR) reverse current protection (RCP).

All of these features are programmable through the I²C/PMBus digital bus interface. This interface is also used for calibrations. Other information, such as input current, output current, and fault flags, is also available through this digital bus interface.

The internal EEPROM can store all programmed values and allows standalone control without a microcontroller. A free, downloadable GUI is available that provides all the necessary software to program the ADP1052. To obtain the latest GUI software and a user guide, visit http://www.analog.com/digitalpower.

The ADP1052 operates from a single 3.3 V power supply and is specified from −40°C to +125°C.

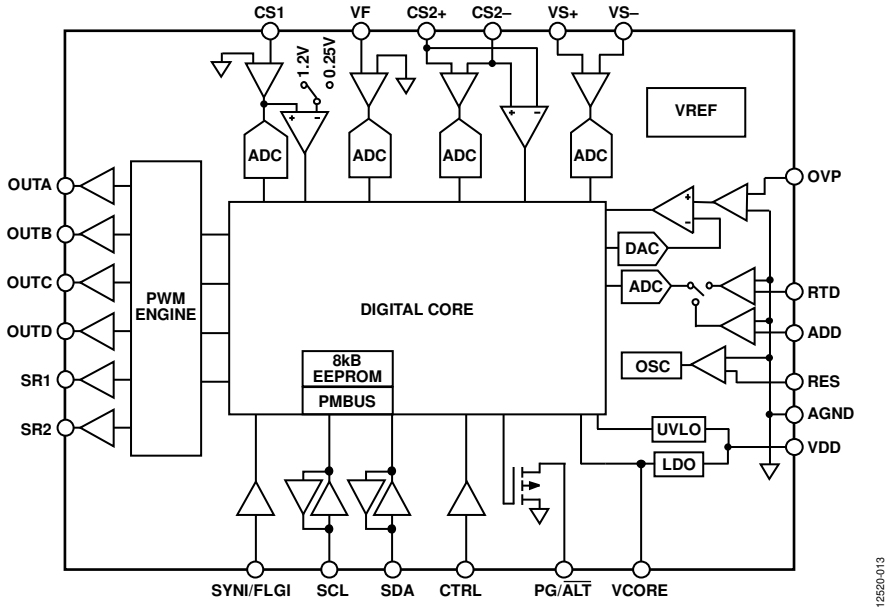

Figure 11. Functional Block Diagram

PWM OUTPUTS (OUTA, OUTB, OUTC, OUTD, SR1, AND SR2)

The PWM outputs control the primary side drivers and the synchronous rectifier drivers. They can be used for several topologies, such as hard-switched full bridge, zero-voltage-switched full bridge, phase shifted full bridge, half bridge, push pull, two-switch forward, active clamp forward, and interleaved buck. Delays between rising and falling edges are individually programmable. Special care is required to avoid shoot through and cross conduction. The ADP1052 GUI software is recommended to program these outputs.

Figure 12 shows an example configuration to drive a zero-voltage-switched full bridge topology with synchronous rectification. The QA, QB, QC, QD, QSR1, and QSR2 switches are driven separately by the PWM outputs (OUTA, OUTB, OUTC, OUTD, SR1, and SR2). Figure 13 shows an example of PWM settings for the power stage shown in Figure 12.

All PWM and SRx outputs are synchronized with each other. Therefore, when reprogramming more than one of these outputs, it is important to first update all of the registers and then latch the information into the shadow registers simultaneously. During the reprogramming operation, the outputs are temporarily disabled.

To ensure that new PWM timings and the switching frequency setting are programmed simultaneously, a special instruction is sent to the ADP1052 by setting Register 0xFE61[2:1] (the GO commands, see Table 181). It is recommended to disable the PWM outputs that are not in use via Register 0xFE53[5:0]. See the PWM Outputs Timing Registers section for additional information about the PWM timings.

SYNCHRONOUS RECTIFICATION

SR1 and SR2 are recommended to serve as the PWM control signals when synchronous rectification is in use. These PWM signals can be configured much like the other PWM outputs.

An optional soft start can be applied to the SR PWM outputs. Use Register 0xFE08[4:0] to program the SR soft start.

When the SR soft start is disabled (Register 0xFE08[1:0] = 00), the SRx pin signals are immediately turned on to their modulated PWM duty cycle values.

When the SR soft start is enabled (Register 0xFE08[1:0] = 11), the SR1 and SR2 rising edges move left from the t_{RX} + t_{MODU_LIMIT} position to the t_{RX} + $t_{MODULATION}$ position in steps that are set in Register 0xFE08[3:2]. In these positions, t_{RX} represents the rising edge timing of SR1 (t_{R5}) and the rising edge timing of SR2 (t_{R6}) (see Figure 68); t_{MODU_LIMIT} represents the modulation limit defined in Register 0xFE3C (see Figure 67); $t_{MODULATION}$ represents the real-time modulation value.

The SR soft start is applicable even when the SR1 and SR2 pins are not programmed for modulation. When the SR soft start is enabled, the SR1 and SR2 rising edges move left from the t_{RX} + t_{MODU_LIMIT} position to the t_{RX} position in steps that are set in Register 0xFE08[3:2].

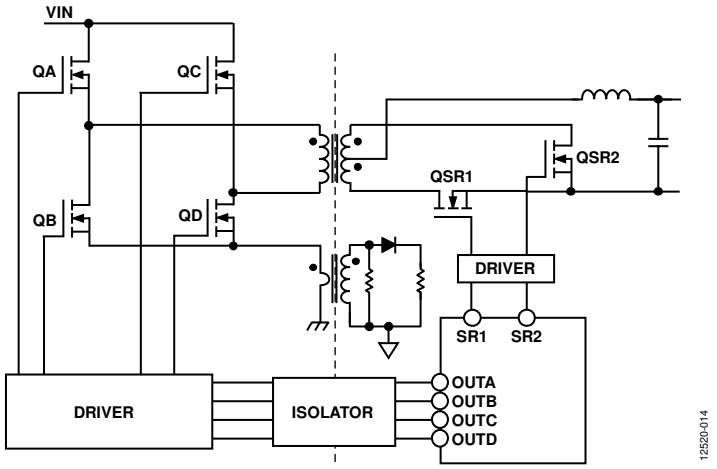

Figure 12. PWM Assignment for Zero-Voltage-Switched Full Bridge Topology with Synchronous Rectification

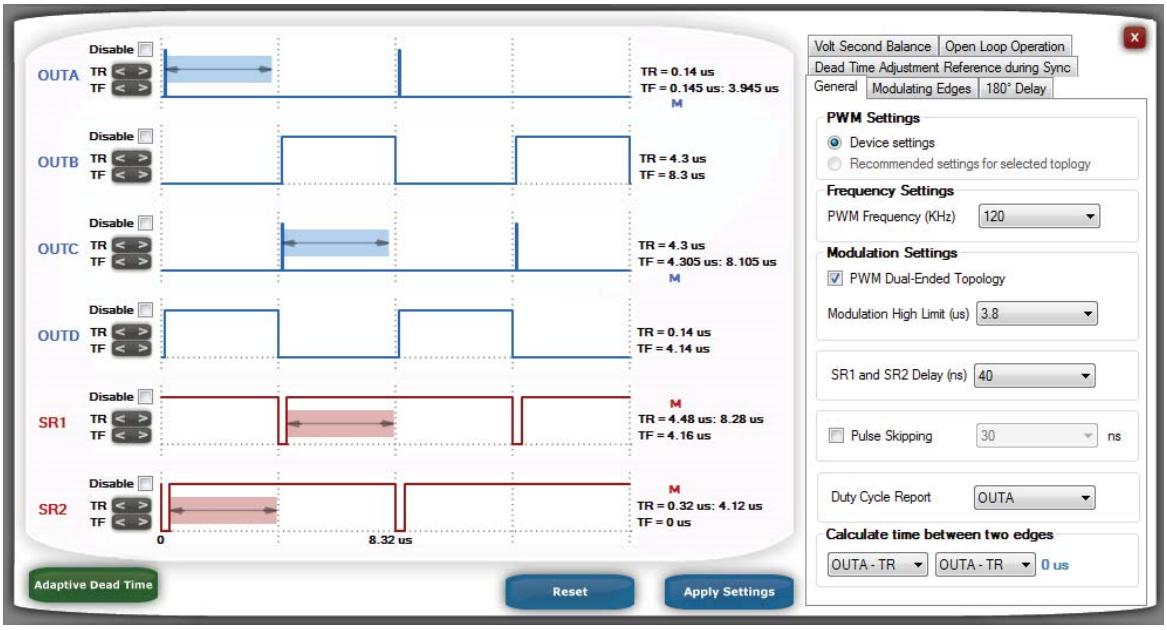

Figure 13. PWM Settings for Zero-Voltage-Switched Full Bridge Topology with Synchronous Rectification Using the ADP1052 GUI

The advantage of the SR soft start is that it minimizes the output voltage undershoot that occurs when the SR FETs are turned on without a soft start. The advantage of immediately and completely turning on the SRx signals is that they help minimize the voltage transient caused during a load step.

Using Register 0xFE08[4], the SR soft start can be programmed to occur one time only (the first time that the SRx signals are enabled) or every time that the SRx signals are enabled (for example, when the system enters or exits deep light load mode).

When programming the ADP1052 to use the SR soft start, ensure the correct operation of this function by setting the falling edge of SR1 (t_{F5}) to a lower value than the rising edge of SR1 (t_{R5}) and setting the falling edge of SR2 (t_{F6}) to a lower value than the rising edge of SR2 (t_{R6}). During the SR soft start, the rising edges of SRx move gradually from the right side (the t_{RX} + t_{MODU_LIMIT} position) to the left side to increase the duty cycle.

The ADP1052 is well suited for dc-to-dc converters in isolated topologies. Every time a PWM signal crosses the isolation barrier, a propagation delay is added because of the isolating components. Using Register 0xFE3A[5:0], an adjustable delay (0 ns to 315 ns in steps of 5 ns) can be programmed to move both SR1 and SR2 later in time to compensate for the added propagation delay. In this way, all the PWM edges can be aligned (see Figure 68).

PWM MODULATION LIMIT AND 180° PHASE SHIFT

The modulation limit register (Register 0xFE3C, see Table 159) can be programmed to apply a maximum modulation limit to any PWM signal, thus limiting the modulation range of any PWM output. If modulation is enabled, the maximum modulation limit is applied to all PWM outputs collectively. This limit, t_{MODU_LIMIT}, is the maximum time variation for the modulated edges from the default timing, following the configured modulation direction (see Figure 14).

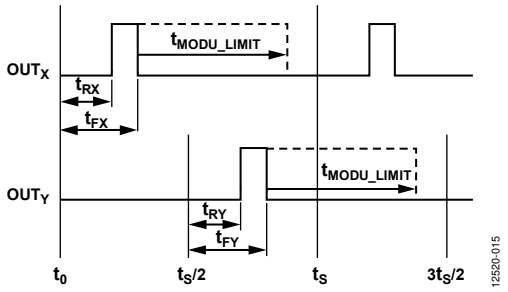

Figure 14. Setting Modulation Limits

There is no setting for the minimum duty cycle limit. Therefore, the user must set the rising edges and falling edges based on the case with the least amount of modulation.

Each least significant bit (LSB) in Register 0xFE3C corresponds to a different time step size, depending on the switching frequency (see Table 159). If the ADP1052 is to control a dual-ended topology (such as full bridge, half bridge, or push pull), enable the dual-ended topology mode using Register 0xFE13[6]; thus, the modulation limit in each half cycle is one half of the modulation value programmed by Register 0xFE3C.

The modulated edges cannot go beyond one switching cycle. To extend the modulation range for some applications, the 180° phase shift can be enabled using Register 0xFE3B[5:0].

When the 180° phase shift is disabled, the rising edge timing and the falling edge timing are referred to the start of the switching cycle (see t_{RX} and t_{FX} in Figure 14). When the 180° phase shift is enabled, the rising edge timing and the falling edge timing are referred to half of the switching cycle (see t_{RY} and t_{FY} in Figure 14, which are referred to $t_S/2$). Therefore, when the 180° phase shift

is disabled, the edges are always located between t_0 and t_S. When the 180° phase shift is enabled, the edges are located between $t_S/2$ and $3t_S/2$.

Use the 180° phase shift function to extend the maximum duty cycle in a multiphase, interleaved converter. Figure 15 shows a dual-phase, interleaved buck converter. The OUTC and OUTD PWM outputs are programmed as a 180° phase shift with the OUTA and OUTB PWM outputs.

Use the phase shedding function for light load efficiency improvement. See the Light Load Mode and Deep Light Load Mode section for more information. The ADP1052 GUI is recommended for evaluating this feature.

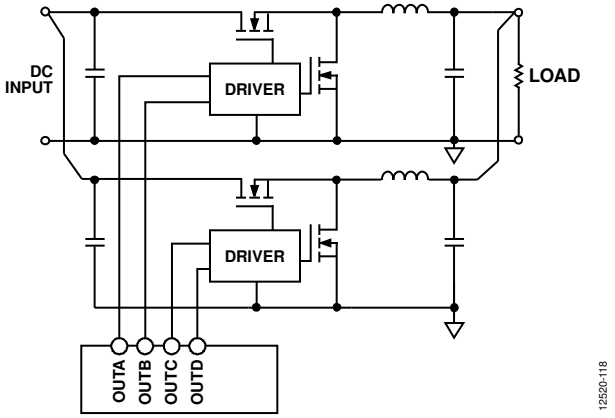

Figure 15. Dual-Phase Interleaved Buck Converter Controlled by the ADP1052

ADAPTIVE DEAD TIME COMPENSATION (ADTC)

The ADTC registers (Register 0xFE5A to Register 0xFE60 and Register 0xFE66) allow the dead time between the PWM edges to be adapted on the fly. The ADP1052 uses the ADTC function only when the CS1 current value (which represents the input current) falls below the ADTC threshold (programmed in Register 0xFE5A, see Table 174). The ADP1052 GUI allows the user to program the dead time values easily, and it is recommended to use the GUI for this purpose.

Before configuring the ADTC, its threshold must be programmed. Each individual PWM rising and falling edge (t_{RX} and t_{FX}) can then be programmed (Register 0xFE5B to Register 0xFE60) to have a specific dead time offset at a CS1 current of 0 A.

This offset can be positive or negative and is relative to the nominal edge position. When the CS1 current is between 0 A and the ADTC threshold, the amount of dead time is linearly adjusted in steps of 5 ns.

The averaging period of the CS1 current and the speed of the dead time adjustment can also be programmed in Register 0xFE66 to accommodate faster or slower adjustment.

For example, if the ADTC threshold is set to 0.8 A, t_{R1} has a nominal rising edge of 100 ns. If the ADTC offset setting for t_{R1} is 100 ns at a CS1 current of 0 A, t_{R1} moves to 200 ns when the CS1 current is 0 A and to 150 ns when the CS1 current is 0.4 A. Similarly, the ADTC can be applied in the negative direction.

LIGHT LOAD MODE AND DEEP LIGHT LOAD MODE

To facilitate efficiency over the load range, the following three operation modes can be configured in the ADP1052, according to the voltage on the CS2± pins (to delineate this voltage from the pins, this data sheet refers to this voltage as the CS2 current, or sometimes the CS2 threshold):

- Normal mode. In normal mode, the SR PWM outputs are in complement with the primary PWM outputs.
- Light load mode. The SR PWM outputs work, but they are in phase with the primary PWMs.
- Deep light load mode. All PWM outputs can be disabled.

Figure 16 shows the operation timing of a hard switched, full bridge converter. When the CS2 current (output current) drops across the light load mode threshold programmed by Register 0xFE19[3:0], the SR1 and SR2 PWM signals switch from complementary mode (normal mode) to in-phase mode (light load mode), as shown in Figure 16.

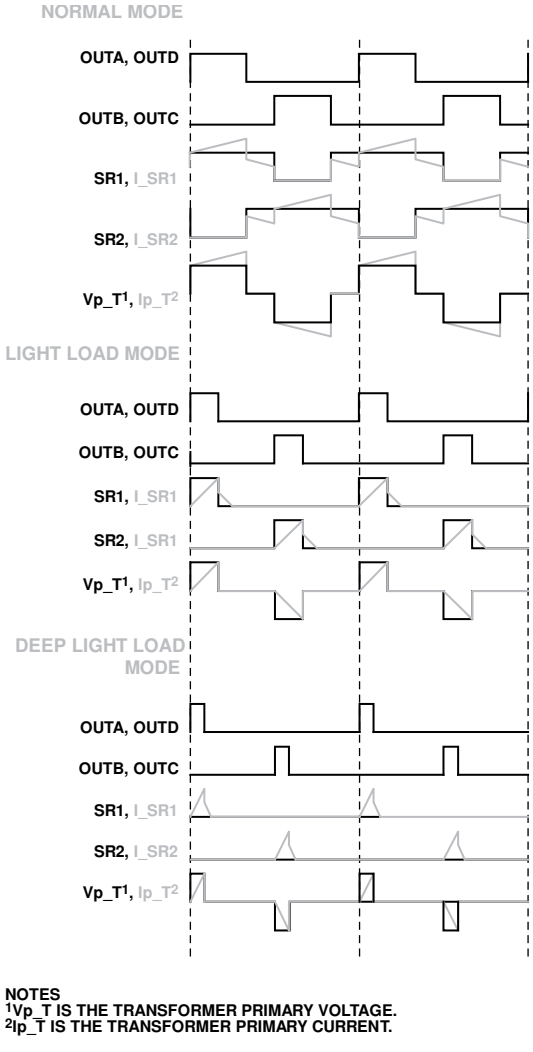

Figure 16. Light Load Mode and Deep Light Load Mode

To achieve normal operation of light load mode, keep in mind the following:

In a hard switched, full bridge topology having the same power stage as shown in Figure 12, if QA to QD are driven by OUTA to OUTD separately, program the SR1 output in complement with OUTB and OUTC in normal mode, and program the SR2 output in complement with OUTA and OUTD (as shown in Figure 16). In this case, the OUTA to OUTD outputs are all modulated.

In a zero-voltage-switched full bridge topology having the same power stage shown in Figure 12 and the PWM settings shown in Figure 13, SR1 is in complement with OUTC and SR2 is in complement with OUTA in normal mode. In light load mode, SR1 is in phase with OUTA, and SR2 is in phase with OUTC.

If using the hard switched full bridge, half bridge, and push pull topologies and the primary switches are controlled by OUTA and OUTB only, SR1 is in complement with OUTB, and SR2 is in complement with OUTA in normal mode. Then, in the light load mode, SR1 is in phase with OUTA, and SR2 is in phase with OUTB.

When the CS2 current drops across the deep light load mode threshold programmed by Register 0xFE1B[3:0], all PWM channels can be disabled by Register 0xFE1C[5:0]. This allows use of the ADP1052 in interleaved topologies, incorporating the automatic phase shedding function in light load mode.

In both light load mode and deep light load mode, the CS2 averaging speed for the threshold can be set from 41 µs to 328 µs in four discrete steps, using Register 0xFE1E[5:4]. Set the hysteresis in Register 0xFE1E[3:2].

The light load mode digital compensator is also used during light load mode and deep light load mode.

FREQUENCY SYNCHRONIZATION

The frequency synchronizing function of the ADP1052 includes the synchronization input (SYNI function of SYNI/FLGI) as a slave device and the synchronization output (SYNO, using the OUTC or OUTD pin) as a master device.

Synchronization as a Slave Device

The ADP1052 can be programmed to take the SYNI/FLGI pin signal as the reference to synchronize the internal programmed PWM clock with an external clock. Note that where the SYNI or the FLGI function only of the SYNI/FLGI pin is referenced, the pin name reflects the relevant function only (see the Pin Configuration and Function Descriptions section for full pin mnemonics and descriptions).

The frequency capture range requirement is for the period of the external clock that is applied at the SYNI pin to be 90% to 110% of the period of the internal programmed PWM clock. The minimum pulse width of the SYNI signal is 360 ns. From the rising edge of the SYNI signal to the start of the internal clock cycle, there is a 760 ns propagation delay. Additional delay time is programmed, using Register 0xFE11, to realize interleaving control with different controllers.

To achieve a smooth synchronization transition between asynchronous operation and synchronous operation, there is a phase capture range bit for synchronization in Register 0xFE12[6] for capturing the phase of the external clock signal. The ADP1052 detects the phase shift between the external clock signal and the internal clock signal when synchronization is enabled. When the phase shift falls within the phase capture range, synchronization begins.

The ADP1052 synchronizes to the external clock frequency as follows:

1. Bit 3 and Bit 0 in Register 0xFE12 enable the synchronization function; the ADP1052 starts to detect the period of the external clock signal applied at the SYNI/FLGI pin.
2. If all the periods of the consecutive 64 most recent cycles of the external clocks fall within 90% to 110% of the internal switching clock period, the ADP1052 uses the latest current cycle as the synchronization reference, and the period of the external clock is identified. This interval is t_2 or t_4, as shown in Figure 17. Otherwise, the ADP1052 discards this cycle and looks for the next cycle (frequency capture mode).
3. After the external clock period is determined, the ADP1052 detects the phase shift between the external clock (plus the delay time set by Register 0xFE11) and the internal PWM signal. If the phase shift is within the phase capture range, the internal and external clocks are synchronized (phase capture mode).
4. At this point, the PWM clock is synchronized with the external clock. Cycle-by-cycle synchronization starts.
5. If the external clock signal is lost at any time, or if the period exceeds the minimum limit (89% of the internal programmed frequency) or the maximum limit (114% of the internal programmed frequency), the ADP1052 takes the last valid external clock signal as the synchronization reference source. At the same time, the phase shift between the synchronization reference and the internal clock is detected. When the phase shift falls within the phase capture range, the PWM clock returns to the internal clock set by the internal oscillator. This interval is t_1 or t_3, as shown in Figure 17.

   This is the first synchronization unlock condition, called Synchronization Unlocked Mode 1, in which the switching frequency is out of range (range is 89% to approximately 114% of the internal programmed frequency).
6. If the period of the external SYNI signal changes significantly (for example, if the period difference between contiguous cycles exceeds 280 ns), the ADP1052 adopts the last valid external clock signal for the synchronization reference source. At the same time, the phase shift between the synchronization reference and the internal clock is detected. When the phase shift falls within the phase capture range, the PWM clock returns to the internal clock

set by the internal oscillator. This is the second synchronization unlock condition, called Synchronization Unlocked Mode 2, in which the phase shift exceeds 280 ns.

Figure 17 shows the synchronous operation. The internal frequency, f_{SW_INT}, is the internal free running frequency of the ADP1052. Before the synchronization is locked, the ADP1052 runs at f_{SW_INT}. The external frequency, f_{SW_EXT}, is the frequency of the external clock that the ADP1052 needs to synchronize. After synchronization is locked, the ADP1052 runs at f_{SW_EXT}.

The ADP1052 does not allow the switching frequency to run across the boundaries of 97.5 kHz, 195.5 kHz, or 390.5 kHz on-the-fly. Ensure that the external clock does not run across these boundaries; otherwise, the internal switching frequency cannot be set within ±10% of these boundaries.

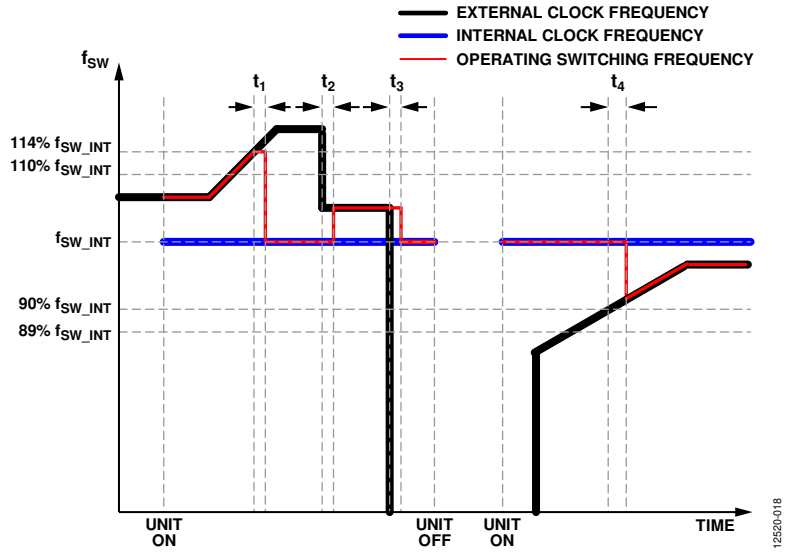

Figure 17. Synchronization Operation

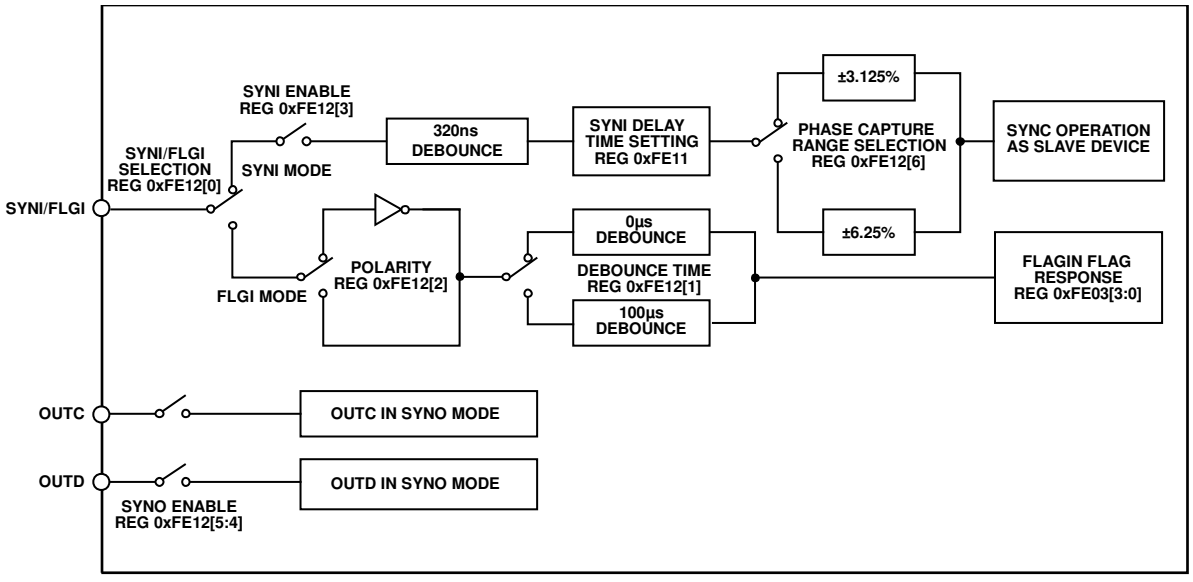

Figure 18. Synchronization Configuration

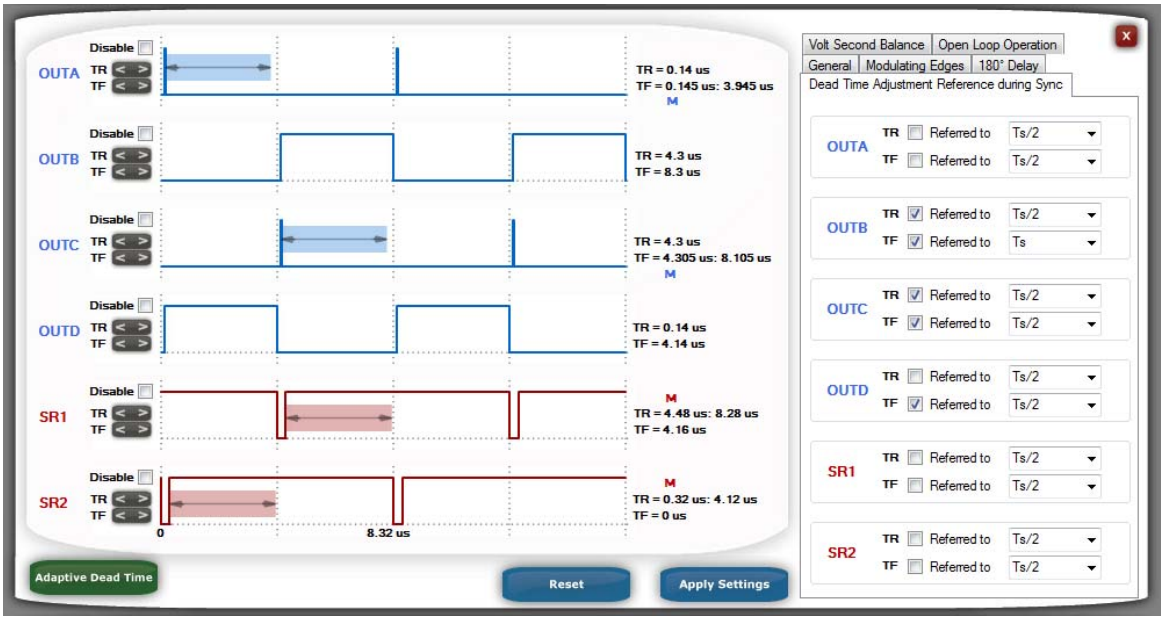

Figure 19. Edge Adjustment Reference During Synchronization

To ensure a constant dead time before and after synchronization, Register 0xFE6D to Register 0xFE6F can be set for edge adjustment referred to $t_S/2$ or t_S. For example, the falling edge of OUTA (t_{F1}) is referred to the ½ × t_S position, which means that the time difference between t_{F1} and ½ × t_S is a constant during synchronization transition. Figure 19 shows an example of the edge adjustment reference settings in a full bridge topology.

Synchronization as a Master Device

Use Register 0xFE12[5:4] to program the synchronization output (SYNO) function, in which the OUTC pin (Pin 11) or the OUTD pin (Pin 12) generates a synchronization reference clock output. When Bit 4 is set, OUTC generates a 640 ns pulse width clock signal that represents the internal switching frequency. When Bit 5 is set, OUTD generates a 640 ns pulse width clock signal that also represents the internal switching frequency.

To compensate the propagation delays in the synchronization scheme of the ADP1052, the synchronization output signal has a 760 ns lead time before the start of the internal switching cycle.

The synchronization output signal is always available when VDD is applied. The VDD_OV fault is the only fault condition that suspends the synchronization output signal.

OUTPUT VOLTAGE SENSE AND ADJUSTMENT

The output voltage sense and adjustment function is used for control, monitoring, and undervoltage protection of the remote output voltage. VS− (Pin 1) and VS+ (Pin 2) are fully differential inputs. The voltage sense point can be calibrated digitally to remove any errors due to external components. This calibration can be performed in the production environment, and the settings stored in the EEPROM of the ADP1052 (see the Power Supply Calibration and Trim section for more information).

For voltage monitoring, the READ_VOUT output voltage command (Register 0x8B) is updated every 10 ms. The ADP1052 stores every ADC sample for 10 ms and then calculates the average value at the end of the 10 ms period. Therefore, if Register 0x8B is read at least every 10 ms, a true average value is obtained. The voltage information is available through the I²C/PMBus interface.

The control loop of the ADP1052 features a patented multipath architecture. The output voltage is converted simultaneously by two ADCs: a high accuracy ADC and a high speed ADC. To provide a high performance and cost competitive solution, the complete signal is reconstructed and processed in the digital compensator.

Voltage Feedback Sensing (VS+, VS− Pins)

The output voltage feedback sense point on the power rail requires an external resistor divider (R1 and R2 in Figure 20) to bring the nominal differential mode signal to 1 V between the VS+ and VS− pins (see Figure 20). This external resistor divider is necessary because the VS ADC input range of the ADP1052 is 0 V to 1.6 V. When R1 and R2 are known, the VOUT_SCALE_LOOP parameter can be calculated using the following equation:

$$VOUT\_SCALE\_LOOP = R2/(R1 + R2)$$

In a 12 V system with resistor dividers of 11 kΩ and 1 kΩ, the VOUT_SCALE_LOOP can be calculated as follows:

$$VOUT\_SCALE\_LOOP = 1\ k\Omega/(11\ k\Omega + 1\ k\Omega) = 0.08333$$

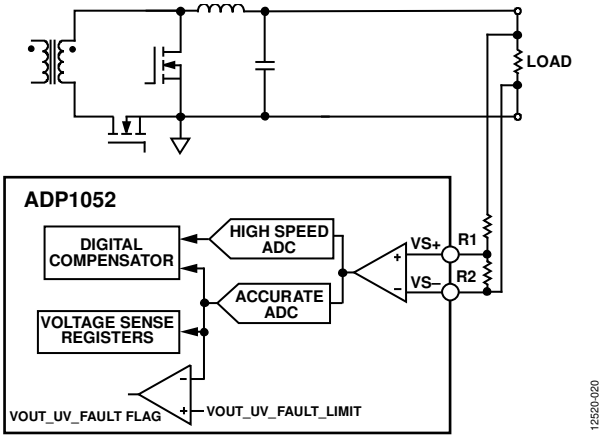

Figure 20. Voltage Sense Configuration

Voltage Sense ADCs

Two varieties of sigma-delta (Σ-Δ) ADCs are used in the ADP1052 feedback loop, as follows:

- Low frequency ADC, running at 1.56 MHz
- High frequency ADC, running at 25 MHz

The Σ-Δ ADCs have a resolution of one bit and operate differently from traditional flash ADCs. The equivalent resolution that can be obtained depends on the length of time the output bit stream of the Σ-Δ ADC is filtered.

The Σ-Δ ADCs also differ from Nyquist rate ADCs in that the quantization noise is not uniform across the frequency spectrum. At lower frequencies, the noise decreases. At higher frequencies, the noise increases (see Figure 21).

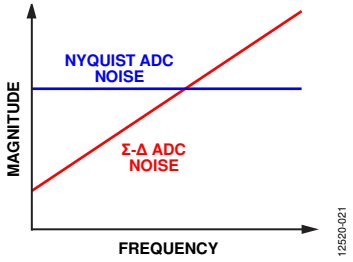

Figure 21. ADC Noise Performance

The low frequency ADC runs at approximately 1.56 MHz. For a specified bandwidth, the equivalent resolution is calculated as

$$\ln(1.56\ \text{MHz}/BW)/\ln(2) = N\ \text{bits}$$

For example, at a bandwidth of 95 Hz, the equivalent resolution/noise is

$$\ln(1.56\ \text{MHz}/95\ \text{Hz})/\ln(2) = 14\ \text{bits}$$

At a bandwidth of 1.5 kHz, the equivalent resolution/noise is

$$\ln(1.56\ \text{MHz}/1.5\ \text{kHz})/\ln(2) = 10\ \text{bits}$$

The high frequency ADC has a 25 MHz clock. It is comb filtered and outputs at the switching frequency into the digital compensator. See Table 5 for the equivalent resolution at selected sampling frequencies.

Table 5. Equivalent Resolutions for High Frequency ADC at Selected Switching Frequencies

f_{SW} (kHz)	High Frequency ADC Resolution (Bits)
49 to 87	9
97.5 to 184	8
195.5 to 379	7
390.5 to 625	6

The high frequency ADC has a range of ±25 mV. Using a base switching frequency of 97.5 kHz at an 8-bit high frequency ADC resolution, the quantization noise is 0.195 mV.

$$1\ \text{LSB} = 2 \times 25\ \text{mV}/2^8 = 0.195\ \text{mV}$$

When the switching frequency increases to 195.5 kHz at a 7-bit high frequency ADC resolution, the quantization noise is 0.391 mV ($1\ \text{LSB} = 2 \times 25\ \text{mV}/2^7 = 0.391\ \text{mV}$). Increasing the switching frequency to 390.5 kHz increases the quantization noise to 0.781 mV, as follows:

$$1\ \text{LSB} = 2 \times 25\ \text{mV}/2^6 = 0.781\ \text{mV}$$

Output Voltage Adjustment Commands

In the ADP1052, the voltage data for commanding or reading the output voltage or related parameters is in linear data format. The linear format exponent is fixed at −10 decimal (see the VOUT_MODE command, Register 0x20, in Table 22).

The following three basic commands are used for setting the output voltage:

- VOUT_COMMAND command (Register 0x21, Table 23)
- VOUT_MARGIN_HIGH command (Register 0x25, Table 27)
- VOUT_MARGIN_LOW command (Register 0x26, Table 28)

One of these three values is selected by the OPERATION command (Register 0x01, Table 14).

The VOUT_MAX command (Register 0x24, Table 26) sets an upper limit on the output voltage that the ADP1052 can command, regardless of any other commands or combinations.

During output voltage adjustment, use the VOUT_TRANSITION_RATE command (Register 0x27, Table 29) to set the rate (in mV/µs) at which the VS± pins change voltage.

DIGITAL COMPENSATOR

Use the internal programmable digital compensator to change the control loop of the power supply. A Type III digital compensator architecture is implemented in this device. This Type III compensator is reconstructed by a low frequency filter with input from the low frequency ADC and a high frequency filter with input from the high frequency ADC.

From the voltage sense ADC outputs to the digital compensator output, the transfer function of the digital compensator in z-domain is as follows:

$$H(z) = \frac{d}{204.8 \times m} \times \frac{z}{z-1} + \frac{c}{12.8} \times \frac{z-b}{z-a}$$

where:
d = low frequency filter gain register values (Register 0xFE30 for normal mode or Register 0xFE34 for light load mode).
m is the scale factor, as follows:

m = 1 when 49 kHz ≤ f_{SW} < 97.5 kHz.
m = 2 when 97.5 kHz ≤ f_{SW} < 195.5 kHz.
m = 4 when 195.5 kHz ≤ f_{SW} < 390.5 kHz.
m = 8 when 390.5 kHz ≤ f_{SW}.

c = high frequency filter gain register values (Register 0xFE33 for normal mode or Register 0xFE37 for light load mode).
b = high frequency filter zero register values ÷ 256 (Register 0xFE31 ÷ 256 for normal mode or Register 0xFE35 ÷ 256 for light load mode).
a = high frequency filter pole register values ÷ 256 (Register 0xFE32 ÷ 256 for normal mode or Register 0xFE36 ÷ 256 for light load mode).

To tailor the loop response to the specific application, set up the low frequency gain (represented by d), the zero location of the high frequency filter (represented by b), the pole location of the high frequency filter (represented by a), and the high frequency gain (represented by c). These can all be set up individually (see the Digital Compensator and Modulation Setting Registers section).

It is recommended that the ADP1052 GUI be used to program the compensator. The GUI displays the filter response, using a Bode plot in the s-domain, and calculates all stability criteria for the power supply.

To transfer the z-domain value to the s-domain, plug the following bilinear transformation equation into the H(z) equation:

$$z(s) = \frac{2f_{SW} + s}{2f_{SW} - s}$$

The filter introduces an extra phase delay element into the control loop. The digital compensator circuit sends the information about the duty cycle to the digital PWM engine at the beginning of each switching cycle (unlike an analog controller, which makes decisions on the duty cycle information continuously). There is an additional delay for ADC sampling and decimation filtering. This extra phase delay for phase margin (Φ) is expressed as follows:

$$\Phi = 360 \times f_C/f_{SW}$$

where f_C is the crossover frequency and f_{SW} is the switching frequency.

At one-tenth of the switching frequency, the phase delay is 36°. The GUI incorporates this phase delay into its calculations.

Note that the ADP1052 GUI does not account for other delays, such as gate driver and propagation delays.

Two sets of registers allow for two distinct compensator responses. The main compensator, called the normal mode compensator, is controlled by programming Register 0xFE30 to Register 0xFE33. The light load mode compensator is controlled by programming Register 0xFE34 to Register 0xFE37. The ADP1052 uses the light load mode compensator only when it operates in light load mode or deep light load mode.

In addition, a dedicated filter is used during soft start. The filter is disabled at the end of the soft start routine, after which time the voltage loop digital compensator is used. The soft start filter gain is a programmable value of 1, 2, 4, or 8, using Bits[1:0] in Register 0xFE3D.

CLOSED-LOOP INPUT, VOLTAGE FEEDFORWARD CONTROL, AND VF SENSE

The ADP1052 supports closed-loop input, voltage feedforward control to improve input transient performance. The voltage feedforward (VF) value is sensed by the feedforward ADC and divides the output of the digital compensator; the result is fed into the digital PWM engine. The input voltage signal can be sensed at the center tap in the secondary windings of the isolation transformer and must be filtered by a residual current device (RCD) circuit network to eliminate the voltage spike at the switching node. Alternatively, the input voltage signal can be sensed from a winding of the auxiliary power transformer.

The VF pin voltage (Pin 5) must be set to 1 V when the nominal input voltage is applied. The feedforward ADC sampling period is 10 µs. Therefore, the decision to modify the PWM outputs, based on the input voltage, is performed at this rate.

As shown in Figure 22, the feedforward scheme modifies the modulation value, based on the VF voltage. When the VF input is 1 V, the line voltage feedforward has no effect. For example, if the digital compensator output remains unchanged and the VF voltage changes to 50% of its original value (still greater than 0.5 V), the modulation of the edges of OUTx (that are configured for modulation) doubles.

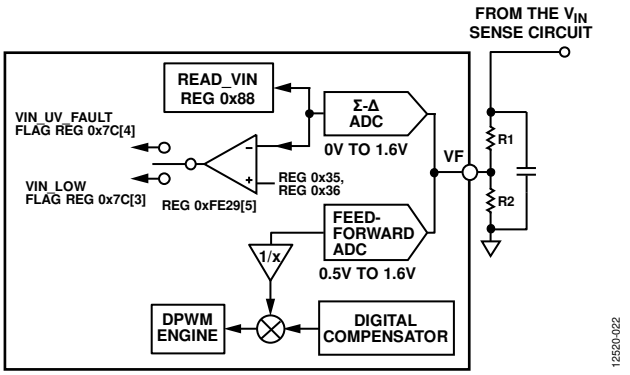

Figure 22. Closed-Loop Input Voltage Feedforward Configuration

As shown in Figure 23, if the digital compensator output remains unchanged and the VF voltage changes to 200% of its original value (still smaller than 1.6 V), the modulation of the OUTx edges (that are configured for modulation) is divided by 2. Use Register 0xFE3D, Bits[3:2] to program the optional input voltage feedforward function.

The VF pin also has a low speed, high resolution Σ-Δ ADC. The ADC has an update rate of 800 Hz with 11-bit resolution. The ADC output value is stored in Register 0xFEAC and converted to the READ_VIN command (Register 0x88). This value provides information for the input voltage monitoring and flag functions.

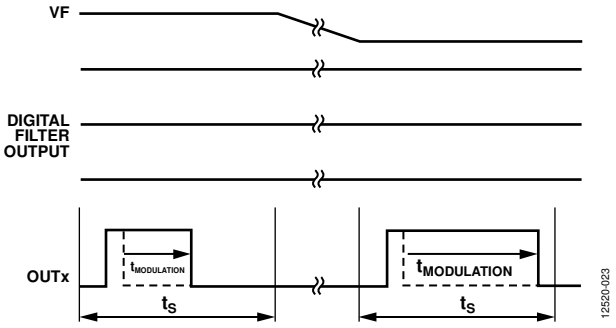

Figure 23. Closed-Loop Input Voltage Feedforward Changes Modulation Values

OPEN-LOOP INPUT, VF OPERATION

The ADP1052 can run in open-loop input voltage feedforward operation mode. In this mode, the input voltage is sensed as the feedforward signal for generation of the PWM outputs.

As shown in Figure 24, the digital compensator output is modified by a programmable modulation reference.

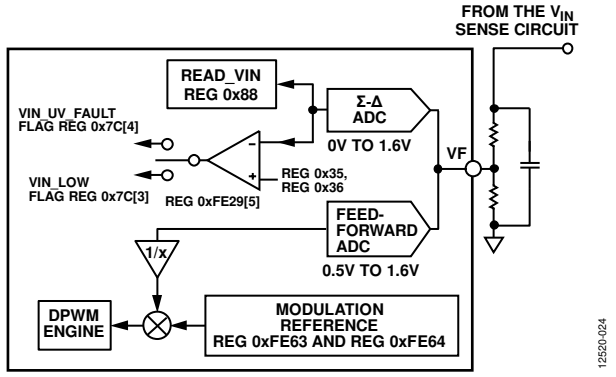

Figure 24. Open-Loop Feedforward Operation

The VF value, which represents the input voltage, is fed into the feedforward ADC to divide the modulation reference. The result of this division is then fed into the PWM engine. The duty cycle value is in inverse proportion to the input voltage.

Using the following equations:

$$D = \frac{V_{IN\_NOM}}{V_{IN}} \times (t_{REF} \times f_{SW})$$

and

$$V_{OUT} = \frac{V_{IN} \times D}{n}$$

where D is the duty cycle value and V_{OUT} is the output voltage.

The output voltage can be derived by

$$V_{OUT} = \frac{V_{IN\_NOM} \times (t_{REF} \times f_{SW})}{n}$$

where:
V_{IN_NOM} is the nominal input voltage.
V_{IN} is the input voltage.
t_{REF} is the modulation reference, which is set by Register 0xFE63 and Register 0xFE64.
f_{SW} is the switching frequency.
n is the turn ratio of the main transformer.

In the equation to derive V_{OUT}, the input voltage, V_{IN}, is cancelled out. Therefore, the output voltage does not change when the input voltage changes.

Register 0xFE63 and Register 0xFE64 set the modulation reference, based on the target output voltage and the nominal input voltage at which the VF pin voltage is 1 V (see Figure 24).

The PWM settings of open-loop input VF operation are similar to those of general closed-loop operation. The falling edge timings, rising edge timings, and modulation are set in the same manner as for closed-loop operation, by using Register 0xFE3E to Register 0xFE52.

- Register 0xFE09[4:3] sets the soft start speed of the modulation edges.
- Register 0xFE3D[6] enables open-loop feedforward operation.
- Register 0xFE3D[7] enables the soft start procedure of open-loop feedforward operation.

The flag settings of open-loop input VF operation are also similar to those of general closed-loop operation.

Because the output voltage is not regulated in the same manner as closed-loop operation, some settings are not functional, such as the V_{OUT} setting, the digital compensator settings, and the constant current mode setting. Other settings can be programmed in a manner that is similar to general closed-loop operation.

OPEN-LOOP OPERATION

The ADP1052 can also run in open-loop operation mode. In this mode, the rising edges and falling edges of the PWM outputs are fixed during normal operation. Therefore, the output voltage varies with the input voltage. The topologies include full bridge, half bridge, and push pull converters.

The PWM settings of open-loop operation are different from those of general closed-loop operation.

1. Set the rising edge timings and falling edge timings by using Register 0xFE3E to Register 0xFE4F. Typically, a duty cycle setting of ~50% is recommended for ease of zero-voltage-switching operation. A phase shift function of 180° is preferred to guarantee balanced PWM outputs.
2. Program Register 0xFE3C to a value of 0x00, which sets the modulation limit to 0 µs.
3. Apply negative modulation to the falling edges of all PWM outputs, OUTA to OUTD (or just one pair of them), for soft start. The soft start of SR1 and SR2 is not recommended.
4. Write 111111 binary to Register 0xFE67[5:0] to set all PWM channels to follow open-loop operation. Set Register 0xFE09[7] to enable the soft start procedure. The soft start speed is specified by Register 0xFE09[4:3].
5. Always set Register 0xFE09[2] = 1. The soft start ramp time is determined by $t_{F2} - t_{R2}$.

Because the output voltage is not regulated, some of the settings, such as the V_{OUT} setting, digital compensator settings, and constant current control, are not functional. Other settings can be programmed to be similar to those of general closed-loop operation.

CURRENT SENSE

The ADP1052 has two current sense inputs: CS1 (Pin 6) and CS2– and CS2+ (Pin 3 and Pin 4, respectively). These inputs sense, protect, and control the primary side input current and the secondary side output current. They can be calibrated to reduce errors caused by the external components.

CS1 Operation (CS1 Pin)

Current Sense 1 (CS1) is typically used for the monitoring and protection of the primary side current, which is commonly sensed using a current transformer (CT). The input signal at the CS1 pin is fed into an ADC for current monitoring. The range of the ADC is 0 V to 1.60 V. The input signal is also fed into an analog comparator for cycle-by-cycle current limiting and I_{IN} overcurrent fast protection, with a reference of 0.25 V or 1.2 V set by Register 0xFE1B[6]. The typical configuration for the CS1 current sense is shown in Figure 25.

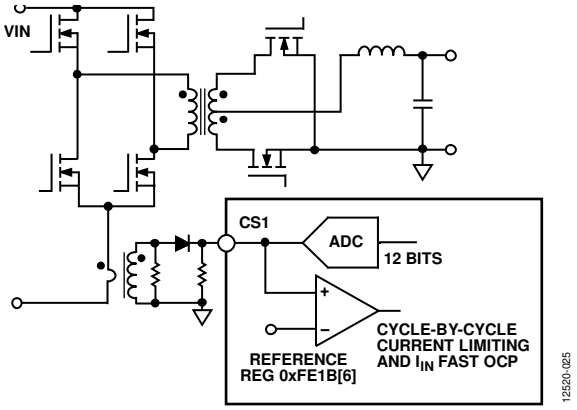

Figure 25. CS1 Operation

The CS1 ADC measures the average value of the primary side current. The ADC samples at a frequency of 1.56 MHz and reports a CS1 reading (12 bits) in the READ_IIN command (Register 0x89), with an asynchronously averaged rate of 10 ms, 63 ms, 126 ms, 252 ms, or 504 ms set by Register 0xFE65[2:0].

Various I_{IN} overcurrent fast fault limits and response actions can be set for CS1. These are described in the Current Sense and Limit Setting Registers section.

CS2 Operation (CS2–, CS2+ Pins)

Current Sense 2 (CS2) is typically used for the monitoring and protection of the output current. The full-scale range of the CS2 ADC is 120 mV. The differential inputs are fed into an ADC through a pair of external resistors that provide the necessary level shifting. The CS2+ and CS2– device pins are regulated to approximately 1.12 V by internal current sources.

Depending on the configuration of the current sense resistor, the ADP1052 must be programmed in low-side mode or high-side mode, using Register 0xFE19[7]. Typical configurations are shown in Figure 26 and Figure 27.

When using low-side current sensing, as shown in Figure 26, the current sources are 225 µA. Therefore, the required resistor value is 1.12 V/225 µA = 4.98 kΩ, and 4.99 kΩ resistors are preferred.

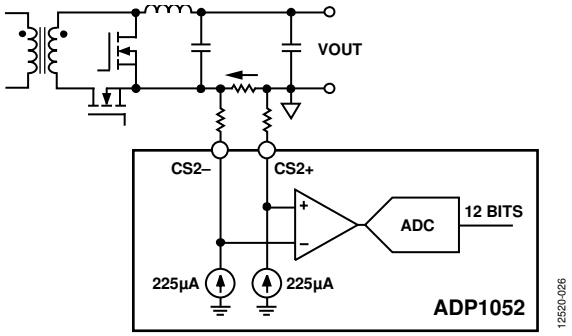

Figure 26. CS2 Low-Side Resistive Current Sense

When using high-side current sensing, as shown in Figure 27, the current sources are 1.915 mA. Therefore, the required resistor value is (V_{OUT} – 1.12 V)/1.915 mA. If V_{OUT} = 12 V, 5.62 kΩ resistors are required.

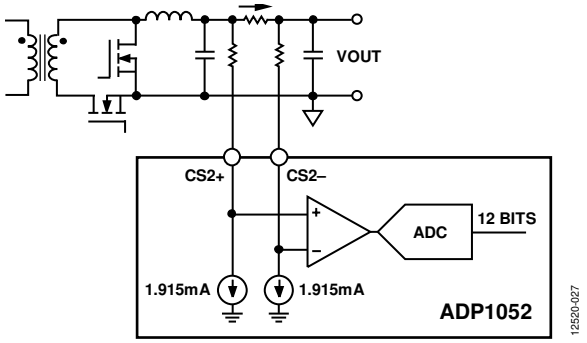

Figure 27. CS2 High-Side Resistive Current Sense