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3-Channel Digital Power Supply Controller

Data Sheet

ADP1053

FEATURES

- Configurable 8-PWM engine with up to 3 channels
- 2 independent digitally controlled channel outputs
- Voltage mode PWM control with 625 ps resolution
- Remote voltage sensing on both channels
- Programmable compensation filters
- Voltage feedforward option
- Flexible start-up sequencing and tracking
- Switching frequency: 50 kHz to 625 kHz
- Frequency synchronization
- Independent channel protections: OVP and OCP
- 2 independent OTP circuits
- Programmable fault protection sequence
- Volt-second balance and dual-phase current balance for interleaved configurations
- On-board EEPROM
- PMBus-compliant
- Graphical user interface (GUI) for ease of programming
- Available in a 40-lead, 6 mm × 6 mm LFCSP

APPLICATIONS

- AC-to-DC power supplies
- Isolated dc-to-dc power supplies
- Intermediate rail power supplies
- Nonisolated dc-to-dc power converter

GENERAL DESCRIPTION

The ADP1053, based on a voltage mode PWM architecture, is a flexible, application dedicated digital controller designed for isolated and nonisolated dc-to-dc power supply applications. The ADP1053 enables highly efficient power supply design and facilitates the introduction of intelligent power management techniques to improve energy efficiency at a system level.

The ADP1053 provides control, monitoring, and protection of up to three independent channel outputs. The eight flexible PWM outputs can be configured as three independent channels: two regulated channels with feedback control plus one additional unregulated channel with a fixed duty cycle. The frequency of these three channels can be programmed individually from 50 kHz to 625 kHz; all channels can be synchronized internally or to an external signal.

All eight PWM outputs can also be assigned to enable a single-channel solution, which may be required in high power, high efficiency applications.

Features include differential voltage sensing, fast current sensing, flexible start-up sequencing and tracking, and synchronization between devices to reduce low frequency system noise. Protection and monitoring features include overcurrent protection (OCP), undervoltage protection (UVP), overvoltage protection (OVP), and overtemperature protection (OTP).

SIMPLIFIED TYPICAL APPLICATION CIRCUIT

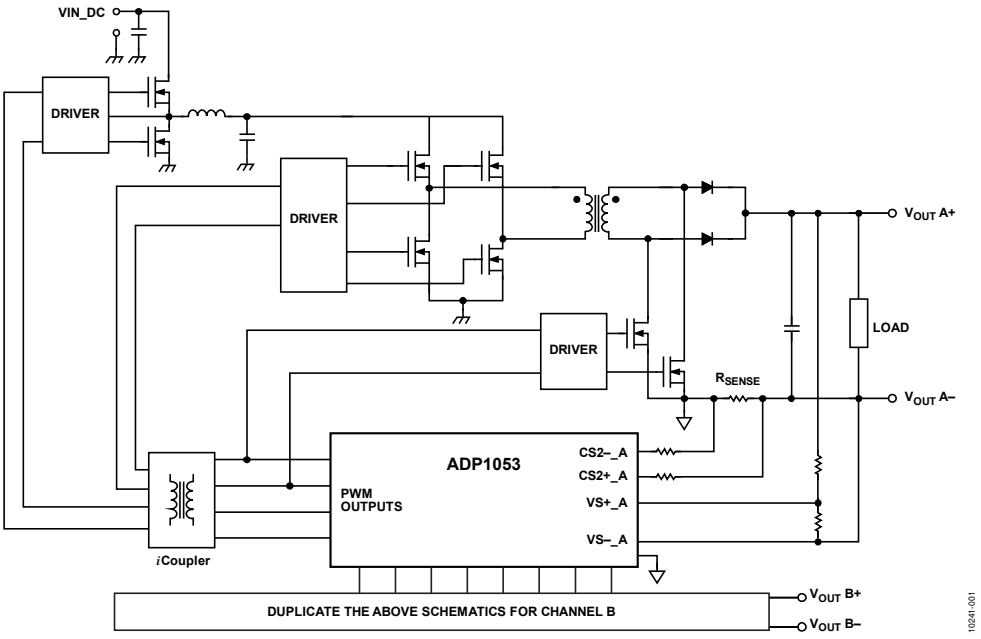

Figure 1.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
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EVALUATION KITS

- ADP1053 Evaluation Board

DOCUMENTATION

Data Sheet

- ADP1053: 3-Channel Digital Power Supply Controller DataSheet

User Guides

- UG-388: Daughter Card Evaluation Board for the ADP1053 Digital Power Supply Controller

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADP1053 Software

REFERENCE MATERIALS

Technical Articles

- Designing Digital Power Supplies With A State Machine

DESIGN RESOURCES

- ADP1053 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADP1053 EngineerZone Discussions.

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6/12—Rev. 0 to Rev. A

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Changes to Table 121 and Table 122 76
Changes to Ordering Guide 84

1/12—Revision 0: Initial Version

The ADP1053 provides local and remote differential sensing of the output voltage, which is converted to the digital domain using high speed, high resolution Σ-Δ converters. The proprietary conversion system maximizes the bandwidth of the converter and minimizes output noise due to digital quantization error, thus dramatically reducing the power consumption of the digital controller.

Configurable compensation networks provide three poles and two zeros to control feedback loop stability and optimize output response. In addition, a programmable feedforward feature can be enabled to enhance input voltage response.

The ADP1053 provides extensive protection and monitoring capabilities. For example, each regulated output has its own independent voltage threshold, and overvoltage protection is provided for each regulated output. The protection and monitoring features combine to eliminate the possibility of a single point of failure.

Fast overcurrent protection is provided to protect the system from short circuits. Accurate current sensing and overcurrent limit protections are also included. In addition, two overtemperature protection circuits are provided for use with 100 kΩ thermistors to sense the hot spots.

Other protection and monitoring features include a programmable power-on (PSON) function and power-good monitoring for Channel A and Channel B.

All these features are programmable through the PMBus/I²C interface. This interface is also used for calibration. Additional information, such as input current, output current, and fault flag status, can be read via the PMBus/I²C interface.

The built-in EEPROM is used to store programmed values and instructions. System reliability is improved through a built-in checksum and redundancy of critical circuits. In the event of a system fault, the EEPROM can be configured to capture the first instance of failure; this stored fault data can be analyzed to improve overall system reliability and reduce failure mode analysis time.

The ADP1053 is designed to maximize ease of use and reduce time to market with the provision of a comprehensive, easy to use graphical user interface (GUI) that allows programming of most parameters and protection and monitoring limits.

The ADP1053 is available in a 40-lead LFCSP package and operates from a single 3.3 V supply.

FUNCTIONAL BLOCK DIAGRAM

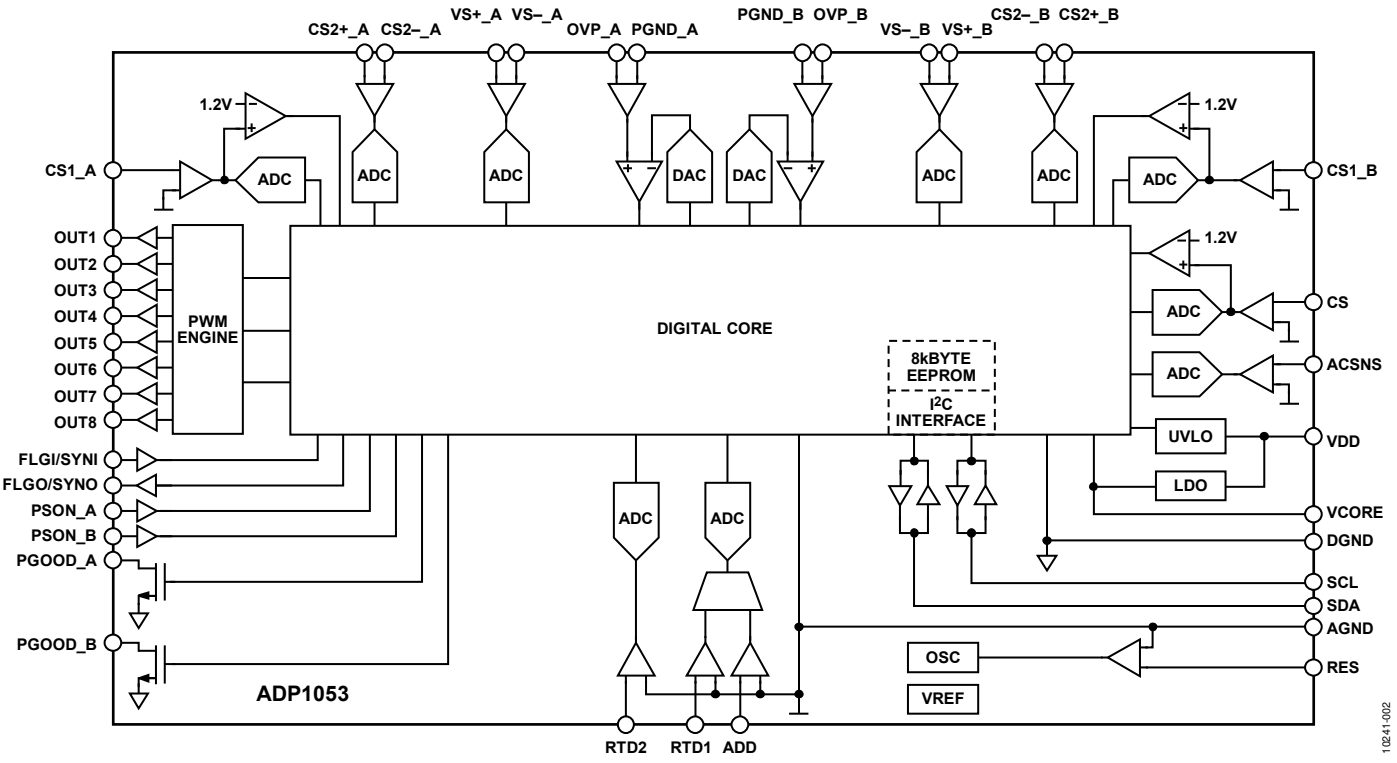


Figure 2.

SPECIFICATIONS

V_{DD} = 3.0 V to 3.6 V, T_A = −40°C to +125°C, unless otherwise noted. FSR = full-scale range.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY					
V_{DD}		3.0	3.3	3.6	V
I_{DD}	PWM pins unloaded				
	Normal operation (PSON high)		30		mA
	Power supply off (PSON low)		30		mA
	Shutdown (V_{DD} below UVLO)		100		µA
	During EEPROM programming		I_{DD} + 8		mA
POWER-ON RESET					
UVLO Threshold					
V_{DD} Rising				3.0	V
V_{DD} Falling		2.750	2.85	2.975	V
OVLO Threshold		3.7	3.9	4.1	V
OVLO Debounce	When set to 2 µs		2		µs
	When set to 500 µs		500		µs
VCORE PIN					
Output Voltage	330 nF capacitor between VCORE and DGND	2.3	2.5	2.7	V
OSCILLATOR AND PLL					
PLL Frequency	RES = 10 kΩ		200		MHz
DPWM Resolution			625		ps
VS_A, VS_B VOLTAGE SENSE					
Input Voltage	Differential voltage from VS+_A to VS−_A and from VS+_B to VS−_B	0	1	1.6	V
Input Voltage FSR			1.6		V
VS_A, VS_B Accurate ADCs					
Valid Input Voltage Range		0		1.5	V
ADC Register Update Rate			100		Hz
Resolution			12		Bits
Measurement Accuracy	From 0% to 100% of valid input voltage	−2.8		+2.1	% FSR
		−44.8		+33.6	mV
	From 10% to 90% of valid input voltage	−1.35		+2.1	% FSR
		−21.6		+33.6	mV
	From 900 mV to 1.1 V	−1.2		+1.65	% FSR
		−19.2		+26.4	mV
Temperature Stability	From 900 mV to 1.1 V	−0.1		+0.1	mV/°C
Common-Mode Voltage Offset	Voltage from VS−_A and VS−_B to AGND to achieve measurement accuracy	−200	0	+200	mV
VS_A, VS_B High Speed ADCs					
Equivalent Resolution	At 390.6 kHz switching frequency		6		Bits
Dynamic Range	Regulation voltage 300 mV to 1.4 V		±10		mV
VS_A, VS_B UVP	Based on VS_A, VS_B accurate ADC				
Threshold Accuracy	Same as accurate ADC measurement accuracy specifications				
Comparator Update Speed			10		ms
OVP_A, OVP_B PINS					
Threshold Accuracy		−1.7		+1.6	%
Propagation Delay (Latency)	Debounce time not included		58	110	ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
AC SENSE					
Input Voltage	Voltage from ACSNS to AGND	0	1	1.6	V
Input Voltage FSR			1.6		V
ACSNS ADC					
Valid Input Voltage Range		0	1	1.4	V
ADC Register Update Rate			800		Hz
Resolution			11		Bits
Measurement Accuracy	From 10% to 90% of valid input voltage	−1.25		+1.8	% FSR
		−20		+28.8	mV
	From 0% to 100% of valid input voltage	−5.4		+1.9	% FSR
		−86.4		+30.4	mV
ACSNS					
Threshold Accuracy	Same as ACSNS ADC measurement accuracy specifications				
Comparator Update Speed			1		ms
CS, CS1_A, CS1_B CURRENT SENSE					
Input Voltage	Voltage from CS/CS1_A/CS1_B to AGND	0		1.6	V
Input Voltage FSR			1.6		V
CS, CS1_A, CS1_B ADCs					
Valid Input Voltage Range		0	1	1.4	V
ADC Register Update Rate			100		Hz
Resolution			12		Bits
Measurement Accuracy	From 10% to 90% of valid input voltage	−1.3		+1.8	% FSR
		−20.8		+28.8	mV
	From 0% to 100% of valid input voltage	−5.6		+1.8	% FSR
		−89.6		+28.8	mV
Fast OCP					
Threshold Value		1.18	1.2	1.22	V
Propagation Delay (Latency)	Debounce/blanking time not included		58	110	ns
CS2_A, CS2_B CURRENT SENSE					
Input Voltage	Differential voltage from CS2+_A to CS2−_A and from CS2+_B to CS2−_B	0		120	mV
Input Voltage FSR			120		mV
Common-Mode Voltage	Common-mode voltage from CS2+_A/CS2−_A and CS2+_B/CS2−_B to AGND to achieve measurement accuracy	0.8	1	1.3	V
CS2_A, CS2_B ADCs					
Valid Input Voltage Range		0		120	mV
Resolution			12		Bits
Measurement Accuracy					
Low-Side Mode with User Trim	V_{OUT} = 0 V, 5 kΩ level-shifting resistor				
	From 0 mV to 110 mV	−1.85		+2.1	% FSR
		−2.22		+2.52	mV
	From 110 mV to 120 mV	−6.1		+1.5	% FSR
		−6.36		+0.84	mV
High-Side Mode with User Trim	V_{OUT} = 11 V, 5 kΩ level-shifting resistor				
	From 0 mV to 110 mV	−1.6		+2.3	% FSR
		−1.92		+2.76	mV
	From 110 mV to 120 mV	−5.3		+0.7	% FSR
		−6.36		+0.84	mV

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Accurate OCP					
Threshold Accuracy	Same as ADC accuracy				
ADC Register Update Rate			100		Hz
Current Sink (High Side)	V_{OUT} = 11 V, 5 kΩ level-shifting resistor	1.81	1.9	1.99	mA
Current Source (Low Side)	V_{OUT} = 0 V, 5 kΩ level-shifting resistor	180	230	280	µA
Fast Reverse Current Threshold (CS2+, CS2−)					
Threshold Accuracy	−17 mV setting	−23.2	−17	−9.6	mV
	−27 mV setting	−34.7	−27	−18.1	mV
Threshold Speed	Debounce time = 40 ns		110	150	ns
RTD1, RTD2 TEMPERATURE SENSE PINS					
Input Voltage	Voltage from RTDx to AGND	0		1.6	V
Input Voltage FSR			1.6		V
Source Current	Set to 46 µA	44.3	46	47.3	µA
	Set to 40 µA	38.6	40	42	µA
	Set to 30 µA	28.8	30	31.7	µA
	Set to 20 µA	18.8	20	21.5	µA
	Set to 10 µA (factory default setting)	9.1	10	11	µA
RTD1, RTD2 ADCs					
Valid Input Voltage Range		0		1.28	V
ADC Register Update Rate			100		Hz
Resolution			12		Bits
Measurement Accuracy	From 2% to 20% of valid input voltage	−0.3		+0.45	% FSR
		−4.8		+7.2	mV
	From 0% to 100% of valid input voltage	−2.6		+1.6	% FSR
		−41.6		+25.6	mV
Temperature Readings According to Internal Linearization Scheme	Factory trimmed to 10 µA; Register 0xFE80 and Register 0xFE81 = 0x00; NTC R_0 = 100 kΩ, 1%; beta = 4250, 1%; R_{EXT} = 16.5 kΩ, 1%				
	T = 25°C to 100°C			7	°C
	T = 100°C to 125°C			5	°C
OTP1, OTP2, OTW1, OTW2					
Threshold Accuracy	T = 85°C with 100 kΩ||16.5 kΩ	−0.9		+0.25	% FSR
		−14.4		+4	mV
	T = 100°C with 100 kΩ||16.5 kΩ	0.5		1.1	% FSR
		8		17.6	mV
Comparator Update Speed			10		ms
OUT1 TO OUT8, FLGO/SYNO PINS	Digital output pins				
Output Low Voltage, V_{OL}	Source current = 10 mA			0.4	V
Output High Voltage, V_{OH}	Source current = 10 mA	V_{DD} − 0.4			V
Rise Time	C_{LOAD} = 50 pF		4.5		ns
Fall Time	C_{LOAD} = 50 pF		2.5		ns
PGOOD_A, PGOOD_B PINS	Open-drain output pins				
Output Low Voltage, V_{OL}				0.4	V
PSON_A, PSON_B, FLGI/SYNI PINS	Digital input pins				
Input Low Voltage, V_{IL}				0.8	V
Input High Voltage, V_{IH}		V_{DD} − 0.8			V
SDA/SCL PINS					
Input Low Voltage, V_{IL}				0.8	V
Input High Voltage, V_{IH}		V_{DD} − 0.8			V
Output Low Voltage, V_{OL}				0.8	V
Leakage Current		−5		+5	µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SERIAL BUS TIMING	See Figure 3				
Clock Frequency			100	400	kHz
Glitch Immunity, t_{SW}				50	ns
Bus Free Time, t_{BUF}		1.3			µs
Start Setup Time, $t_{SU;STA}$		0.6			µs
Stop Setup Time, $t_{SU;STO}$		0.6			µs
Start Hold Time, $t_{HD;STA}$		0.6			µs
SCL Low Time, t_{LOW}		0.6			µs
SCL High Time, t_{HIGH}		0.6			µs
SCL, SDA Rise Time, t_R				20	ns
SCL, SDA Fall Time, t_F				20	ns
Data Setup Time, $t_{SU;DAT}$		100			ns
Data Hold Time, $t_{HD;DAT}$					
Read		125			ns
Write		300			ns
EEPROM					
EEPROM Update Time	Time from update command to EEPROM update completed (T_J = 25°C)		40		ms
Reliability					
Endurance[1]	T_J = 85°C	10,000			Cycles
	T_J = 125°C	1000			Cycles
Data Retention[2]	T_J = 85°C	20			Years
	T_J = 125°C	10			Years

[1] Endurance is qualified as per JEDEC Standard 22, Method A117, and is measured at −40°C, +25°C, +85°C, and +125°C. Endurance conditions are subject to change pending EEPROM qualification.
[2] Retention lifetime equivalent at junction temperature (T_J) = 125°C as per JEDEC Standard 22, Method A117. The derated lifetime is subject to change pending EEPROM qualification.

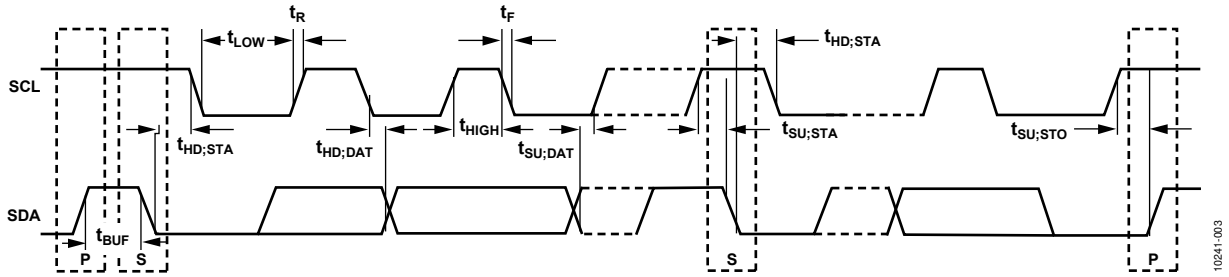


Figure 3. Serial Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (Continuous), V_{DD}	4.2 V
Digital Pins	−0.3 V to V_{DD} + 0.3 V
VS−_A, VS−_B, PGND_A, PGND_B to AGND, DGND	−0.3 V to +0.3 V
Other Analog Pins to AGND	3.6 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS Compliant Assemblies (20 to 40 sec)	260°C
ESD	
Charged Device Model	1.0 kV
Human Body Model	2.5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP (CP-40-10)	28.36	2.1	°C/W

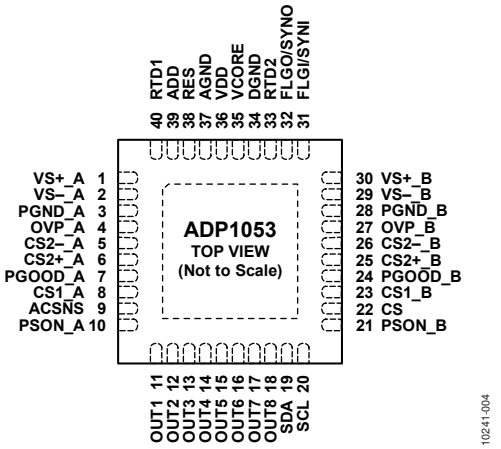
SOLDERING

It is important to follow the correct guidelines when laying out the PCB footprint for the ADP1053 and when soldering the part onto the PCB. For detailed information about these guidelines, see the AN-772 Application Note.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD ON THE UNDERSIDE OF THE PACKAGE SHOULD BE SOLDERED TO AGND.

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VS+_A	Noninverting Input of the Voltage Sense ADC for Channel A Loop Control. This signal is referenced to VS−_A.
2	VS−_A	Inverting Input of the Voltage Sense ADC for Channel A Loop Control. There should be a low ohmic connection to AGND.
3	PGND_A	Reference Pin for Channel A Overvoltage Protection (OVP_A).
4	OVP_A	Overvoltage Protection Comparator Input for Channel A. This signal is referenced to PGND_A.
5	CS2−_A	Inverting Input of the Differential Current Sense ADC for Channel A. The nominal voltage at this pin should be 1 V for optimal operation.
6	CS2+_A	Noninverting Input of the Differential Current Sense ADC for Channel A. The nominal voltage at this pin should be 1 V for optimal operation.
7	PGOOD_A	Power-Good Output (Open-Drain) for Channel A. This signal is referenced to AGND. This pin is controlled by the PGOOD_A flag and is driven low when the flag is set. The PGOOD_A flag is set when the POWER_SUPPLY_A, UVP_A, EEPROM_CRC, or SOFTSTART_FILTER_A flag is set. The ACSNS and OTW1 flags can also be programmed to be included.
8	CS1_A	CS1 ADC Input and Fast Current Sense Input for Channel A. This signal is referenced to AGND.
9	ACSNS	AC Sense ADC and Feedforward Operation Input. This pin is connected upstream of the main inductor through a resistor divider network. The nominal voltage at this pin should be 1 V. This signal is referenced to AGND.
10	PSON_A	Power Supply On Input for Channel A. This signal is referenced to AGND.
11	OUT1	OUT1 PWM Logic Output Drive. This pin is connected to the input of a FET driver; it can be disabled when not in use. This signal is referenced to AGND.
12	OUT2	OUT2 PWM Logic Output Drive. This pin is connected to the input of a FET driver; it can be disabled when not in use. This signal is referenced to AGND.
13	OUT3	OUT3 PWM Logic Output Drive. This pin is connected to the input of a FET driver; it can be disabled when not in use. This signal is referenced to AGND.
14	OUT4	OUT4 PWM Logic Output Drive. This pin is connected to the input of a FET driver; it can be disabled when not in use. This signal is referenced to AGND.
15	OUT5	OUT5 PWM Logic Output Drive. This pin is connected to the input of a FET driver; it can be disabled when not in use. This signal is referenced to AGND.
16	OUT6	OUT6 PWM Logic Output Drive. This pin is connected to the input of a FET driver; it can be disabled when not in use. This signal is referenced to AGND.
17	OUT7	OUT7 PWM Logic Output Drive. This pin is connected to the input of a FET driver; it can be disabled when not in use. This signal is referenced to AGND.
18	OUT8	OUT8 PWM Logic Output Drive. This pin is connected to the input of a FET driver; it can be disabled when not in use. This signal is referenced to AGND.

Pin No.	Mnemonic	Description
19	SDA	PMBus/I²C Serial Data Input and Output (Open-Drain). This signal is referenced to AGND.
20	SCL	PMBus/I²C Serial Clock Input and Output (Open-Drain). This signal is referenced to AGND.
21	PSON_B	Power Supply On Input for Channel B. This signal is referenced to DGND.
22	CS	CS ADC Input and Fast Current Sense Input for Overcurrent Protection and Current Monitoring. This signal is referenced to AGND.
23	CS1_B	CS1 ADC Input and Fast Current Sense Input for Channel B. This signal is referenced to AGND.
24	PGOOD_B	Power-Good Output (Open-Drain) for Channel B. This signal is referenced to AGND. This pin is controlled by the PGOOD_B flag and is driven low when the flag is set. The PGOOD_B flag is set when the POWER_SUPPLY_B, UVP_B, EEPROM_CRC, or SOFTSTART_FILTER_B flag is set. The ACSNS and OTW2 flags can also be programmed to be included.
25	CS2+_B	Noninverting Input of the Differential Current Sense ADC for Channel B. The nominal voltage at this pin should be 1 V for optimal operation.
26	CS2−_B	Inverting Input of the Differential Current Sense ADC for Channel B. The nominal voltage at this pin should be 1 V for optimal operation.
27	OVP_B	Overvoltage Protection Comparator Input for Channel B. This signal is referenced to PGND_B.
28	PGND_B	Reference Pin for Channel B Overvoltage Protection (OVP_B).
29	VS−_B	Inverting Input of the Voltage Sense ADC for Channel B Loop Control. There should be a low ohmic connection to AGND.
30	VS+_B	Noninverting Input of the Voltage Sense ADC for Channel B Loop Control. This signal is referenced to VS−_B.
31	FLGI/SYNI	Flag Input/Synchronization Input. When this pin is programmed as a flag input, an external signal can be input to generate a flag condition. The polarity is configurable. When this pin is programmed as a synchronization input, the input signal is used as a reference for the internal PWM frequencies. This signal is referenced to AGND.
32	FLGO/SYNO	Flag Output/Synchronization Output. When this pin is programmed as a flag output, it can be used to indicate the light load mode operation. The polarity is configurable. When this pin is programmed as a synchronization output, it can be used as a frequency reference for synchronization. This signal is referenced to AGND.
33	RTD2	Thermistor ADC Input from Zone 2. Typically, a 100 kΩ thermistor in parallel with a 16.5 kΩ resistor are placed from this pin to AGND. This signal is referenced to AGND.
34	DGND	IC Digital Ground. Reference ground for the digital circuitry of the ADP1053. This pin should be star-connected to AGND.
35	VCORE	Output of 2.5 V Regulator. Connect a 330 nF capacitor between this pin and DGND.
36	VDD	Positive Supply Voltage, 3.0 V to 3.6 V. This signal is referenced to AGND. Connect a 330 nF capacitor from VDD to AGND.
37	AGND	IC Common Analog Ground. This pin should be star-connected to DGND.
38	RES	Resistor Input. This pin sets the internal voltage reference for the ADP1053. Connect a 10 kΩ resistor (±1%) from RES to AGND. This signal is referenced to AGND.
39	ADD	PMBus/I²C Address Select Input. Connect a resistor from ADD to AGND (see the PMBus/I²C Address section). This signal is referenced to AGND.
40	RTD1	Thermistor ADC Input from Zone 1. Typically, a 100 kΩ thermistor in parallel with a 16.5 kΩ resistor are placed from this pin to AGND. This signal is referenced to AGND.
EP	Exposed Pad	The exposed pad on the underside of the package should be soldered to AGND.

APPLICATION CIRCUITS

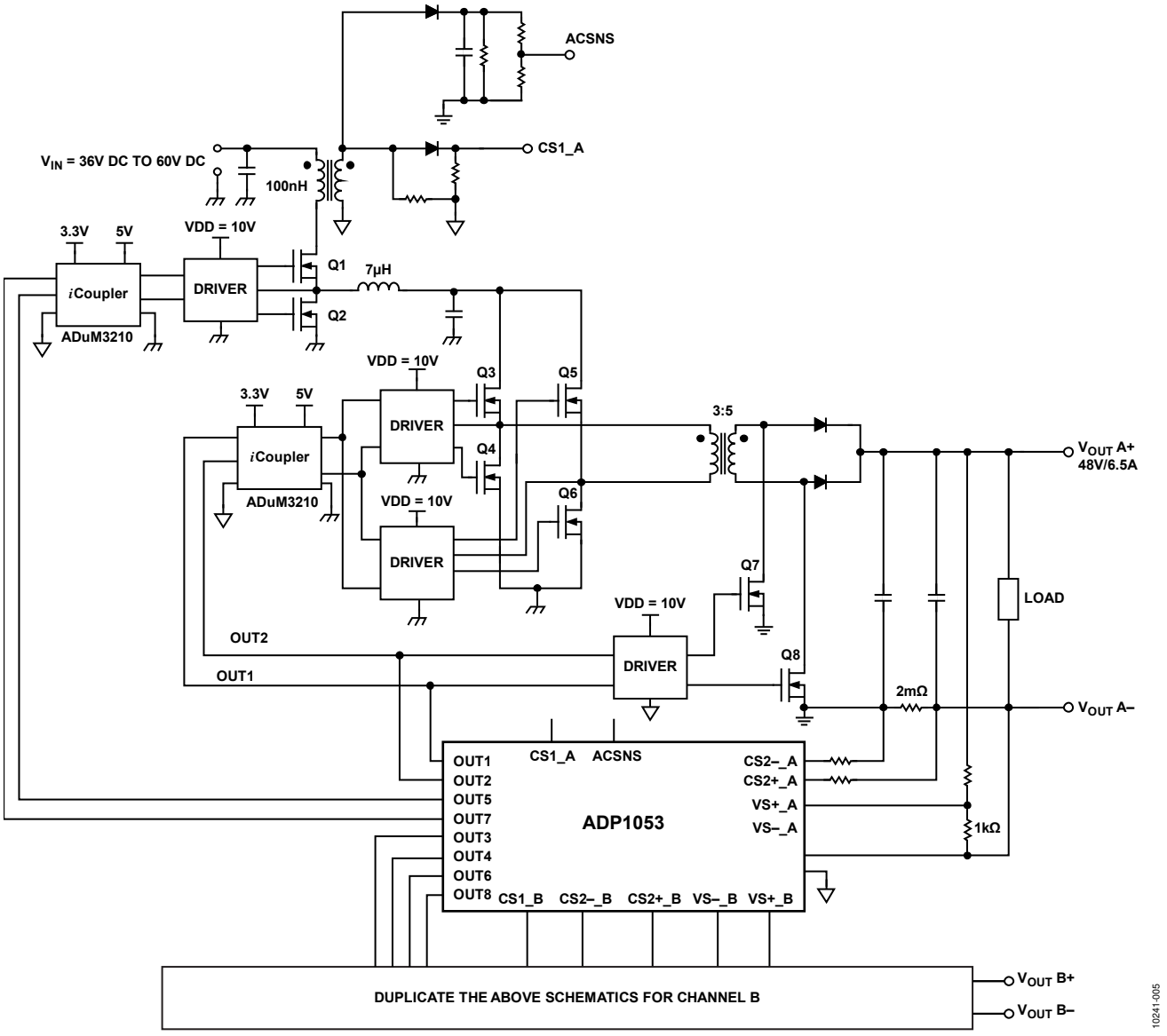


Figure 5. Application Circuit 1—Buck Preregulator Followed by a Fixed PWM Full-Bridge Topology with Synchronous Rectification

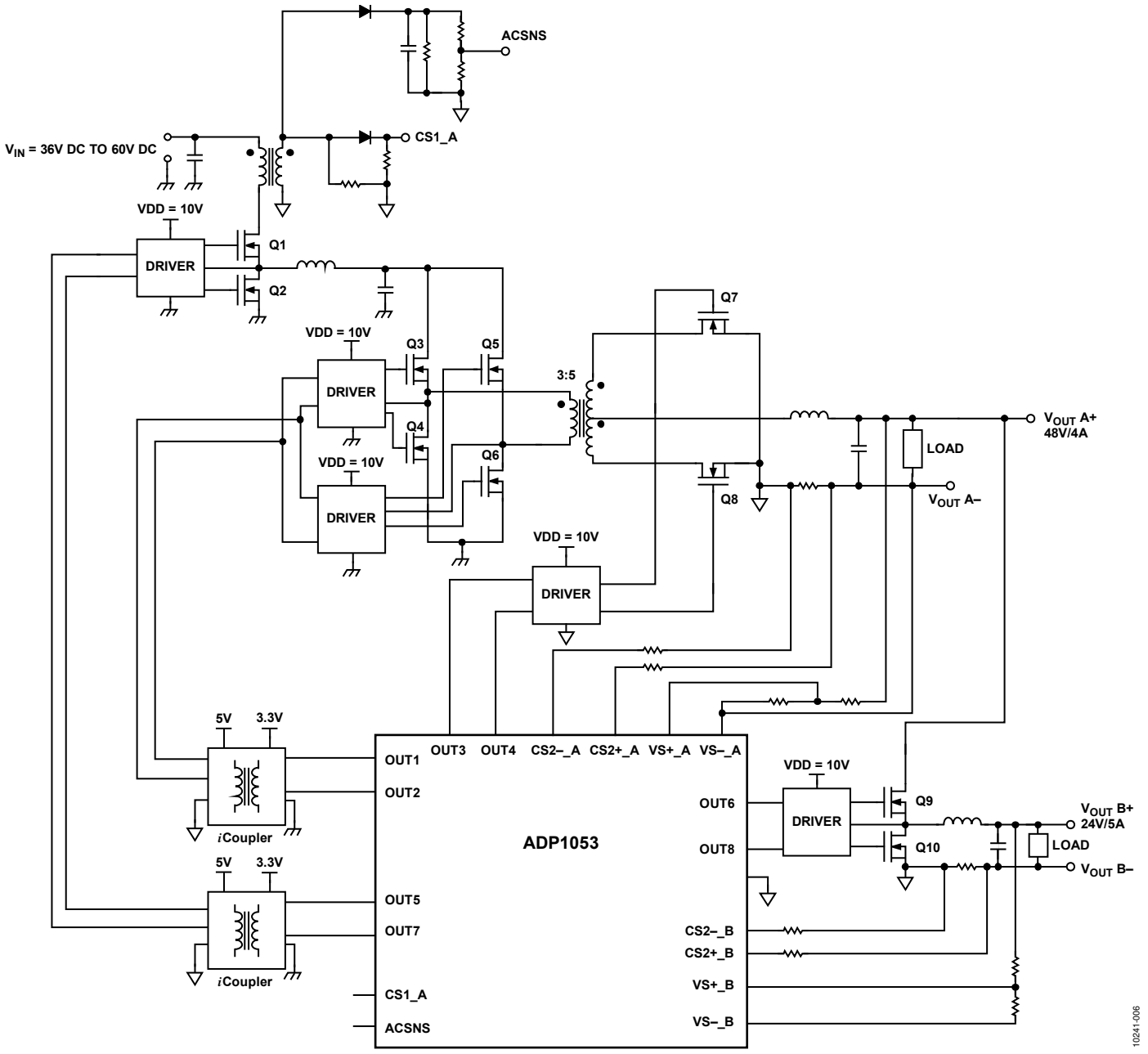


Figure 6. Application Circuit 2—Two Output Channels with Only One Full-Bridge Rectifier

THEORY OF OPERATION

PWM OUTPUTS (OUT1 TO OUT8)

The eight PWM outputs of the ADP1053 can be configured as two regulated channels with feedback control (Channel A and Channel B) and one additional unregulated channel with a fixed duty cycle (Channel C). The frequency of these channels can be individually programmed from 50 kHz to 625 kHz using Register 0xFE0A, Register 0xFE0B, and Register 0xFE0C, respectively.

The PWM engine in the ADP1053 is highly flexible. For example, the user can assign two PWM outputs to Channel A, two PWM outputs to Channel B, and four PWM outputs to Channel C. The user can also assign seven PWM outputs to Channel A and the remaining PWM output to Channel B. Alternatively, all eight PWM outputs can be assigned to Channel A for a single-channel solution.

As an example, Figure 5 shows a typical application circuit consisting of a buck preregulator followed by a fixed PWM full-bridge topology with synchronous rectification. In this example, only Channel A and Channel B are configured. As shown in Figure 5, the OUT1, OUT2, OUT5, and OUT7 PWM outputs are assigned to Channel A, and the OUT3, OUT4, OUT6, and OUT8 PWM outputs are assigned to Channel B. The Analog Devices, Inc., ADuM3210 *i*Coupler® device is used for isolation between the primary and secondary power stages.

All three channels can be enabled to support soft start. Channel A and Channel B use a closed-loop soft start scheme, which increases the reference voltage linearly and uses the feedback to increase the duty cycle gradually. When PWM outputs are assigned to Channel C with a fixed duty cycle, the duty cycle increases linearly until it reaches the preset value. For more information, see the Soft Start and Shutdown section.

Four of the eight PWM outputs (OUT3, OUT4, OUT7, and OUT8) can also be enabled for use as synchronous rectifier (SR) PWM control signals. These SR signals can be disabled during the power supply soft start ramp time. In addition, the SR PWM outputs can be programmed to initiate soft start when the outputs are enabled. For more information, see the Synchronous Rectifier (SR) Soft Start section.

All eight PWM outputs can be enabled or disabled using Register 0xFE60.

Timing of PWM Rising and Falling Edges

The timing of the rising and falling edges of the PWM outputs can be individually programmed. Special care must be taken to avoid shoothrough and cross-conduction. It is recommended that the ADP1053 graphical user interface (GUI) be used to program these outputs.

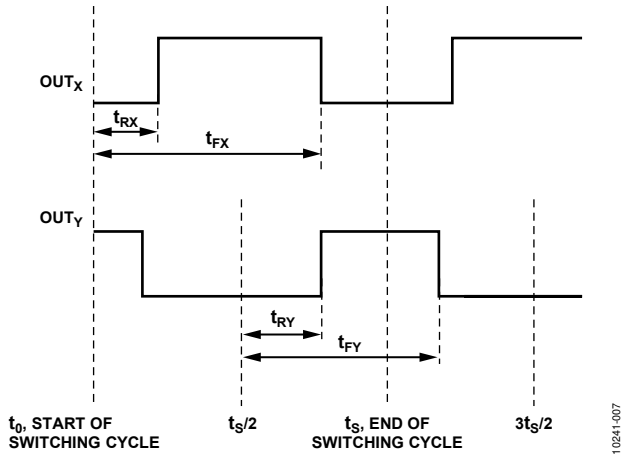


Figure 7. PWM Output Timing Diagram

Register 0xFE40 through Register 0xFE5F set the rising edge timing, falling edge timing, channel assignment, modulation schemes, and balance controls for the PWM outputs. For more information, see the PWM Output Timing Registers section.

One bit sets the 180° phase shift for each PWM output. When this bit is not set, the rising edge timing and the falling edge timing are referenced to the start of the switching cycle of the assigned channel (see t_{RX} and t_{FX} in Figure 7). When this bit is set, the rising edge timing and the falling edge timing are referred to half the switching cycle (see t_{RY} and t_{FY} in Figure 7).

Each LSB in the timing registers corresponds to a 5 ns step. The edge timing cannot exceed one switching cycle. Therefore, when the 180° phase shift is disabled, the edges are always located between t_0 and t_S; when the 180° phase shift is enabled, the edges are located between $t_S/2$ and $3t_S/2$.

Example Configuration of PWM Outputs

Table 6 provides example register settings that configure the OUT1 and OUT2 outputs for Channel A. In this example, the switching frequency of Channel A is 208.3 kHz, that is, a 4.8 µs switching cycle (Register 0xFE0A = 0x15).

GO Command

All eight PWM outputs work together. Therefore, when reprogramming more than one of these outputs, it is important to first update all the registers and then latch the information into the ADP1053 at the same time using the GO command (Bit 2 of Register 0xFE61). During reprogramming, the outputs are temporarily disabled. A special instruction is sent to the ADP1053 to ensure that new timing information is programmed simultaneously. It is recommended that unused PWM outputs be disabled.

Modulation Settings

Bits[3:0] in each PWM output setting register enable/disable rising and falling edge modulation and set the modulation sign. When the modulation sign is positive, an increase of the feedback filter output moves the edge to the right. When the sign is negative, an increase of the filter output moves the edge to the left.

For example, one of the most widely used modulation schemes is trailing edge modulation. To realize this scheme, Bits[3:0] of the PWM output setting registers are set to 0010.

Modulation Limits

Register 0xFE3C and Register 0xFE3D can be programmed to apply a maximum duty cycle modulation limit to PWM signals in Channel A and Channel B, respectively. As shown in Figure 8, this limit is the maximum time variation for the modulated edges from the default timing, following the configured modulation direction. There is no minimum duty cycle limit setting. Therefore, the user must set the rising edges and falling edges based on the case with the least modulation.

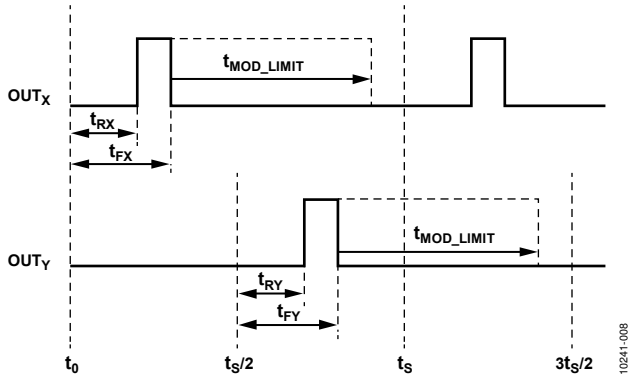


Figure 8. Setting Modulation Limits

The step size of an LSB in Register 0xFE3C and Register 0xFE3D depends on the switching frequency (see Table 5).

Table 5. LSB Step Size and Switching Frequency

Switching Frequency	LSB Step Size
48.8 kHz to 86.8 kHz	80 ns
97.7 kHz to 183.8 kHz	40 ns
195.3 kHz to 378.8 kHz	20 ns
390.6 kHz to 625.0 kHz	10 ns

The modulated edges cannot exceed one switching cycle. For PWM outputs without the 180° phase shift, such as OUT_X in Figure 7, the edges before and after modulation are always from t_0 to t_S. For PWM outputs with the 180° phase shift, such as OUT_Y in Figure 7, the edges before and after modulation are always from $t_S/2$ to $3t_S/2$.

The GUI provided with the ADP1053 is recommended for evaluating this feature.

Table 6. Example OUT1 and OUT2 Configuration

Register Setting	Configuration
Register 0xFE43, Bits[6:5] = 00	The PWM output OUT1 is assigned to Channel A with a frequency of 208.3 kHz.
Register 0xFE43, Bit 7 = 0	The reference for the rising and falling edges of OUT1 is the start of the switching cycle (180° phase shift disabled).
Register 0xFE40 = 0x01 and Register 0xFE42 = 0x00	The rising edge value is 0x010 (16 decimal), and the timing is set to 16 × 5 ns = 80 ns.
Register 0xFE41 = 0x20	The falling edge value is 0x200 (512 decimal), and the timing is set to 512 × 5 ns = 2.56 µs.
Register 0xFE47, Bits[6:5] = 00	The PWM output OUT2 is also assigned to Channel A with a frequency of 208.3 kHz.
Register 0xFE47, Bit 7 = 1	The reference for the rising and falling edges of OUT2 is half the switching cycle, $t_S/2$ (180° phase shift enabled).
Register 0xFE44 = 0x01 and Register 0xFE46 = 0x00	The rising edge value is 0x010 (16 decimal). Due to the 180° phase shift, the timing is set to 16 × 5 ns + 2.4 µs = 2.48 µs.
Register 0xFE45 = 0x20	The falling edge value is 0x200 (512 decimal), and the timing is set to 512 × 5 ns + 2.48 µs = 5.04 µs.

FREQUENCY SYNCHRONIZATION

Synchronization Output

The FLGO/SYNO pin can be programmed to generate a synchronization reference output using Bit 3 of Register 0xFE0F. The pin outputs a 320 ns pulse-width signal, whose frequency follows either Channel A or Channel C (programmable using Bit 3 of Register 0xFE0E).

To compensate for the propagation delays in the ADP1053 synchronization scheme, the SYNO signal has a 760 ns lead time before the start of the switching cycle.

Figure 9 shows an example of the SYNO timing when using Channel A as the reference.

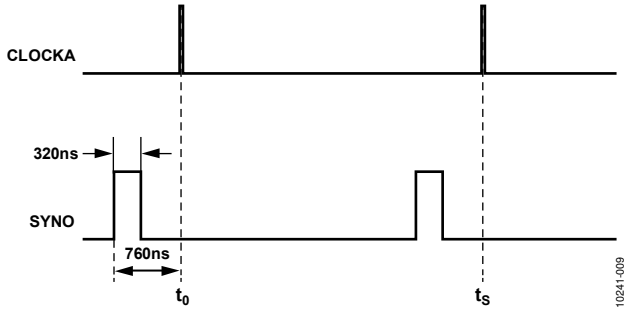


Figure 9. SYNO Timing

Synchronization Input

When the FLGI/SYNI pin is configured as a synchronization input, the external clock frequency at the pin must be between 90% and 110% of the internal switching frequency set by the channel's internal switching frequency register. If the switching cycle is out of this range or if there is no rising edge detected for 80 µs, the part exits synchronization mode, and each channel operates at its preset internal switching frequency. The maximum external synchronization clock frequency should be less than 625 kHz. If the FLGI/SYNI pin is programmed for the FLGI function, the synchronization function is disabled.

If two or more channels are enabled for synchronization, the valid synchronization frequency range is determined by the channel with the lowest synchronization multiple. The multiple is set using Bits[7:6] of Register 0xFE0A (Channel A), Register 0xFE0B (Channel B), and Register 0xFE0C (Channel C). If the multiple value is the same for two or more channels, the value set for Channel A has the highest priority and the value set for Channel C has the lowest priority.

Note that if Channel A or Channel C is synchronized with an external clock at the SYNI pin, the SYNO frequency is the preset internal frequency but not the operating switching frequency. For example, if the preset frequency of Channel A is 100 kHz and the SYNO frequency is configured to follow Channel A, the SYNO frequency is still 100 kHz even when the external synchronization clock is at 105 kHz.

To ensure proper operation of the synchronization mode, the synchronization multiple for at least one channel must be set to 1 (Bits[7:6] = 00).

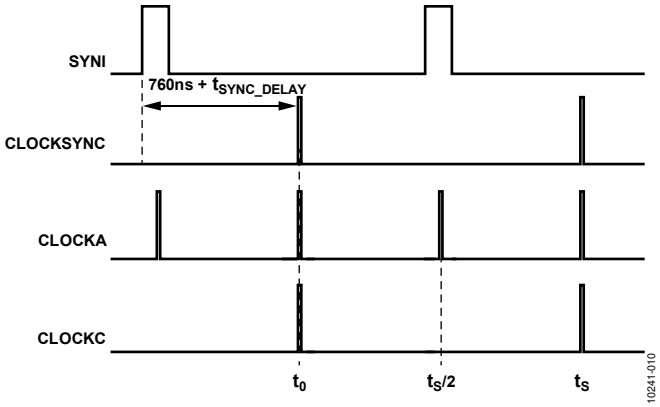


Figure 10. Synchronization Timing

VOLTAGE SENSE

Multiple voltage sense inputs on the ADP1053 are used for the monitoring, control, and protection of the power supply output. The voltage information is available through the PMBus/I²C interface. All voltage sense points can be calibrated digitally to remove any errors due to external components. This calibration can be performed in the production environment, and the settings saved in the EEPROM of the ADP1053. For more information, see the Power Supply Calibration and Trim section.

The update rate of the ADC from a control loop standpoint is set to the switching frequency. For example, if the switching frequency is set to 100 kHz, the ADC outputs a signal at a rate of 100 kHz to the control loop. Because the Σ-Δ ADC samples at 1.6 MHz, the output of the ADC is the average of the 16 readings per switching cycle.

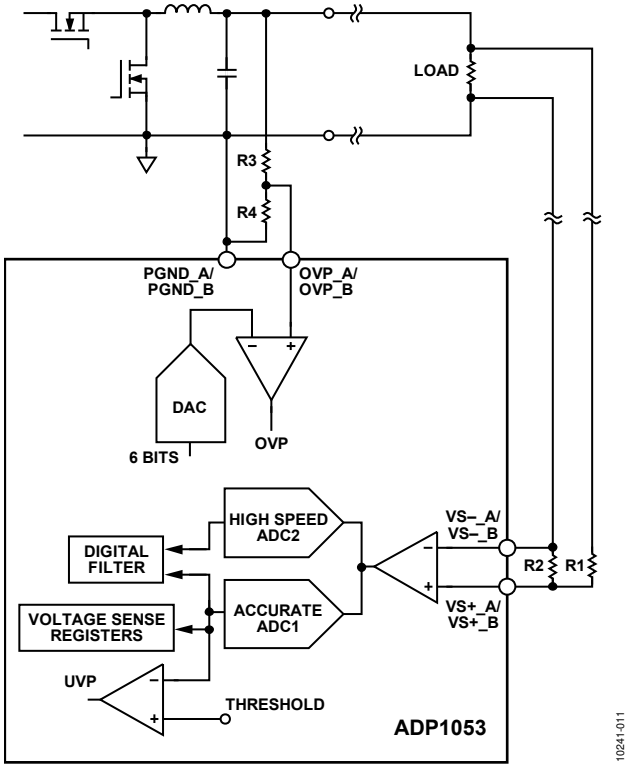


Figure 11. Voltage Sense Configuration

Voltage Feedback Sensing (VS+_A/VS+_B, VS−_A/VS−_B)

VS_A and VS_B are used for the control, monitoring, and undervoltage protection (UVP) of the remote output voltage of Channel A and Channel B, respectively. VS_A and VS_B are differential inputs; they function as the main feedback sense points for the control loop.

The VS_A/VS_B sense points on the power rail require an external resistor divider to bring the nominal voltage to 1 V at the VS pins (see Figure 11). This voltage provides the best accuracy for the ADC reading.

VS_A/VS_B use ADC1 for the high accuracy feedback loop and ADC2 for the high speed feedback loop.

ADCs

Σ-Δ ADCs have a resolution of one bit and operate differently from traditional flash ADCs. The equivalent resolution obtainable depends on how long the output bit stream of the Σ-Δ ADC is sampled.

Σ-Δ ADCs also differ from Nyquist rate ADCs in that the quantization noise is not uniform across the frequency spectrum. At lower frequencies the noise is lower, and at higher frequencies the noise is higher (see Figure 12).

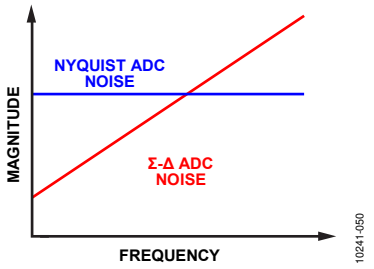


Figure 12. Noise Performance for Nyquist Rate and Σ-Δ ADCs

Two types of Σ-Δ ADCs are used in the feedback loop of the ADP1053: a low frequency ADC and a high frequency ADC.

The low frequency ADC runs at approximately 1.56 MHz. For a specified bandwidth, the equivalent resolution can be calculated as follows:

$$\ln(1.56\ M/BW)/\ln(2) = N \text{ bits}$$

For example, at a bandwidth of 95 Hz, the equivalent resolution/noise is

$$\ln(1.5\ M/95)/\ln(2) = 14 \text{ bits}$$

At a bandwidth of 1.5 kHz, the equivalent resolution/noise is

$$\ln(1.56\ M/1.5\ k)/\ln(2) = 10 \text{ bits}$$

The high frequency ADC has a clock of 25 MHz. It is comb filtered and outputs at the switching frequency (f_{SW}) into the digital filter.

The equivalent resolution for some sample frequencies is listed in Table 7.

Table 7. Equivalent Resolution for High Frequency ADC at Various Switching Frequencies

f_{SW} (kHz)	High Frequency ADC Resolution
48.8	9 bits
97.7	8 bits
195.3	7 bits
390.6	6 bits

The high frequency ADC has a range of ±10 mV. With the switching frequency (f_{SW}) set to 200 kHz, the quantization noise is 0.156 mV, which is one LSB ($2 \times 10\ mV/2^7 = 0.156\ mV$). Increasing f_{SW} to 400 kHz increases the quantization noise to 0.3125 mV (1 LSB = $2 \times 10\ mV/2^6 = 0.3125\ mV$).

OVP Sensing (OVP_A, OVP_B)

OVP_A and OVP_B are used for overvoltage protection of Channel A and Channel B, respectively. They are referenced to PGND_A and PGND_B.

The OVP_A/OVP_B sense points on the power rail require an external resistor divider to bring the nominal voltage to 1 V at the OVP_A/OVP_B pins (see Figure 11). This divided-down signal is internally fed into a comparator. The output of the comparator goes to the OVP fault flags. The OVP threshold level can be programmed from 0.75 V to 1.5 V. For more information about the OVP flags, see the Overvoltage Protection (OVP) Flags section.

CURRENT SENSE

The ADP1053 has five separate current sense inputs: CS, CS1_A, CS1_B, CS2_A, and CS2_B. These inputs are used to protect the power supply when the current exceeds the preset current limit. The registers that configure the current sensing inputs must be calibrated to remove errors due to external components. For more information, see the Power Supply Calibration and Trim section.

CS and CS1 (CS1_A/CS1_B) Sensing

CS1_A and CS1_B are typically used for the monitoring and protection of Channel A and Channel B, respectively, whereas CS is used for the unregulated Channel C. Generally, the current inputs are sensed through a current transformer (CT). The input signals at the pins are fed into ADCs for current monitoring. The valid input range of these ADCs is from 0 V to 1.4 V. The input signal is also fed into a comparator for fast overcurrent protection (fast OCP). Typical configurations for current sensing are shown in Figure 13 and Figure 14.

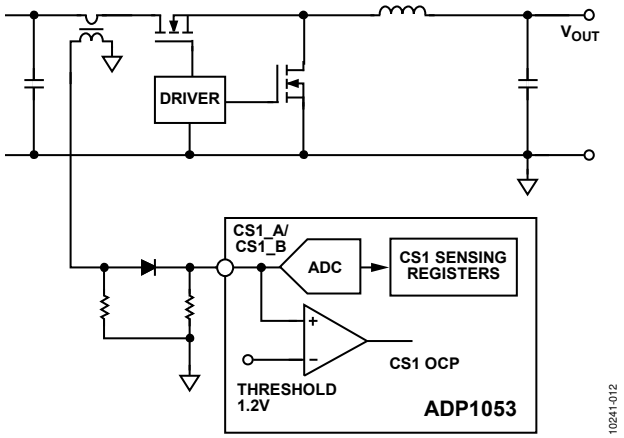


Figure 13. Current Sense 1 (CS1) Operation

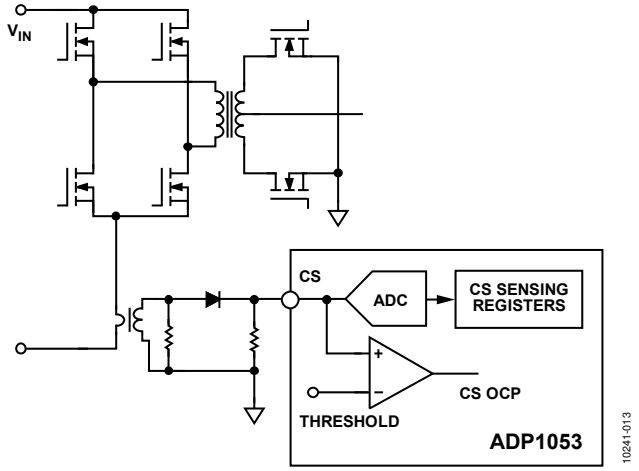


Figure 14. Current Sense (CS) Operation

The CS ADCs measure the average current information, which can be read via the PMBus/I²C interface. This information can also be used for volt-second balance or current balance control. For more information, see the Volt-Second Balance and Current Balance section.

CS2 (CS2+_A/CS2+_B, CS2−_A/CS2−_B) Sensing

CS2_A and CS2_B are typically used for the monitoring and protection of Channel A and Channel B, respectively. CS2_A/CS2_B provide accurate current sensing and monitoring of OCP conditions.

CS2_A/CS2_B current sensing can be configured using a low-side sense resistor or a high-side sense resistor. Depending on the common-mode voltage of the current sensing resistor, the part must be programmed for low-side or high-side mode using Bit 7 of Register 0xFE1A and Register 0xFE1B.

Typical configurations are shown in Figure 15 and Figure 16. The differential inputs are fed into an ADC through a pair of external resistors. Internal matching current sources (nominal value of 200 µA for low-side sensing and 2 mA for high-side sensing) are used to regulate the common-mode voltage of the CS2 pins at approximately 1 V.

For both high-side and low-side current sensing, it is recommended that a 500 pF to 1000 pF capacitor be connected from the CS2_A/CS2_B pins to AGND.

When using low-side resistor current sensing, as shown in Figure 15, the common-mode voltage at the sensing resistor is approximately 0 V. The current sources are 200 µA in low-side current sensing mode. Two matching 5 kΩ resistors are recommended.

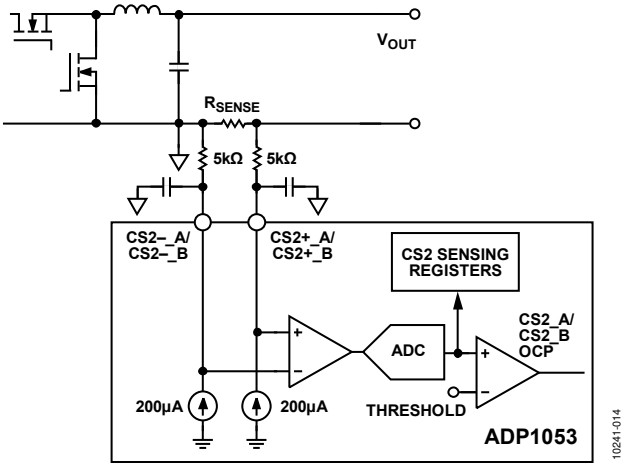


Figure 15. CS2 Low-Side Resistive Current Sensing

When high-side resistor current sensing is required, as shown in Figure 16, the resistor value is calculated based on a 2 mA high-side current source, as follows:

$$R = (V_{OUT} - 1\text{ V})/2\text{ mA}$$

For example, in a 28 V system with high-side current sensing, the value of the resistors used at the CS2 pins is calculated by

$$R = (28\text{ V} - 1\text{ V})/2\text{ mA} = 13.5\text{ k}\Omega$$

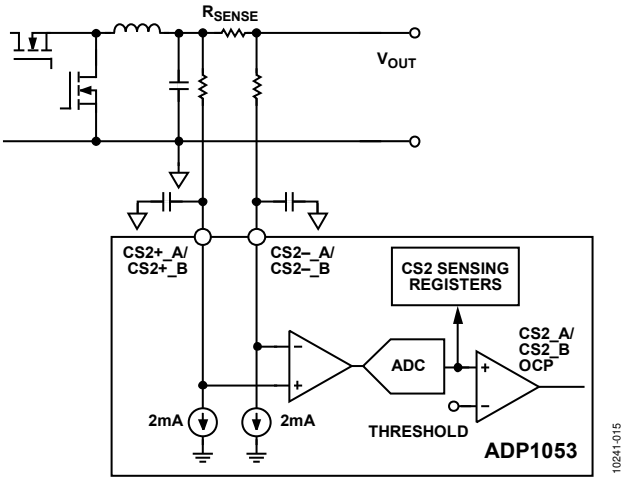


Figure 16. CS2 High-Side Resistive Current Sensing

Matching resistors with 0.1% or better accuracy are recommended to achieve the accuracy specifications.

The full-scale range of the CS2_A/CS2_B ADC is 120 mV. The ADC registers have an update rate of 100 Hz with 12-bit resolution.

The accurate ADC reading is used for CS2 overcurrent protection (OCP) and monitoring. For more information, see the CS2_A and CS2_B Accurate OCP Flags section and the CS2 (CS2_A/CS2_B) Readings section.

SR FETs REVERSE CURRENT PROTECTION

In synchronous rectification applications, reverse current may flow from V_{OUT} through an output inductor, SR FETs, and a sense resistor to the power ground. If the SR FETs are kept on, the large reverse current can damage the SR FETs or the gate driver circuit under extreme conditions.

SR FET reverse current protection is implemented using analog comparators. The reverse current protection threshold can be set using Register 0xFE84 and Register 0xFE85. If the voltage difference between CS2− and CS2+ is greater than the reverse current protection threshold programmed in these registers, the flag (REVERSE_A or REVERSE_B) is triggered. The action taken when the threshold is triggered can be programmed in Register 0xFE83.

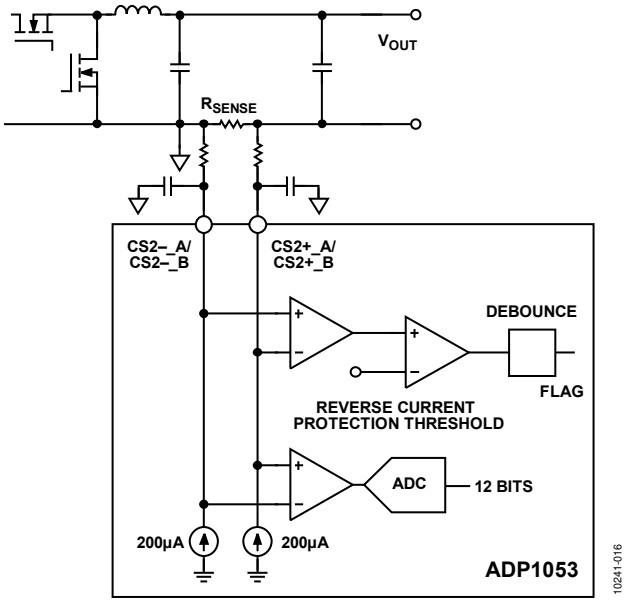


Figure 17. SR FET Reverse Current Protection

CONTROL LOOPS AND FEEDBACK REFERENCES

Channel A and Channel B each have an independent voltage feedback control loop. The feedback uses the sensed signals from VS+_A and VS−_A (for Channel A) and VS+_B and VS−_B (for Channel B).

Register 0xFE22 and Register 0xFE24 set the reference voltage for Channel A; Register 0xFE23 and Register 0xFE25 set the reference voltage for Channel B. Each LSB corresponds to the LSB of the VS_A/VS_B accurate ADC, which is 390.6 µV (see the VS_A and VS_B Readings section).

The output voltage must be divided down using a resistor divider network (R1 and R2 in Figure 11) to set up a feedback voltage at the VS_A/VS_B pins. To convert the register value to an output voltage reference, use the following equation:

$$V_{OUT} = VS\_Ref\_Voltage\_Value \times 390.6\ \mu V \times (R1 + R2)/R2$$

For example, in a 12 V system with an 11 kΩ and 1 kΩ resistor divider, the reference voltage register value for Channel A is 0xB00 (2816 decimal). This register value is converted as follows:

$$V_{OUT} = 2816 \times 390.6\ \mu V \times (11\ k\Omega + 1\ k\Omega)/1\ k\Omega = 13.2\ V$$

To prevent the writing of invalid voltage reference values to the registers, the value written to the registers does not take effect in the closed-loop operation until the GO command is executed. For Channel A, the GO command is executed by writing 1 to Bit 0 in Register 0xFE61. For Channel B, the GO command is executed by writing 1 to Bit 1 in Register 0xFE61. This function allows the user to read back and confirm the reference register value before implementing it for closed-loop operation.

In addition, to prevent a channel from outputting a voltage that is outside its capability, Register 0xFE1E through Register 0xFE21 can be used to set the high and low limits for the feedback references. The reference registers can only be set to values between the low and high limits. If the user attempts to write a value that is out of range to the reference register, the value is ignored and the voltage setting error flag (VS_SET_ERR_A or VS_SET_ERR_B) is set.

Note that the VS_SET_ERR_x flag is set during the writing of the invalid value and is cleared when the write fails; the latched flag is also set but is not cleared.

If the reference register value is not modified but the reference limit register is modified such that the reference is out of range, the write is successful. However, the reference value remains unchanged, and the VS_SET_ERR_x flag is set.

VOLTAGE SETTING WITH SLEW RATE

The ADP1053 provides a method for output voltage adjustment with slew rate control. The slew rate is set using Bits[3:1] of Register 0xFE86 (for VS_A) and Register 0xFE87 (for VS_B). The slew rate function is enabled by setting Bit 0 in Register 0xFE86 or Register 0xFE87. When a slew rate is enabled and the ADP1053 receives an output voltage adjustment command, the ADP1053 adjusts the voltage setting with the preset slew rate.

DIGITAL FILTERS

Channel A and Channel B each have an internal programmable digital filter. A Type III filter architecture is implemented in both digital filters. The low frequency gain, zero location, pole location, and high frequency gain can all be set individually to optimize the loop response.

It is recommended that the ADP1053 GUI be used to program the digital filter. The GUI displays the filter and loop response in Bode plot format. Together with the parameters from the power stages, all stability criteria can be evaluated.

From sensed voltage to the duty cycle, the transfer function of the filter in z-domain is

$$H(z) = \frac{d}{204.8 \times m} \times \frac{z}{z-1} + \frac{c}{5.12} \times \frac{z-b}{z-a}$$

where:
a = filter_pole_register_value/256.
b = filter_zero_register_value/256.
c = high_frequency_gain_register_value.
d = low_frequency_gain_register_value.
m = 1 when 48.8 kHz ≤ f_{SW} < 97.7 kHz.
m = 2 when 97.7 kHz ≤ f_{SW} < 195.3 kHz.
m = 4 when 195.3 kHz ≤ f_{SW} < 390.6 kHz.
m = 8 when 390.6 kHz ≤ f_{SW}.

where f_{SW} is the switching frequency.

To transfer the z-domain value to the s-domain, plug the following equation into Equation 1:

$$z(s) = \frac{2f_S + s}{2f_S - s}$$

Another set of registers configures the filter parameters for light load mode (see the Light Load Mode and Phase Shedding section). These separate registers allow the controller to regulate properly at different load conditions and to move smoothly between normal mode and light load mode.

ACSNS AND INPUT FEEDFORWARD

ACSNS has a low speed, high resolution ADC. This ADC samples at the same PWM switching frequency as Channel C. The ACSNS ADC has an update rate of 800 Hz with 11-bit resolution. The ACSNS value register (Register 0xFED9) provides information for the ACSNS monitoring and flag functions.

To improve line transient performance, a feedforward function is implemented in the ADP1053 using the ACSNS voltage. As shown in Figure 19, the input voltage signal is filtered by an RCD network. The ACSNS value is used to modify the output of the digital filter, and the modified result is fed to the PWM engine.

When the ACSNS input is set to a nominal voltage of 1 V (1280 decimal in the ACSNS value register), there is no effect on the modulation value.

When the output of the ACSNS ADC is below 0x280 (640 decimal), the feedforward function uses 0x280 as the effective input value. This means that the digital filter modulation value can be increased up to twice the original value.

For example, if the digital filter output remains unchanged and the ACSNS voltage changes to 50% of its original value (under an input voltage dip condition), the modulation value of OUT_X doubles (see Figure 18). The modulation edge is still limited by the maximum modulation limit.

The feedforward function is optional. It can be enabled or disabled using Bit 2 of Register 0xFE3E (for Channel A) and Register 0xFE3F (for Channel B).

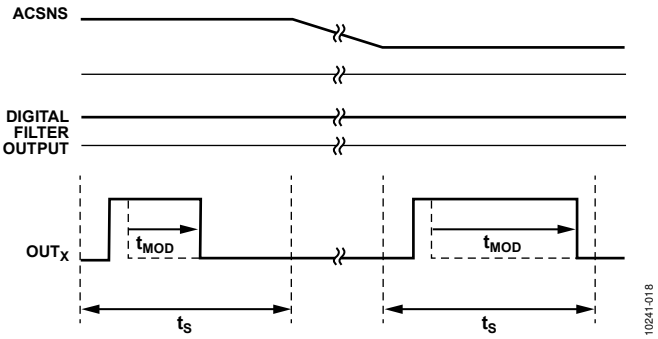


Figure 18. Feedforward Changes Modulation Values

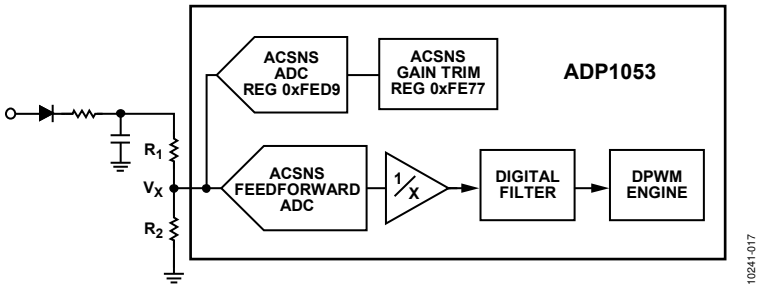


Figure 19. Feedforward Configuration

LIGHT LOAD MODE AND PHASE SHEDDING

The ADP1053 can be configured to disable PWM outputs under light load conditions based on the value of CS2_A and CS2_B. This function is programmed in Register 0xFE69 (for Channel A) and Register 0xFE6A (for Channel B) and can be used to implement phase shedding for multiphase operation. The light load condition flags, LIGHTLOAD_A (Bit 1 of Register 0xFEC0) and LIGHTLOAD_B (Bit 1 of Register 0xFEC1), are based on the reading of CS2_A and CS2_B, respectively.

The light load current thresholds can be programmed independently with Bits[3:0] of Register 0xFE1A and Register 0xFE1B. Each LSB of the threshold setting represents 64 LSBs of the 12-bit CS2_A/CS2_B readings. Because the input range of the CS2_A/CS2_B ADCs is 120 mV, each LSB of the threshold is equal to 1.875 mV. When Bits[3:0] are set to 0, the light load flag remains cleared.

Hysteresis is added to avoid switching between normal mode and light load mode. The threshold setting is the value that causes the part to enter light load mode. The value to exit light load mode is 2.8125 mV (96 LSBs) greater than the threshold to enter light load mode.

For example, in a system with a 2 mΩ sensing resistor, Bits[3:0] of Register 0xFE1A are set to 1001 (9 decimal). Therefore, the threshold to enter light load mode is

$$I_{LIGHTLOAD\_IN} = 9 \times 1.875\ mV/2\ m\Omega = 8.44\ A$$

where $I_{LIGHTLOAD\_IN}$ is the output current below which the part enters light load mode.

The threshold to exit light load mode and enter forced PWM mode is

$$I_{LIGHTLOAD\_OUT} = (9 \times 1.875\ mV + 2.8125\ mV)/2\ m\Omega = 9.84\ A$$

where $I_{LIGHTLOAD\_OUT}$ is the output current above which the part exits light load mode.

When a channel enters light load mode, the following actions take place:

- The LIGHTLOAD_A/LIGHTLOAD_B flag is set.
- The configured PWM outputs (programmable using Register 0xFE69 and Register 0xFE6A) are disabled.
- The feedback digital filter changes to the values for the light load condition.

When a channel exits light load mode, the light load flag is cleared, the disabled PWM outputs are reenabled, and the feedback filter changes back to the values for normal mode.

The signal at the FLGO/SYNO pin can be configured as a flag output by setting Bit 3 of Register 0xFE0F. This signal can be programmed to respond to either the LIGHTLOAD_A or LIGHTLOAD_B flag using Bit 4 of Register 0xFE0F. The polarity of the FLGO/SYNO pin can be set to inverted or noninverted using Bit 5 of Register 0xFE0F.

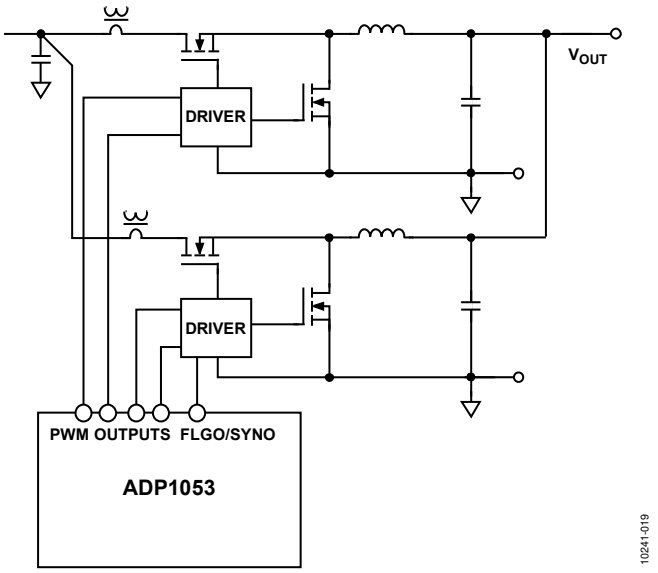


Figure 20. Phase Shedding in Dual-Phase Buck Controller

POWER-GOOD SIGNALS

Each regulated channel of the ADP1053 has a power-good pin: PGOOD_A for Channel A and PGOOD_B for Channel B. The PGOOD_A or PGOOD_B fault flag (Bit 6 of Register 0xFEC0 or Register 0xFEC1) is set when the EEPROM_CRC, POWER_SUPPLY_x, UVP_x, or SOFTSTART_FILTER_x flag is set. The ACSNS and OTWx flags can also be included in the setting of the PGOOD_A and PGOOD_B flags.

An overvoltage or overcurrent event does not directly trigger PGOOD_x, but it can trigger a POWER_SUPPLY_x fault that in turn triggers PGOOD_x. For example, if an overcurrent condition sets the OCP flag and the configured response to the OCP flag is to disable the appropriate PWM outputs, thus causing the power supply output to fall, a POWER_SUPPLY_x fault can be triggered that in turn triggers PGOOD_x. In the same way, an overvoltage condition can also indirectly trigger PGOOD_x.

The PGOOD_A and PGOOD_B pins are open-drain, active low pins. The on and off debounce times for the PGOOD_A and PGOOD_B fault flags are programmable for each flag at 0 ms, 200 ms, 320 ms, or 600 ms using Register 0xFE09.

SOFT START AND SHUTDOWN

PSON Control

The turning on and off of regulated Channel A is controlled by the hardware PSON_A pin and/or the software PSON_A register, depending on the configured settings in Register 0xFE79. In the same way, the turning on and off of regulated Channel B is controlled by the hardware PSON_B pin and/or the software PSON_B register, depending on the configured settings in Register 0xFE7A.

The PSON_A and PSON_B pins and registers can be controlled independently by different enable signals. The pins can also be tied together and triggered by the same signal.

The unregulated Channel C can be programmed to be always on, or it can be programmed to be on when either PSON_A or PSON_B is on. This option is configured using Bit 4 of Register 0xFE7B.

Software Reset

The user can reset the ADP1053 power supply by writing the GO command to Register 0xFE88 (Bit 0 for Channel A; Bit 1 for Channel B). When the GO bit is written, the power supply for Channel A or Channel B is immediately turned off, and the channel is restarted with a soft start after a preset delay. The delay can be programmed to 0 ms, 500 ms, 1 sec, or 2 sec using Bits[3:2] of Register 0xFE88.

PSON Sequencing

For both the regulated Channel A and Channel B and the unregulated Channel C, the turn-on delay, turn-off delay, and ramp rate can be independently configured. The register settings can be used to set up the sequencing of the channels.

Figure 21 shows a typical sequencing diagram.

- The turn-on delays (t_{DON_A}, t_{DON_B}, and t_{DON_C}) are the delay times between the activation of the PSON_A/PSON_B pins or commands that trigger the turn-on signal and the start of the output ramp-up.
- The turn-off delays (t_{DOFF_A}, t_{DOFF_B}, t_{DOFF_C}) are the delay times between the activation of the PSON_A/PSON_B pins or commands that trigger the turn-off signal and the start of the output shutdown.

The turn-on and turn-off delays for Channel A, Channel B, and Channel C can be set to 0 ms, 50 ms, 250 ms, or 1 sec using Register 0xFE79, Register 0xFE7A, and Register 0xFE7B, respectively.

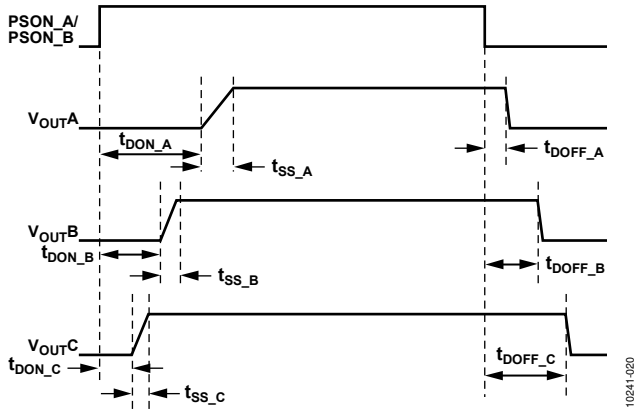


Figure 21. PSON Sequencing Diagram

The PGOOD signal of a master controller can be configured to trigger the PSON signals of multiple slave controllers.

The ADP1053 also has fault link functionality; that is, the part can be configured to shut down an output after another output is shut down.

Soft Start Ramp

For either regulated channel of the ADP1053, the VS_A/VS_B reference voltage increases from 0 V to the regulated reference voltage after the PSON signal is received and after the turn-on delay. The ramp rate for the reference voltage is set in Register 0xFE2A for Channel A and Register 0xFE2B for Channel B. The first column of Table 8 shows the possible ramp rates for the VS_A and VS_B references.

A non-zero prebias may result in a longer turn-on delay and shorter rise time.

Table 8. Soft Start Ramp Timing

VS_A/VS_B Reference Ramp Rate	Channel C Duty Cycle Ramp Rate
1 V/1.75 ms	40 ns/1 switching cycle
1 V/10.5 ms	40 ns/2 switching cycles
1 V/21.0 ms	40 ns/4 switching cycles
1 V/40.2 ms	40 ns/8 switching cycles

For the unregulated Channel C, the duty cycle can be programmed to increase or decrease at a rate set by Bits[5:4] of Register 0xFE68. The duty cycle variation can be set to 40 ns per one, two, four, or eight switching cycles. The soft start time for Channel C is usually faster than the soft start time for the regulated channels.

Two variation values are used for Channel C soft start:

$$t_{SS\_C1} = |t_{F1} - t_{R1}|$$

$$t_{SS\_C2} = |t_{F2} - t_{R2}|$$

where:
t_{R1} and t_{R2} are the timing values for the rising edges of OUT1 and OUT2, respectively.
t_{F1} and t_{F2} are the timing values for the falling edges of OUT1 and OUT2, respectively.
t_{SS_C1} sets the variation for OUT1, OUT3, OUT5, and OUT7 if these PWM outputs are assigned to Channel C.
t_{SS_C2} sets the variation for OUT2, OUT4, OUT6, and OUT8 if these PWM outputs are assigned to Channel C.

Both edges of a PWM signal assigned to Channel C can implement modulation during soft start. At the initiation of soft start, a modulated edge assigned to Channel C behaves as follows:

- If the edge is configured for positive modulation, the edge timing is the preset value plus the variation value. During soft start, the edge moves to the left until it reaches the preset value.
- If the edge is configured for negative modulation, the edge timing is the preset value minus the variation value. During soft start, the edge moves to the right until it reaches the preset value.

Example

In a fixed duty cycle, full-bridge application, OUT1 through OUT 4 are assigned to Channel C with soft start enabled. The switching frequency is 104.2 kHz, the switching cycle is 9.6 µs, t_{R1} = 0 µs, t_{F1} = 4 µs, t_{R2} = 4.8 µs, t_{F2} = 8.8 µs, t_{R3} = 4.2 µs, t_{F3} = 9.4 µs, t_{R4} = 9 µs, and t_{F4} = 4.6 µs. Therefore, $t_{SS\_C1} = t_{SS\_C2}$ = 4 µs.

For soft start, the falling edges of OUT1 and OUT2 are configured for negative modulation, and the rising edges of OUT3 and OUT4 are configured for negative modulation.

Given this setup, soft start for Channel C operates as follows:

- OUT1: The rising edge is fixed. At the beginning of soft start, the falling edge is located at $t_{F1} - t_{SS\_C1} = 0$, which means a zero duty cycle. The edge moves to the right during soft start and stops at the t_{F1} value of 4 µs.
- OUT2: The rising edge is fixed. At the beginning of soft start, the falling edge is located at $t_{F2} - t_{SS\_C2}$ = 4.8 µs, which means a zero duty cycle. The edge moves to the right during soft start and stops at the t_{F2} value of 8.8 µs.
- OUT3: The falling edge is fixed. At the beginning of soft start, the rising edge is located at $t_{R3} - t_{SS\_C1}$ = 0.2 µs. The edge moves to the right during soft start and stops at the t_{R3} value of 4.2 µs.
- OUT4: The falling edge is fixed. At the beginning of soft start, the rising edge is located at $t_{R4} - t_{SS\_C2}$ = 5 µs. The edge moves to the right during soft start and stops at the t_{R4} value of 9 µs.

To implement soft start for Channel C using a different PWM timing configuration, the user can configure additional bit settings in Register 0xFE68.

- When Bit 3 is set, t_{SS_C1} is forced to follow t_{SS_C2}.
- When Bit 2 is set, $t_{SS\_C2} = |t_S - t_{R2}|$, where t_S is the switching cycle for Channel C.
- When Bit 1 is set, $t_{SS\_C1} = |t_{F3} - t_{R3}|$.
- When Bit 0 is set, $t_{SS\_C2} = |t_{F4} - t_{R4}|$.

Bits[7:6] of Register 0xFE68 are used to prevent the unintentional overlap of the PWM outputs, especially when synchronization is enabled.

When Bit 7 is set, the falling edges of OUT1, OUT2, OUT5, and OUT6 are always after the rising edges in one cycle during soft start.

Bit 6 is valid only when Bit 7 of Register 0xFE68 is set to 1. If Bit 6 is set to 0, the rising edges of OUT3, OUT4, OUT7, and OUT8 are always after the falling edges in one cycle during soft start. If Bit 6 is set to 1, the falling edges of OUT3, OUT4, OUT7, and OUT8 are always after the rising edges in one cycle during soft start.

Flag Timing During Soft Start

The user can program which flags are active during the soft start. All flags are active at the end of the soft start. For more information, see the Flag Blanking During Soft Start section.

For either regulated channel of the ADP1053, the following procedure occurs after the user turns on the power supply (enables PSON_A or PSON_B). See Figure 22.

1. The PSON signal is enabled at t = t_0. The ADP1053 checks that initial flags are OK.
2. The ADP1053 waits for the t_{DON} time before it begins to ramp up the power stage reference voltage at t_1.
3. When the output voltage reaches a steady state, the soft start is completed, and the SOFTSTART_FILTER_A or SOFTSTART_FILTER_B flag is cleared.
4. The PGOOD signal waits for the t_{DGOOD} time before it is enabled at t_3.

The values for t_{DON_A}, t_{DON_B}, t_{DGOOD_A}, and t_{DGOOD_B} are all programmable.

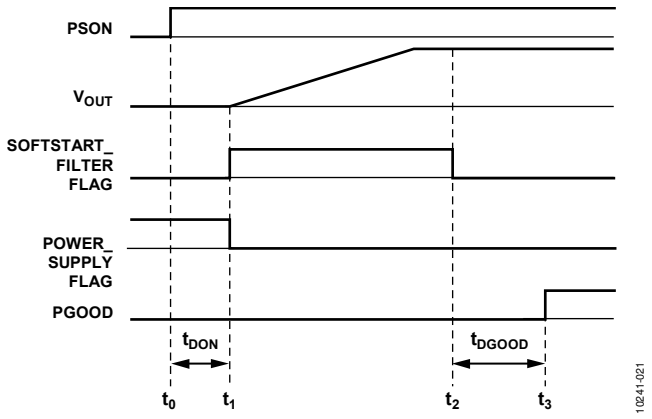


Figure 22. Soft Start Timing Diagram

The restart delay time can be programmed using Register 0xFE88. For example, in the case of a short circuit, the ADP1053 restarts in a soft start sequence every restart delay time. This restart feature, also called "hiccup mode," helps to minimize power dissipation in the event of a short circuit. For more information, see the Protection Actions section.

The SR PWM outputs and the current balance function can be disabled during soft start. For more information, see the PWM Outputs (OUT1 to OUT8) section and the Synchronous Rectifier (SR) Soft Start section.

Flag Timing During Shutdown

When a fault condition occurs, the following flags are set:

- The PGOOD_A or PGOOD_B fault flag is set.
- Depending on the fault and how it is configured, the POWER_SUPPLY_A or POWER_SUPPLY_B flag is enabled after a programmed time.

Digital Filters During Soft Start

A dedicated filter is used during soft start. The filter is disabled at the end of the soft start routine, after which the voltage loop digital filter is used. The soft start filter gain is programmable using Bits[1:0] of Register 0xFE3E and Register 0xFE3F.

The soft start filter is used during the reference ramp time until the high frequency ADCs of VS_A/VS_B are settled. The user can program a debounce time for detecting the settling of the high frequency ADC using Bits[5:4] of Register 0xFE3E and Register 0xFE3F. The debounce time can be set to 5 ms or 10 ms with Bit 5. During the time that the soft start filter is used, the SOFTSTART_FILTER_x flag is set.

SYNCHRONOUS RECTIFIER (SR) SOFT START

The turning on of the synchronous rectification (SR) signals (OUT3, OUT4, OUT7, and OUT8) during a soft start can be programmed in two ways. The SR signals can either be turned on to their full PWM values immediately, or they can be turned on in a soft start fashion, which ensures a smooth output ramp during the soft start.

SR soft start changes the rising edge of the PWM output. Note that the falling edge of an SR PWM output should not be modulated. When turned on in a soft start, the rising edge of the SR PWM output starts at the same instant as the falling edge, which means a zero duty cycle. The rising edge moves left in a step of 40 ns per 1, 4, 16, or 64 switching cycles (programmable using Register 0xFE67). In this way, the SR output ramps up from a zero duty cycle to the desired duty cycle. When the rising edge reaches 0, it wraps to restart at the end of the switching cycle.

When the ADP1053 is programmed to use SR during soft start, the falling edge of SR outputs must be set to a lower value than the rising edge of the following PWM output.

VOLT-SECOND BALANCE AND CURRENT BALANCE

The ADP1053 has two dedicated circuits to maintain current balance/volt-second balance. To configure a PWM output for volt-second balance or current balance, program Bit 4 in the appropriate PWM output setting register. (The PWM output setting registers are Register 0xFE43, Register 0xFE47, Register 0xFE4B, Register 0xFE4F, Register 0xFE53, Register 0xFE57, Register 0xFE5B, and Register 0xFE5F.) Volt-second balance control can be disabled during soft start using Bit 3 of Register 0xFE08.

The balance control gains are programmable in Register 0xFE72. The maximum modulation limit on the duty cycles is programmable at 80 ns and 160 ns using Bit 6 of Register 0xFE72.

When OUT1, OUT2, OUT3, and OUT4 are used for balance control, the user can enable or disable the rising and falling edges using Register 0xFE62 and Register 0xFE63. The direction of the modulation is also programmable.

When OUT5, OUT6, OUT7, and OUT8 are used for balance control, the user can enable or disable the rising and falling edges using Register 0xFE64. The modulation direction is fixed.

When OUT5 and OUT7 are used and edge modulation for balance control is enabled, increasing the balance control modulation moves the edge to the right. For OUT6 and OUT8, increasing the balance control modulation moves the edge to the left.

Volt-Second Balancing (Based on CS Pin Signal)

Volt-second balance control is based on the sensed signal at the CS pin following the rising edge of the OUT1 and OUT2 signals. When enabled, volt-second balance control makes the programmed adjustment to the enabled PWM edges. This feature can be effectively used in full-bridge applications, eliminating the need for a dc blocking capacitor. The circuit monitors the dc current flowing in both halves of the full bridge, stores this information, and compensates the PWM drive signals to ensure equal current flow in both halves of the full bridge. The time required for the circuit to operate effectively can be programmed and is typically in the range of 100 ms. Therefore, during a transient condition, the volt-second balance relies on the overcurrent condition to limit the PWM duty cycle.

Volt-second balance control uses the CS signal; it can be assigned to Channel A or Channel C using Bit 7 of Register 0xFE72. When volt-second balance control is used, OUT1 and OUT2 must be assigned to the appropriate channel (Channel A or Channel C) because the balance control circuit looks only for the rising edges of OUT1 and OUT2 to start the balance control integration.

When the CS signal in the half cycle after the rising edge of OUT1 is higher than the signal in the half cycle after the rising edge of OUT2, the modulation value increases. The PWM output edges move according to the values programmed in Register 0xFE62.

Leading edge blanking functions can also be used at the sensed CS signals for more accurate control results. The blanking time follows the CS OCP blanking time. For more information, see the Overcurrent Protection (OCP) Flags section.

Current Balancing (Based on CS1/CS2 Pin Signals)

Current balancing with regulated feedback is designed for operation in dual-phase, single-output topologies. Current balancing is implemented to control the balance between CS1_A and CS1_B or between CS2_A and CS2_B (use Bit 3 of Register 0xFE72 to select CS1_A/CS1_B or CS2_A/CS2_B).

For dual-phase current balance control, when the CS1_A or CS2_A value is larger than the CS1_B or CS2_B value, the modulation value increases. The actions for different PWM output edges are programmable using Register 0xFE62, Register 0xFE63, and Register 0xFE64.