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### FEATURES

- 40°C to +125°C operation
- PMBus Revision 1.2 compliant with PEC and extended manufacturer specific commands
- 32-bit password protection with command masking
- 64 address selections (16 base addresses, expandable to 64)
- 6 PWM control signals, 625 ps resolution
- Frequency from 48 kHz to 1 MHz
- Duty cycle double update rate
- Digital control loop (PID + additional pole or zero configurability)
- Programmable loop filters (CCM, DCM, low/normal temperature)
- Fast line voltage feedforward
- Adaptive dead time compensation for improved efficiency
- Remote voltage sense
- Redundant programmable OVP
- Current sense
  - Primary side cycle-by-cycle fast protection
  - Secondary side cycle-by-cycle fast overcurrent protection
  - Secondary side averaged reverse current protection using diode emulation mode with fixed debounce
- Synchronous rectifier control for improved efficiency in light load mode
- Nonlinear gain for faster transient response from DCM to CCM
- Frequency synchronization
- Soft start and soft stop functionality
- Average and peak constant current mode
- External PN junction temperature sensing
- 4 GPIOs (2 GPIOs configurable as active clamp snubber PWMs)

- Extended black box data recorder for fault recording
- User trimming on input and output voltages and currents
- Digital current sharing

### APPLICATIONS

- Isolated dc-to-dc power supplies and modules
- Redundant power supply systems

### GENERAL DESCRIPTION

The ADP1055 is a flexible, feature-rich digital secondary side controller that targets ac-to-dc and isolated dc-to-dc secondary side applications. The ADP1055 is optimized for minimal component count, maximum flexibility, and minimum design time. Features include differential remote voltage sense, primary and secondary side current sense, pulse-width modulation (PWM) generation, frequency synchronization, redundant OVP, and current sharing. The control loop digital filter and compensation terms are integrated and can be programmed over the PMBus™ interface. Programmable protection features include overcurrent (OCP), overvoltage (OVP) limiting, undervoltage lockout (UVLO), and external overtemperature (OTP).

The built-in EEPROM provides extensive programming of the integrated loop filter, PWM signal timing, inrush current, and soft start timing and sequencing. Reliability is improved through a built-in checksum and programmable protection circuits.

A comprehensive GUI is provided for easy design of loop filter characteristics and programming of the safety features. The industry-standard PMBus provides access to the many monitoring and system test functions. The ADP1055 is available in a 32-lead LFCSP and operates from a single 3.3 V supply.

### TYPICAL APPLICATION DIAGRAM

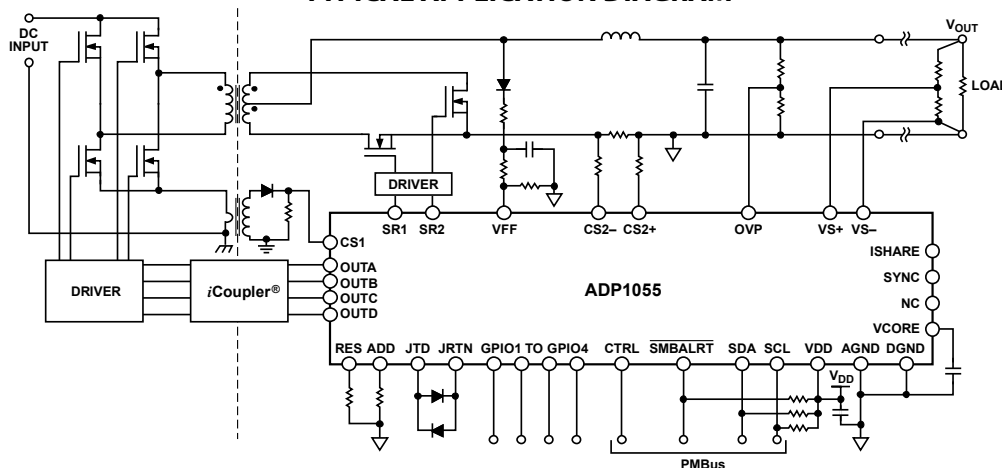


Figure 1.

Rev. A

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# ADP1055\* PRODUCT PAGE QUICK LINKS

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## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- ADP1055 Evaluation Board

## DOCUMENTATION

### Application Notes

- AN-1336: Adaptive Dead Time in Full Bridge Phase Shifted Topology Using ADP1055
- AN-1382: ADP1055 EEPROM Programming

### Data Sheet

- ADP1055: Digital Controller for Power Supply Applications with PMBus Interface Data Sheet

### User Guides

- UG-710: Evaluating the 240 Watts ADP1055 Digital Controller for Isolated Power Supply with PMBus Interface

## SOFTWARE AND SYSTEMS REQUIREMENTS

- ADP1055 Software, Ver. 2.0.16

## REFERENCE MATERIALS

### Press

- Analog Devices' Breaks Through the Digital Power Barrier

### Technical Articles

- Designing Digital Power Supplies With A State Machine
- Digital Control Enables High Reliability DC-to-DC Power Conversion with Active Snubbing

## DESIGN RESOURCES

- ADP1055 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

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## SAMPLE AND BUY

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## DOCUMENT FEEDBACK

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## REVISION HISTORY

### 3/15—Rev. 0 to Rev. A

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### 3/14—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

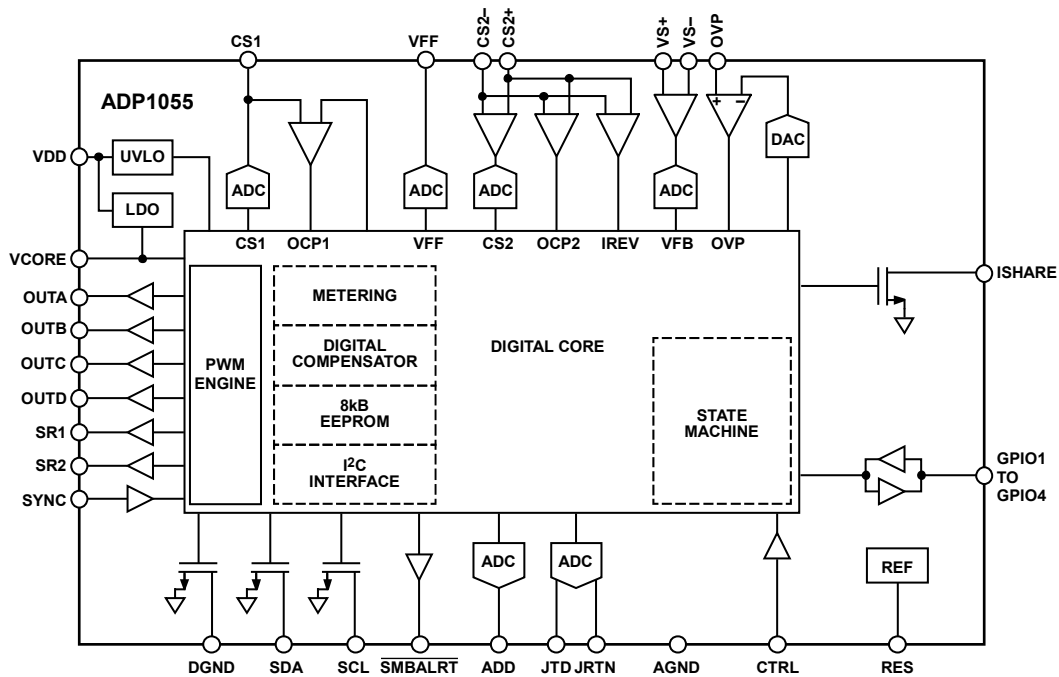


Figure 2. Functional Block Diagram (Simplified Internal Structure)

12004-002

## SPECIFICATIONS

$V_{DD} = 3.0\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }+125^\circ\text{C}$ , unless otherwise noted. FSR = full-scale range.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>SUPPLY</b>						
Supply Voltage	$V_{DD}$	4.7 $\mu\text{F}$ capacitor connected to AGND	3.0	3.3	3.6	V
Supply Current	$I_{DD}$	Normal operation (CTRL pin is high)		63		mA
		Normal operation (CTRL pin is low)		55		mA
		During EEPROM programming (40 ms)		$I_{DD} + 8$		mA
		During black box write		$I_{DD} + 8$		mA
		Current with $V_{DD} < V_{CORE\ POR}$		100		$\mu\text{A}$
<b>POWER-ON RESET</b>						
Power-On Reset	POR	$V_{DD}$ rising			3.0	V
Undervoltage Lockout	UVLO	$V_{DD}$ falling	2.75	2.85	2.97	V
Overvoltage Lockout	OVLO		3.8	4.0	4.1	V
OVLO Debounce		Set to 2 $\mu\text{s}$ (Register 0xFE4D[5] = 0)		2.0		$\mu\text{s}$
		Set to 500 $\mu\text{s}$ (Register 0xFE4D[5] = 1)		500		$\mu\text{s}$
<b>VCORE PIN</b>						
Power-On Reset (POR)		0.33 $\mu\text{F}$ capacitor connected to DGND				
Output Voltage		$V_{DD}$ falling		2.1		V
Maximum Time from POR to Outputs Switching		$T_A = 25^\circ\text{C}$		2.6		V
		No black box recording (Register 0xFE48[1:0] = 00)		10		ms
		With black box recording (Register 0xFE48[1:0] = 01, 10, or 11)		45		ms
<b>OSCILLATOR AND PLL</b>						
PLL Frequency		RES = 10 k $\Omega$ ( $\pm 0.1\%$ )	190	200	210	MHz
<b>OUTA, OUTB, OUTC, OUTD, SR1, SR2 PINS</b>						
Output Low Voltage	$V_{OL}$	Sink current = 10 mA			0.8	V
Output High Voltage	$V_{OH}$	Source current = 10 mA	$V_{DD} - 0.8$			V
Rise Time		$C_{LOAD} = 50\text{ pF}$		3.5		ns
Fall Time		$C_{LOAD} = 50\text{ pF}$		1.5		ns
<b>VOLTAGE FEEDFORWARD (VFF PIN)</b>						
ADC Clock Frequency				1.56		MHz
Feedforward (Slow) Input Voltage Range	$V_{FF}$	For reporting; equivalent resolution of 12 bits	0	1	1.6	V
ADC Usable Input Voltage Range		Factory trimmed at 1.0 V	0		1.57	V
Measurement Accuracy (Slow and Fast Feedforward)		0% to 100% of usable input voltage range	-2.5		+2.5	% FSR
		10% to 90% of usable input voltage range	-2.0		+2.0	% FSR
		900 mV to 1.1 V	-1.5		+1.5	% FSR
Leakage Current					1.0	$\mu\text{A}$
<b>FEEDFORWARD FUNCTION (VFF PIN)</b>						
Feedforward (Fast) Input Voltage Range			0.6	1	1.6	V
Sampling Period for Feedforward (Fast) ADC		Equivalent resolution of 12 bits		1		$\mu\text{s}$
<b>VS LOW SPEED ADC</b>						
Input Voltage Range		Differential voltage from VS+ to VS-	0	1	1.6	V
Usable Input Voltage Range			0		1.55	V
ADC Clock Frequency				1.56		MHz

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit	
ADC Update Rate		Registers are updated at this rate, equivalent resolution of 12 bits		10.5		ms	
Measurement Accuracy		Factory trimmed at 1.0 V					
		0% to 100% of usable input voltage range	-2.75		+2.75	% FSR	
		10% to 90% of usable input voltage range	-2.0		+2.0	% FSR	
Temperature Coefficient		900 mV to 1.1 V	-1.75		+1.75	% FSR	
Leakage Current		$V_{DD} = 3.3\text{ V}$ , $V_{S\pm} = 1.0\text{ V}$			110	ppm/°C	
Common-Mode Voltage Offset Error		Maximum voltage differential from $V_{S-}$ to AGND of $\pm 200\text{ mV}$	-0.25		+0.25	% FSR	
VS OVP DIGITAL COMPARATOR							
VS OVP Accuracy		Register 0xFE4D[3:2] = 00, equivalent resolution of 7 bits	-2.0		+2.0	% FSR	
VS OVP Comparator Speed			82			$\mu\text{s}$	
VS UVP DIGITAL COMPARATOR							
VS UVP Accuracy		Does not include debounce time (Register 0xFE30[13:11] = 00)	-2.0		+2.0	% FSR	
Propagation Delay			80			$\mu\text{s}$	
VS HIGH SPEED ADC							
Sampling Frequency				10		MHz	
Equivalent Resolution				6		Bits	
Dynamic Range				$\pm 50$		mV	
FAST OVP COMPARATOR (OVP PIN)							
Threshold Accuracy		Factory trimmed at 1.206 V	-1.2	0	+1.5	%	
		Other thresholds (0.8 V to 1.6 V)	-2.0		+2.0	%	
Propagation Delay (Latency)		Register 0xFE2F[1:0] = 00		40	80	ns	
CURRENT SENSE 1 (CS1 PIN)							
Input Voltage Range	$V_{IN}$	Registers are updated at this rate, equivalent resolution of 12 bits Factory trimmed at 1.0 V; tested under dc input conditions	0	1	1.6	V	
Usable Input Voltage Range			0		1.56	V	
ADC Clock Frequency					1.56	MHz	
Update Rate					10.5	ms	
Current Sense Measurement Accuracy			10% to 60% of usable input voltage range	-1.5		+1.5	% FSR
			10% to 90% of usable input voltage range	-2.0		+2.0	% FSR
			0% to 100% of usable input voltage range	-2.5		+2.5	% FSR
Current Sense Measurement CS1 Fast OCP Threshold			Register 0xFE2C[2] = 0	1.17	1.2	1.23	V
			Register 0xFE2C[2] = 1	242	250	258	mV
CS1 Fast OCP Speed					40	80	ns
CS1 Accurate OCP Speed					10.5		ms
Leakage Current						1.5	$\mu\text{A}$
CURRENT SENSE 2 (CS2+, CS2- PINS)							
Current Sense Measurement Resolution		For updating registers (constant current mode enabled or disabled)		12		Bits	
ADC Clock Frequency				1.56		MHz	
30 mV Range <sup>1</sup>		Register 0xFE4F[1:0] = 00	0		30	mV	
Usable Input Range			0		21	mV	
60 mV Range <sup>1</sup>		Register 0xFE4F[1:0] = 01	0		60	mV	
Usable Input Range			0		45	mV	
480 mV Range <sup>1</sup>		Register 0xFE4F[1] = 10	0		480	mV	
Usable Input Range			0		414	mV	



Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Temperature Coefficient 30 mV Range		$V_{DD} = 3.3\text{ V}$ 0 mV to 19 mV			326	ppm/°C
60 mV Range		0 mV to 21 mV			354	ppm/°C
480 mV Range		0 mV to 41 mV 0 mV to 45 mV 0 mV to 374 mV 0 mV to 414 mV			172 194 83 84	ppm/°C ppm/°C ppm/°C ppm/°C
CURRENT SENSE MEASUREMENT ACCURACY (CS2+, CS2– PINS)						
30 mV Setting		0 mV to 19 mV 0 mV to 21 mV	–2.9 –3.1		+2.9 +3.1	% FSR % FSR
60 mV Setting		0 mV to 41 mV 0 mV to 45 mV	–1.9 –2.1		+1.9 +2.1	% FSR % FSR
480 mV Setting		0 mV to 374 mV 0 mV to 414 mV	–1.5 –1.7		+1.5 +1.7	% FSR % FSR
Internal Level Shifting Current CS2 Accurate OCP Speed		All ranges		25 2.6		μA ms
COMMON-MODE VOLTAGE OFFSET ERROR (CS2+, CS2– PINS)		Maximum voltage differential from CS2– to AGND of ±50 mV				
30 mV Range			–1.0		+1.0	% FSR
60 mV Range			–0.5		+0.5	% FSR
480 mV Range			–0.25		+0.25	% FSR
CS2 OCP FAST COMPARATORS (CS2+, CS2– PINS)		For CS2 fast OCP and peak constant current mode				
CS2 Forward Comparator Accuracy						
Range of 0 mV to 60 mV		Threshold set at 0 mV Threshold set at 15.24 mV Threshold set at 30.48 mV Threshold set at 45.71 mV Threshold set at 60 mV	–23.8	–10.3 –10.1 –10.2 –10.2	+16.7	% FSR % FSR % FSR % FSR % FSR
Range of 0 mV to 600 mV		Threshold set at 0 mV Threshold set at 152.4 mV Threshold set at 304.8 mV Threshold set at 457.1 mV Threshold set at 600 mV	–7.1	–0.8 0.1 0.9 1.3	+7.6	% FSR % FSR % FSR % FSR % FSR
Reverse Comparator Accuracy						
Range of 0 mV to 30 mV		Threshold set at 0 mV Threshold set at 7.62 mV Threshold set at 15.24 mV Threshold set at 22.86 mV	–13.8	–11.8 –11.8 12.7	+16.9	% FSR % FSR % FSR % FSR
Range of –30 mV to 0 mV		Threshold set at 30 mV Threshold set at 0 mV Threshold set at –7.62 mV Threshold set at –15.24 mV Threshold set at –22.86 mV Threshold set at –30 mV	–9.5	12.5 17.1 16.9 17.6 17.4	+23.2	% FSR % FSR % FSR % FSR % FSR % FSR
Propagation Delay		Register 0xFE2D[1:0] = 00 (diode emulation mode)		40	80	ns
JTD TEMPERATURE SENSE						
ADC Clock Frequency				1.56		MHz
Update Rate		For updating registers (14-bit resolution)				
Reverse Sensing Enabled				200		ms
Reverse Sensing Disabled				130		ms

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Measurement Accuracy for External Temperature Sensor Forward Temperature Sensor		With BC847A transistor ( $n_f = 1.00$ ); Register 0xFE5A[2:0] = 0x04 Error from $-40^{\circ}\text{C}$ to $+25^{\circ}\text{C}$	-11.7		+13.4	$^{\circ}\text{C}$
Reverse Temperature Sensor		Error from $25^{\circ}\text{C}$ to $125^{\circ}\text{C}$ Error from $25^{\circ}\text{C}$ to $125^{\circ}\text{C}$	-8.9		+14.7	$^{\circ}\text{C}$
CTRL, SMBALRT, SYNC, GPIO1 TO GPIO4, ISHARE PINS		Digital inputs/outputs				
Input Low Voltage	$V_{IL}$				0.8	V
Input High Voltage	$V_{IH}$		$V_{DD} - 0.8$			V
Propagation Delay				40		ns
GPIOx Rise Time		GPIOx configured as an output		3.5		ns
GPIOx Fall Time		GPIOx configured as an output		1.5		ns
Leakage Current		SMBALRT, SYNC, GPIO1 TO GPIO4, and ISHARE pins			1.0	$\mu\text{A}$
		CTRL pin			10.0	$\mu\text{A}$
SYNC PIN		Synchronization to external frequency	50		1000	kHz
Minimum On Pulse			40			ns
Synchronization Range <sup>2</sup>			-10.0		+10.0	% $f_{sw}$
Leakage Current					1.0	$\mu\text{A}$
BLACK BOX PROGRAMMING TIME			1.2		$36 \times 1.2$	ms
SDA/SCL PINS						
Input Low Voltage	$V_{IL}$				0.8	V
Input High Voltage	$V_{IH}$		2.1			V
Output Low Voltage	$V_{OL}$				0.4	V
Leakage Current					1.0	$\mu\text{A}$
SERIAL BUS TIMING		See Figure 3				
Clock Operating Frequency			10	100	400	kHz
Bus Free Time	$t_{BUF}$	Between stop and start conditions	1.3			$\mu\text{s}$
Start Hold Time	$t_{HD,STA}$	Hold time after (repeated) start condition; after this period, the first clock is generated	0.6			$\mu\text{s}$
Start Setup Time	$t_{SU,STA}$	Repeated start condition setup time	0.6			$\mu\text{s}$
Stop Setup Time	$t_{SU,STO}$		0.6			$\mu\text{s}$
SDA Setup Time	$t_{SU,DAT}$		100			ns
SDA Hold Time	$t_{HD,DAT}$	For write and for readback	300			ns
SCL Low Timeout	$t_{TIMEOUT}$		25		35	ms
SCL Low Period	$t_{LOW}$		1.3			$\mu\text{s}$
SCL High Period	$t_{HIGH}$		0.6			$\mu\text{s}$
Clock Low Extend Time	$t_{LO,SEXT}$				25	ms
SCL, SDA Fall Time	$t_F$		20		300	ns
SCL, SDA Rise Time	$t_R$		20		300	ns
EEPROM RELIABILITY						
Endurance <sup>3</sup>		$T_J = 85^{\circ}\text{C}$	10,000			Cycles
		$T_J = 125^{\circ}\text{C}$	1000			Cycles
Data Retention <sup>4</sup>		$T_J = 85^{\circ}\text{C}$	20			Years
		$T_J = 125^{\circ}\text{C}$	15			Years

<sup>1</sup> Differential voltage from CS2+ to CS2-.

<sup>2</sup>  $f_{sw}$  is the switching frequency set in Register 0x33.

<sup>3</sup> Endurance is qualified as per JEDEC Standard 22, Method A117, and is measured at  $-40^{\circ}\text{C}$ ,  $+25^{\circ}\text{C}$ ,  $+85^{\circ}\text{C}$ , and  $+125^{\circ}\text{C}$ .

<sup>4</sup> Retention lifetime equivalent at junction temperature ( $T_J$ ) =  $85^{\circ}\text{C}$  as per JEDEC Standard 22, Method A117. Retention lifetime derates with junction temperature.

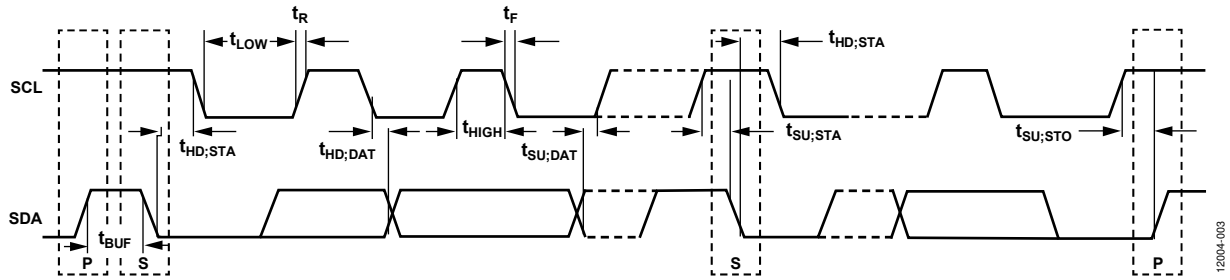


Figure 3. Serial Bus Timing Diagram

12004-003

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (Continuous), VDD	4.2 V
Digital Pins: OUTA, OUTB, OUTC, OUTD, SR1, SR2, GPIO1, GPIO2, GPIO3, GPIO4, SMBALRT, SYNC	-0.3 V to VDD + 0.3 V
VS-, AGND, DGND	-0.3 V to +0.3 V
VS+	-0.3 V to VDD + 0.3 V
JTD, JRTN, ADD	-0.3 V to VDD + 0.3 V
CS1, CS2+, CS2-	-0.3 V to VDD + 0.3 V
SDA, SCL	-0.3 V to VDD + 0.3 V
ISHARE	-0.3 V to VDD + 0.3 V
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS-Compliant Assemblies (20 sec to 40 sec)	260°C
ESD	
Charged Device Model	500 V
Human Body Model	2.5 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
32-Lead LFCSP	44.4	6.4	°C/W

## SOLDERING

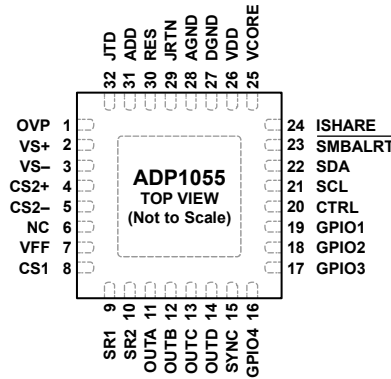
It is important to follow the correct guidelines when laying out the PCB footprint for the [ADP1055](#) and when soldering the device onto the PCB. For detailed information about these guidelines, see the [AN-772 Application Note](#).

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**
1. NC = NO CONNECT. LEAVE THIS PIN UNCONNECTED.
  2. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE EXPOSED PAD ON THE UNDERSIDE OF THE PACKAGE BE SOLDERED TO THE PCB AGND PLANE.

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OVP	Overvoltage Protection. This signal is referenced to AGND and is used for redundant OVP protection. The nominal voltage at this pin should be 1 V. If this pin is not used, connect it to AGND.
2	VS+	Noninverting Voltage Sense Input. This signal is referenced to VS-. The nominal input voltage at this pin is 1 V. The resistor divider on this input must have a tolerance specification of 0.5% or better to allow for trimming. This pin is the input to the high frequency flash ADC.
3	VS-	Inverting Voltage Sense Input. There should be a low ohmic connection to AGND. The resistor divider on this input must have a tolerance specification of 0.5% or better to allow for trimming. To reduce common-mode noise, connect a 0.1 μF capacitor from VS- to AGND.
4	CS2+	Noninverting Differential Current Sense Input. This signal is referenced to CS2-. If this pin is not used, connect it to AGND.
5	CS2-	Inverting Differential Current Sense Input. If this pin is not used, connect it to AGND. This pin must have a low ohmic connection to AGND through the sense resistor.
6	NC	No Connect. Leave this pin unconnected.
7	VFF	Voltage Feedforward. Two optional functions can be implemented using this pin: feedforward and input voltage loss detection. This pin is typically connected upstream of the output inductor through a resistor divider network in an isolated converter. The nominal voltage at this pin should be 1 V. This signal is referenced to AGND. If this pin is not used, connect it to AGND.
8	CS1	Primary Side Current Sense Input. This pin is connected to the primary side current sensing ADC and to the fast OCP comparator. This signal is referenced to PGND. The resistors on this input must have a tolerance specification of 0.5% or better to allow for trimming. If this pin is not used, connect it to AGND.
9	SR1	Synchronous Rectifier Output. This PWM output connects to the input of a FET driver. This pin can be disabled when not in use. This signal is referenced to AGND.
10	SR2	Synchronous Rectifier Output. This PWM output connects to the input of a FET driver. This pin can be disabled when not in use. This signal is referenced to AGND.
11	OUTA	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referenced to AGND.
12	OUTB	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referenced to AGND.
13	OUTC	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referenced to AGND.
14	OUTD	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referenced to AGND.
15	SYNC	Synchronization Input Signal. This pin is used as a reference for the internal PWM frequency. This signal is referenced to AGND and must have a nominal duty cycle of 50%. If this pin is not used, connect it to AGND and program Register 0xFE55[6] = 1.
16	GPIO4	Programmable General-Purpose Input/Output. If this pin is not used, connect it to AGND. This pin can also be configured as an active snubber PWM output.
17	GPIO3	Programmable General-Purpose Input/Output. If this pin is not used, connect it to AGND. This pin can also be configured as an active snubber PWM output.

Pin No.	Mnemonic	Description
18	GPIO2	Programmable General-Purpose Input/Output. If this pin is not used, connect it to AGND.
19	GPIO1	Programmable General-Purpose Input/Output. If this pin is not used, connect it to AGND.
20	CTRL	Power Supply On Input. This signal is referenced to AGND. This pin is the hardware PSON control signal. It is recommended that a 1 nF capacitor be connected from the CTRL pin to AGND for decoupling. If this pin is not used, connect it to AGND.
21	SCL	I <sup>2</sup> C/PMBus Serial Clock Input and Output (Open Drain). This signal is referenced to AGND.
22	SDA	I <sup>2</sup> C/PMBus Serial Data Input and Output (Open Drain). This signal is referenced to AGND.
23	$\overline{\text{SMBALRT}}$	Power-Good Output (Open Drain). This signal is referenced to AGND. This pin is also used as the PMBus $\overline{\text{ALERT}}$ signal.
24	ISHARE	Digital Current Sharing Input and Output (Open Drain). This signal is referenced to AGND.
25	VCORE	VDD for the Digital Core. Connect a decoupling capacitor of at least 330 nF (1 $\mu$ F maximum) from this pin to DGND as close to the IC as possible to minimize the PCB trace length. Do not use the VCORE pin as a reference or load it in any way.
26	VDD	Positive Supply Input. This signal is referenced to AGND. Connect a 4.7 $\mu$ F decoupling capacitor from this pin to AGND as close to the IC as possible to minimize the PCB trace length.
27	DGND	Digital Ground. This pin is the ground reference for the digital circuitry. Star connect to AGND.
28	AGND	IC Analog Ground.
29	JRTN	Temperature Sensor Return. If this pin is not used, connect it to AGND.
30	RES	Resistor Input. This pin sets the internal reference for the internal PLL frequency. Connect a 10 k $\Omega$ resistor ( $\pm 0.1\%$ ) from RES to AGND. Do not load this pin with any capacitance. This signal is referenced to AGND.
31	ADD	I <sup>2</sup> C/PMBus Address Select Input. Connect a resistor from ADD to AGND. This signal is referenced to AGND.
32	JTD	Thermal Sensor Input. A PN junction sensor is connected from this pin to the JRTN pin. If this pin is not used, connect it to JRTN.
	EP	Exposed Pad. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the exposed pad on the underside of the package be soldered to the PCB AGND plane.

# TYPICAL PERFORMANCE CHARACTERISTICS

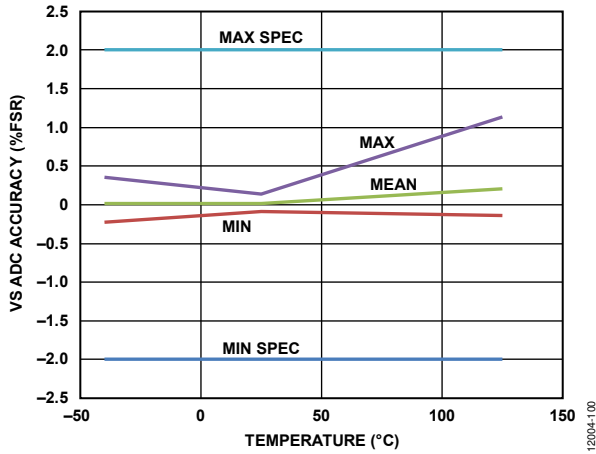


Figure 5. VS ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

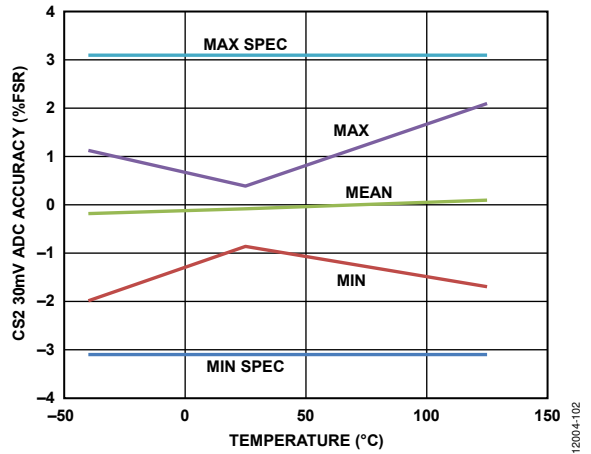


Figure 8. CS2 30mV ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

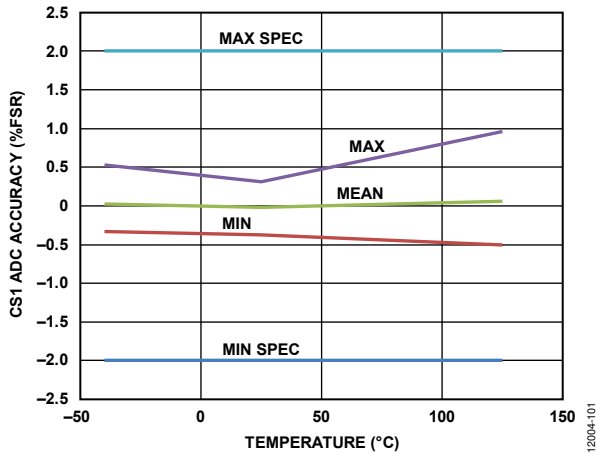


Figure 6. CS1 ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

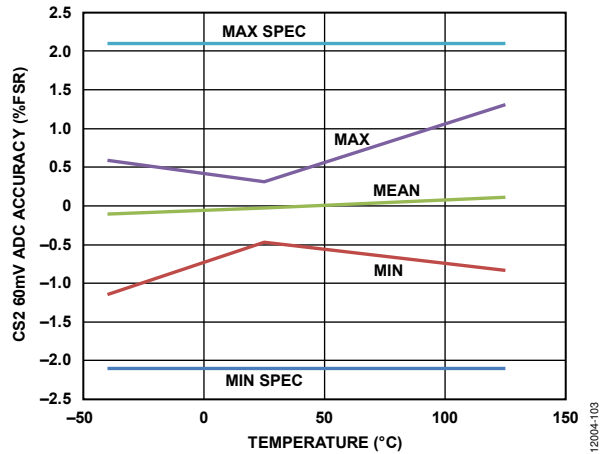


Figure 9. CS2 60mV ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

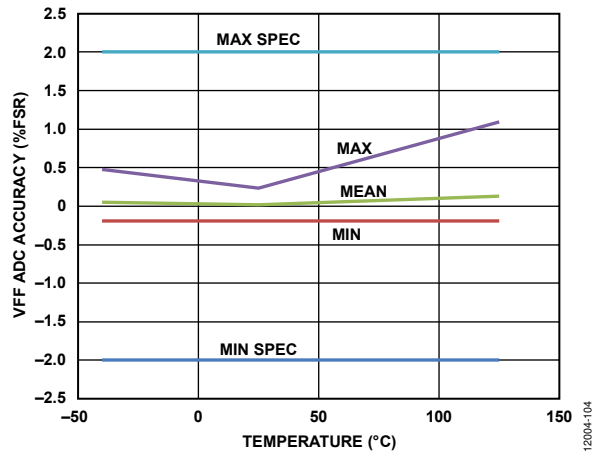


Figure 7. VFF ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

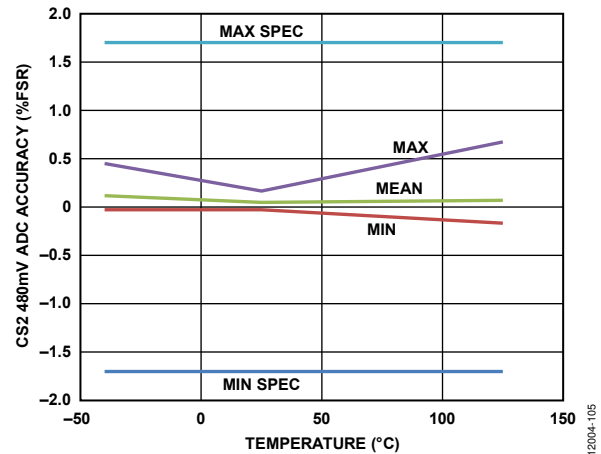


Figure 10. CS2 480mV ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

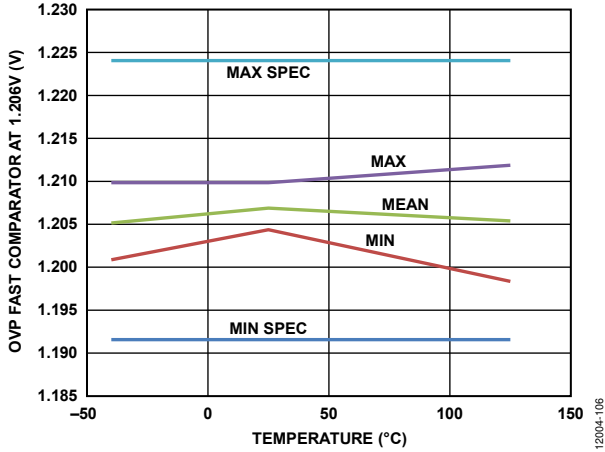


Figure 11. OVP Fast Comparator at 1.206 V vs. Temperature

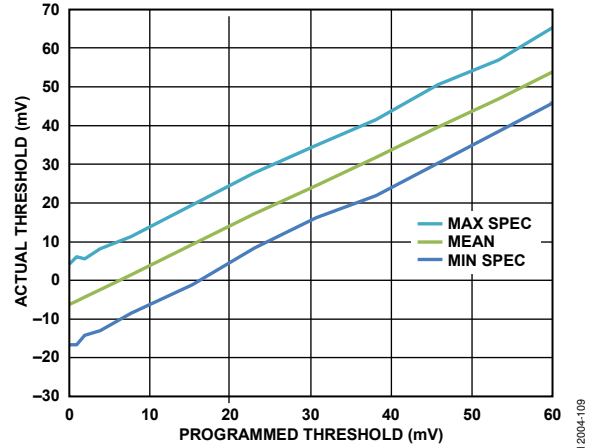


Figure 14. CS2 Forward Comparator Accuracy, 0 mV to 60 mV Range

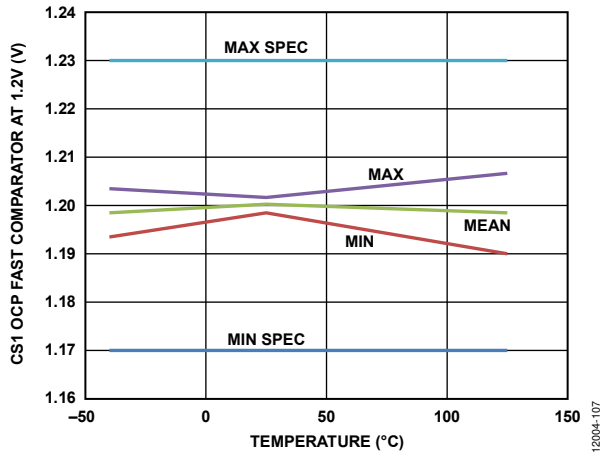


Figure 12. CS1 OCP Fast Comparator at 1.2 V vs. Temperature

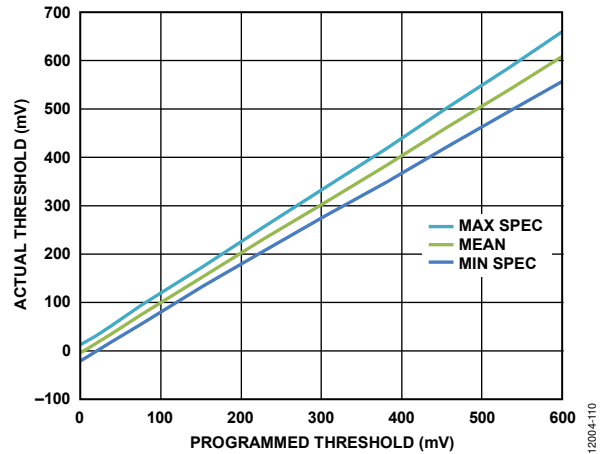


Figure 15. CS2 Forward Comparator Accuracy, 0 mV to 600 mV Range

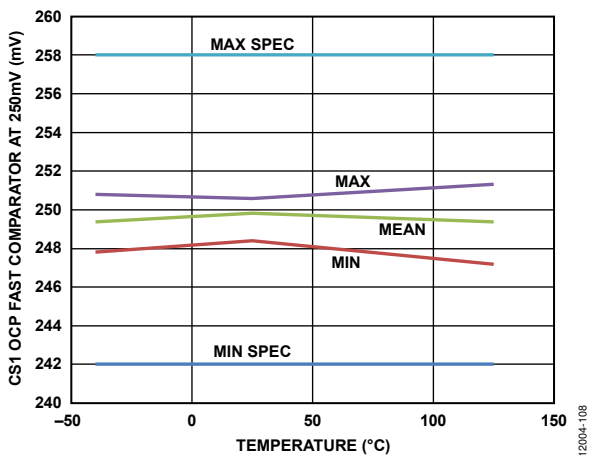


Figure 13. CS1 OCP Fast Comparator at 250 mV vs. Temperature

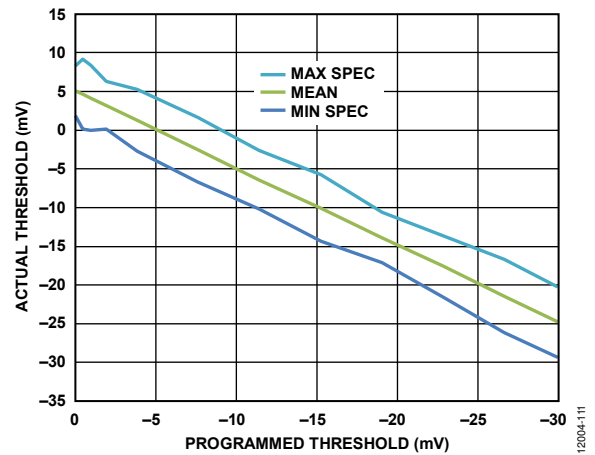


Figure 16. CS2 Reverse Comparator, 0 mV to -30 mV Range



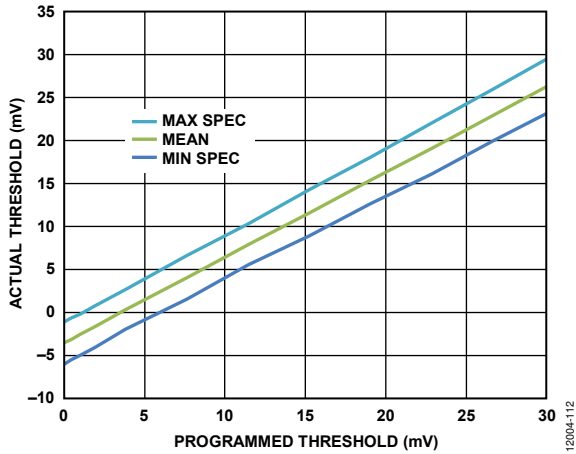


Figure 17. CS2 Reverse Comparator, 0 mV to 30 mV Range

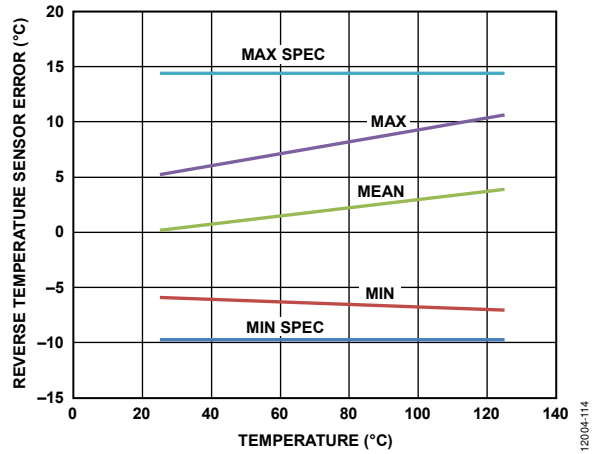


Figure 19. Reverse Temperature Sensor Error vs. Temperature

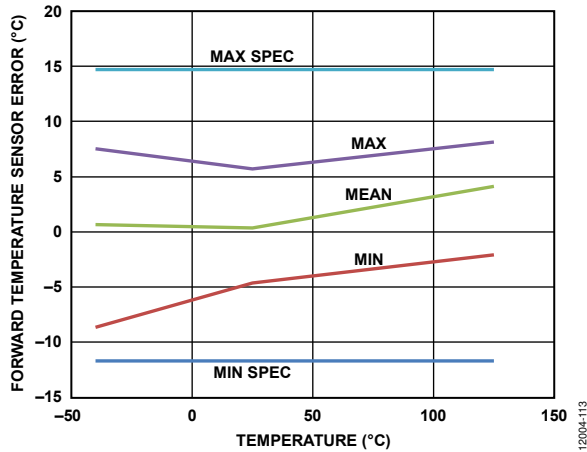


Figure 18. Forward Temperature Sensor Error vs. Temperature

## CONTROLLER ARCHITECTURE

The **ADP1055** is an application specific digital controller based on finite state machine (FSM) architecture. The **ADP1055** supports a subset of the PMBus Revision 1.2 standard and also has extended manufacturer specific commands to provide a feature rich digital power product.

Dedicated ADCs and comparators constitute the analog front end of the controller, feeding information to the digital core. The information is processed and used to generate the programmable PWM signals and to take action for various features such as light load or overvoltage/overcurrent protection.

The **ADP1055** has six PWM outputs: OUTA to OUTD for the primary side switches and SR1 and SR2 for the secondary side synchronous rectifiers. The **ADP1055** allows individual programming of the PWM outputs to form the timing of the power switches for any power topology, such as full bridge, full bridge phase shifted, current doubler, or active clamp.

Primary side information (current or voltage) is sensed and processed via the CS1 and VFF pins, whereas secondary side information is obtained via the CS2±, ISHARE, VS±, and OVP pins. A dedicated temperature sensor uses the JTD and JRTN pins. The input voltage is measured using the VFF pin and is used for line voltage feedforward. Extensive fault protection schemes are provided, and the controller also has a black box to record the state of the device (all sensor information including voltages, currents, temperatures, and flags) upon shutdown.

I<sup>2</sup>C/PMBus communication is facilitated by the SDA, SCL, and SMBALRT pins. Four GPIO pins can be used as flag output signals or as an interrupt service routine (ISR) to trigger a PMBus fault action. The CTRL pin is used as described in the PMBus specification.

Detailed descriptions of all **ADP1055** features are provided in the Theory of Operation section.

## START-UP AND POWER-DOWN SEQUENCING

### VDD AND VCORE PINS

The proper amount of decoupling capacitance must be placed between the VDD and AGND pins, as close as possible to the device to minimize the trace length. It is recommended that the VCORE pin not be loaded in any way.

### POWER-UP AND POWER-DOWN COMMANDS

The PMBus commands OPERATION (Register 0x01) and ON\_OFF\_CONFIG (Register 0x02) control the power-up and power-down behavior of the ADP1055.

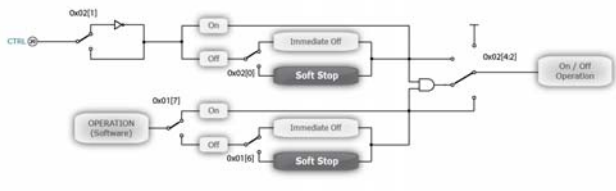


Figure 20. OPERATION (Register 0x01) and ON\_OFF\_CONFIG (Register 0x02)

### POWER SEQUENCING

Power sequencing is controlled using Register 0x60 through Register 0x66. The delays for the turn-on command (Register 0x60, TON\_DELAY) and the turn-off command (Register 0x64, TOFF\_DELAY) can each be programmed from 0 ms to 1024 ms in steps of 1 ms.

The soft start ramp-up time (Register 0x61, TON\_RISE) and the ramp-down time (Register 0x65, TOFF\_FALL) can be programmed from 0 ms to 100 ms in steps of 1 ms.

All values are rounded to the nearest available value. If a value is programmed outside the allowed range, it is forced to the nearest legal value.

### POWER-UP AND SOFT START ROUTINE

When VDD is applied to the device, a certain time elapses before the ADP1055 can regulate the power supply.

- When VDD is above UVLO and VCORE reaches above VCORE POR through an internal regulator, the ADP1055 downloads the user settings from Page 1 of the EEPROM into the internal registers.
- After the EEPROM download, the ADP1055 determines its address, programmed by the ADD pin and the I<sup>2</sup>C slave base address (Register 0xD0, SLV\_ADDR\_SELECT).
- The ADP1055 waits for an idle time, after which the device is ready for normal operation. If the black box must erase a page to precondition the EEPROM for storing, the idle time is extended by ~35 ms (see the Black Box Timing section).
- If the ADP1055 is programmed to power up at this time (OPERATION is enabled), the soft start ramp begins. Otherwise, the ADP1055 waits for the OPERATION command.

The outputs start switching, depending on the configuration of the OPERATION command (Register 0x01) and the ON\_OFF\_CONFIG command (Register 0x02).

If the ADP1055 is programmed to be always on (Register 0x02[4] = 0), the device begins the soft start ramp. Figure 21 shows the entire soft start process.

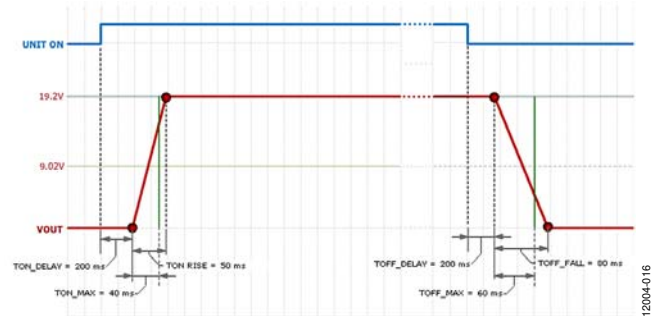


Figure 21. Example of Soft Start and Soft Stop Settings in the GUI

The soft start proceeds as follows.

- Upon power-up, the ADP1055 waits for the programmed TON\_DELAY (Register 0x60) and ramps to the regulation voltage according to the time programmed in TON\_RISE (Register 0x61).
- The soft start begins to ramp up the internal digital reference. The total duration of the soft start ramp is programmable using the TON\_RISE command. The TON\_MAX command specifies the maximum on time before which the output voltage must exceed the VOUT\_UV\_FAULT\_LIMIT (Register 0x44). If the VOUT\_UV\_FAULT\_LIMIT is set to 0, the TON\_MAX value is ignored.

If the soft start from precharge function is enabled (Register 0xFE51[0] = 1), the soft start ramp starts from the current value of the output voltage sensed on VS± and, therefore, the soft start ramp time is reduced proportionally.

### SOFT STOP ROUTINE

The soft stop process occurs in a manner similar to the soft start process, using the TOFF\_DELAY, TOFF\_MAX, and TOFF\_FALL commands. These commands are the counterparts of the TON\_DELAY, TON\_MAX, and TON\_RISE commands used for soft start. For more information about soft stop, see the Soft Stop section.

**VDD/VCORE OVLO**

The [ADP1055](#) has built-in overvoltage protection (OVP) on its supply rails. When the VDD or VCORE voltage rises above the OVLO threshold, the response can be programmed using Register 0xFE4D. It is recommended that when a VDD/VCORE OVP fault occurs, the response be set to download the EEPROM before restarting the [ADP1055](#). All features related to the OVLO function—such as debounce, fault ignore, and download EEPROM upon receiving a fault condition—are programmable using Register 0xFE4D[7:4].

VDD overvoltage is ignored when the device is downloading information from the EEPROM, even if the overvoltage occurs during the initial power-up or due to the setting of Register 0xFE4D[6]. VDD overvoltage is recognized as a fault only after the EEPROM download is complete. The [ADP1055](#) has a 4 ms idle time after an EEPROM download.

If the VDD overvoltage occurs during the ramp-up of VDD and the [ADP1055](#) has not initiated the EEPROM download, the device responds according to the default setting of Bit 7 in Register 0xFE4D, which is to ignore VDD OV.

## CONTROL LOOP AND PWM OPERATION

### VOLTAGE SENSE, FEEDBACK, AND CONTROL LOOP

The  $VS_{\pm}$  pins are used for the monitoring and protection of the remote load voltage. The differential  $VS_{\pm}$  input pins are the main feedback sense point for the power supply control loop. The  $VS_{\pm}$  sense point on the power rail requires an external resistor divider to bring the nominal common-mode signal to 1 V at the  $VS_{\pm}$  pins. This resistor divider is programmed into `VOUT_SCALE_LOOP` and `VOUT_SCALE_MONITOR` accordingly. The resistor divider is necessary because the input range is 0 V to 1.6 V. The divided-down signal is internally fed into a high frequency (HF) ADC. The HF ADC is also the high frequency feedback loop for the power supply.

### OUTPUT VOLTAGE SENSE

The output voltage is fed back to the  $VS_{\pm}$  pins, where it is compared with a reference set by a 12-bit DAC (see Figure 22). The difference is then fed into the flash ADC; in this configuration, the flash ADC does not see the fraction of the output voltage set by the resistor divider, but instead sees only the error voltage. The error voltage is then fed into the digital filter, which decides the duty cycle command for the next switching period. The number of samples taken by the flash ADC can be configured in Register `0xFE67[7:4]` (see Table 215). The recommended configuration of this register is automatically configured using the GUI.

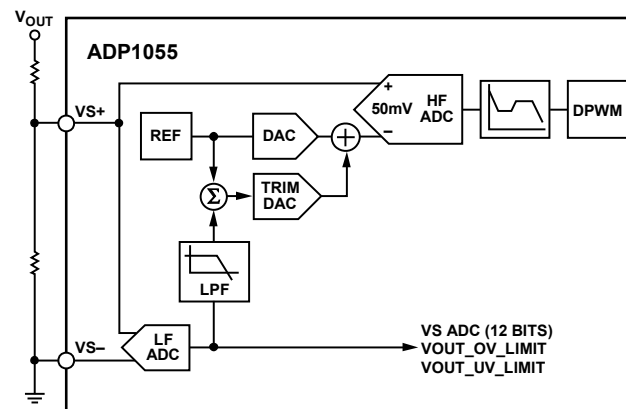


Figure 22. Output Voltage Sense and Feedback

The output voltage is also sampled using a low frequency ADC. The output voltage is fed to a low-pass filter that is used to set the output of a trim DAC; the trim DAC finely adjusts the output voltage as part of the autocorrection loop (see the Voltage Loop Autocorrection section).

### DIGITAL FILTER

The loop response of the power supply can be changed using the internal programmable digital filter. A Type 3 filter architecture has been implemented. To tailor the loop response to the specific application, the low frequency gain, zero location, pole location, and high frequency gain can all be set individually (see the Digital Filter Programming Registers section). It is recommended that the Analog Devices, Inc., software GUI be used to program the filter. The software GUI displays the filter response in Bode plot

format and can be used to calculate all stability criteria for the power supply.

From the sensed voltage to the duty cycle, the transfer function of the filter in z-domain is as follows:

$$H(z) = \left( \frac{D}{LFG} \times \frac{1}{(1-z^{-1})} + \frac{C}{HFG} \frac{\left(1 - \frac{B}{256}z^{-1}\right)}{\left(1 - \frac{A}{256}z^{-1}\right)} \times ADD\_PZ \right)$$

where:

A = filter pole register value (in decimal).

B = filter zero register value (in decimal).

C = high frequency gain register value (in decimal).

D = low frequency gain register value (in decimal).

$LFG = 5.968 \times m \times 10^6 / f_{sw}$ .

$HFG = 3.73 \times m \times 10^5 / f_{sw}$ .

$m = 1$  when  $48.8 \text{ kHz} \leq f_{sw} < 97.7 \text{ kHz}$ .

$m = 2$  when  $97.7 \text{ kHz} \leq f_{sw} < 195.3 \text{ kHz}$ .

$m = 4$  when  $195.3 \text{ kHz} \leq f_{sw} < 390.6 \text{ kHz}$ .

$m = 8$  when  $390.6 \text{ kHz} \leq f_{sw}$ .

`ADD_PZ` is an additional pole or additional zero that can be added to the compensator.

The additional zero takes this form:

$$1 - \frac{E}{256} \times z^{-1}$$

The additional pole takes this form:

$$\frac{1}{\left(1 - \frac{E}{256} \times z^{-1}\right)}$$

where  $E$  is the value (in decimal) of the additional pole zero frequency gain register (Register `0xFE60` and Register `0xFE61`).

To transfer the z-domain value to the s-domain, plug the following bilinear transformation equation into the  $H(z)$  equation:

$$z(s) = \frac{2f_{sw} + s}{2f_{sw} - s}$$

where  $f_{sw}$  is the switching frequency.

The digital filter introduces an extra phase delay element into the control loop. The digital filter circuit sends the duty cycle information to the PWM circuit at the beginning of each switching cycle (unlike an analog controller, which makes decisions on the duty cycle information continuously). Therefore, the extra phase delay for phase margin,  $\Phi$ , introduced by the filter block is

$$\Phi = 360 \times (f_c / f_{sw})$$

where:

$f_c$  is the crossover frequency.

$f_{sw}$  is the switching frequency.

At one-tenth the switching frequency, the phase delay is  $36^\circ$ . For double update rate, the phase delay is reduced to  $18^\circ$ . The GUI

incorporates this phase delay into its calculations. Note that the GUI does not account for other delays such as gate driver and propagation delays.

**DIGITAL FILTER PROGRAMMING REGISTERS**

Three sets of registers allow three different filters to be programmed.

- Normal mode filter (used for CCM or heavy load and configured in Register 0xFE01 to Register 0xFE04)
- Light load mode filter (configured in Register 0xFE05 to Register 0xFE08)
- Soft start filter (configured in Register 0xFE09 to Register 0xFE0C)

The software GUI allows the user to program the light load mode filter in the same manner as the normal mode filter. It is recommended that the GUI be used for this purpose.

**DIGITAL COMPENSATION FILTERS DURING SOFT START**

The ADP1055 has a dedicated soft start filter (SSF) that can be used to fine-tune and optimize the dynamic response during the output voltage ramp-up.

During soft start, the ADP1055 determines the load condition and after the voltage reaches 12.5% of the nominal output voltage value, it determines the current load condition and switches filters accordingly to the light load mode threshold (Register 0xFE5F[3:1]). If the load current is below the light load mode threshold, the ADP1055 switches to the light load mode filter (LLF). If the load current is above the light load mode threshold, the normal mode filter is used until the end of the soft start ramp, even if the device subsequently enters light load mode based on a change to the load current.

Other configurations can be programmed to use different filters during soft start, as follows:

- Force soft start filter (Register 0xFE51[2]). This option forces the ADP1055 to use the soft start filter. In some cases, this option allows better fine-tuning of the ramp-up voltage.
- Disable light load mode during soft start (Register 0xFE51[1]). This option prevents the use of the light load mode filter during soft start, even if the light load condition is met. The light load mode filter is available for use after the end of the soft start ramp.

Figure 23 shows the use of filters during soft start.

**Table 5. State of Synchronous Rectifiers and Filter Used**

Load	State of SRx Outputs		Filter Used
	Regular Mode	Diode Emulation Mode	
Medium to heavy load Below LLM threshold	SRs in CCM SRs in LLM	SRs in CCM Diode emulation SRs	Normal mode filter (Register 0xFE01 to Register 0xFE04). LLM filter (Register 0xFE05 to Register 0xFE08.) When diode emulation mode is in use, the LLM filter is activated after the LLM threshold is crossed.
Deep LLM	SRs are off	SRs are off	LLM filter (Register 0xFE05 to Register 0xFE08).

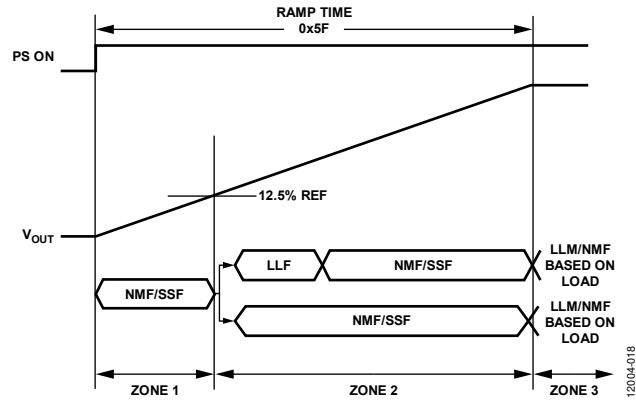


Figure 23. Digital Filters During Soft Start (Low Temperature Filter Not Shown)

As shown in Figure 23, in Zone 1, the ADP1055 starts with the normal mode filter or the soft start filter. Zone 2 begins when the voltage reaches 12.5% of the nominal output voltage value. At this point, the ADP1055 checks whether the system is in light load mode, and the choice of filter is based on the following criteria:

- If the system is in light load mode, the ADP1055 switches to the light load mode filter (unless the option to disable the LLM filter was previously selected).
- If the system is not in light load mode, the ADP1055 continues to use the filter used in Zone 1: the normal mode filter or the soft start filter.

The ADP1055 changes to the LLM filter if the load changes during Zone 2 (voltage rises from 12.5% to 100% of the soft start ramp). The filter does not revert to LLM if the load drops until after the end of soft start.

In Zone 3 the filter changes to the NMF or LLM filter, depending on the load.

**FILTER TRANSITION**

To avoid output voltage glitches and to provide a seamless transition from one filter to another, the ADP1055 supports programmable filter transitions. This feature allows a gradual transition from one filter to another. Filter transitions are programmed using Register 0xFE4A[2:0]. When the ADP1055 switches filters, the switching action is changed in 32 steps. The step size can be programmed over several cycles (1t<sub>sw</sub> to 32t<sub>sw</sub>) to avoid glitches in the output. The filter used depends on the state of the synchronous rectifiers and whether the system is in continuous conduction mode (CCM) or discontinuous conduction mode (DCM) (see Table 5).

**PWM AND SYNCHRONOUS RECTIFIER OUTPUTS (OUTA, OUTB, OUTC, OUTD, SR1, SR2)**

The PWM and SR outputs are used for control of the primary side drivers and the synchronous rectifier drivers. These outputs can be used for several control topologies, such as full-bridge, phase-shifted ZVS configurations and interleaved, two switch forward converter configurations. Delays between the rising and falling edges can be individually programmed (see Figure 24).

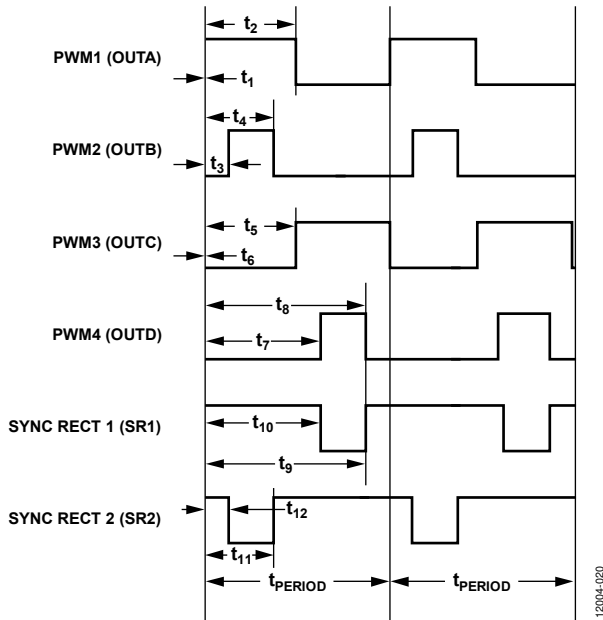


Figure 24. PWM Timing Diagram

Take special care to avoid shoot-through and cross-conduction. It is recommended that the software GUI be used to program these outputs. Figure 25 shows an example configuration to drive a full-bridge topology with synchronous rectification.

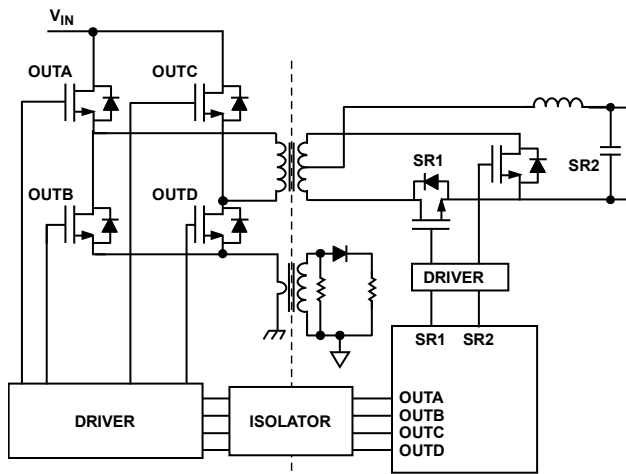


Figure 25. PWM Pin Assignment for Full-Bridge, Phase-Shifted Topology with Synchronous Rectification

**Go and Auto Go Command**

The PWM outputs (OUTA to OUTD) and the SR outputs (SR1 and SR2) are all synchronized with each other. Therefore, when reprogramming more than one of these outputs, it is important to first update all the registers and then latch the information into the ADP1055 at the same time. This simultaneous updating of the PWM outputs is facilitated by the GO command (Register 0xFE00). The GO command acts as a gate to apply all functions related to the commands at the same time.

The GO command gates the following functions:

- Frequency synchronization
- Line voltage feedforward
- Double update rate, volt-second balance
- Digital filter settings
- Frequency and PWM settings
- Voltage reference change

During reprogramming, the outputs are temporarily disabled. It is recommended that the PWM outputs be disabled when not in use.

The PMBus allows the user to change the voltage setting and the switching frequency on-the-fly. The auto go command (Register 0xFE5B) is an added level of protection that restricts the user from making a change to certain commands (see Table 203).

For more information about the various programmable switching frequencies and PWM timings, see the Switching Frequency Programming section.

**SYNCHRONOUS RECTIFICATION**

SR1 and SR2 are recommended for use as the PWM control signals when using synchronous rectification. These PWM signals can be configured much like the other PWM outputs.

## MODULATION LIMIT

The modulation limit register (Register 0xFE53) can be programmed to apply a maximum duty cycle modulation limit to any PWM signal, thus acting as a clamp for the maximum modulation range of any PWM output. When modulation is enabled, the maximum modulation limit is applied to all PWM outputs collectively. As shown in Figure 26, this limit is the maximum time variation for the modulated edges from the default timing, following the configured modulation direction.

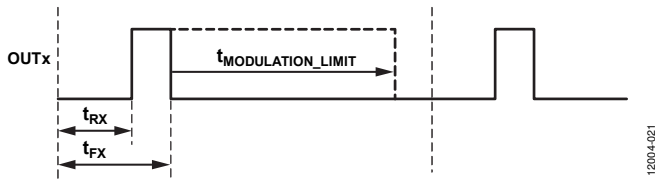


Figure 26. Modulation Limit Settings

There is no minimum duty cycle limit setting. Therefore, the user must set the rising edges and falling edges based on the case with the least modulation to enter pulse skipping mode under very light load conditions.

Each LSB in Register 0xFE53[6:0] corresponds to a unit of a base time step size. The base time step size (20 ns, 40 ns, 80 ns, or 160 ns) depends on the switching frequency; therefore, the modulation limit is based on the value in Register 0xFE53[6:0] multiplied by the corresponding base time step size. The modulated edges are prevented from extending beyond one switching cycle, but the maximum duty cycle is 100% (the minimum pulse width is 5 ns).

The GUI provided with the [ADP1055](#) is recommended for programming this feature (see Figure 27).



Figure 27. Setting Modulation Limits (Modulation Range Shown by Arrows)

## SWITCHING FREQUENCY PROGRAMMING

The FREQUENCY\_SWITCH command (Register 0x33) sets the switching frequency of the [ADP1055](#) in kilohertz. This command has two data bytes formatted in the linear data format; the programmable frequency ranges from 48 kHz to 1000 kHz.

The [ADP1055](#) does not support every possible frequency due to the infinite combinations of exponent and mantissa values that can be programmed. If a programmed frequency does not exactly match a supported value, it is rounded up to the nearest available frequency. It is recommended that the READ\_FREQUENCY command (Register 0x95) be used to determine the exact value of the switching frequency. Table 244 lists the supported frequencies.



## ADCs AND TELEMETRY

Two kinds of ADCs are used in the [ADP1055](#):

- Low frequency (LF)  $\Sigma$ - $\Delta$  ADCs that runs at 1.56 MHz for accurate measurement and telemetry
- High frequency (HF) flash ADCs for the feedback and control loop

$\Sigma$ - $\Delta$  ADCs have a resolution of one bit and operate differently from traditional flash ADCs. The equivalent resolution obtainable depends on how long the output bit stream of the  $\Sigma$ - $\Delta$  ADC is sampled.

$\Sigma$ - $\Delta$  ADCs also differ from Nyquist rate ADCs in that the quantization noise is not uniform across the frequency spectrum. At lower frequencies, the noise is lower, and at higher frequencies, the noise is higher (see Figure 28).

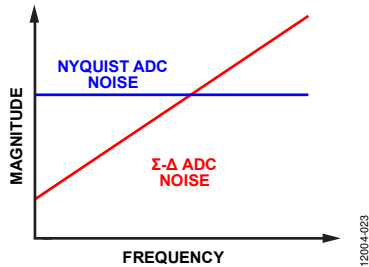


Figure 28. Noise Performance for Nyquist Rate and  $\Sigma$ - $\Delta$  ADCs

The low frequency ADC runs at approximately 1.56 MHz. For a specified bandwidth, the equivalent resolution can be calculated as follows:

$$\ln(1.56 \text{ MHz}/BW)/\ln 2 = N \text{ bits}$$

For example, at a bandwidth of 95 Hz, the equivalent resolution/noise is

$$\ln(1.56 \text{ MHz}/95)/\ln 2 = 14 \text{ bits}$$

At a bandwidth of 1.5 kHz, the equivalent resolution/noise is

$$\ln(1.56 \text{ MHz}/1.5 \text{ kHz})/\ln 2 = 10 \text{ bits}$$

The ADC output information is available in the value registers (Register 0xFE96 to Register 0xFE A3) or through the PMBus READ\_x commands, where x = VOUT, IOUT, and so on.

## ADCs FOR CURRENT SENSING

The [ADP1055](#) has two current sense inputs: CS1 and CS2±. These inputs sense, protect, and control the primary input current and the secondary output current information. The CS1 and CS2± inputs can be calibrated to reduce errors due to external components for accurate telemetry.

### CS1 ADC for Primary Side Current

The CS1 pin is typically used for the monitoring and protection of the primary side current. The primary side current is sensed using a current transformer (CT). The input signal at the CS1 pin is fed into the CS1 ADC for current monitoring. Figure 29 shows the typical configuration for the current sense. The READ\_IIN command reports the average input current; this reading is updated every 10.5 ms.

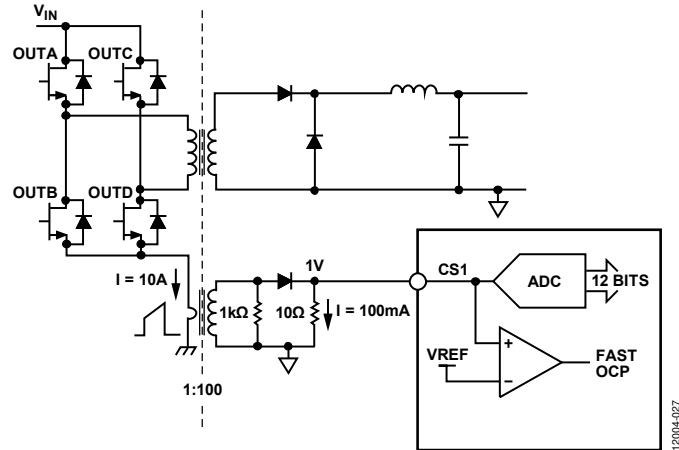


Figure 29. Current Sense 1 (CS1) Operation

### CS2 ADC for Secondary Side Current

The CS2+ and CS2- pins are differential inputs used for the monitoring and protection of the secondary side current. The [ADP1055](#) supports differential sensing using low-side current sensing with two ranges for the ADC: 30 mV and 60 mV.

The low input range is used to operate in level shifting mode, when the CS2 terminals are connected directly to the shunt resistor (see Figure 30). In this mode, a pair of internal resistors and current sources are used to perform the necessary level shifting. In this mode, only low-side current sensing is possible, and the ADC range is programmable to 30 mV or 60 mV.

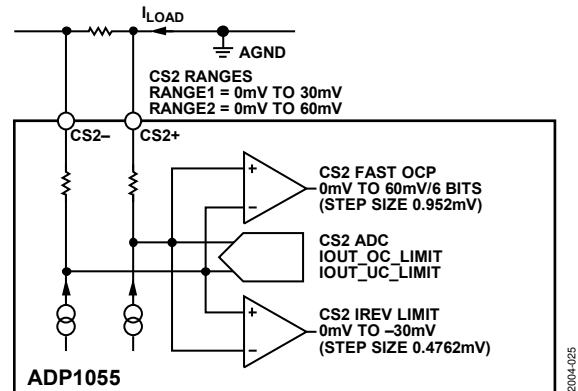


Figure 30. Differential Low-Side Sensing

An additional range of 480 mV (single-ended input only) can be used for high-side sensing or simply as an input with a higher range (see Figure 31). The high input range is used for operation in single-ended mode, where external circuitry must be provided for level shifting of the current signal.

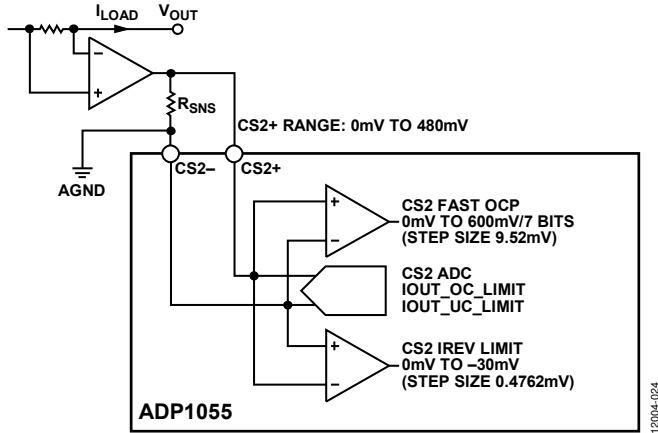


Figure 31. Single-Ended High-Side Sensing

The READ\_IOUT command reports the average output current; this reading is updated every 2.6 ms.

**ADCs FOR VOLTAGE SENSING**

**VFF ADC for Input Voltage**

The VFF pin is typically used for the monitoring and protection of the primary side voltage. Figure 32 shows a typical configuration for the feedforward circuit.

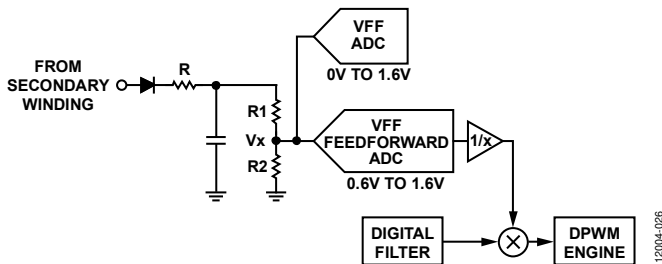


Figure 32. Feedforward Configuration

The input voltage signal can be sensed at the secondary winding of the isolation transformer before the output inductor and must be filtered by an RCD network to eliminate the voltage spike at the switch node (see Figure 32).

In nonisolated topologies, the VFF ADC is connected directly to the primary voltage via a resistive divider with some filtering to eliminate voltage spikes on the bulk capacitor when the power switch is turned on or off. The READ\_VIN command reports the average input voltage; this reading is updated every 10.5 ms.

**VS ADC for Output Voltage**

The VS± pins of the ADP1055 are used for the monitoring, control, and protection of the power supply output. Typically, the output voltage is divided down using a resistive divider such that at the rated output, there is 1.0 V on the VS± pins. The READ\_VOUT command reports the average output voltage; this reading is updated every 10.5 ms.

**ADCs FOR TEMPERATURE SENSING**

For information about the temperature sensing ADCs, see the Temperature Sensing section.