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3 MHz, 600 mA, Low Quiescent Current Buck with 300 mA LDO Regulator

Data Sheet

ADP2140

FEATURES

- Input voltage range: 2.3 V to 5.5 V
- LDO input (VIN2) 1.65 V to 5.5 V
- Buck output voltage range: 1.0 V to 3.3 V
- LDO output voltage range: 0.8 V to 3.3 V
- Buck output current: 600 mA
- LDO output current: 300 mA
- LDO quiescent current: 22 µA with zero load
- Buck quiescent current: 20 µA in PSM mode
- Low shutdown current: <0.3 µA
- Low LDO dropout 110 mV @ 300 mA load
- High LDO PSRR
  - 65 dB @ 10 kHz at V_{OUT2} = 1.2 V
  - 55 dB @ 100 kHz at V_{OUT2} = 1.2 V
- Low noise LDO: 40 µV rms at V_{OUT2} = 1.2 V
- Initial accuracy: ±1%
- Current-limit and thermal overload protection
- Power-good indicator
- Optional enable sequencing
- 10-lead 0.75 mm × 3 mm × 3 mm LFCSP package

APPLICATIONS

- Mobile phones
- Personal media players
- Digital camera and audio devices
- Portable and battery-powered equipment

TYPICAL APPLICATION CIRCUITS

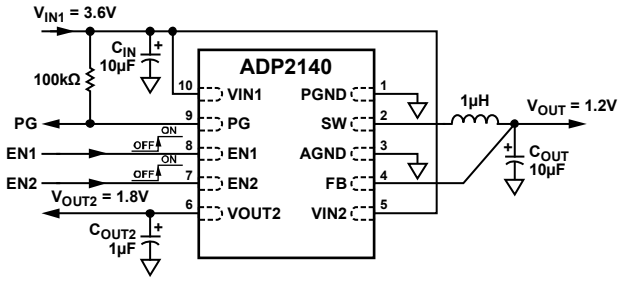

Figure 1. ADP2140 with LDO Connected to V_{IN1}

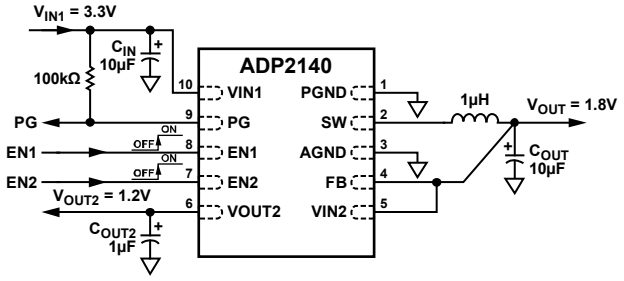

Figure 2. ADP2140 with LDO Connected to Buck Output

GENERAL DESCRIPTION

The ADP2140 includes a high efficiency, low quiescent 600 mA stepdown dc-to-dc converter and a 300 mA LDO packaged in a small 10-lead 3 mm × 3 mm LFCSP. The total solution requires only four tiny external components.

The buck regulator uses a proprietary high speed current-mode, constant frequency, pulse-width modulation (PWM) control scheme for excellent stability and transient response. To ensure the longest battery life in portable applications, the ADP2140 has a power saving variable frequency mode to reduce switching frequency under light loads.

The LDO is a low quiescent current, low dropout linear regulator designed to operate in a split supply mode with V_{IN2} as low as 1.65 V. The low input voltage minimum allows the LDO to be powered from the output of the buck regulator increasing efficiency and reducing power dissipation. The ADP2140 runs from input voltages of 2.3 V to 5.5 V allowing single Li+/Li− polymer cell, multiple alkaline/NiMH cell, PCMCIA, and other standard power sources.

ADP2140 includes a power-good pin, soft start, and internal compensation. Numerous power sequencing options are user-selectable through two enable inputs. In autosequencing mode, the highest voltage output enables on the rising edge of EN1. During logic controlled shutdown, the input disconnects from the output and draws less than 300 nA from the input source. Other key features include: undervoltage lockout to prevent deep battery discharge, soft start to prevent input current overshoot at startup, and both short-circuit protection and thermal overload protection circuits to prevent damage in adverse conditions.

When the ADP2140 is used with two 0603 capacitors, one 0402 capacitor, one 0402 resistor, and one 0805 chip inductor, the total solution size is approximately 90 mm^2 resulting in the smallest footprint solution to meet a variety of portable applications.

Rev. A
Document Feedback

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ADP2140* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADP2140 Evaluation Board

DOCUMENTATION

Data Sheet

- ADP2140: 3 MHz, 600 mA, Low Quiescent Current Buck with 300 mA LDO Regulator Data Sheet

User Guides

- UG-089: RedyKit for the ADP2140
- UG-122: Evaluating the ADP2140 Buck and LDO Combination Regulator

TOOLS AND SIMULATIONS

- ADI Linear Regulator Design Tool and Parametric Search
- ADIsimPower™ Voltage Regulator Design Tool

DESIGN RESOURCES

- ADP2140 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADP2140 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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REVISION HISTORY

9/12—Rev. 0 to Rev. A

Updated Outline Dimensions ... 30
Changes to Ordering Guide ... 30

6/10—Revision 0: Initial Version

SPECIFICATIONS

V_{IN1} = 3.6 V, V_{IN2} = V_{OUT2} + 0.3 V or 1.65 V, whichever is greater; 5 V EN1 = EN2 = V_{IN1}; I_{OUT} = 200 mA, I_{OUT2} = 10 mA, C_{IN} = 10 µF, C_{OUT} = 10 µF, C_{OUT2} = 1 µF, L_{OUT} = 1 µH; T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
BUCK SECTION						
Input Voltage Range	V_{IN1}		2.3		5.5	V
Buck Output Accuracy	V_{OUT}	I_{OUT} = 10 mA	−1.5		+1.5	%
		V_{IN1} = 2.3 V or (V_{OUT} + 0.5 V) to 5.5 V, I_{OUT} = 1 mA to 600 mA	−2.5		+2.5	%
Transient Load Regulation	$V_{TR-LOAD}$	V_{OUT} = 1.8 V				
		Load = 50 mA to 250 mA, rise/fall time = 200 ns		75		mV
		Load = 200 mA to 600 mA, rise/fall time = 200 ns		75		mV
Transient Line Regulation	$V_{TR-LINE}$	Line transient = 4 V to 5 V, 4 µs rise time				
		V_{OUT} = 1.0 V		40		mV
		V_{OUT} = 1.8 V		25		mV
		V_{OUT} = 3.3 V		25		mV
PWM To PSM Threshold		V_{IN1} = 2.3 V or (V_{OUT} + 0.5 V) to 5.5 V		100		mA
Output Current	I_{OUT}				600	mA
Current Limit	I_{LIM}	V_{IN1} = 2.3 V or (V_{OUT} + 0.5 V) to 5.5 V		1100	1300	mA
Switch On Resistance						
PFET	R_{PFET}	V_{IN1} = 2.3 V to 5.5 V		250		mΩ
NFET	R_{NFET}	V_{IN1} = 2.3 V to 5.5 V		250		mΩ
Switch Leakage Current	$I_{LEAK-SW}$	EN1 = GND, VIN1 = 5.5 V, and SW = 0 V			−1	µA
Quiescent Current	I_Q	No load, device not switching		20	30	µA
Minimum On Time	$ON\text{-}TIME_{MIN}$			70		ns
Oscillator Frequency	FREQ		2.55	3.0	3.15	MHz
Frequency Foldback Threshold	V_{FOLD}	Output voltage where f_{SW} ≤ 50% of nominal frequency		50		%
Start-Up Time[1]	$t_{START-UP}$	V_{OUT} = 1.8 V, 600 mA load		70		µs
Soft Start Time[2]	SS_{TIME}	V_{OUT} = 1.8 V, 600 mA load		150		µs
LDO SECTION						
Input Voltage Range	V_{IN2}		1.65		5.5	V
LDO Output Accuracy	V_{OUT2}	I_{OUT2} = 10 mA, T_J = 25°C	−1		+1	%
		1 mA < I_{OUT2} < 300 mA, V_{IN2} = (V_{OUT2} + 0.3 V) to 5.5 V, T_J = 25°C	−1.5		+1.5	%
		1 mA < I_{OUT2} < 300 mA, V_{IN2} = (V_{OUT2} + 0.3 V) to 5.5 V	−3		+3	%
Line Regulation	$\Delta V_{OUT2}/\Delta V_{IN2}$	V_{IN2} = (V_{OUT2} + 0.3 V) to 5.5 V, I_{OUT2} = 10 mA	−0.05		+0.05	%/V
Load Regulation[3]	$\Delta V_{OUT2}/\Delta I_{OUT2}$	I_{OUT2} = 1 mA to 300 mA		0.001	0.005	%/mA
Dropout Voltage[4]	$V_{DROPOUT}$	I_{OUT2} = 10 mA, V_{OUT2} = 1.8 V		4	7	mV
		I_{OUT2} = 300 mA, V_{OUT2} = 1.8 V		110	200	mV
Ground Current	I_{AGND}	No load, buck disabled		22	35	µA
		I_{OUT2} = 10 mA		65	90	µA
		I_{OUT2} = 300 mA		150	220	µA
Power Supply Rejection Ratio	PSRR	V_{IN2} = V_{OUT2} + 1 V, V_{IN1} = 5 V, I_{OUT2} = 10 mA				
PSRR on V_{IN2}		10 kHz, V_{OUT2} = 1.2 V, 1.8 V, 3.3 V		65		dB
		100 kHz, V_{OUT2} = 3.3 V		53		dB
		100 kHz, V_{OUT2} = 1.8 V		54		dB
		100 kHz, V_{OUT2} = 1.2 V		55		dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Output Noise	OUT_{NOISE}	$V_{IN2} = V_{IN1} = 5$ V, $I_{OUT2} = 10$ mA				
		10 Hz to 100 kHz, $V_{OUT2} = 0.8$ V		29		μV rms
		10 Hz to 100 kHz, $V_{OUT2} = 1.2$ V		40		μV rms
		10 Hz to 100 kHz, $V_{OUT2} = 1.8$ V		50		μV rms
		10 Hz to 100 kHz, $V_{OUT2} = 2.5$ V		66		μV rms
		10 Hz to 100 kHz, $V_{OUT2} = 3.3$ V		88		μV rms
Current Limit	I_{LIM}	$T_J = 25°C$	360	500	760	mA
Input Leakage Current	$I_{LEAK-LDO}$	EN2 = GND, $V_{IN2} = 5.5$ V and $V_{OUT2} = 0$ V			1	μA
Start-Up Time[1]	$t_{START-UP}$	$V_{OUT2} = 3.3$ V, 300 mA load		70		μs
Soft Start Time[2]	SS_{TIME}	$V_{OUT2} = 3.3$ V, 300 mA load		130		μs
ADDITIONAL FUNCTIONS						
Undervoltage Lockout	UVLO					
Input Voltage Rising	$UVLO_{RISE}$			2.23	2.3	V
Input Voltage Falling	$UVLO_{FALL}$		2.05	2.16		V
EN Input						
EN1, EN2 Input Logic High	V_{IH}	$2.3 \text{ V} \le V_{IN1} \le 5.5$ V	1.0			V
EN1, EN2 Input Logic Low	V_{IL}	$2.3 \text{ V} \le V_{IN1} \le 5.5$ V			0.27	V
EN1, EN2 Input Leakage	I_{EN-LKG}	EN1, EN2 = V_{IN1} or GND		0.05		μA
		EN1, EN2 = V_{IN1} or GND			1	μA
Shutdown Current	I_{SHUT}	$V_{IN1} = 5.5$ V, EN1, EN2 = GND, $T_J = -40°C$ to $+85°C$		0.3	1.2	μA
Thermal Shutdown						
Threshold	TS_{SD}	T_J rising		150		°C
Hysteresis	TS_{SD-HYS}			20		°C
Power Good						
Rising Threshold	PG_{RISE}			92		$\%V_{OUT}$
Falling Threshold	PG_{FALL}			86		$\%V_{OUT}$
Power-Good Hysteresis	PG_{HYS}			6		$\%V_{OUT}$
Output Low	V_{OL}	$I_{SINK} = 4$ mA			0.2	V
Leakage Current	I_{OH}	Power-good pin pull-up voltage = 5.5 V			1	μA
Buck to LDO Delay	t_{DELAY}	PWM mode only		5		ms
Power-Good Delay	t_{RESET}	PWM mode only		5		ms

[1] Start-up time is defined as the time between the rising edge of ENx to V_{OUTx} being at 10% of the V_{OUTx} nominal value.
[2] Soft start time is defined as the time between V_{OUTx} being at 10% to V_{OUTx} being at 90% of the V_{OUTx} nominal value.
[3] Based on an endpoint calculation using 1 mA and 300 mA loads.
[4] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 2.3 V.

RECOMMENDED SPECIFICATIONS: CAPACITORS AND INDUCTOR

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
MINIMUM INPUT AND OUTPUT CAPACITANCE[1]		$T_A = -40°C$ to $+125°C$				
Buck	C_{MIN}		7.5	10		μF
LDO	C_{MIN}		0.7	1.0		μF
CAPACITOR ESR		$T_A = -40°C$ to $+125°C$				Ω
Buck	R_{ESR}		0.001		0.01	Ω
LDO	R_{ESR}		0.001		1	Ω
MINIMUM INDUCTOR	IND_{MIN}		0.7	1		μH

[1] The minimum input and output capacitance should be greater than 0.70 μF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R- and X5R-type capacitors are recommended, Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN1, VIN2 to PGND, AGND	−0.3 V to +6.5 V
VOUT2 to PGND, AGND	−0.3 V to V_{IN2}
SW to PGND, AGND	−0.3 V to V_{IN1}
FB to PGND, AGND	−0.3 V to +6.5 V
PG to PGND, AGND	−0.3 V to +6.5 V
EN1, EN2 to PGND, AGND	−0.3 V to +6.5 V
Storage Temperature Range	−65°C to +150°C
Operating Ambient Temperature Range	−40°C to +85°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP2140 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may need to be derated.

In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 in. × 3 in. circuit board. Refer to JESD 51-7 for detailed information on the board construction.

For more information, see AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path, as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

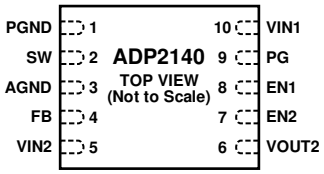
Table 4. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
10-Lead 3 mm × 3 mm LFCSP	35.3	16.9	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD ON THE BOTTOM OF THE LFCSP PACKAGE ENHANCES THERMAL PERFORMANCE AND IS ELECTRICALLY CONNECTED TO GROUND INSIDE THE PACKAGE. IT IS RECOMMENDED THAT THE EXPOSED PAD BE CONNECTED TO THE GROUND PLANE ON THE CIRCUIT BOARD.

07932-003

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin	Mnemonic	Description
1	PGND	Power Ground.
2	SW	Connection from Power MOSFETs to Inductor.
3	AGND	Analog Ground.
4	FB	Feedback from Buck Output.
5	VIN2	LDO Input Voltage.
6	VOUT2	LDO Output Voltage.
7	EN2	Logic 1 to Enable LDO or No Connect for Autosequencing.
8	EN1	Logic 1 to Enable Buck or Initiate Sequencing. This is a dual function pin and the state of EN2 determines which function is operational.
9	PG	Power Good. Open-drain output. PG is held low until both output voltages (which includes the external inductor and capacitor sensed by the FB pin) rise above 92% of nominal value. PG is held high until both outputs fall below 85% of nominal value.
10	VIN1	Analog Power Input.
	EP	Exposed Pad. The exposed pad on the bottom of the LFCSP package enhances thermal performance and is electrically connected to ground inside the package. It is recommended that the exposed pad be connected to the ground plane on the circuit board.

TYPICAL PERFORMANCE CHARACTERISTICS

BUCK OUTPUT

V_{IN1} = 4 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10 µF, T_A = 25°C, unless otherwise noted.

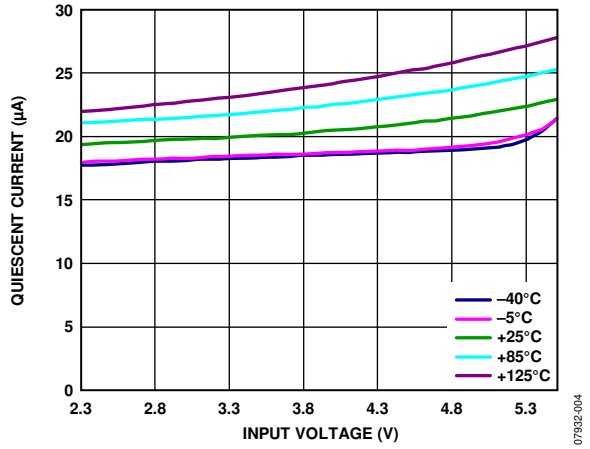


Figure 4. Quiescent Supply Current vs. Input Voltage, Different Temperatures

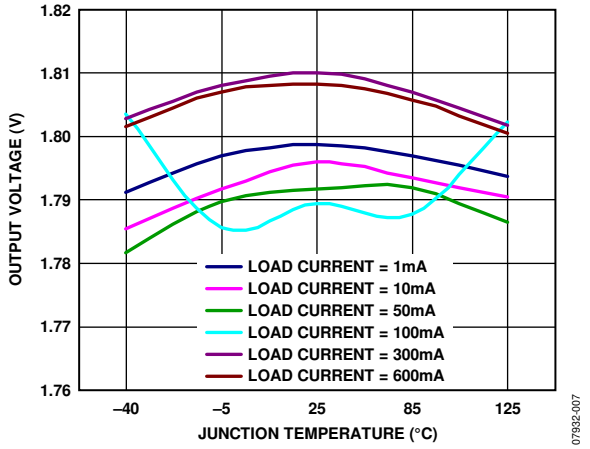


Figure 7. Output Voltage vs. Temperature, V_{IN1} = 2.3 V, Different Loads

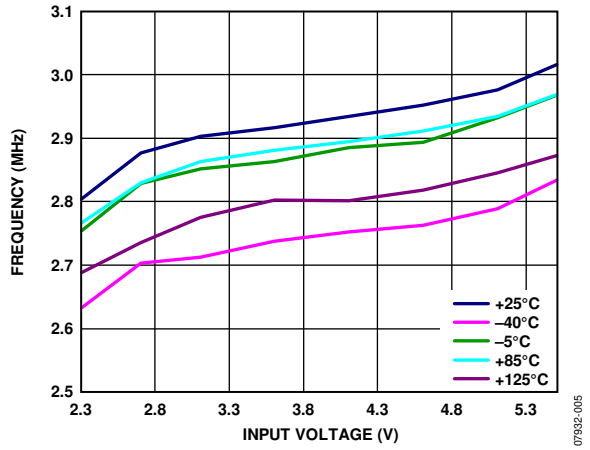


Figure 5. Switching Frequency vs. Input Voltage, Different Temperatures

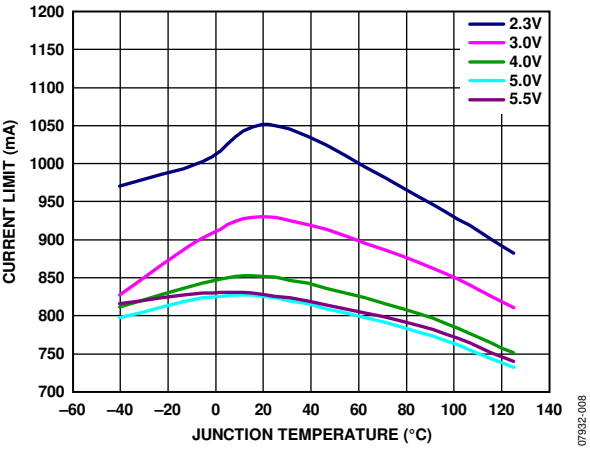


Figure 8. Current Limit vs. Temperature, Different Input Voltages

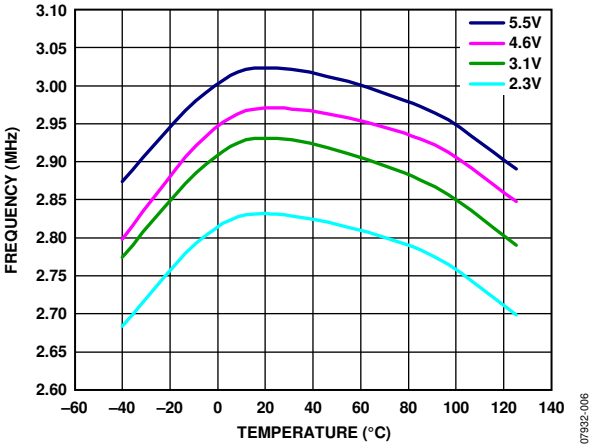


Figure 6. Switching Frequency vs. Temperature, Different Input Voltages

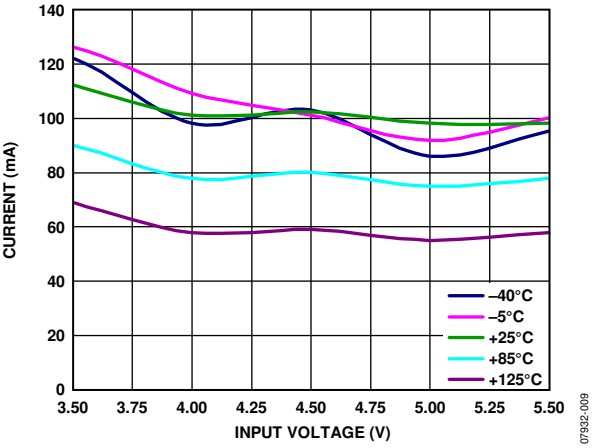


Figure 9. PSM to PWM Mode Transition vs. Input Voltage, Different Temperatures

V_{IN1} = 4 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10 µF, T_A = 25°C, unless otherwise noted.

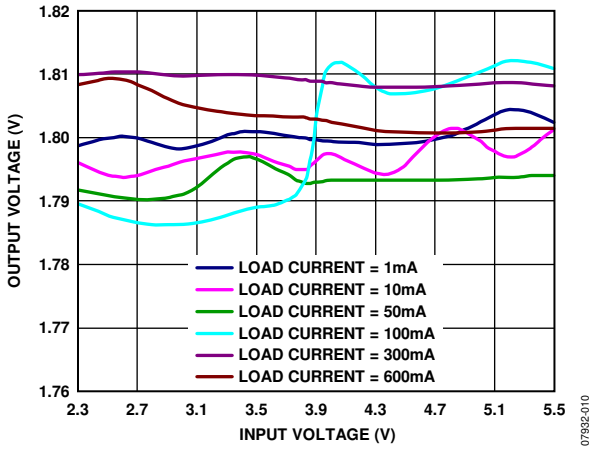


Figure 10. Line Regulation, V_{OUT} = 1.8 V, Different Loads

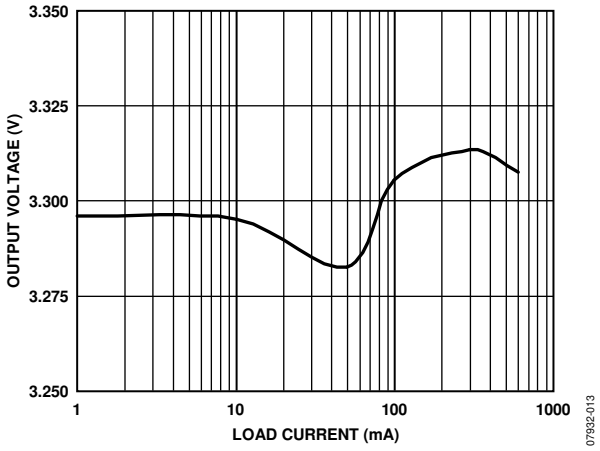


Figure 13. Load Regulation, V_{OUT} = 3.3 V

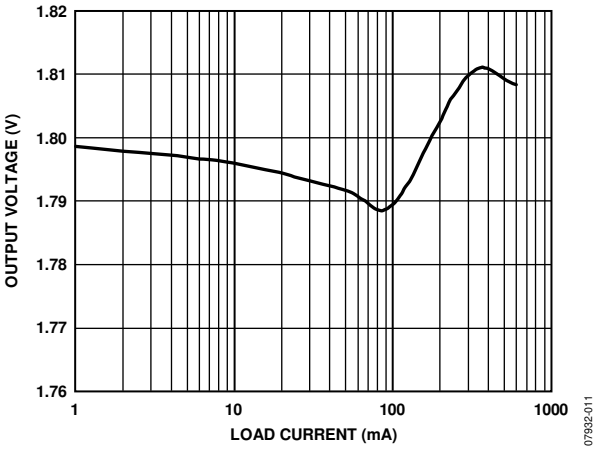


Figure 11. Load Regulation, V_{OUT} = 1.8 V, V_{IN1} = 2.3 V

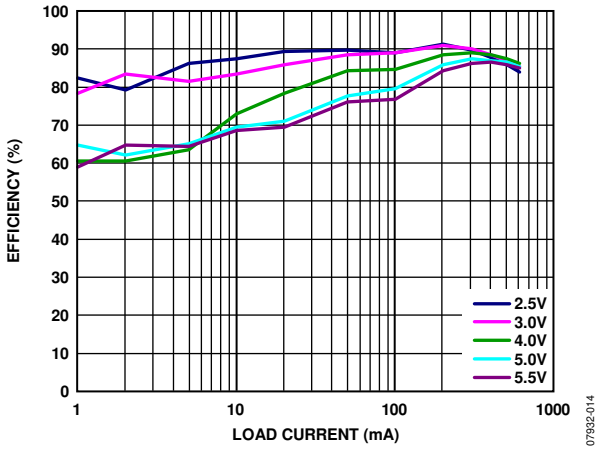


Figure 14. Efficiency vs. Load Current, V_{OUT} = 1.8 V, Different Input Voltages

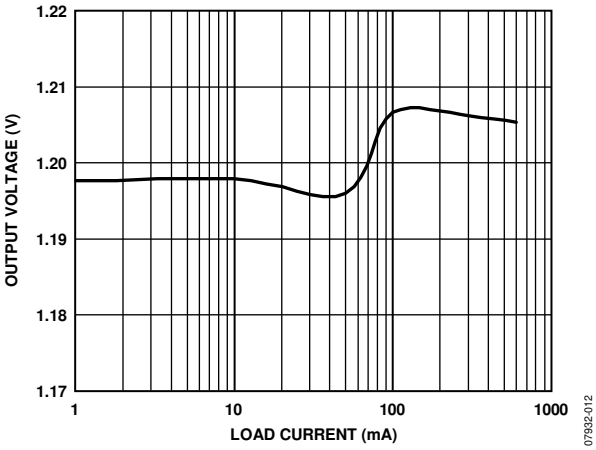


Figure 12. Load Regulation, V_{OUT} = 1.2 V, V_{IN1} = 2.3 V

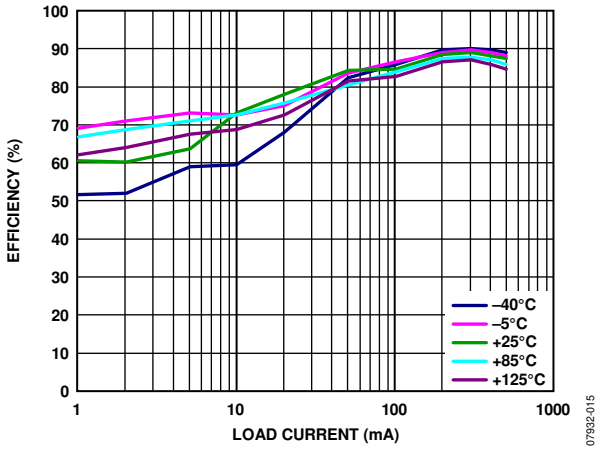


Figure 15. Efficiency vs. Load Current, V_{OUT} = 1.8 V, Different Temperatures

V_{IN1} = 4 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10 µF, T_A = 25°C, unless otherwise noted.

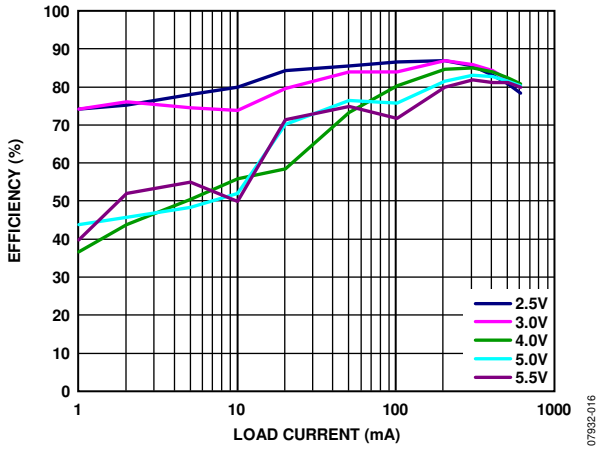


Figure 16. Efficiency vs. Load Current, V_{OUT} = 1.2 V, Different Input Voltages

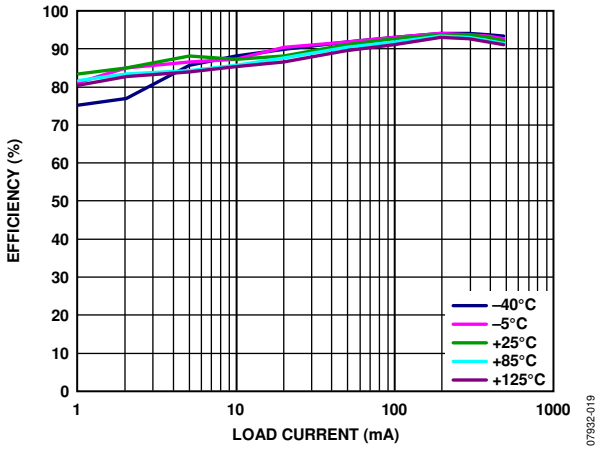


Figure 19. Efficiency vs. Load Current, V_{OUT} = 3.3 V, Different Temperatures

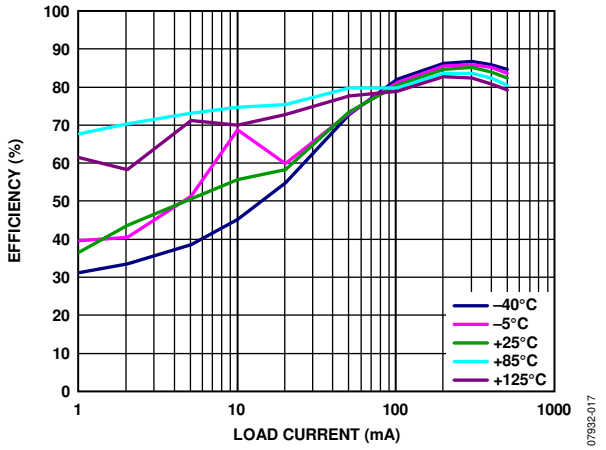


Figure 17. Efficiency vs. Load Current, V_{OUT} = 1.2 V, Different Temperatures

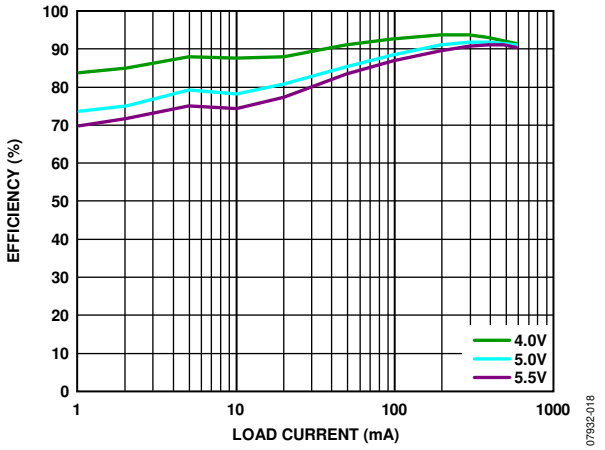


Figure 20. Efficiency vs. Load Current, V_{OUT} = 3.3 V, Different Input Voltages

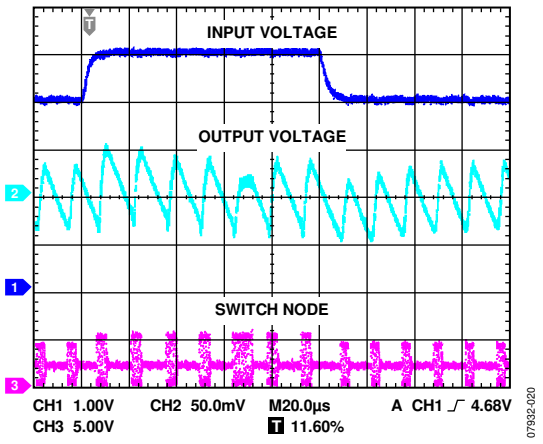


Figure 18. Line Transient, V_{OUT} = 1.8 V, Power Save Mode, 50 mA, V_{IN1} = 4 V to 5 V, 4 µs Rise Time

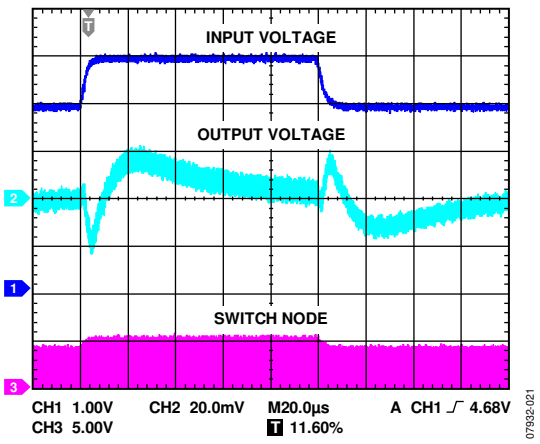


Figure 21. Line Transient, V_{OUT} = 1.8 V, PWM Mode, 600 mA, V_{IN1} = 4 V to 5 V, 4 µs Rise Time

V_{IN1} = 4 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10 µF, T_A = 25°C, unless otherwise noted.

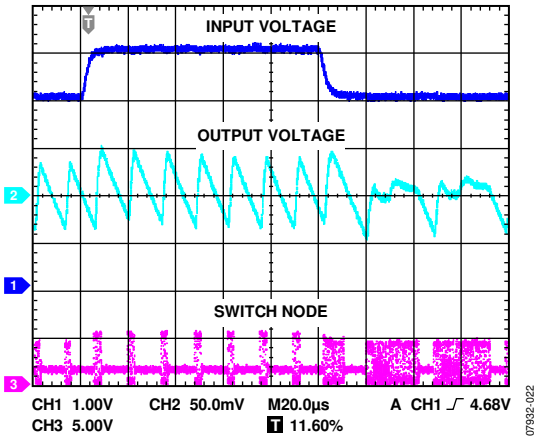


Figure 22. Line Transient, V_{OUT} = 1.2 V, PSM Mode, 50 mA, V_{IN1} = 4 V to 5 V, 4 µs Rise Time

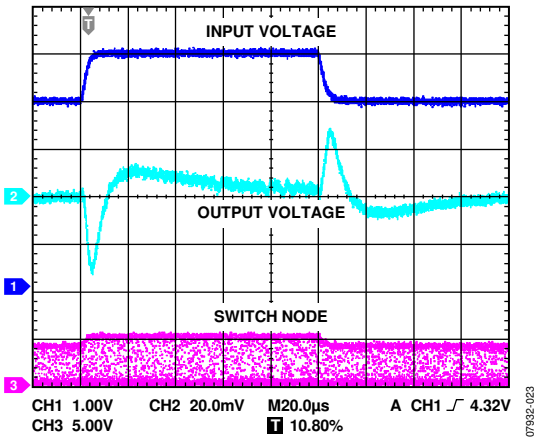


Figure 23. Line Transient, V_{OUT} = 1.2 V, PWM Mode, 600 mA, V_{IN1} = 4 V to 5 V, 4 µs Rise Time

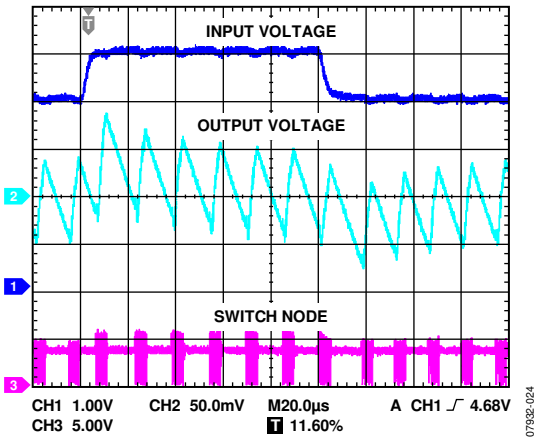


Figure 24. Line Transient, V_{OUT} = 3.3 V, PSM Mode, 50 mA, V_{IN1} = 4 V to 5 V, 4 µs Rise Time

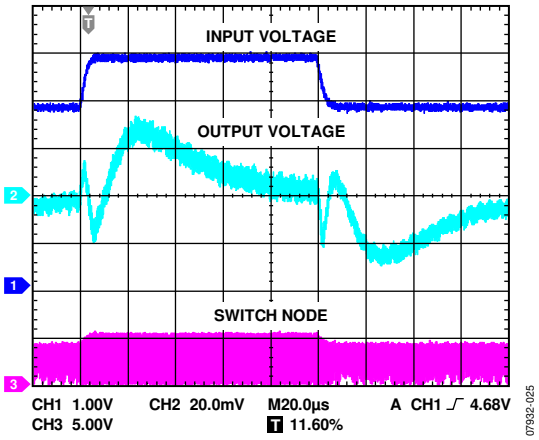


Figure 25. Line Transient, V_{OUT} = 3.3 V, PWM Mode, 600 mA, V_{IN1} = 4 V to 5 V, 4 µs Rise Time

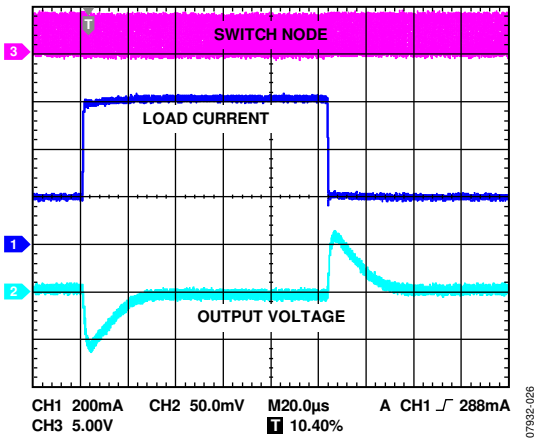


Figure 26. Load Transient, V_{OUT} = 1.8 V, 200 mA to 600 mA, Load Current Rise Time = 200 ns

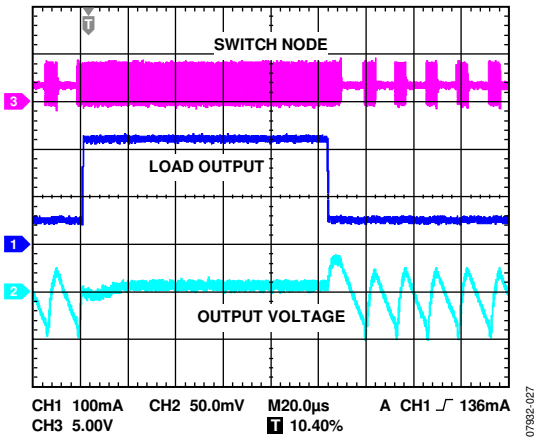


Figure 27. Load Transient, V_{OUT} = 1.8 V, 50 mA to 250 mA, Load Current Rise Time = 200 ns

V_{IN1} = 4 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10 µF, T_A = 25°C, unless otherwise noted.

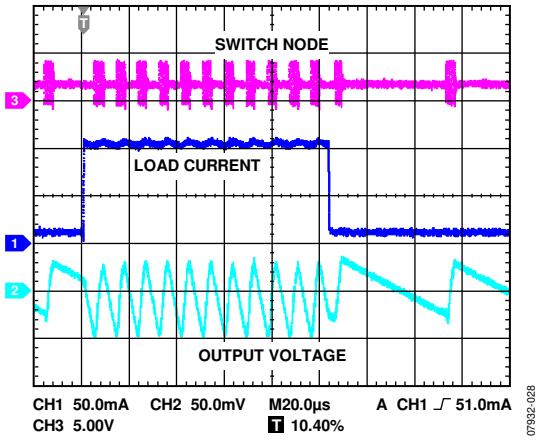


Figure 28. Load Transient, V_{OUT} = 1.8 V,10 mA to 110 mA, Load Current Rise Time = 200 ns

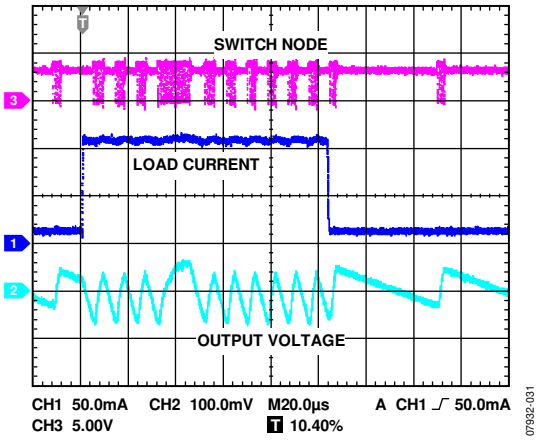


Figure 31. Load Transient, V_{OUT} = 3.3 V,10 mA to 110 mA, Load Current Rise Time = 200 ns

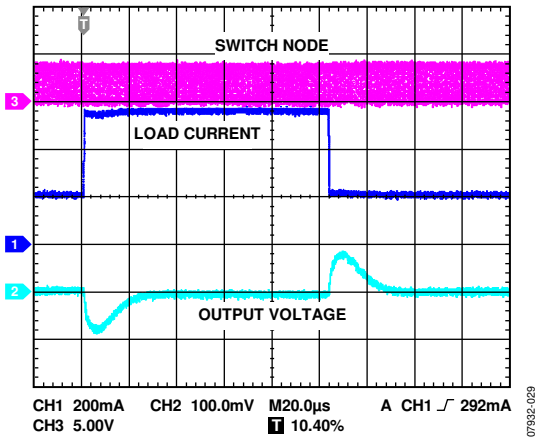


Figure 29. Load Transient, V_{OUT} = 3.3 V, 200 mA to 600 mA, Load Current Rise Time = 200 ns

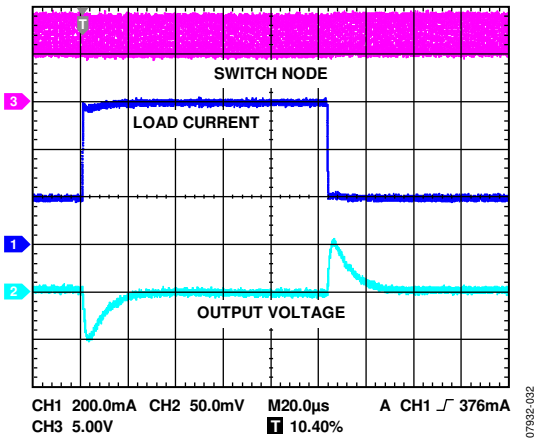


Figure 32. Load Transient, V_{OUT} = 1.2 V, 200 mA to 600 mA, Load Current Rise Time = 200 ns

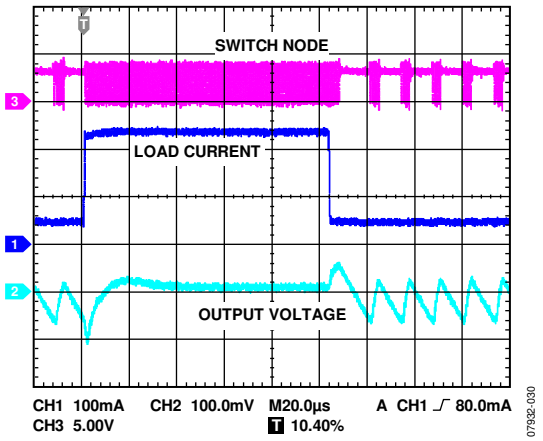


Figure 30. Load Transient, V_{OUT} = 3.3 V, 50 mA to 250 mA, Load Current Rise Time = 200 ns

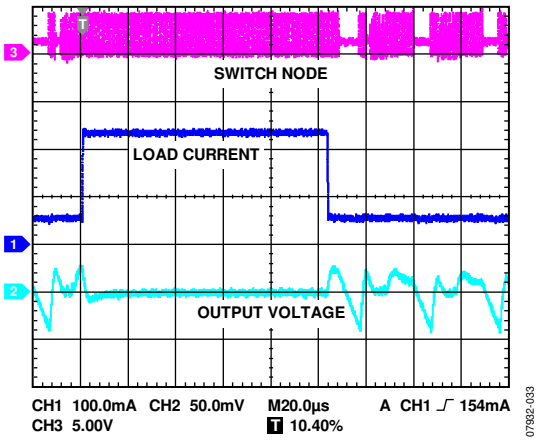


Figure 33. Load Transient, V_{OUT} = 1.2 V, 50 mA to 250 mA, Load Current Rise Time = 200 ns

V_{IN1} = 4 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10 µF, T_A = 25°C, unless otherwise noted.

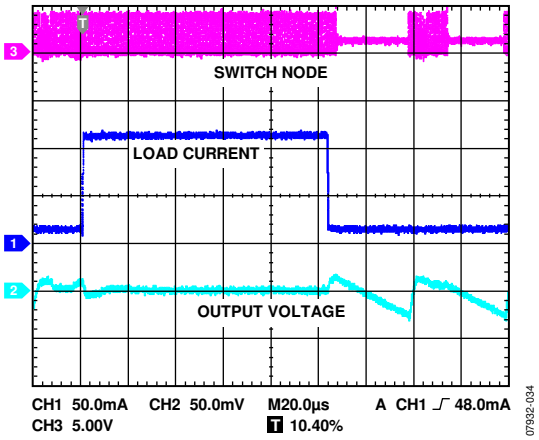


Figure 34. Load Transient, V_{OUT} = 1.2 V,10 mA to 110 mA, Load Current Rise Time = 200 ns

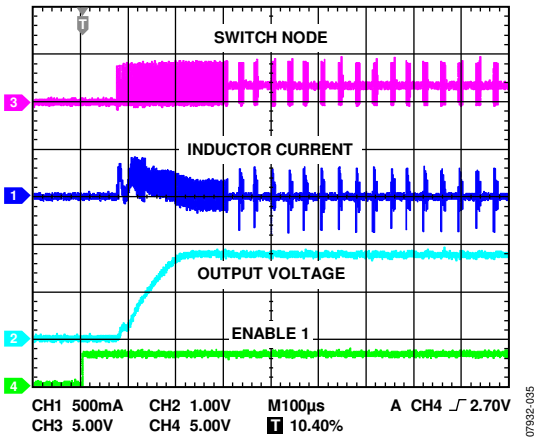


Figure 35. Startup, V_{OUT} = 1.8 V, 10 mA

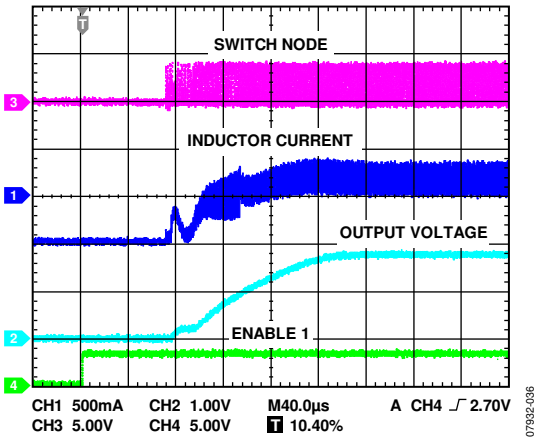


Figure 36. Startup, V_{OUT} = 1.8 V, 600 mA

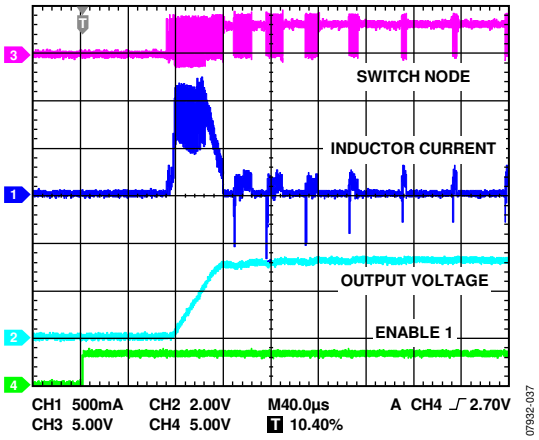


Figure 37. Startup, V_{OUT} = 3.3 V, 10 mA

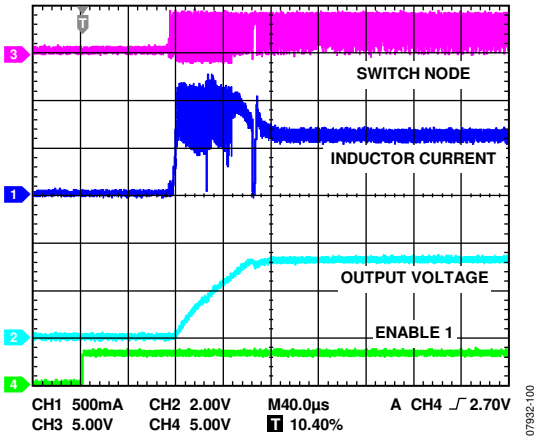


Figure 38. Startup, V_{OUT} = 3.3 V, 600 mA

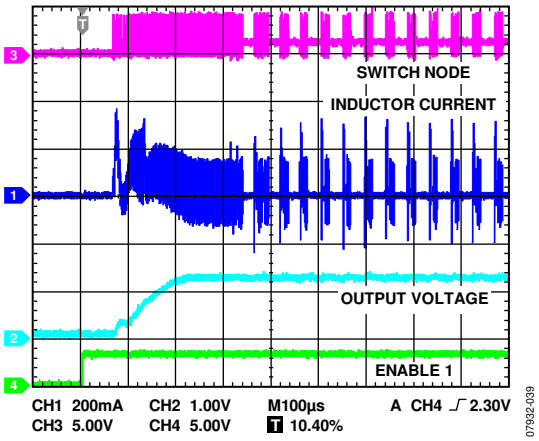


Figure 39. Startup, V_{OUT} = 1.2 V, 10 mA

V_{IN1} = 4 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10 µF, T_A = 25°C, unless otherwise noted.

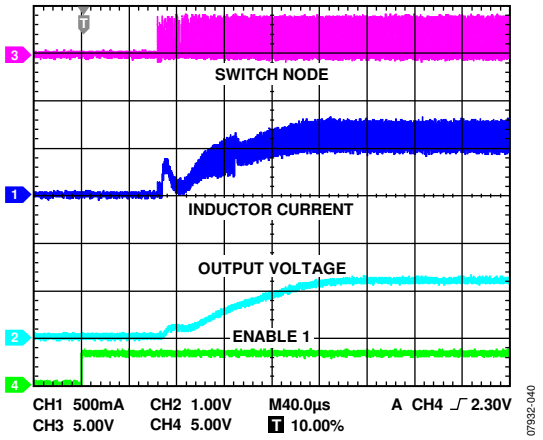


Figure 40. Startup, V_{OUT} = 1.2 V, 600 mA

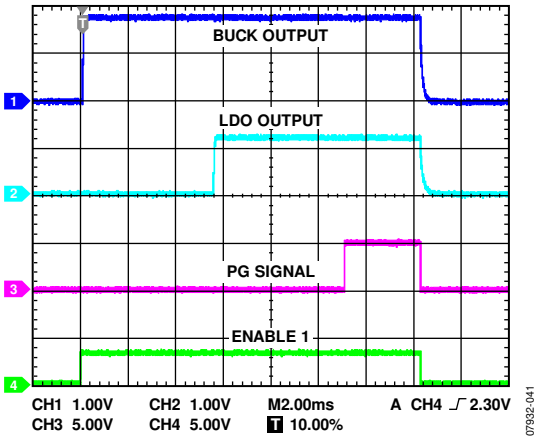


Figure 41. Startup, Autosequence Mode, V_{OUT} = 1.8 V, V_{OUT2} = 1.2 V

LDO OUTPUT

V_{IN1} = 5 V, V_{IN2} = 2.3 V, V_{OUT2} = 1.8 V, I_{OUT2} = 10 mA, C_{IN2} = C_{OUT2} = 1 µF, T_A = 25°C, unless otherwise noted.

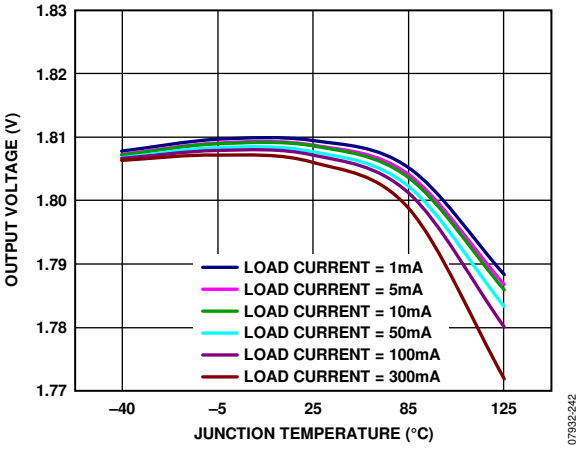


Figure 42. Output Voltage vs. Junction Temperature, Different Loads

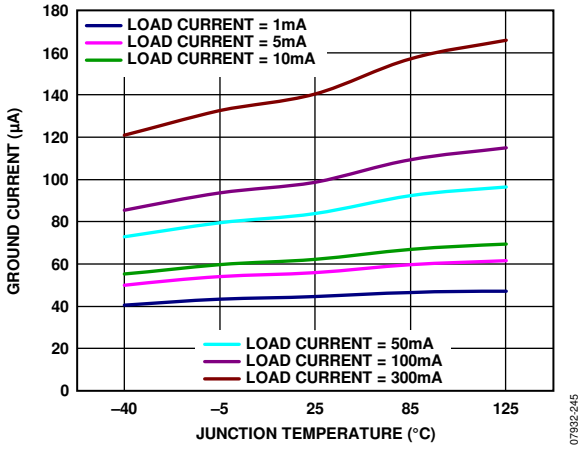


Figure 45. Ground Current vs. Junction Temperature, Different Loads

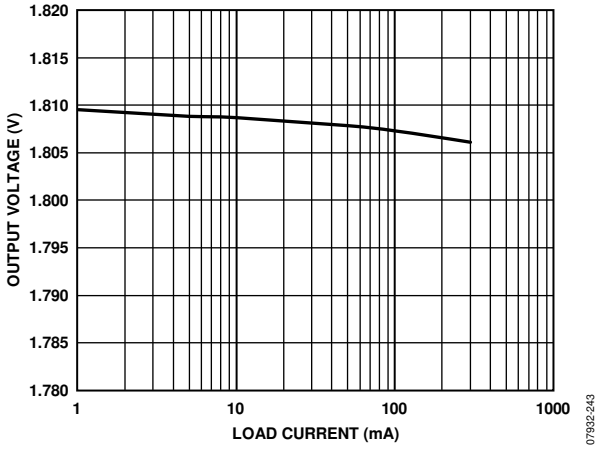


Figure 43. Output Voltage vs. Load Current

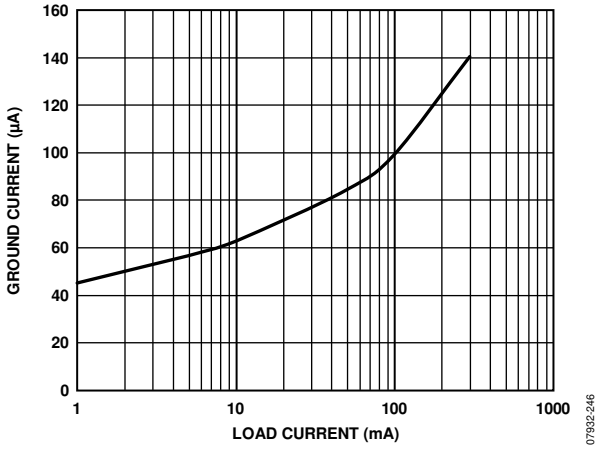


Figure 46. Ground Current vs. Load Current

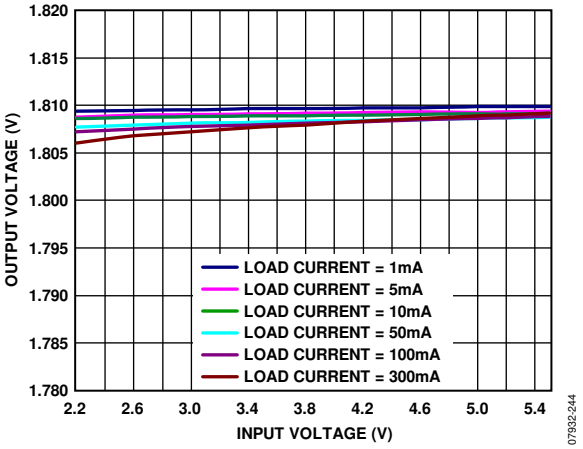


Figure 44. Output Voltage vs. Input Voltage, Different Loads

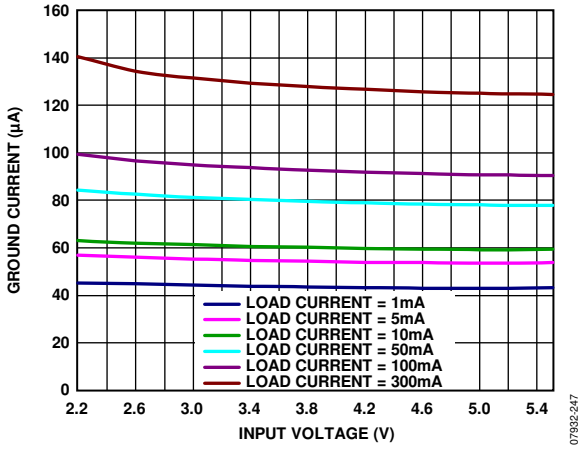


Figure 47. Ground Current vs. Input Voltage, Different Loads

V_{IN1} = 5 V, V_{IN2} = 2.3 V, V_{OUT2} = 1.8 V, I_{OUT2} = 10 mA, C_{IN2} = C_{OUT2} = 1 µF, T_A = 25°C, unless otherwise noted.

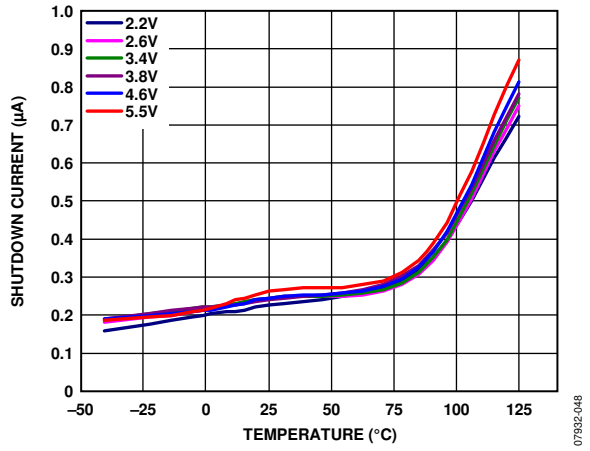


Figure 48. Shutdown Current vs. Temperature at Various Input Voltages

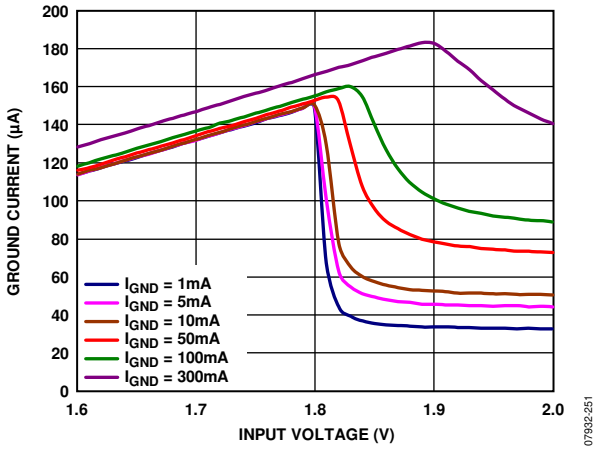


Figure 51. Ground Current vs. Input Voltage (in Dropout)

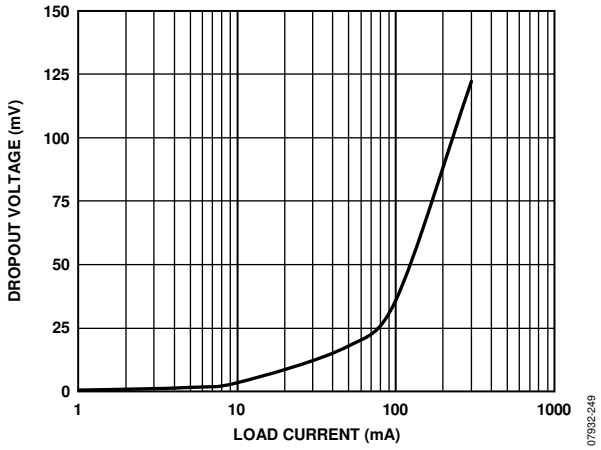


Figure 49. Dropout Voltage vs. Load Current

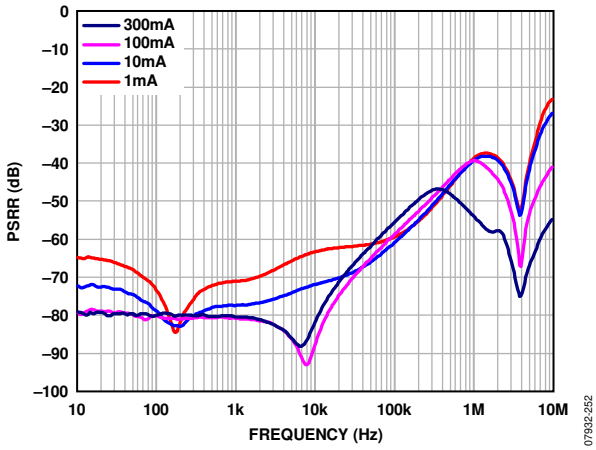


Figure 52. Power Supply Rejection Ratio vs. Frequency V_{OUT2} = 1.2 V, V_{IN1} = 5 V, V_{IN2} = 2.2 V

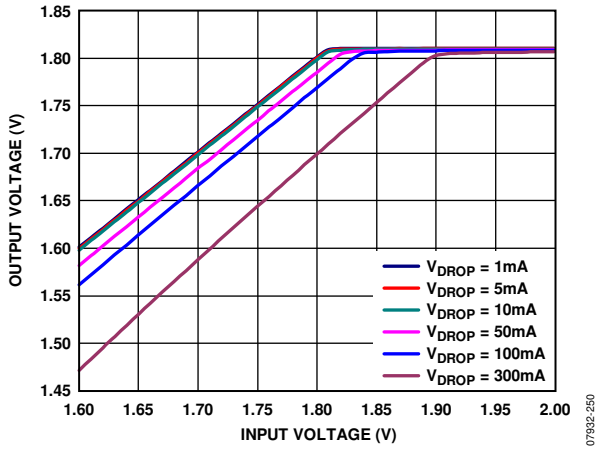


Figure 50. Output Voltage vs. Input Voltage (in Dropout)

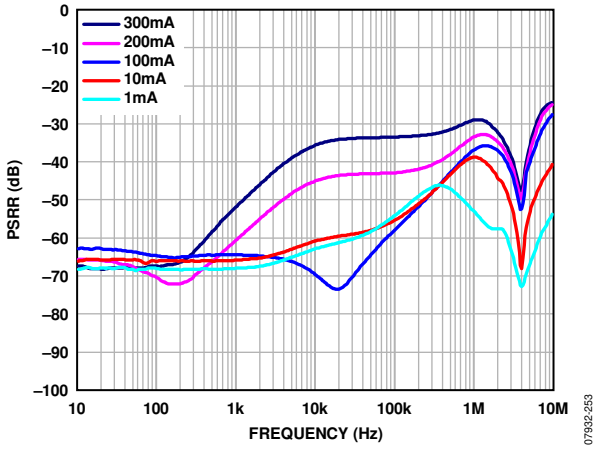


Figure 53. Power Supply Rejection Ratio vs. Frequency V_{OUT2} = 1.2 V, V_{IN1} = 5 V, V_{IN2} = 1.7 V

V_{IN1} = 5 V, V_{IN2} = 2.3 V, V_{OUT2} = 1.8 V, I_{OUT2} = 10 mA, C_{IN2} = C_{OUT2} = 1 µF, T_A = 25°C, unless otherwise noted.

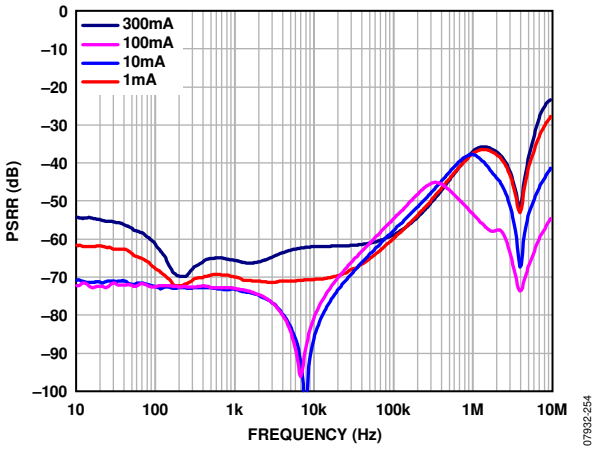


Figure 54. Power Supply Rejection Ratio vs. Frequency, V_{OUT2} = 3.3 V, V_{IN1} = 5 V, V_{IN2} = 4.3 V

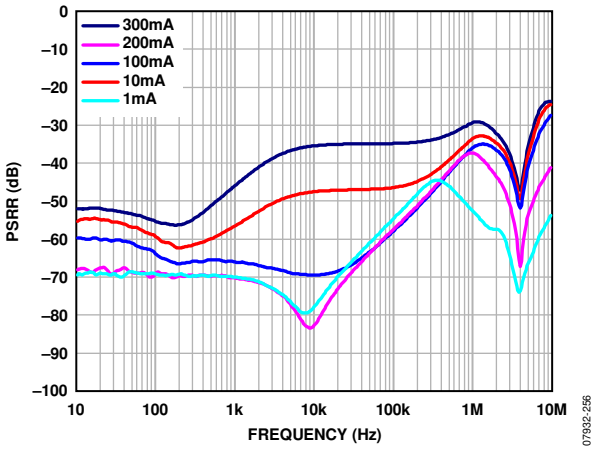


Figure 57. Power Supply Rejection Ratio vs. Frequency, V_{OUT2} = 3.3 V, V_{IN1} = 5 V, V_{IN2} = 3.8 V

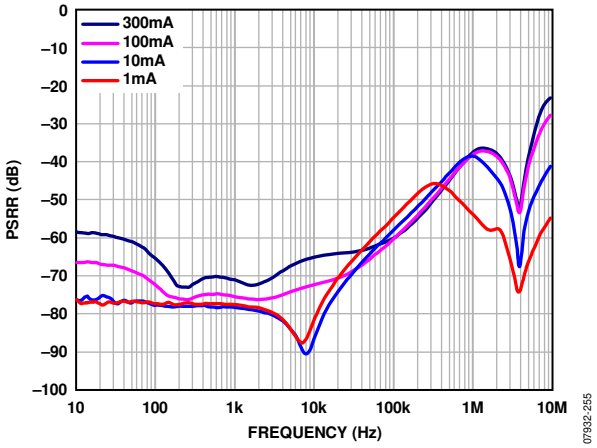


Figure 55. Power Supply Rejection Ratio vs. Frequency, V_{OUT2} = 1.8 V, V_{IN1} = 5 V, V_{IN2} = 2.8 V

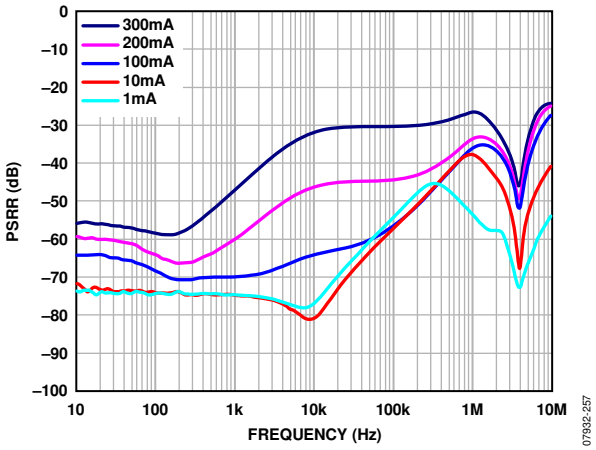


Figure 58. Power Supply Rejection Ratio vs. Frequency V_{OUT2} = 1.8 V, V_{IN1} = 5 V, V_{IN2} = 2.3 V

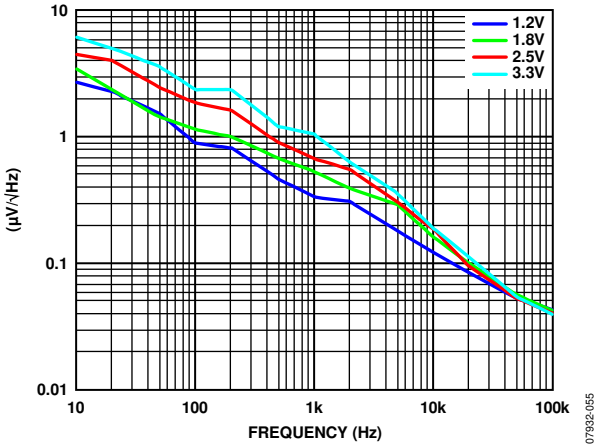


Figure 56. Output Noise Spectrum, V_{IN2} = 5 V, Load Current = 10 mA

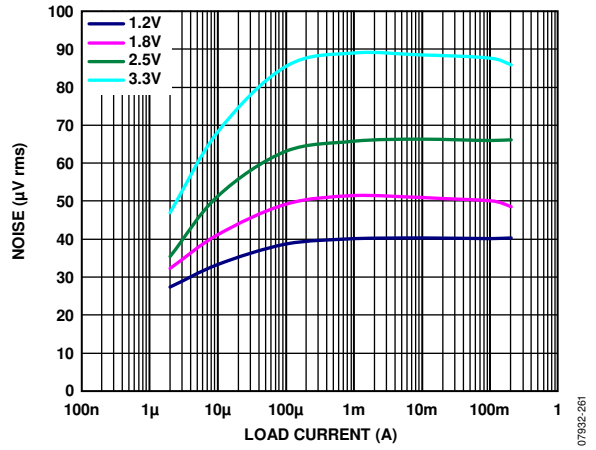


Figure 59. Output Noise vs. Load Current and Output Voltage V_{IN2} = 5 V

V_{IN1} = 5 V, V_{IN2} = 2.3 V, V_{OUT2} = 1.8 V, I_{OUT2} = 10 mA, C_{IN2} = C_{OUT2} = 1 µF, T_A = 25°C, unless otherwise noted.

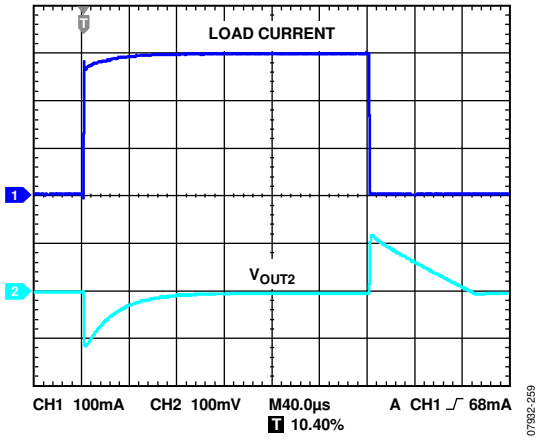


Figure 60. Load Transient Response, V_{IN2} = 4 V, V_{OUT2} = 1.2 V, 1 mA to 300 mA, Load Current Rise Time = 200 ns

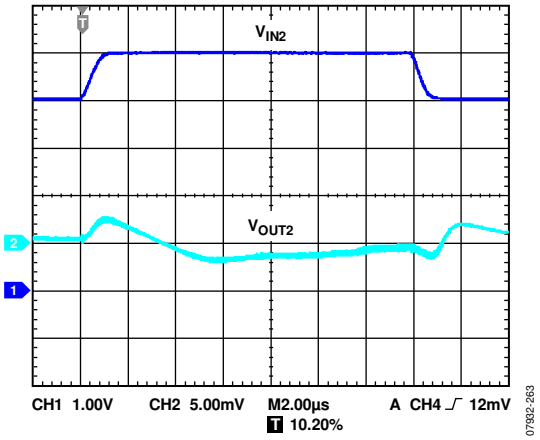


Figure 63. Line Transient Response, V_{OUT2} = 1.8 V, Load Current = 1 mA, V_{IN2} = 4 V to 5 V, 1 µs Rise Time

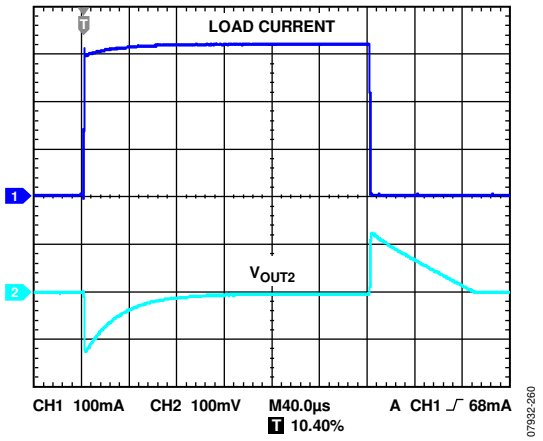


Figure 61. Load Transient Response, V_{IN2} = 4 V, V_{OUT2} = 1.8 V, 1 mA to 300 mA, Load Current Rise Time = 200 ns

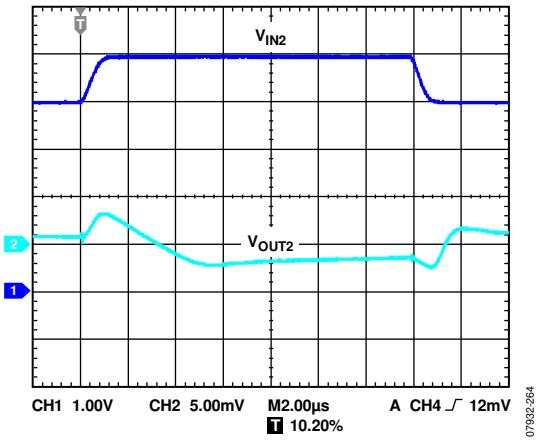


Figure 64. Line Transient Response, V_{OUT2} = 1.2 V, Load Current = 1 mA, V_{IN2} = 4 V to 5 V, 1 µs Rise Time

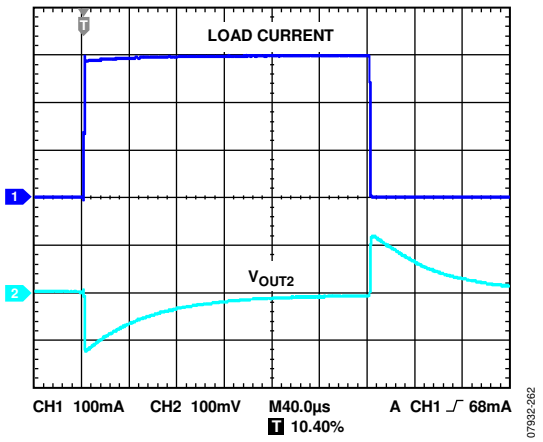


Figure 62. Load Transient Response, V_{IN2} = 4 V, V_{OUT2} = 3.3 V, 1 mA to 300 mA, Load Current Rise Time = 200 ns

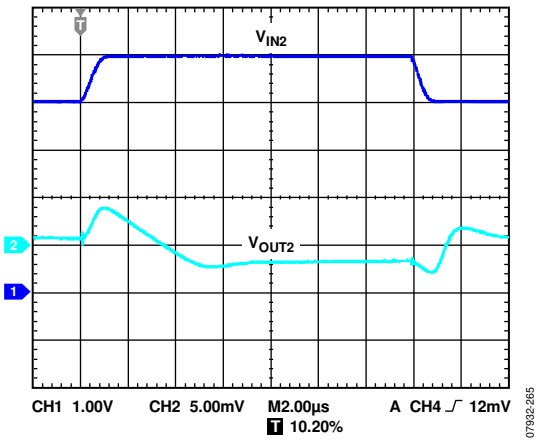


Figure 65. Line Transient Response, V_{OUT2} = 3.3 V, Load Current = 1 mA, V_{IN2} = 4 V to 5 V, 1 µs Rise Time

V_{IN1} = 5 V, V_{IN2} = 2.3 V, V_{OUT2} = 1.8 V, I_{OUT2} = 10 mA, C_{IN2} = C_{OUT2} = 1 µF, T_A = 25°C, unless otherwise noted.

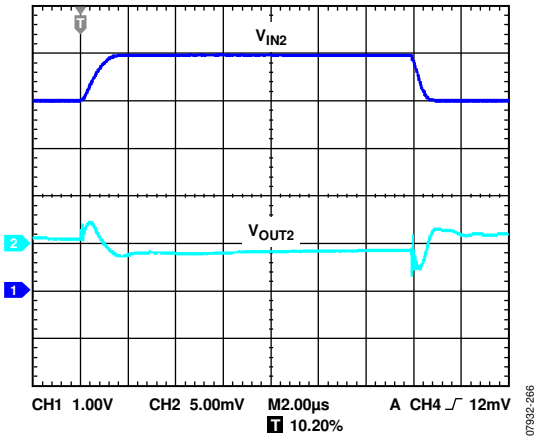


Figure 66. Line Transient Response, V_{OUT2} = 1.8 V, Load Current = 300 mA, V_{IN2} = 4 V to 5 V, 1 µs Rise Time

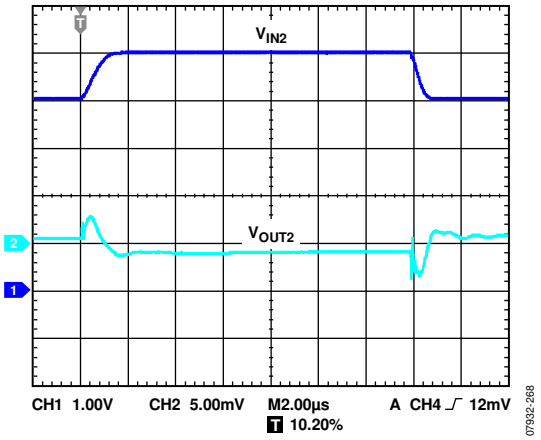


Figure 68. Line Transient Response, V_{OUT2} = 3.3 V, Load Current = 300 mA, V_{IN2} = 4 V to 5 V, 1 µs Rise Time

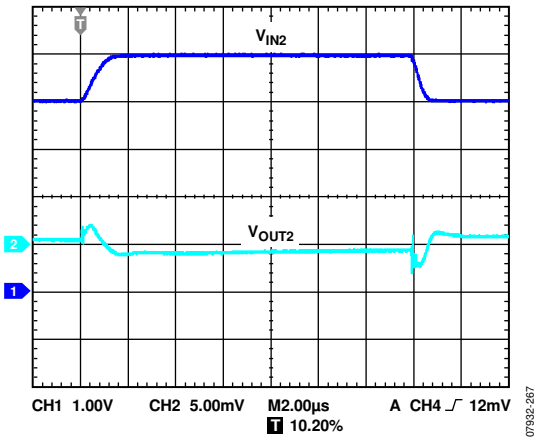


Figure 67. Line Transient Response, V_{OUT2} = 1.2 V, Load Current = 300 mA, V_{IN2} = 4 V to 5 V, 1 µs Rise Time

THEORY OF OPERATION

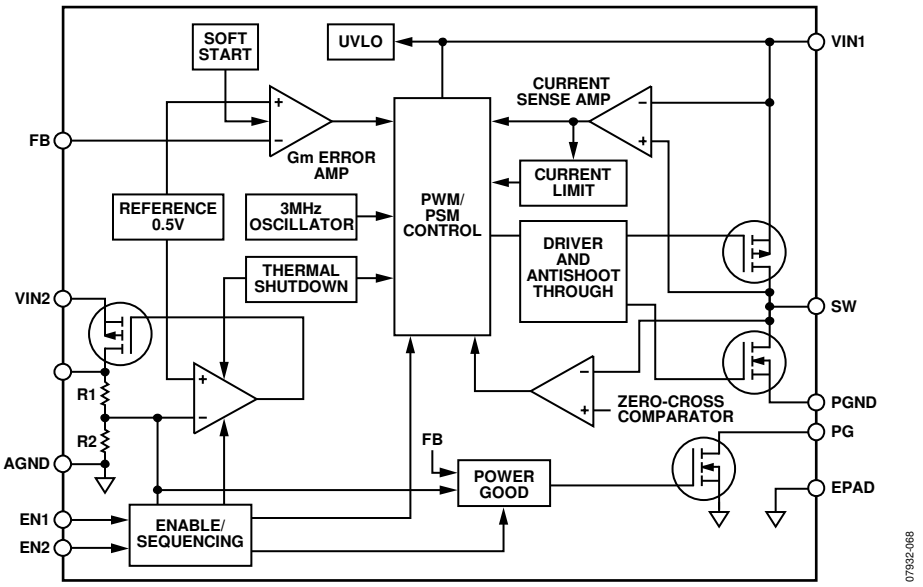


Figure 69. Internal Block Diagram

BUCK SECTION

The ADP2140 contains a step-down dc-to-dc converter that uses a fixed frequency, high speed current-mode architecture. The high 3 MHz switching frequency and tiny 10-lead, 3 mm × 3 mm LFCSP package allow for a small step-down dc-to-dc converter solution.

The ADP2140 operates with an input voltage from 2.3 V to 5.5 V. Output voltage options are 1.0 V, 1.1 V, 1.2 V, 1.5 V, 1.8 V, 1.875 V, 2.5 V, and 3.3 V.

CONTROL SCHEME

The ADP2140 operates with a fixed frequency, current-mode PWM control architecture at medium to high loads for high efficiency, but shifts to a variable frequency control scheme at light loads for lower quiescent current. When operating in fixed frequency PWM mode, the duty cycle of the integrated switches adjust to regulate the output voltage, but when operating in power saving mode (PSM) at light loads, the switching frequency adjusts to regulate the output voltage.

The ADP2140 operates in the PWM mode only when the load current is greater than the pulse skipping threshold current. At load currents below this value, the converter smoothly transitions to the PSM mode of operation.

PWM OPERATION

In PWM mode, the ADP2140 operates at a fixed frequency of 3 MHz set by an internal oscillator. At the start of each oscillator cycle, the P-channel MOSFET switch is turned on, putting a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current level that turns off the P-channel MOSFET switch and turns on the N-channel MOSFET synchronous rectifier. This puts a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the remainder of the cycle, unless the inductor current reaches zero, which causes the zero-crossing comparator to turn off the N-channel MOSFET.

PSM OPERATION

The ADP2140 has a smooth transition to the variable frequency PSM mode of operation when the load current decreases below the pulse skipping threshold current, switching only as necessary to maintain the output voltage within regulation. When the output voltage dips below regulation, the ADP2140 enters PWM mode for a few oscillator cycles to increase the output voltage back to regulation. During the wait time between bursts, both power switches are off, and the output capacitor supplies the entire load current. Because the output voltage occasionally dips and recovers, the output voltage ripple in this mode is larger than the ripple in the PWM mode of operation.

PULSE SKIPPING THRESHOLD

The output current at which the ADP2140 transitions from variable frequency PSM control to fixed frequency PWM control is called the pulse skipping threshold. The pulse skipping threshold has been optimized for excellent efficiency over all load currents.

SELECTED FEATURES

SHORT-CIRCUIT PROTECTION

The ADP2140 includes frequency foldback to prevent output current runaway on a hard short. When the voltage at the feedback pin falls below 50% of the nominal output voltage, indicating the possibility of a hard short at the output, the switching frequency is reduced to 1/2 of the internal oscillator frequency. The reduction in the switching frequency gives more time for the inductor to discharge, preventing a runaway of output current.

UNDERVOLTAGE LOCKOUT

To protect against battery discharge, undervoltage lockout circuitry is integrated on the ADP2140. If the input voltage drops below the 2.15 V UVLO threshold, the ADP2140 shuts down and both the power switch and synchronous rectifier turn off. When the voltage rises again above the UVLO threshold, the soft start period initiates and the part is enabled.

THERMAL PROTECTION

In the event that the ADP2140 junction temperatures rises above 150°C, the thermal shutdown circuit turns off the converter. Extreme junction temperatures can be the result of high current operation, poor circuit board design, and/or high ambient temperature. A 20°C hysteresis is included; thus, when thermal shutdown occurs, the ADP2140 does not return to operation until the on-chip temperature drops below 130°C. When emerging from a thermal shutdown, soft start initiates.

SOFT START

The ADP2140 has an internal soft start function that ramps the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the converter.

CURRENT LIMIT

The ADP2140 has protection circuitry to limit the direction and amount of current to 1000 mA flowing through the power switch and synchronous rectifier. The positive current limit on the power switch limits the amount of current that can flow from the input to the output, and the negative current limit on the synchronous rectifier prevents the inductor current from reversing direction and flowing out of the load.

The ADP2140 also provides a negative current limit to prevent an excessive reverse inductor current when the switching section sinks current from the load in forced continuous conduction mode. Under negative current limit conditions, both the high-side and low-side switches are disabled.

POWER-GOOD PIN

The ADP2140 has a dedicated pin (PG) to signal the state of the monitored output voltages. The voltage monitor circuit has an active high, open-drain output requiring an external pull-up resistor typically supplied from the I/O supply rail, as shown in . The voltage monitor circuit has a small amount of hysteresis and is deglitched to ensure that noise or external perturbations do not trigger the PG line.

LDO SECTION

The ADP2140 low dropout linear regulator uses an advanced proprietary architecture to achieve low quiescent current, and high efficiency regulation. It also provides high power supply rejection ratio (PSRR), low output noise, and excellent line and load transient response with just a small 1 µF ceramic output capacitor. The wide input voltage range of 1.65 V to 5.5 V allows it to operate from either the input or output of the buck. Supply current in shutdown mode is typically 0.3 µA.

Internally, the LDO consists of a reference, an error amplifier, a feedback voltage divider, and a pass device. The output current is delivered via the pass device, which is controlled by the error amplifier, forming a negative feedback system ideally driving the feedback voltage to be equal to the reference voltage. If the feedback voltage is lower than the reference voltage, the negative feedback drives more current, increasing the output voltage. If the feedback voltage is higher than the reference voltage, the negative feedback drives less current, decreasing the output voltage. The positive supply for all circuitry, except the pass device, is the VIN1 pin.

The LDO has an internal soft start that limits the output voltage ramp period to approximately 130 µs.

The LDO is available in 0.8 V, 1.0 V, 1.1 V, 1.2 V, 1.3 V, 1.5 V, 2.5 V, 2.8 V, 3.0 V, and 3.3 V output voltage options.

APPLICATIONS INFORMATION

POWER SEQUENCING

The ADP2140 has a flexible power sequencing system supporting two distinct activation modes:

- Individual activation control is where EN1 controls only the buck regulator and EN2 controls only the LDO. A high level on Pin EN1 turns on the buck and a high level on Pin EN2 turns on the LDO. A logic low level turns off the respective regulator.
- Autosequencing is where the two regulators turn on in a specified order and delay after a low-to-high transition on the EN1 pin.

Select the activation mode (individual or autosequence) by decoding the state of Pin EN2. The individual activation mode is selected when the EN2 pin is driven externally or hardwired to a voltage level (VIN1 or PGND). The autosequencing mode is selected when the EN2 pin remains unconnected (floating).

To minimize quiescent current consumption, the mode selection executes one time only during the rising edge of VIN1. The detection circuit then activates for the time needed to assess the EN2 state, after which time the circuit is disabled until VIN1 falls below 0.5 V.

When EN2 is unconnected, the internal control circuit provides a termination resistance to ground. The 100 kΩ termination resistance is low enough to guarantee insensitivity to noise and transients. The termination resistor is disabled in the event that the EN2 pin is driven externally to a logic level high (individual activation mode assumed) to reduce the quiescent current consumption.

When the autosequencing mode is selected, the EN1 pin is used to start the on/off sequence of the regulators. A logic high sequences the regulators on whereas a logic low sequences the regulators off. The regulator activation order is associated with the voltage selected for the buck regulator and the LDO.

When the turn on or turn off autosequence starts, the start-up delay between the first and the second regulator is fixed to 5 ms in PWM mode (t_{REG12}, as shown in Figure 71 and Figure 72).

When the application requires activating and deactivating the regulators at the same time, use the individual activation mode, which connects the EN1 and EN2 pins together, as shown in Figure 75.

Table 6. Power Sequencing Modes

EN2[1]	EN1	Description
0	0	Individual mode: both regulators are off.
0	1	Individual mode: buck regulator is on.
1	0	Individual mode: LDO regulator is on.
1	1	Individual mode: both regulators are on.
NC	Rising edge	Autosequence: Buck regulator turns on, then the LDO regulator turns on. The LDO voltage is less than the buck voltage.
NC	Rising edge	Autosequence: LDO regulator turns on, then the buck regulator turns on. The LDO voltage is greater than the buck voltage.
NC	Rising edge	Autosequence: If the buck voltage is 1.875 V, then the LDO regulator always turns on first.
NC	Falling edge	Autosequence: The LDO and buck regulators turn off at the same time.

[1] NC means not connected.

Figure 70 to Figure 75 use the following symbols, as described in Table 7.

Table 7. Timing Symbols

Symbol	Description	Typical Value
t_{START}	Time needed for the internal circuitry to activate the first regulator	60 µs
t_{SS}	Regulator soft start time	330 µs
t_{RESET}	Time delay from power-good condition to the release of PG	5 ms
t_{REG12}	Delay time between buck and LDO activation	5 ms

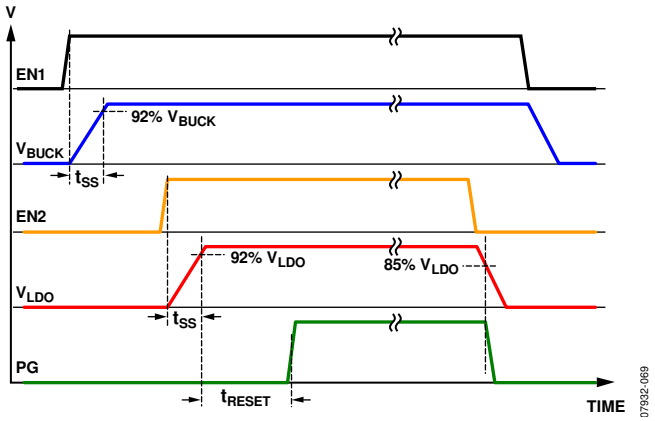


Figure 70. Individual Activation Mode

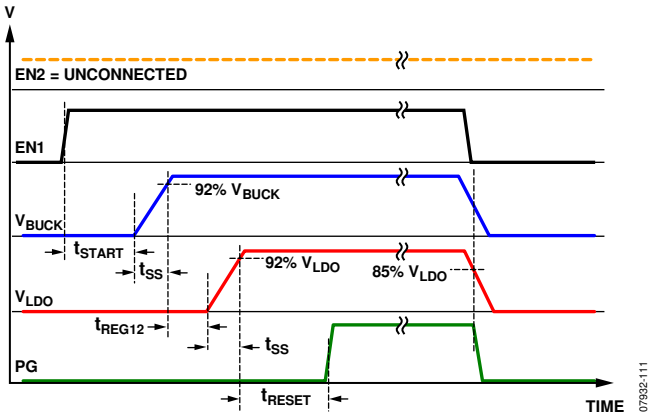


Figure 71. Autosequencing Mode, Buck First Then LDO

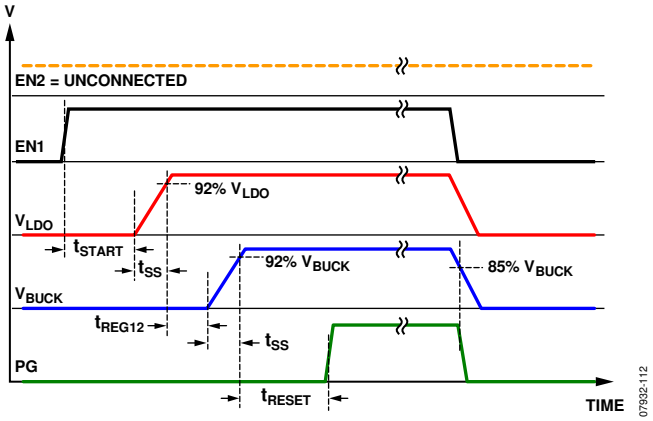


Figure 72. Autosequencing Mode, LDO First Then Buck

The PG responds to the last activated regulator. As described in the Power Sequencing section, the regulator order in the auto-sequencing mode is defined by the voltage option combination. Therefore, if the sequence is buck first, the LDO and the PG signal are active low for t_{RESET} after V_{LDO} reaches 92% of the rated output voltage, at which time PG goes high and remains high for as long as V_{LDO} is above 86% of the rated output voltage. When the sequencing is LDO first then buck, V_{BUCK} controls PG. This control scheme also applies when the individual activation mode is selected.

As soon as either regulator output voltage drops below 86% of the respective nominal level, the PG pin is forced low.

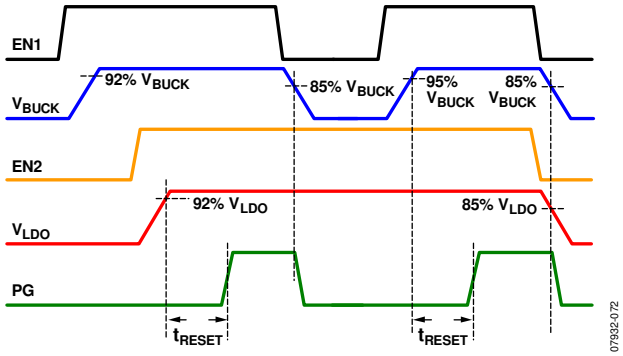


Figure 73. Individual Activation Mode, Both Regulators Sensed

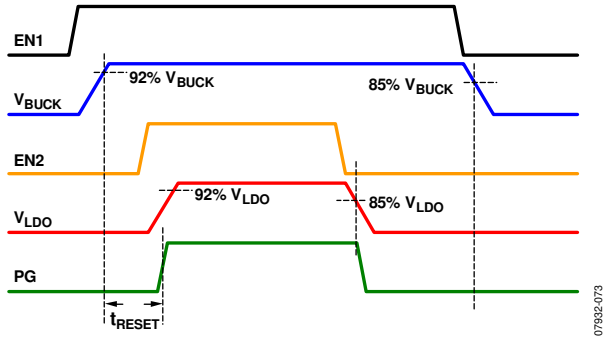


Figure 74. Individual Activation Mode, One Regulator Only (Buck) Sensed

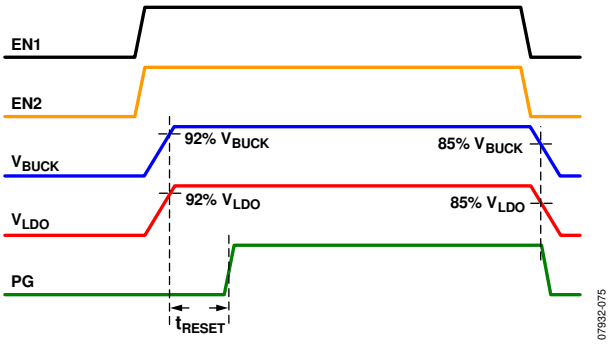


Figure 75. Individual Activation Mode, No Activation/Deactivation Delay Between Regulators, EN1 and EN2 Pins Tied Together

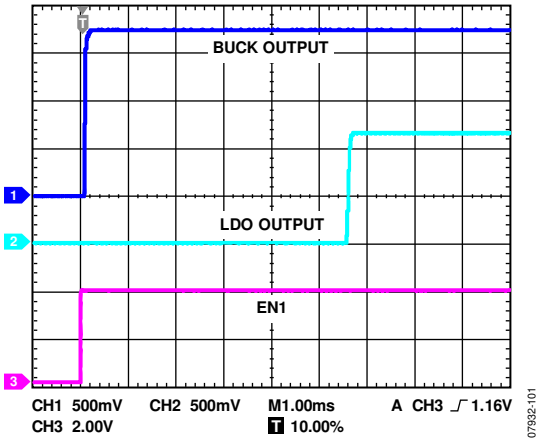


Figure 76. Autosequence Mode Turn On Behavior, Buck Voltage = 1.8 V, LDO Voltage = 1.2 V, Buck Load = 500 mA, LDO Load = 100 mA

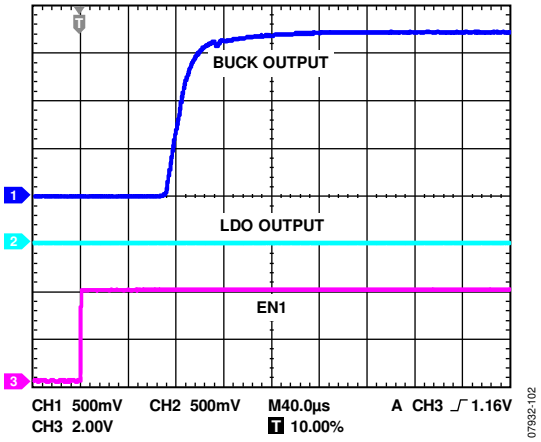


Figure 77. Autosequence Mode Turn On Behavior, Buck Voltage = 1.8 V, LDO Voltage = 1.2 V, Buck Load = 500 mA, LDO Load = 100 mA

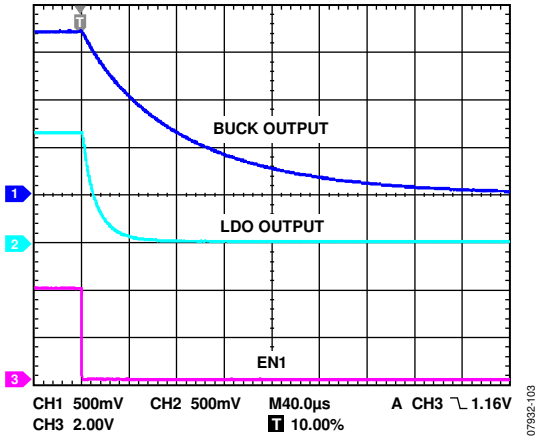


Figure 78. Autosequence Mode Turn On Behavior, Buck Voltage = 1.8 V, LDO Voltage = 1.2 V, Buck Load = 500 mA, LDO Load = 100 mA

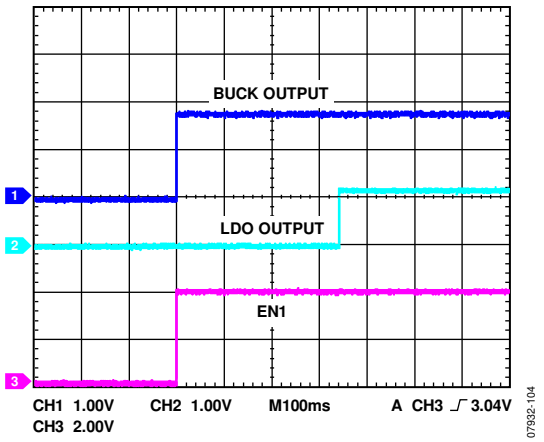


Figure 79. Autosequence Mode Turn On Behavior, Buck Voltage =1.8 V, LDO Voltage = 1.2 V, Buck Load = 1 mA, LDO Load = 100 mA

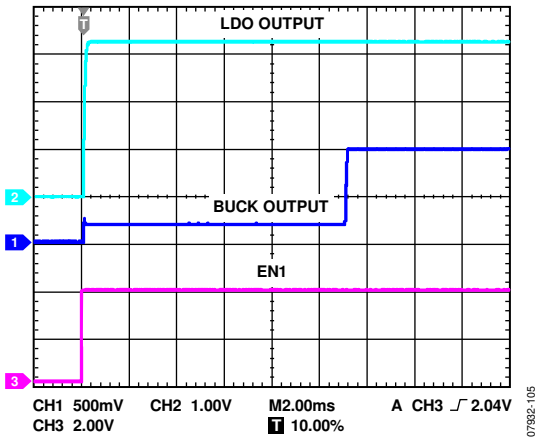


Figure 80. Autosequence Mode Turn On Behavior, Buck Voltage = 1.0 V, LDO Voltage = 3.3 V, Buck Load = 500 mA, LDO Load = 100 mA

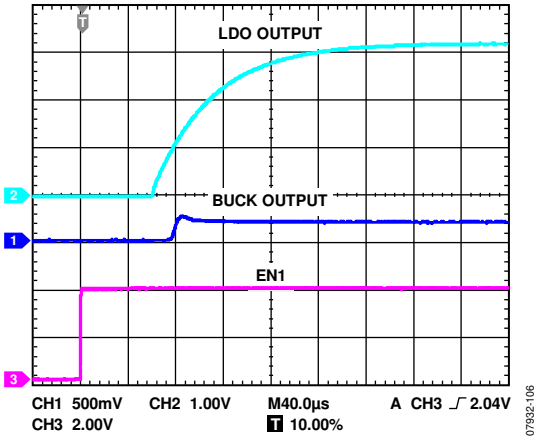


Figure 81. Autosequence Mode Turn On Behavior, Buck Voltage = 1.0 V, LDO Voltage = 3.3 V, Buck Load = 500 mA, LDO Load = 100 mA (Expanded Version of Figure 80)

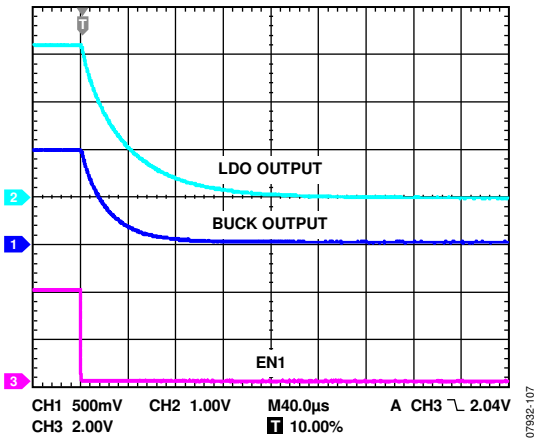


Figure 82. Autosequence Mode Turn Off Behavior, Buck Voltage = 1.0 V, LDO Voltage = 3.3 V, Buck Load = 500 mA, LDO Load = 100 mA

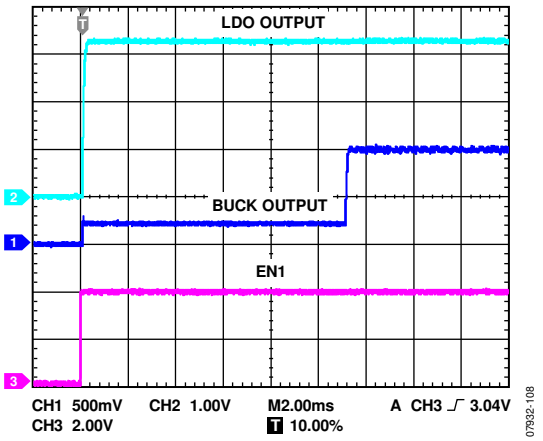


Figure 83. Autosequence Mode Turn On Behavior, Buck Voltage = 1.0 V, LDO Voltage = 3.3 V, Buck Load = 1 mA, LDO Load = 100 mA

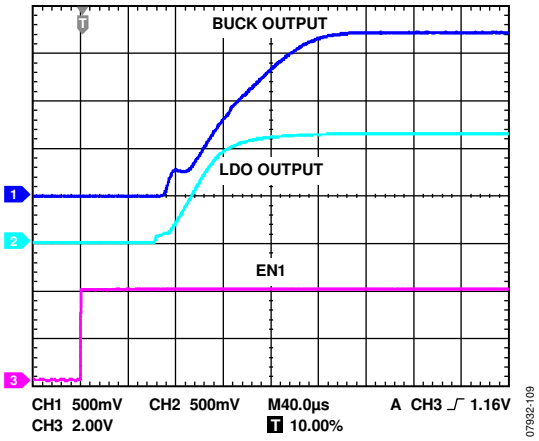


Figure 84. Individual Activation Mode, EN1 and EN2 Pins Tied Together

POWER-GOOD FUNCTION

The ADP2140 power-good (PG) pin indicates the state of the monitored output voltages. The PG function is the logical AND of the state of both outputs. The PG function is an active high, open-drain output, requiring an external pull-up resistor typically supplied from the I/O supply rail, as shown in . When the sensed output voltages are below 92% of their nominal value, the PG pin is held low. When the sensed output voltages rise above 92% of the nominal levels, the PG line is pulled high after t_{RESET}. The PG pin remains high as long as the sensed output voltages are above 86% of the nominal output voltage levels.

The typical PG delay when the buck is in PWM mode is 5 ms. When the part is in PSM mode, the PG delay is load dependent because the internal clock is disabled to reduce quiescent current during the sleep stage. PG delay varies from hundreds of microseconds at 10 mA, up to seconds at current loads of less than 10 µA.

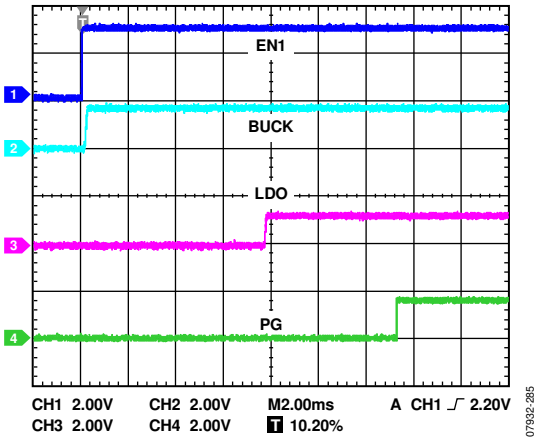


Figure 85. Typical PG Timing

EXTERNAL COMPONENT SELECTION

The external component selection for the ADP2140 application circuit that is shown in Table 8, Table 9, and Figure 86 is dependent on input voltage, output voltage, and load current requirements. Additionally, trade-offs between performance parameters such as efficiency and transient response can be made by varying the choice of external components.

SELECTING THE INDUCTOR

The high frequency switching of the ADP2140 allows the selection of small chip inductors. The inductor value affects the transition between CFM to PSM, efficiency, output ripple, and current limit values. Use the following equation to calculate the inductor ripple current:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{sw} \times L}$$

where:
f_{SW} is the switching frequency (3 MHz typical).
L is the inductor value.

The dc resistance (DCR) value of the selected inductor affects efficiency, but a decrease in this value typically means an increase in root mean square (rms) losses in the core and skin. As a minimum requirement, the dc current rating of the inductor should be equal to the maximum load current plus half of the inductor current ripple, as shown by the following equation:

$$I_{PK} = I_{LOAD(MAX)} + (\frac{\Delta I_L}{2})$$

OUTPUT CAPACITOR

Output capacitance is required to minimize the voltage overshoot and ripple present on the output. Capacitors with low equivalent series resistance (ESR) values produce the lowest output ripple; therefore, use capacitors such as the X5R dielectric. Do not use the Y5V and Z5U capacitors; they are not suitable for this application because of their large variation in capacitance over temperature and dc bias voltage. Because ESR is important, select the capacitor using the following equation:

$$ESR_{COUT} \leq \frac{V_{RIPPLE}}{\Delta I_L}$$

where:
ESR_{COUT} is the ESR of the chosen capacitor.
V_{RIPPLE} is the peak-to-peak output voltage ripple.

Use the following equations to determine the output capacitance:

$$C_{OUT} \geq \frac{V_{IN}}{(2\pi \times f_{SW}) 2 \times L \times V_{RIPPLE}}$$

$$C_{OUT} \geq \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT}}$$

Increasing the output capacitor has no effect on stability and increasing the output capacitance may further reduce output ripple and enhance load transient response. When choosing this value, it is also important to account for the loss of capacitance due to output voltage dc bias.

INPUT CAPACITOR

Input capacitance is required to reduce input voltage ripple; therefore, place the input capacitor as close as possible to the VINx pins. As with the output capacitor, a low ESR X7R- or X5R-type