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FEATURES

- Input voltage range: 3.2 V to 15 V, output current: 800 mA**
- Quiescent current < 14 μ A in power saving mode (PSM)**
- >90% efficiency**
- Force PWM pin (SYNC), 600 kHz/1.2 MHz frequency pin (FSEL)**
- Fixed outputs: 0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, 3.3 V, 5 V, and adjustable option**
- 100% duty cycle capability**
- Initial accuracy: $\pm 1\%$**
- Low shutdown current: <1.2 μ A**
- Quick output discharge (QOD) option**
- Synchronizable to an external clock**
- 8-lead, 0.75 mm \times 3 mm \times 3 mm LFCSP (QFN) package**
- Supported by ADIsimPower design tool**

APPLICATIONS

- Portable and battery-powered equipment**
- Automatic meter readers (WSN)**
- Point of sales and transaction processing instruments**
- Medical instruments**
- Medium format display tablets and pads**

GENERAL DESCRIPTION

The [ADP2370/ADP2371](#) are high efficiency, low quiescent current, 800 mA buck (step-down) dc-to-dc converters in small 8-lead, 3 mm \times 3 mm LFCSP (QFN) packages. The total solution requires only three tiny external components.

The buck regulator uses a proprietary high speed current mode, constant frequency PWM control scheme for excellent stability and transient response. The need for an external rectifier is eliminated by using a high efficiency synchronous rectifier architecture.

To ensure the longest battery life in portable applications, the [ADP2370/ADP2371](#) employ a power saving variable frequency mode that reduces the switching frequency under light load conditions. The [ADP2370/ADP2371](#) operate from input voltages of 3.2 V to 15 V allowing the use of multiple alkaline/NiMH, lithium cells, or other standard power sources.

The [ADP2370/ADP2371](#) offer multiple options for setting the operational frequency. The [ADP2370/ADP2371](#) can be synchronized to a 600 kHz to 1.2 MHz external clock or it can be forced to operate at 600 kHz or 1.2 MHz via the FSEL pin. The [ADP2370/ADP2371](#) can be forced to operate in PWM mode (FPWM) when noise considerations are more important than efficiency.

TYPICAL APPLICATION CIRCUIT

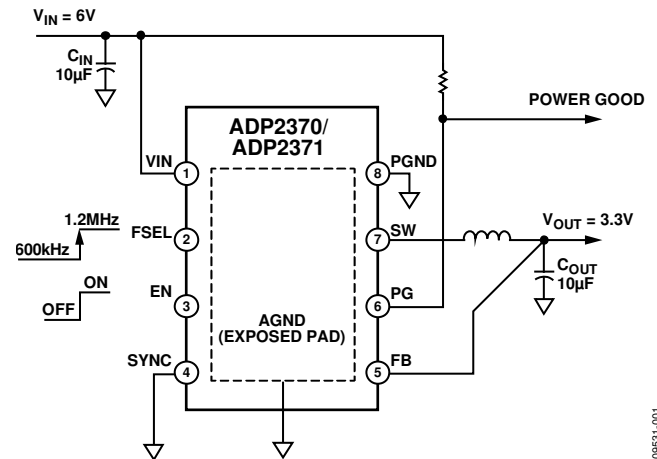


Figure 1.

08531-001

A power-good output is available to indicate when the output voltage is below 92% of its nominal value.

The [ADP2371](#) is identical to the [ADP2370](#) except that the [ADP2371](#) includes the addition of an integrated switched resistor, quick output discharge function (QOD) that automatically discharges the output when the device is disabled.

Both devices include an internal power switch and a synchronous rectifier for minimal external part count and high efficiency. The [ADP2370/ADP2371](#) also include internal soft start and internal compensation for ease of use.

During a logic controlled shutdown, the input is disconnected from the output and the regulator draws less than 1.2 μ A from the input source. Other key features include undervoltage lockout to prevent deep battery discharge and soft start to prevent input overcurrent at startup. Short-circuit protection and thermal overload protection circuits prevent damage under adverse conditions.

The [ADP2370/ADP2371](#) each use one 0805 capacitor, one 1206 capacitor, and one 4 mm \times 4 mm inductor. The total solution size is about 53 mm² resulting in a very small footprint solution to meet a variety of portable applications.

Rev. D

Document Feedback

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REVISION HISTORY

2/14—Rev. C to Rev. D

Change to Figure 13	9
Updated Outline Dimensions	32

11/12—Rev. B to Rev. C

Change to Figure 6	8
Changes to Ordering Guide	32

8/12—Rev. A to Rev. B

Change to Figure 62	17
Changes to Figure 63, Figure 64, Figure 65, and Figure 66	18

5/12—Rev. 0 to Rev. A

Changed Voltage Range for SW to PGND and Ground Plane from -0.3 V to $V_{IN} + 0.3\text{ V}$ to -0.7 V to $V_{IN} + 0.3\text{ V}$	6
Changes to Ordering Guide	32

4/12—Revision 0: Initial Version

SPECIFICATIONS

$V_{IN} = V_{OUT} + 1\text{ V}$ or 3.2 V , whichever is greater, $EN = V_{IN}$, $I_{OUT} = 100\text{ mA}$, $C_{IN} = 10\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$ for typical specifications, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$ for minimum/maximum specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
Input Voltage Range	V_{IN}		3.2		15	V
Quiescent Current	I_{Q-PSM}	FSEL = V_{IN} , SYNC = 0 V, no load, device not switching		13.5		μA
	I_{Q-PWM}	FSEL = V_{IN} , SYNC = V_{IN} , no load, device not switching		725		μA
	I_{SW-PWM}	FSEL = V_{IN} , SYNC = V_{IN} , no load, device switching		5.7		mA
Shutdown Current	I_{SHUT}	EN = GND, $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$		1.2	3.5	μA
FIXED OUTPUT						
Output Current	I_{OUT}		800			mA
Fixed Output Accuracy	V_{OUT}	Initial set point, $I_{OUT} = 250\text{ mA}$, $T_J = 25^\circ\text{C}$	-1		+1	%
		$I_{OUT} = 250\text{ mA}$	-1.5		+1.5	%
		No load to full load, PWM mode	-3		+3	%
ADJUSTABLE OUTPUT						
Feedback Voltage	V_{FB}			0.8		V
Feedback Voltage Accuracy	V_{FB-TOL}	Initial set point, $I_{OUT} = 250\text{ mA}$, $T_J = 25^\circ\text{C}$	-1		+1	%
Output Voltage Range	$V_{OUT-ADJ}$	No load to full load	0.8		14	V
FIXED AND ADJUSTABLE OUTPUT						
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	No load to full load		0.125		%/A
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	$I_{OUT} = 250\text{ mA}$		0.01		%/V
Efficiency	EFF	$I_{OUT} = 250\text{ mA}$, $V_{IN} = 7.2\text{ V}$, $V_{OUT} = 3.3\text{ V}$		92		%
Overcurrent Frequency Foldback Threshold						
Rising	OC _{FOLDBACK-RISE}	% of V_{OUT} , V_{OUT} rising		50		%
Falling	OC _{FOLDBACK-FALL}	% of V_{OUT} , V_{OUT} falling		37.5		%
PSM Threshold	PSM _{THRESHOLD}	$V_{IN} = 7.2\text{ V}$, $V_{OUT} = 3.3\text{ V}$		170		mA
Feedback Pin Input Current						
Fixed	$I_{FB-FIXED}$	Fixed output voltage model		2.5		μA
Adjustable	$I_{FB-ADJUST}$	Adjustable output voltage model		10		nA
Minimum On Time	ON-TIME _{MIN}	$V_{IN} < 5.5\text{ V}$		65	100	ns
		$V_{IN} > 5.5\text{ V}$		40	60	ns
Soft Start Time	SS _{TIME}	When EN rises from 0 V to V_{IN} , and $V_{OUT} = 0.9 \times V_{OUT}$		350		μs
Active Pull-Down Resistance (ADP2371)	R _{PULL-DOWN}			260	400	Ω
POWER SWITCH						
P-Channel On Resistance	RDS _{ON-P}	$V_{IN} > 5.5\text{ V}$, $I_{OUT} = 400\text{ mA}$		400		m Ω
		$V_{IN} < 5.5\text{ V}$, $I_{OUT} = 400\text{ mA}$		500		m Ω
N-Channel On Resistance	RDS _{ON-N}	$V_{IN} > 5.5\text{ V}$, $I_{OUT} = 400\text{ mA}$		280		m Ω
		$V_{IN} < 5.5\text{ V}$, $I_{OUT} = 400\text{ mA}$		400		m Ω
Current Limit						
P-Channel	I_{LIM-P}	Peak inductor current		1200	1300	mA
N-Channel	I_{LIM-N}	Peak inductor current		500	550	mA
Leakage Current	$I_{LEAK-SW}$					
P-Channel				0.01	1	μA
N-Channel				0.01	1	μA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OSCILLATOR						
Oscillator Frequency	f_{OSC}	FSEL = V_{IN} , $3.2\text{ V} \leq V_{IN} \leq 15\text{ V}$	1.0	1.2	1.4	MHz
Frequency Synchronization Range	f_{SYNC_RANGE}	FSEL = 0 V , $3.2\text{ V} \leq V_{IN} \leq 15\text{ V}$	500	600	700	kHz
		FSEL = V_{IN} , $3.2\text{ V} \leq V_{IN} \leq 15\text{ V}$	400		800	
Synchronization Threshold			0.8		1.6	MHz
High	SYNC _{HIGH}	$3.2\text{ V} \leq V_{IN} \leq 15\text{ V}$	1.2			V
Low	SYNC _{LOW}	$3.2\text{ V} \leq V_{IN} \leq 15\text{ V}$			0.4	V
Hysteresis	SYNC _{HYS}	$3.2\text{ V} \leq V_{IN} \leq 15\text{ V}$		200		mV
Typical Sync Duty Cycle Range	SYNC _{DUTY}	V_{IN} (1.2 MHz), $3.2\text{ V} \leq V_{IN} \leq 5\text{ V}$, FSEL = V_{IN}	20		55	%
		V_{IN} (1.2 MHz), $5\text{ V} \leq V_{IN} \leq 15\text{ V}$, FSEL = V_{IN}	20		70	%
SYNC Pin Leakage Current	SYNC _{LKG}	SYNC = 0 V or SYNC = V_{IN}		0.05	1	μA
FSEL Threshold						
High	FSEL _{HIGH}	$3.2\text{ V} \leq V_{IN} \leq 15\text{ V}$	1			V
Low	FSEL _{LOW}	$3.2\text{ V} \leq V_{IN} \leq 15\text{ V}$			0.4	V
Hysteresis	FSEL _{HYS}	$3.2\text{ V} \leq V_{IN} \leq 15\text{ V}$		125		mV
FSEL Pin Leakage Current	FSEL _{LKG}	FSEL = 0 V or FSEL = V_{IN}		0.04	1	μA
POWER GOOD (PG PIN)						
PG Threshold		$3.2\text{ V} \leq V_{IN} \leq 15\text{ V}$				
Rising	PG _{RISE}			92	95	%
Falling	PG _{FALL}		82.5	87		%
Hysteresis	PG _{HYS}			5		%
PG Output Low	PG _{LOW}	Pull-up current < 1 mA			0.3	V
PG Delay						
Rising	PG _{DELAYRISE}	V_{OUT} crossing PG rising threshold, pull-up current < 1 mA		20		μs
Falling	PG _{DELAYFALL}	V_{OUT} crossing PG falling threshold, pull-up current < 1 mA		0.5		μs
PG Leakage	PG _{LKG}			0.04	1	μA
UNDERVOLTAGE LOCKOUT (UVLO)						
Input Voltage Rising	UVLO _{RISE}				3.19	V
Input Voltage Falling	UVLO _{FALL}		2.80			V
Hysteresis	UVLO _{HYS}			190		mV
ENABLE INPUT STANDBY (EN PIN)						
EN Input Logic		$3.2\text{ V} \leq V_{IN} \leq 15\text{ V}$				
High	EN _{STBY-HIGH}		1			V
Low	EN _{STBY-LOW}				0.4	V
Hysteresis	EN _{STBY-HYS}			125		mV
ENABLE INPUT PRECISION (EN PIN)						
EN Input Logic		$3.2\text{ V} \leq V_{IN} \leq 15\text{ V}$				
High	EN _{HIGH}		1.135	1.2	1.26	V
Low	EN _{LOW}		1.045	1.1	1.155	V
Hysteresis	EN _{HYS}			100		mV
EN Input Leakage Current	I _{EN-LKG}	EN = V_{IN} or GND		0.05	1	μA
EN Input Delay Time	T _{EN-DLY}	For $V_{OUT} = 0\text{ V}$ to $0.1 \times V_{OUT}$ when EN rises from 0 V to V_{IN}		70		μs
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS _{SD}	$3.2\text{ V} \leq V_{IN} \leq 15\text{ V}$		150		$^{\circ}\text{C}$
Thermal Shutdown Hysteresis	TS _{SD-HYS}	T_J rising		15		$^{\circ}\text{C}$

RECOMMENDED SPECIFICATIONS: CAPACITORS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
MINIMUM INPUT and OUTPUT CAPACITANCE ¹	C _{MIN}	T _A = -40°C to +125°C	6.5	10		μF
CAPACITOR ESR	R _{ESR}	T _A = -40°C to +125°C	1		10	mΩ

¹ The minimum input and output capacitance should be greater than 7 μF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R- and X5R-type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any buck.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to PGND and Ground Plane	−0.3 V to +17 V
SW to PGND and Ground Plane	−0.7 V to VIN + 0.3 V
FB to PGND and Ground Plane	−0.3 V to +6 V
EN to PGND and Ground Plane	−0.3 V to +17 V
PG to PGND and Ground Plane	−0.3 V to +17 V
SYNC to PGND and Ground Plane	−0.3 V to +17 V
FSEL to PGND and Ground Plane	−0.3 V to +17 V
Temperature Range	
Storage	−65°C to +150°C
Operating Ambient	−40°C to +85°C
Operating Junction	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. Exceeding the junction temperature (T_J) limit can cause damage to the ADP2370/ADP2371. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. The maximum ambient temperature may require derating in applications with high power dissipation and poor thermal resistance.

In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature of the device is dependent on the ambient temperature, the power dissipation of the device, and the junction to ambient thermal resistance of the package (θ_{JA}).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. θ_{JA} is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value

of θ_{JA} can vary, depending on PCB material, layout, and environmental conditions.

The specified values of θ_{JA} are based on a 4-layer, 4 in. × 3 in. circuit board. See JESD 51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*, for detailed information on board construction. For more information, see [Application Note AN-772, A Design and Manufacturing Guide for the Lead Frame Chip Scale Package \(LFCSP\)](#).

Ψ_{JB} is the junction to board thermal characterization parameter with units of °C/W. The Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB} . Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

For more detailed information regarding Ψ_{JB} , see JESD51-12 and JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. θ_{JC} is a parameter for surface-mount packages with top mounted heat sinks.

Table 4. Thermal Resistance

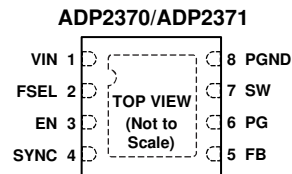
Package Type	θ_{JA}	θ_{JC}	Ψ_{JB}	Unit
8-Lead 3 mm × 3 mm LFCSP	36.7	23.5	17.2	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

**NOTES**

1. THE EXPOSED PAD ON THE BOTTOM OF THE PACKAGE ENHANCES THE THERMAL PERFORMANCE AND IS ELECTRICALLY CONNECTED TO GROUND INSIDE THE PACKAGE. THE EXPOSED PAD MUST BE CONNECTED TO THE GROUND PLANE ON THE CIRCUIT BOARD FOR PROPER OPERATION.

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Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIN	Power Input.
2	FSEL	Frequency Select. High = 1.2 MHz, low = 600 kHz.
3	EN	Enable. Enable input with precision thresholds.
4	SYNC	Synchronize. This pin is used to synchronize the device to an external 600 kHz to 1.2 MHz clock or forces PWM mode when it is held high. SYNC held low forces automatic PWM/PSM operation.
5	FB	Feedback. This pin provides feedback from the output.
6	PG	Power Good. PG is an open-drain output.
7	SW	Switch. This pin serves as the connection from the power MOSFETs to the inductor.
8	PGND EPAD	Power Ground. Exposed Pad. The exposed pad on the bottom of the package enhances the thermal performance and is electrically connected to ground inside the package. The exposed pad must be connected to the ground plane on the circuit board for proper operation.

TYPICAL PERFORMANCE CHARACTERISTICS

BUCK OUTPUT

Using recommended inductor values, $I_{OUT} = 10\text{ mA}$, $C_{IN} = C_{OUT} = 10\text{ }\mu\text{F}$, automatic PSM/PWM mode, $T_A = 25^\circ\text{C}$, unless otherwise noted.

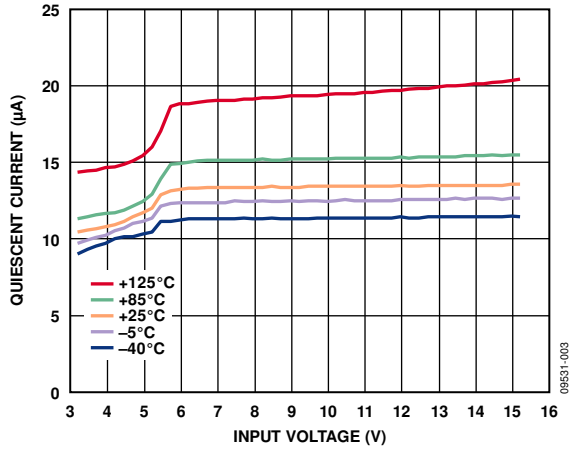


Figure 3. Quiescent Supply Current vs. Input Voltage, Nonswitching, Different Temperatures

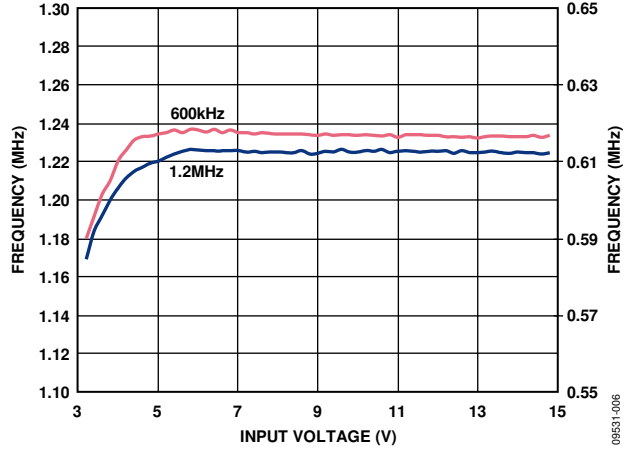


Figure 6. Switching Frequency vs. Input Voltage, FPWM Mode

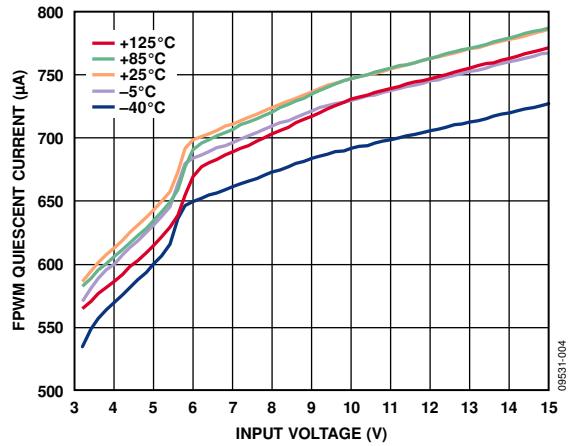


Figure 4. FPWM Quiescent Supply Current vs. Input Voltage, Nonswitching, Different Temperatures

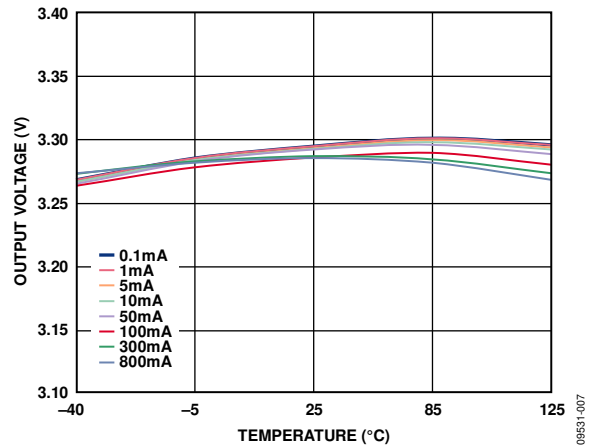


Figure 7. Output Voltage vs. Temperature, $V_{OUT} = 3.3\text{ V}$, $V_{IN} = 7.3\text{ V}$, Different Loads

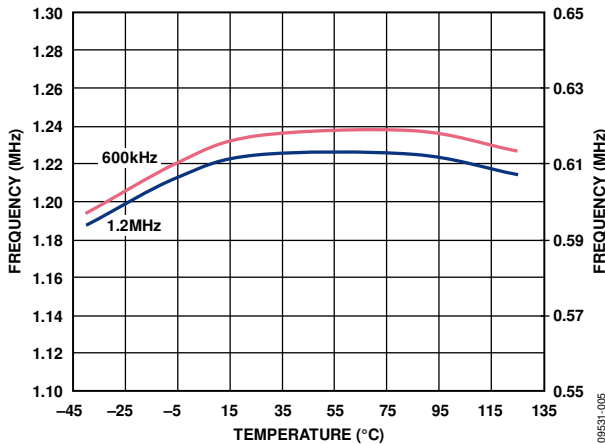


Figure 5. Switching Frequency vs. Temperature, FPWM Mode, $V_{IN} = 8\text{ V}$

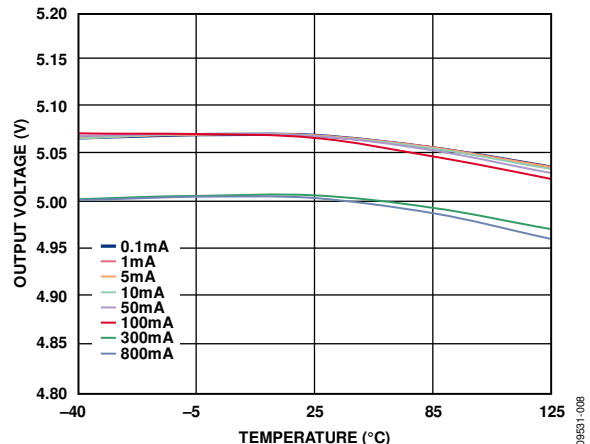


Figure 8. Output Voltage vs. Temperature, $V_{OUT} = 5\text{ V}$, $V_{IN} = 7.2\text{ V}$, Different Loads

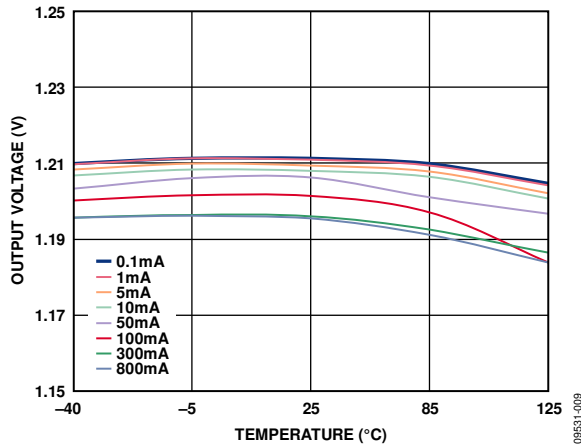


Figure 9. Output Voltage vs. Temperature, $V_{OUT} = 1.2\text{ V}$, $V_{IN} = 4\text{ V}$, Different Loads

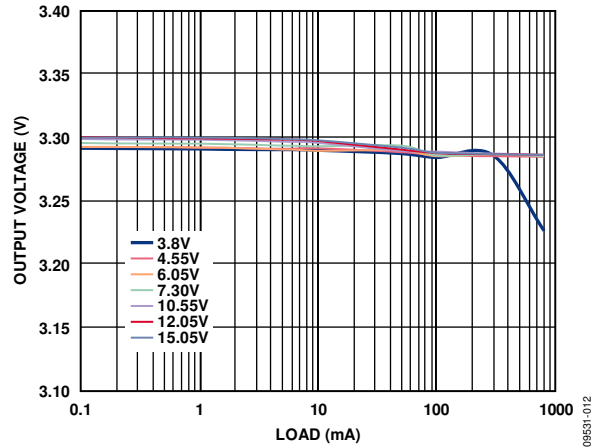


Figure 12. Load Regulation, $V_{OUT} = 3.3\text{ V}$

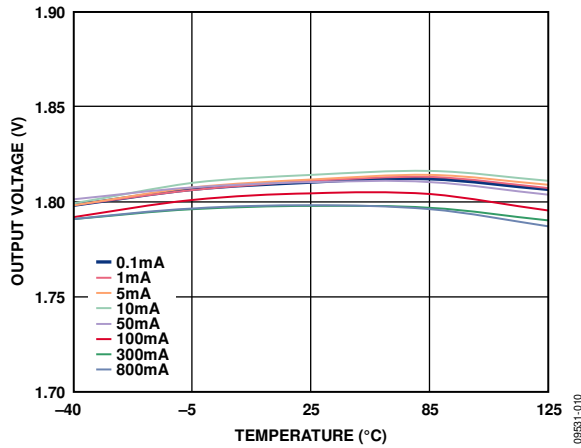


Figure 10. Output Voltage vs. Temperature, $V_{OUT} = 1.8\text{ V}$, $V_{IN} = 7.2\text{ V}$, Different Loads

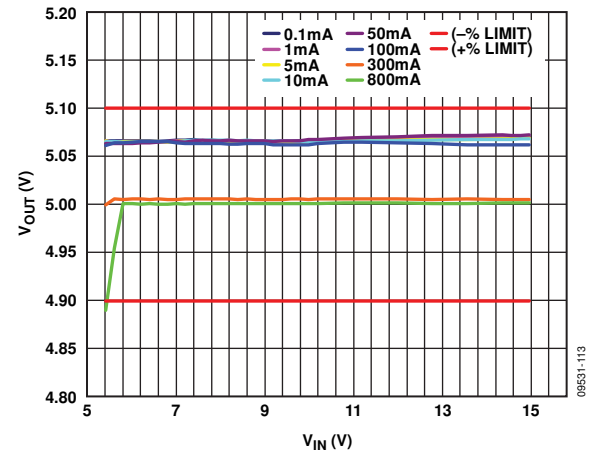


Figure 13. Line Regulation, $V_{OUT} = 5.0\text{ V}$, Different Loads

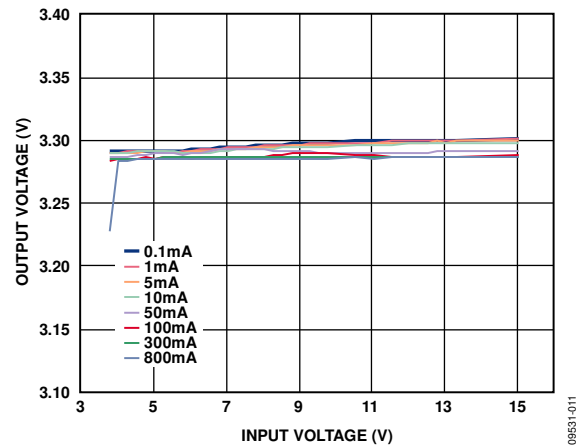


Figure 11. Line Regulation, $V_{OUT} = 3.3\text{ V}$, Different Loads

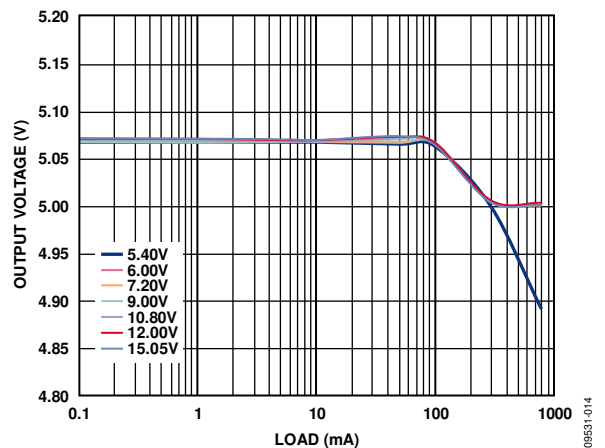


Figure 14. Load Regulation, $V_{OUT} = 5.0\text{ V}$

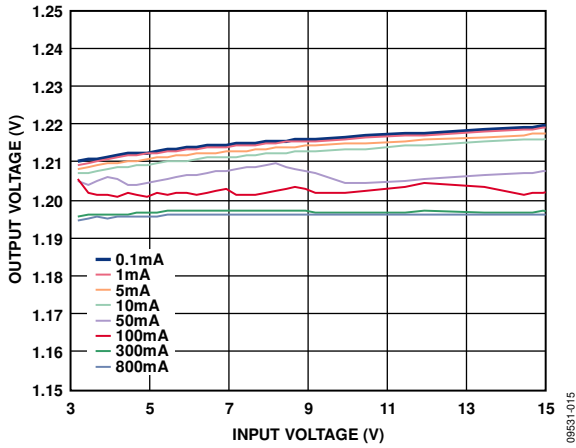


Figure 15. Line Regulation, $V_{OUT} = 1.2V$, Different Loads

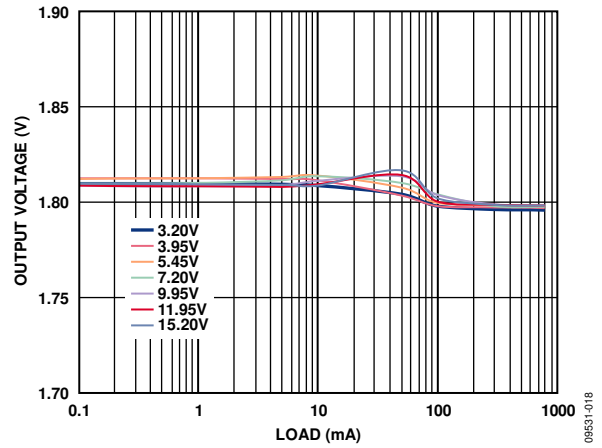


Figure 18. Load Regulation, $V_{OUT} = 1.8V$

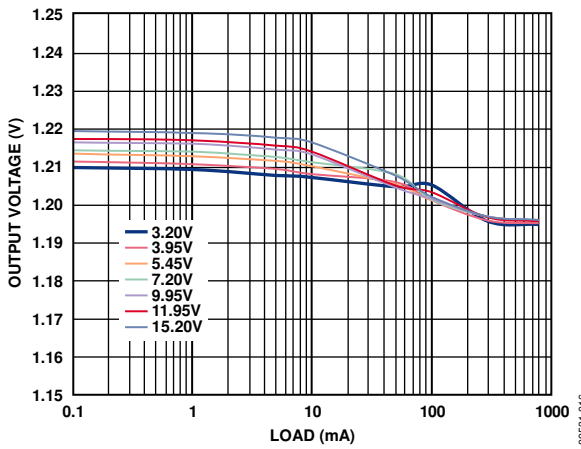


Figure 16. Load Regulation, $V_{OUT} = 1.2V$

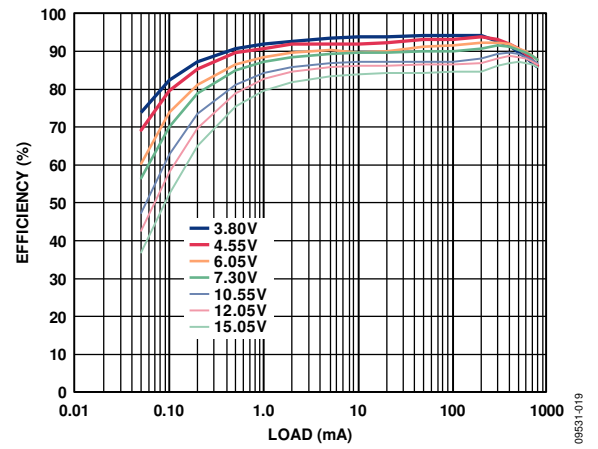


Figure 19. Efficiency vs. Load Current, $V_{OUT} = 3.3V$, Different Input Voltages

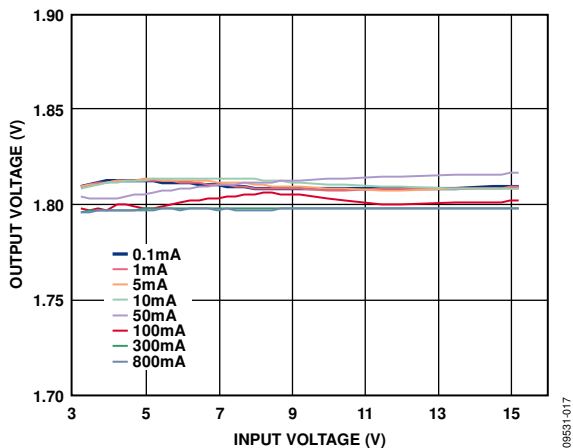


Figure 17. Line Regulation, $V_{OUT} = 1.8V$, Different Loads

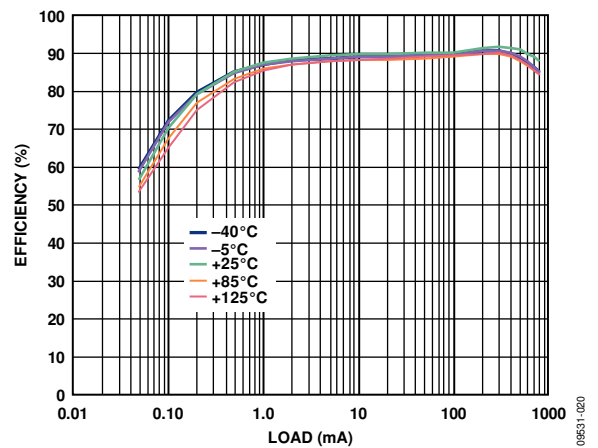


Figure 20. Efficiency vs. Load Current, $V_{OUT} = 3.3V$, Different Temperatures, $V_{IN} = 7.3V$

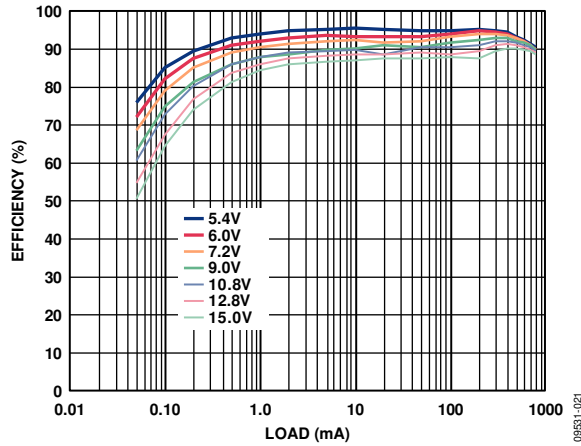


Figure 21. Efficiency vs. Load Current, $V_{OUT} = 5.0\text{ V}$, Different Input Voltages

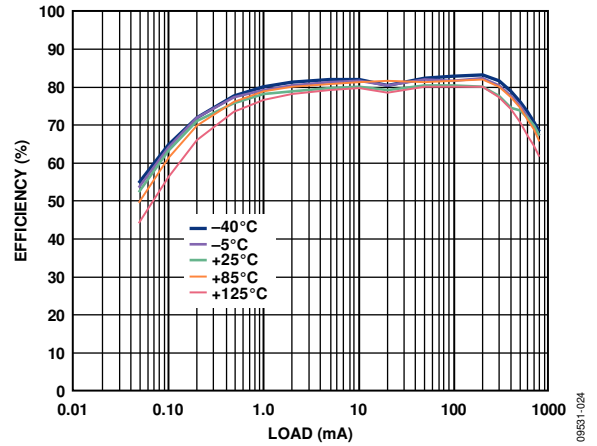


Figure 24. Efficiency vs. Load Current, $V_{OUT} = 1.2\text{ V}$, Different Temperatures, $V_{IN} = 4\text{ V}$

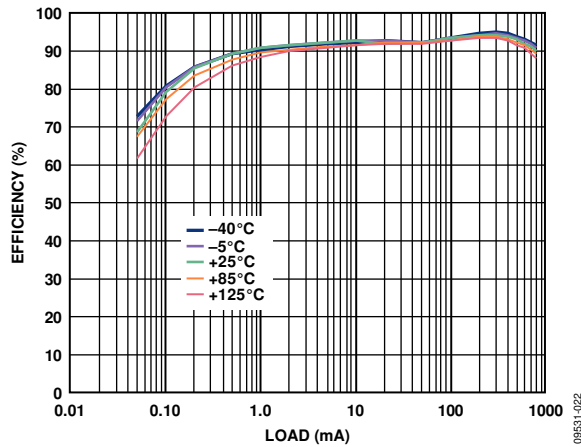


Figure 22. Efficiency vs. Load Current, $V_{OUT} = 5.0\text{ V}$, Different Temperatures

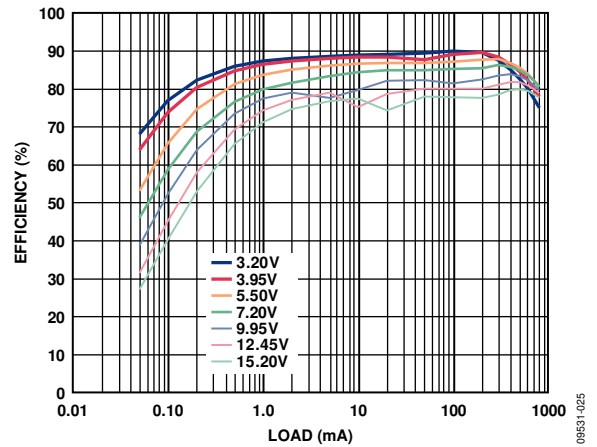


Figure 25. Efficiency vs. Load Current, $V_{OUT} = 1.8\text{ V}$, Different Input Voltages

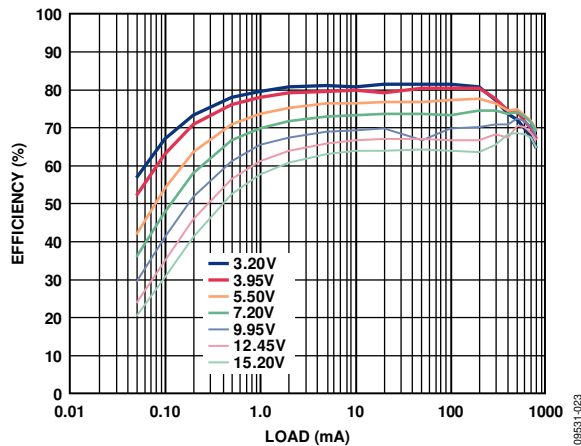


Figure 23. Efficiency vs. Load Current, $V_{OUT} = 1.2\text{ V}$, Different Input Voltages

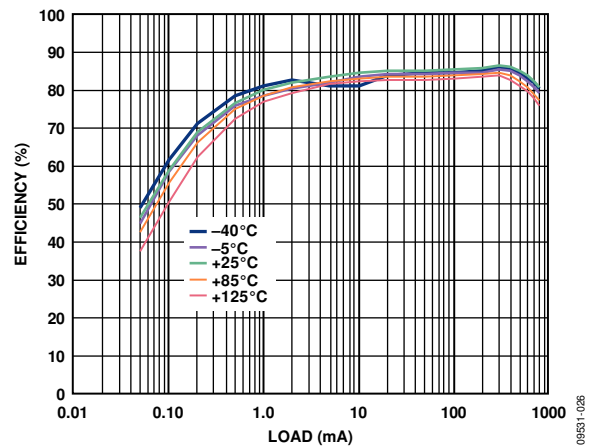


Figure 26. Efficiency vs. Load Current, $V_{OUT} = 1.8\text{ V}$, Different Temperatures, $V_{IN} = 4\text{ V}$

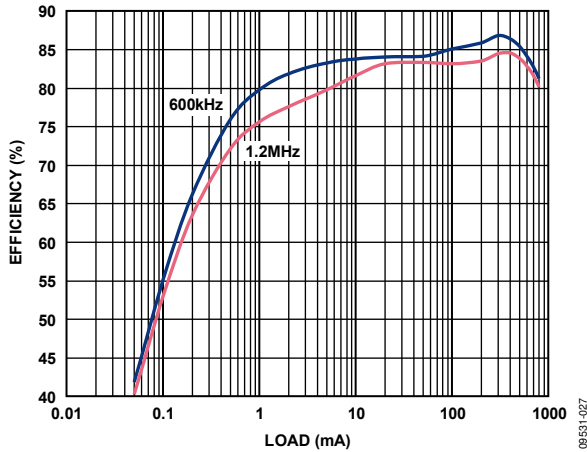


Figure 27. Efficiency vs. Load Current, Different Switching Frequency, $V_{OUT} = 1.8V$, $V_{IN} = 9V$

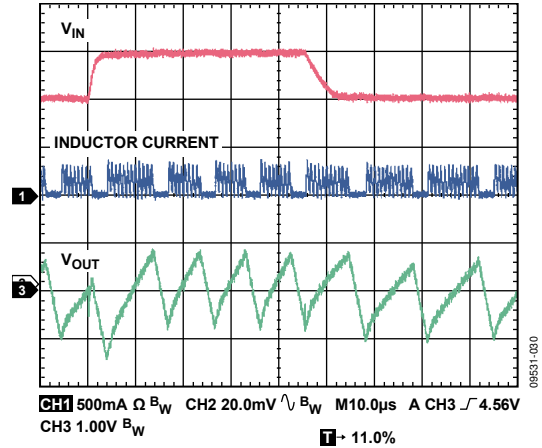


Figure 30. Line Transient, $V_{OUT} = 1.2V$, PSM Mode, 100 mA, $V_{IN} = 4V$ to $5V$, $2\mu s$ Rise Time, $C_{IN} = 3.3\mu F$

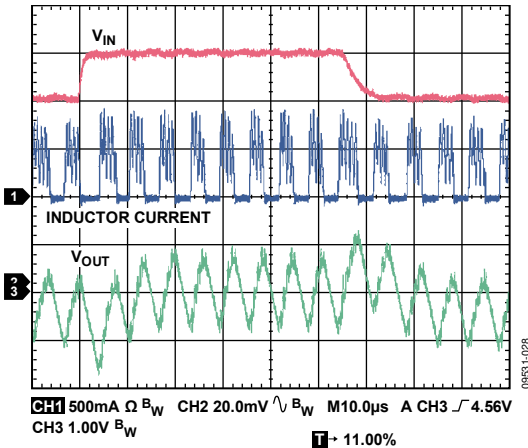


Figure 28. Line Transient, $V_{OUT} = 1.8V$, PSM Mode, 100 mA, $V_{IN} = 4V$ to $5V$, $2\mu s$ Rise Time, $C_{IN} = 3.3\mu F$

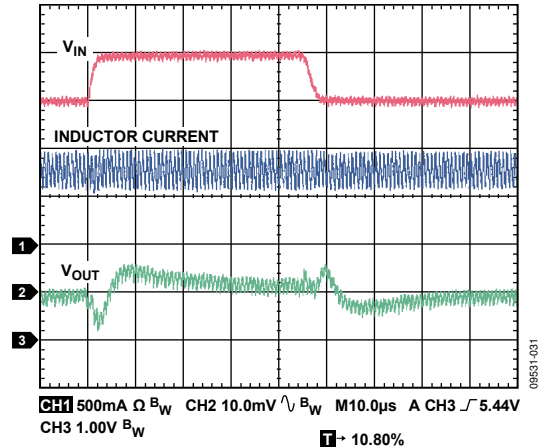


Figure 31. Line Transient, $V_{OUT} = 1.2V$, PWM Mode, 800 mA, $V_{IN} = 4V$ to $5V$, $2\mu s$ Rise Time, $C_{IN} = 3.3\mu F$

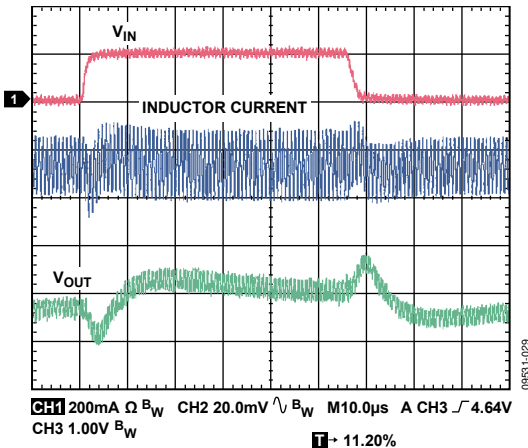


Figure 29. Line Transient, $V_{OUT} = 1.8V$, PWM Mode, 800 mA, $V_{IN} = 4V$ to $5V$, $2\mu s$ Rise Time, $C_{IN} = 3.3\mu F$

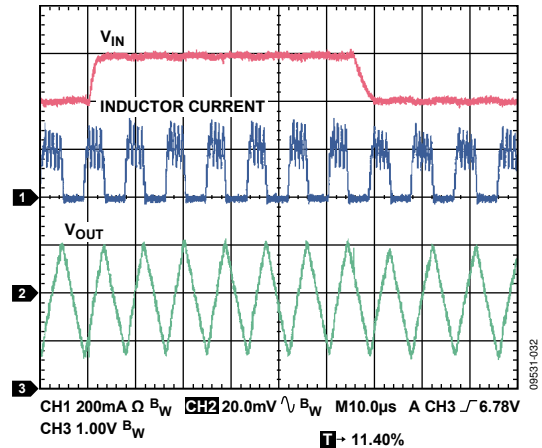


Figure 32. Line Transient, $V_{OUT} = 3.3V$, PSM Mode, 100 mA, $V_{IN} = 6V$ to $7V$, $2\mu s$ Rise Time, $C_{IN} = 3.3\mu F$

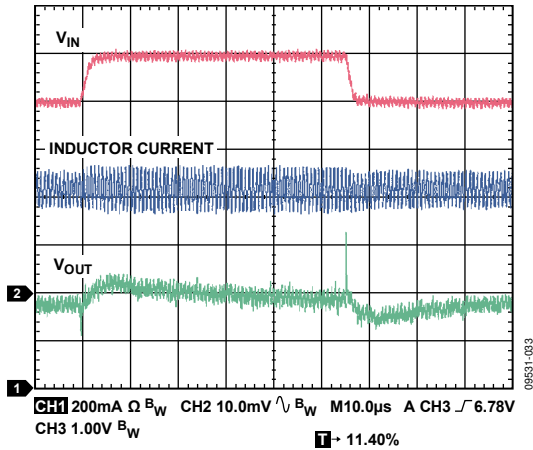


Figure 33. Line Transient, $V_{OUT} = 3.3\text{ V}$, PWM Mode, 800 mA, $V_{IN1} = 6\text{ V}$ to 7 V , $2\text{ }\mu\text{s}$ Rise Time, $C_{IN} = 3.3\text{ }\mu\text{F}$

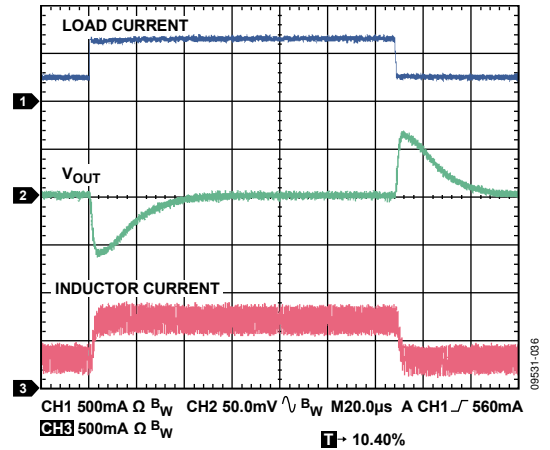


Figure 36. Load Transient, $V_{OUT} = 1.8\text{ V}$, 300 mA to 800 mA, Load Current Rise Time = 200 ns

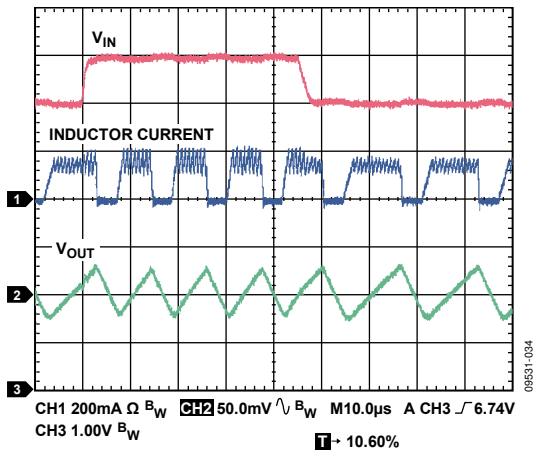


Figure 34. Line Transient, $V_{OUT} = 5\text{ V}$, PSM Mode, 100 mA, $V_{IN1} = 6\text{ V}$ to 7 V , $2\text{ }\mu\text{s}$ Rise Time, $C_{IN} = 3.3\text{ }\mu\text{F}$

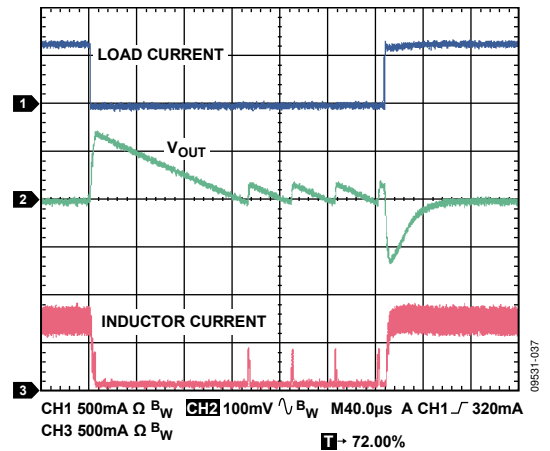


Figure 37. Load Transient, $V_{OUT} = 1.8\text{ V}$, 10 mA to 800 mA, Load Current Rise Time = 200 ns

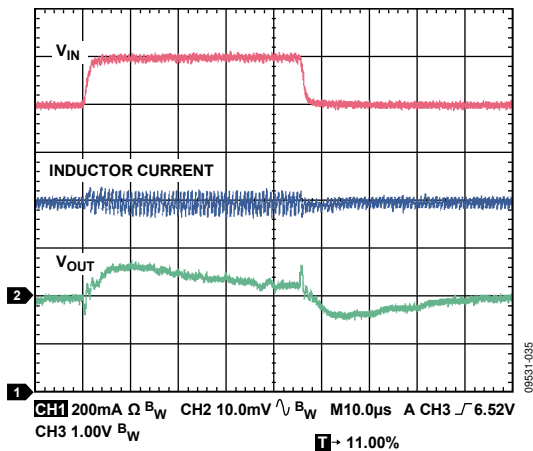


Figure 35. Line Transient, $V_{OUT} = 5\text{ V}$, PWM Mode, 800 mA, $V_{IN1} = 6\text{ V}$ to 7 V , $2\text{ }\mu\text{s}$ Rise Time, $C_{IN} = 3.3\text{ }\mu\text{F}$

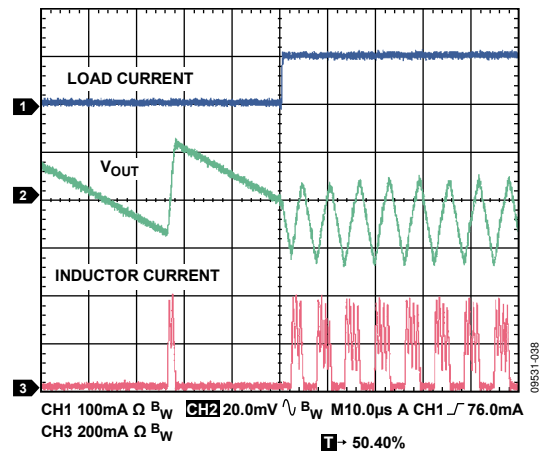


Figure 38. Load Transient, $V_{OUT} = 1.8\text{ V}$, 10 mA to 110 mA, Load Current Rise Time = 200 ns

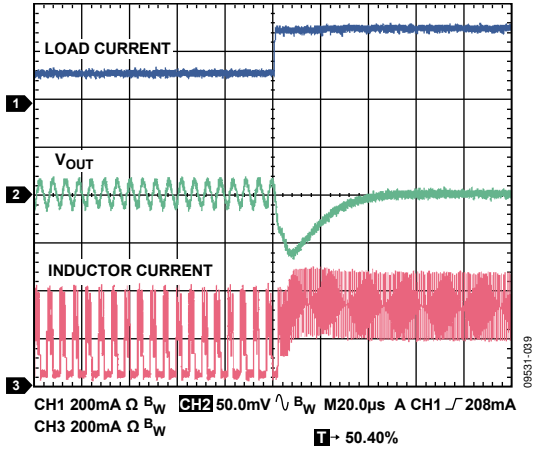


Figure 39. Load Transient, $V_{OUT} = 1.8$ V, 100 mA to 300 mA, Load Current Rise Time = 200 ns

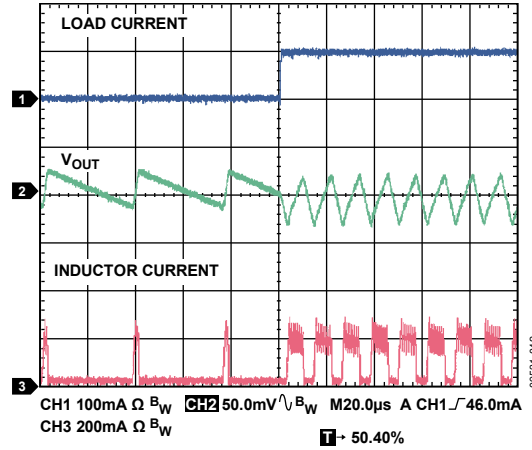


Figure 42. Load Transient, $V_{OUT} = 3.3$ V, 10 mA to 110 mA, Load Current Rise Time = 200 ns

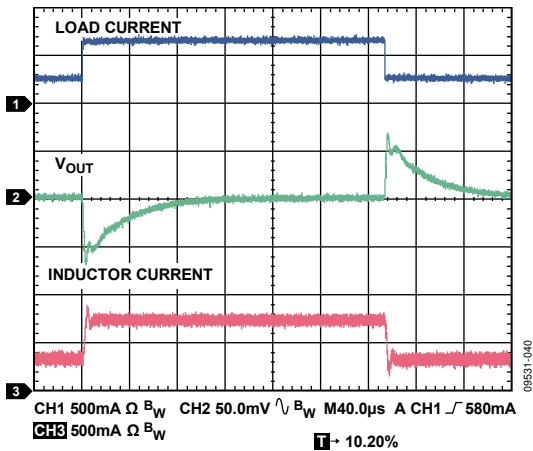


Figure 40. Load Transient, $V_{OUT} = 3.3$ V, 300 mA to 800 mA, Load Current Rise Time = 200 ns

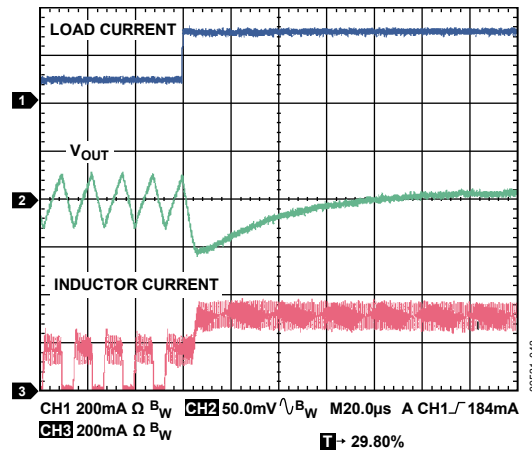


Figure 43. Load Transient, $V_{OUT} = 3.3$ V, 100 mA to 300 mA, Load Current Rise Time = 200 ns

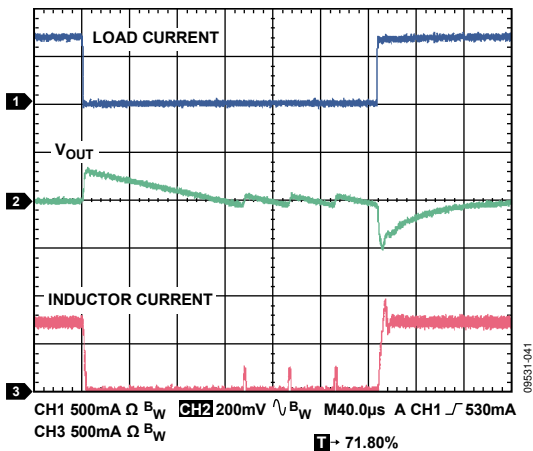


Figure 41. Load Transient, $V_{OUT} = 3.3$ V, 10 mA to 800 mA, Load Current Rise Time = 200 ns

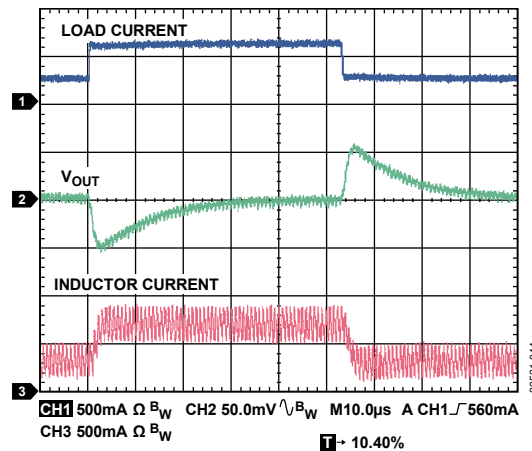


Figure 44. Load Transient, $V_{OUT} = 1.2$ V, 300 mA to 800 mA, Load Current Rise Time = 200 ns, $V_{IN} = 5$ V

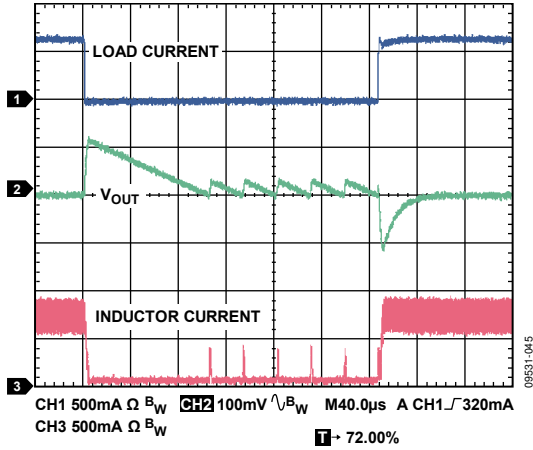


Figure 45. Load Transient, $V_{OUT} = 1.2\text{ V}$, 10 mA to 800 mA, Load Current Rise Time = 200 ns, $V_{IN} = 5\text{ V}$

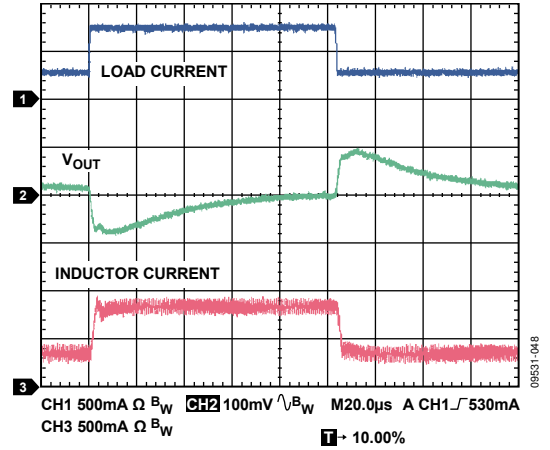


Figure 48. Load Transient, $V_{OUT} = 5\text{ V}$, 300 mA to 800 mA, Load Current Rise Time = 200 ns, $V_{IN} = 8\text{ V}$

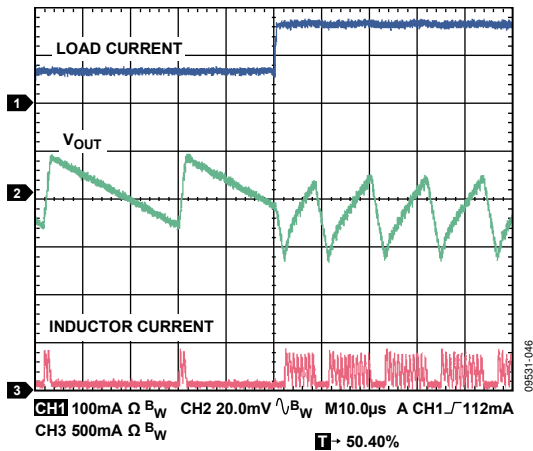


Figure 46. Load Transient, $V_{OUT} = 1.2\text{ V}$, 10 mA to 110 mA, Load Current Rise Time = 200 ns, $V_{IN} = 5\text{ V}$

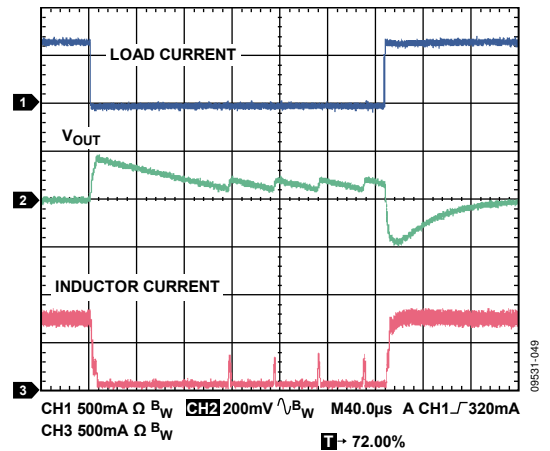


Figure 49. Load Transient, $V_{OUT} = 5\text{ V}$, 1 mA to 800 mA, Load Current Rise Time = 200 ns, $V_{IN} = 8\text{ V}$

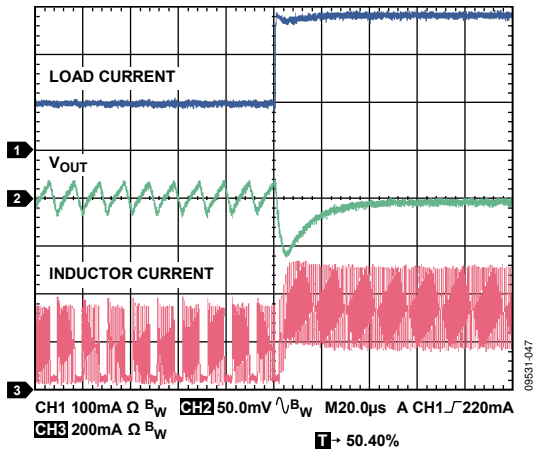


Figure 47. Load Transient, $V_{OUT} = 1.2\text{ V}$, 100 mA to 300 mA, Load Current Rise Time = 200 ns, $V_{IN} = 5\text{ V}$

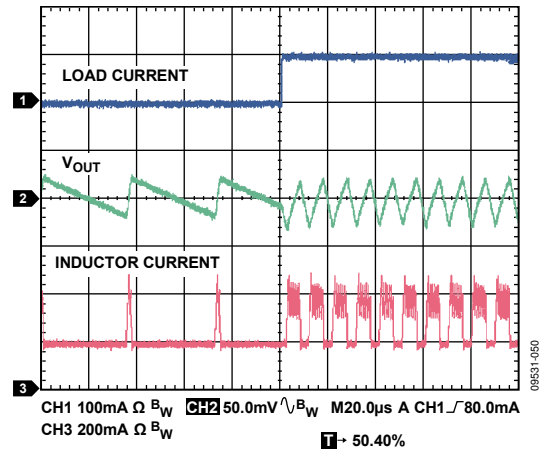


Figure 50. Load Transient, $V_{OUT} = 5\text{ V}$, 10 mA to 110 mA, Load Current Rise Time = 200 ns, $V_{IN} = 8\text{ V}$

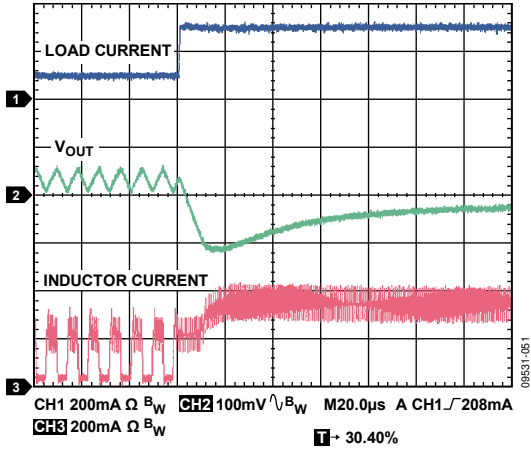


Figure 51. Load Transient, $V_{OUT} = 5\text{ V}$, 100 mA to 300 mA, Load Current Rise Time = 200 ns, $V_{IN} = 8\text{ V}$

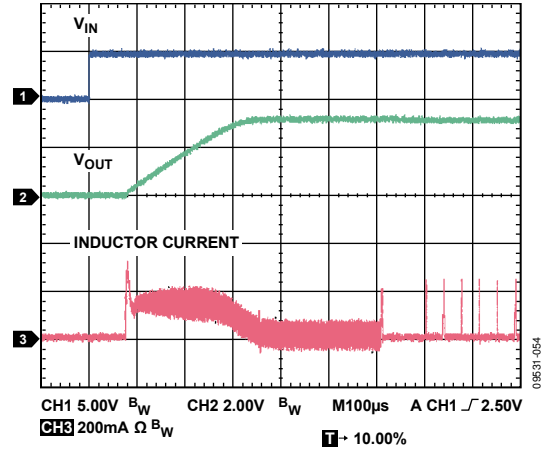


Figure 54. Startup, $V_{OUT} = 3.3\text{ V}$, 10 mA

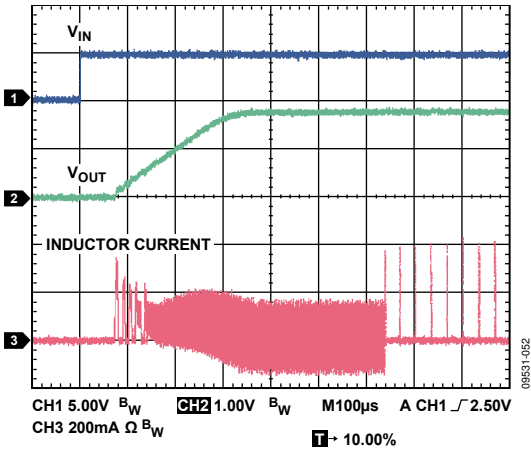


Figure 52. Startup, $V_{OUT} = 1.8\text{ V}$, 10 mA

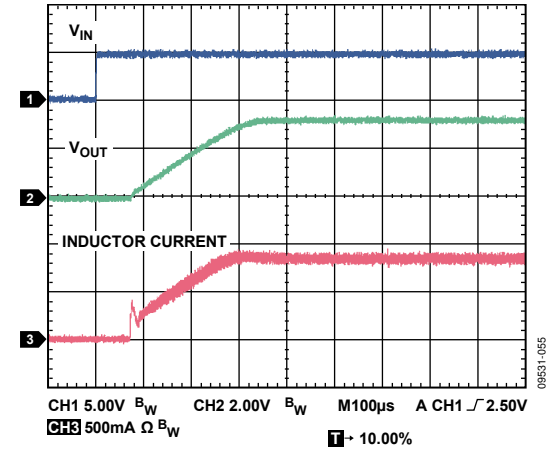


Figure 55. Startup, $V_{OUT} = 3.3\text{ V}$, 800 mA

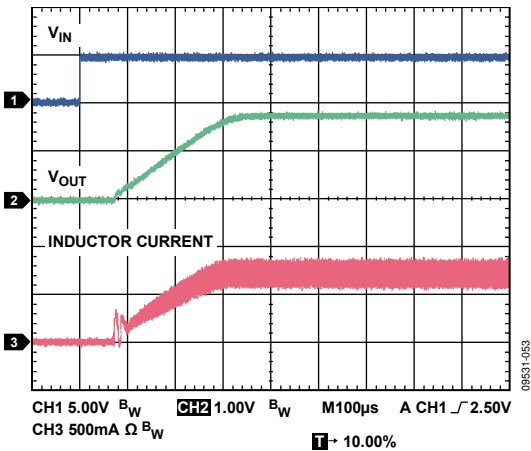


Figure 53. Startup, $V_{OUT} = 1.8\text{ V}$, 800 mA

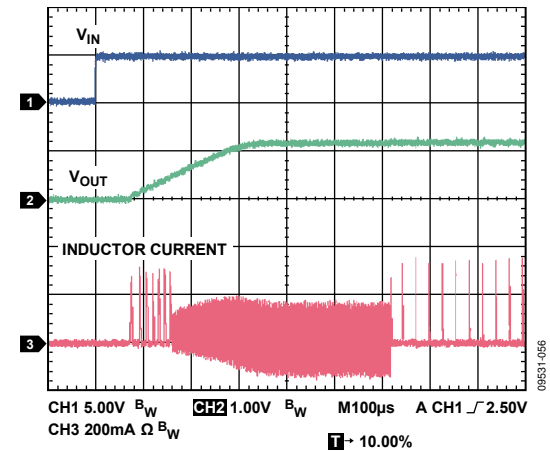


Figure 56. Startup, $V_{OUT} = 1.2\text{ V}$, 10 mA, $V_{IN} = 5\text{ V}$

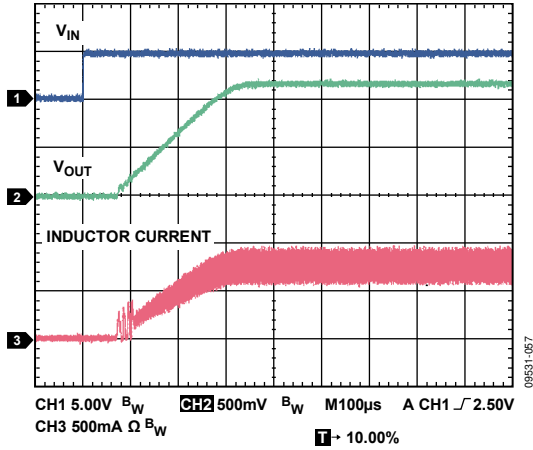


Figure 57. Startup, $V_{OUT} = 1.2V$, 800 mA, $V_{IN} = 5V$

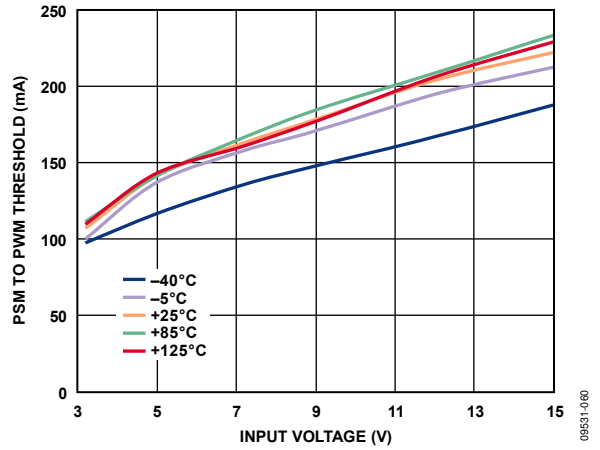


Figure 60. PSM to PWM Mode Transition vs. Input Voltage, Different Temperatures

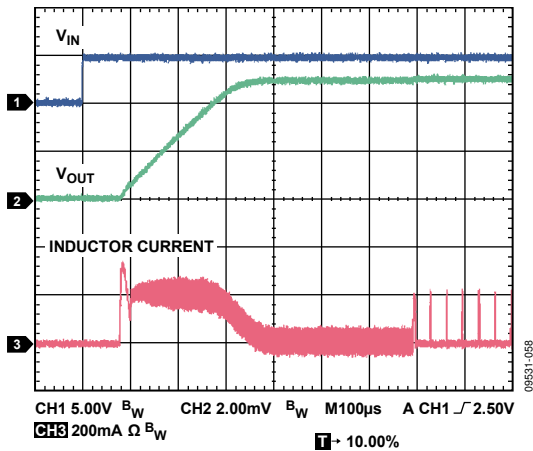


Figure 58. Startup, $V_{OUT} = 5V$, 10 mA, $V_{IN} = 7V$

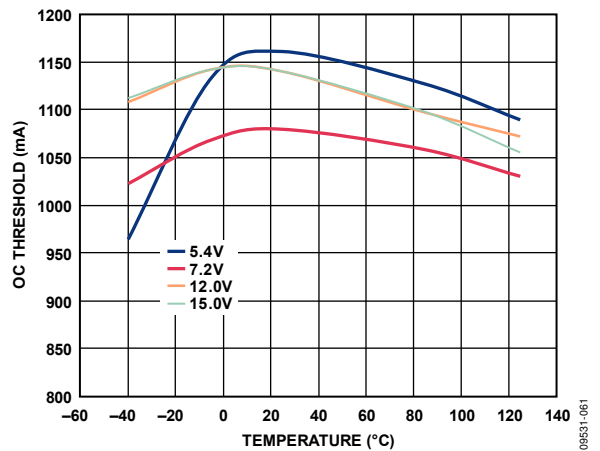


Figure 61. Overcurrent Limit vs. Temperature, $V_{OUT} = 5V$, Different Input Voltages

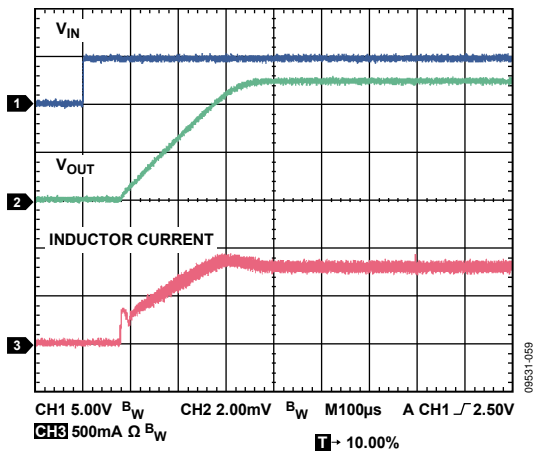


Figure 59. Startup, $V_{OUT} = 5V$, 800 mA, $V_{IN} = 7V$

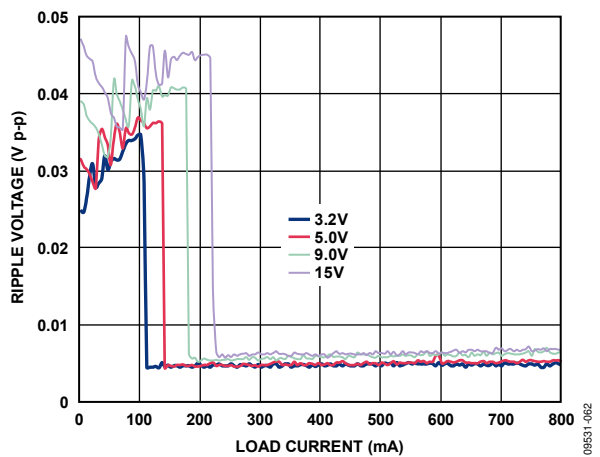


Figure 62. Output Ripple vs. Load Current, $V_{OUT} = 1.2V$, Different Input Voltages, Automatic Mode

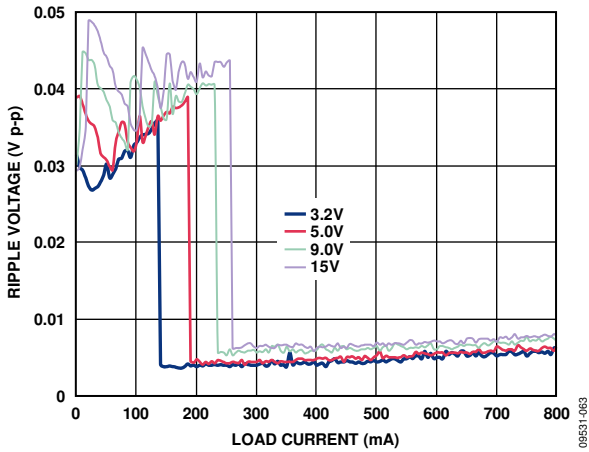


Figure 63. Output Ripple vs. Load Current, $V_{OUT} = 1.8\text{ V}$, Different Input Voltages, Automatic Mode

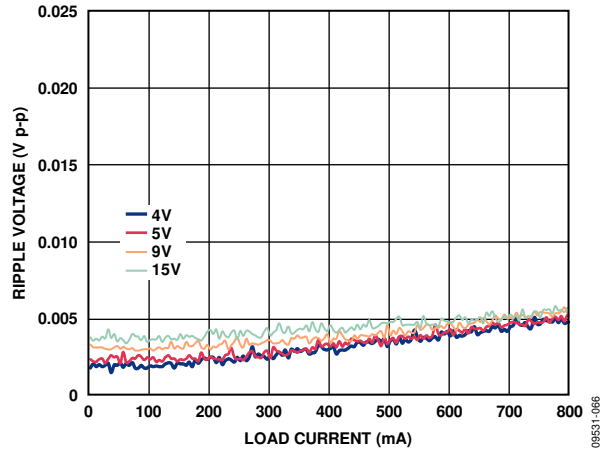


Figure 66. Output Ripple vs. Load Current, $V_{OUT} = 3.3\text{ V}$, Different Input Voltages, Force PWM Mode

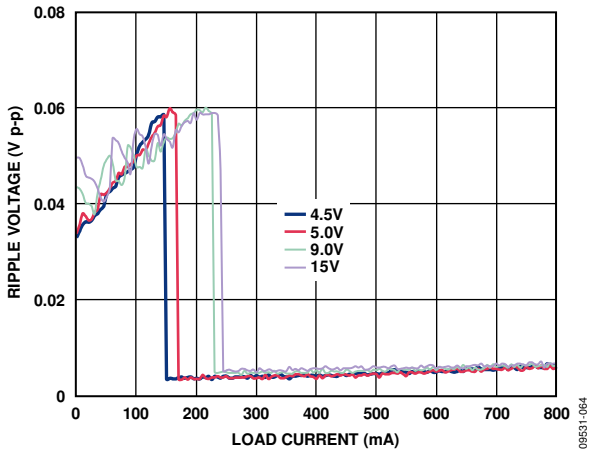


Figure 64. Output Ripple vs. Load Current, $V_{OUT} = 3.3\text{ V}$, Different Input Voltages, Automatic Mode

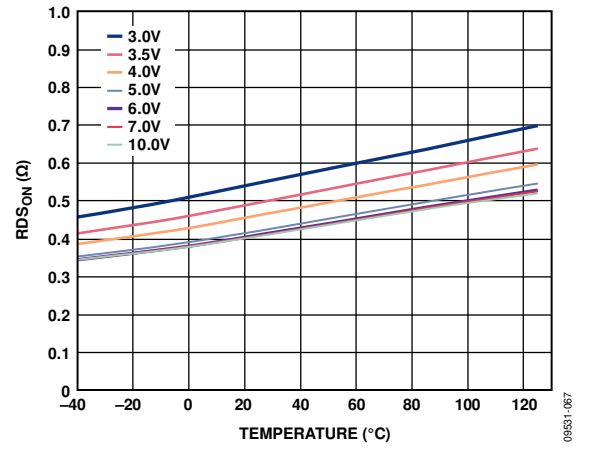


Figure 67. PMOS $R_{DS(on)}$ vs. Temperature at 400 mA, Different Input Voltages

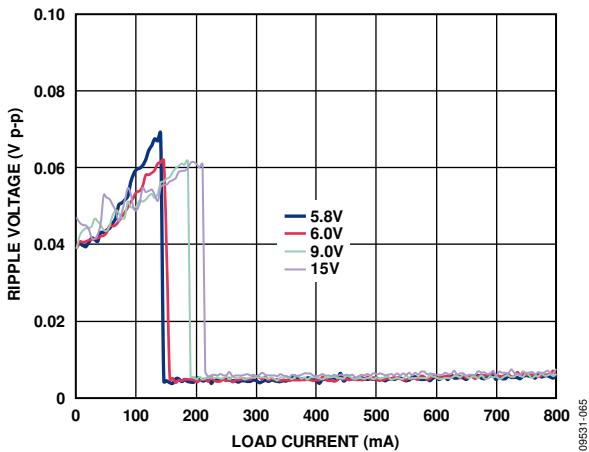


Figure 65. Output Ripple vs. Load Current, $V_{OUT} = 5\text{ V}$, Different Input Voltages, Automatic Mode

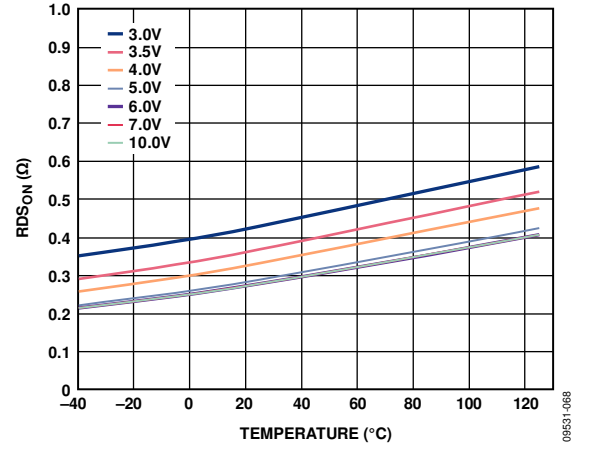


Figure 68. NMOS $R_{DS(on)}$ vs. Temperature at 400 mA, Different Input Voltages

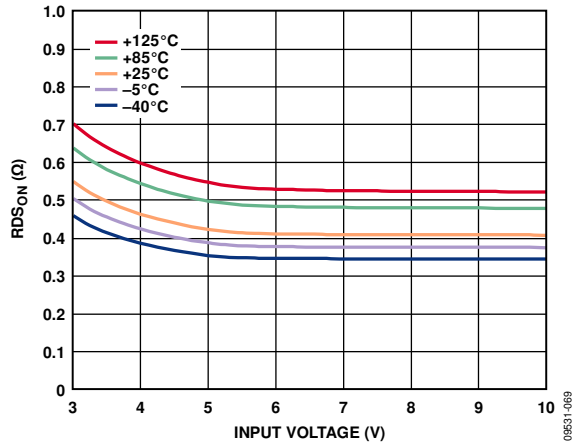


Figure 69. PMOS $R_{DS(on)}$ vs. Input Voltage at 400 mA, Different Temperatures

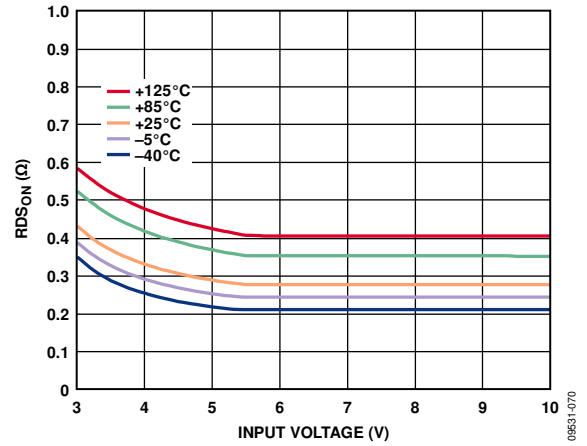


Figure 70. NMOS $R_{DS(on)}$ vs. Input Voltage at 400 mA, Different Temperatures

THEORY OF OPERATION

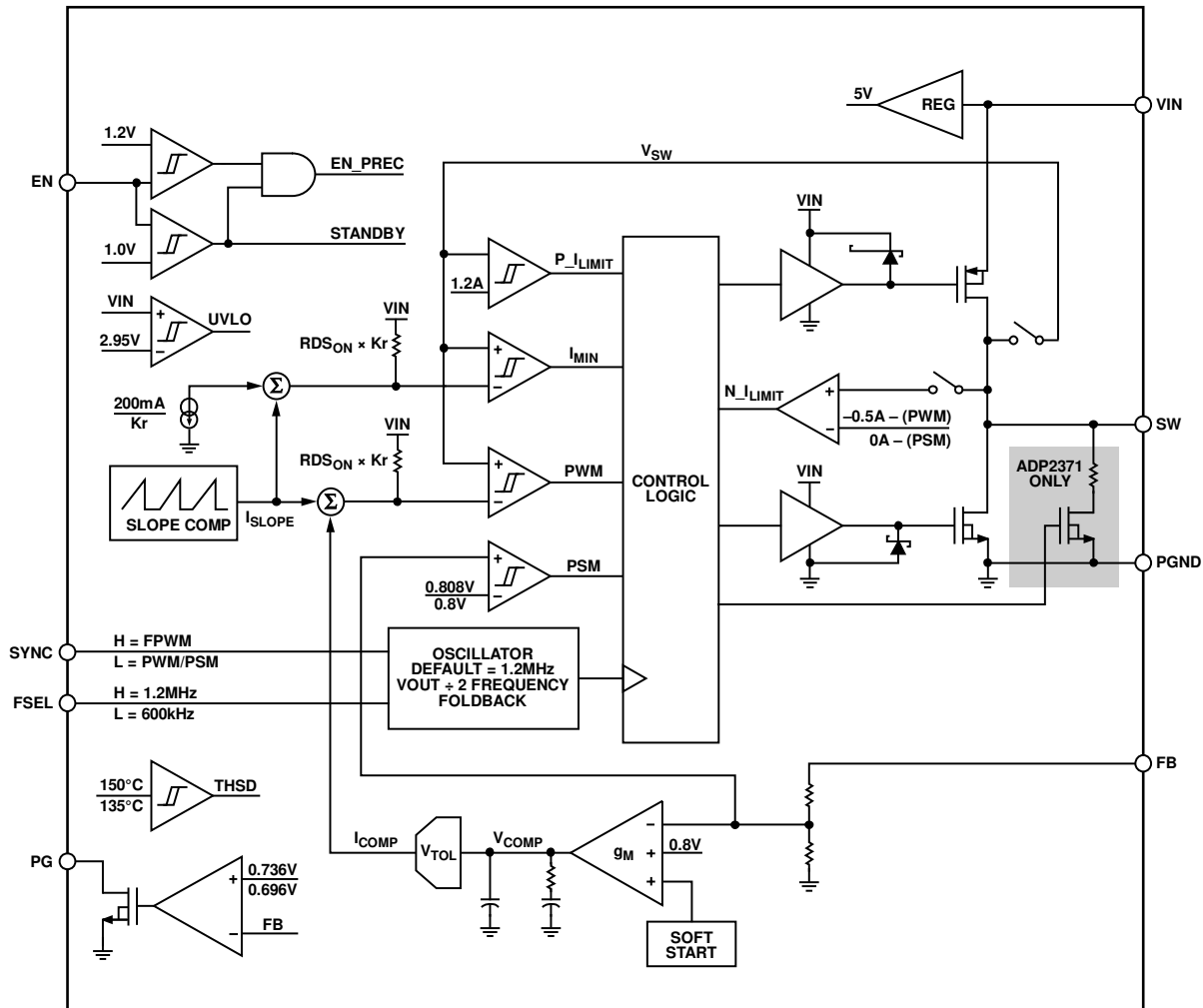


Figure 71. Functional Block Diagram

The ADP2370/ADP2371 use a high speed, current mode, constant frequency PWM control scheme for excellent stability and transient response. To ensure the longest battery life in portable applications, the ADP2370/ADP2371 has a power saving mode. Under light load conditions, the output capacitor is charged as needed to maintain regulation; otherwise, the ADP2370/ADP2371 enter sleep mode, a low 14 μA quiescent state. The architecture ensures smooth transitions from PWM mode to and from PSM, and maintains high efficiencies at light loads. The following sections describe the two modes of operation and provide detailed descriptions of the ADP2370/ADP2371 features.

PWM OPERATION

The ADP2370/ADP2371 PWM mode is a fixed frequency, 1.2 MHz typical, current mode architecture. Use the SYNC pin to synchronize the regulator to an external clock frequency or use the FSEL pin to select an internal clock frequency of 600 kHz or 1.2 MHz.

The ADP2370/ADP2371 use a constant slope compensation scheme where the inductor scales with the output voltage. The equation for choosing the inductor for a particular output voltage is

$$L = \frac{1.2 \times V_{OUT}}{0.478 \times f_{SW}}$$

See the Applications Information section for details regarding choosing an appropriate inductor value.

Cycle to cycle operation of the PWM mode begins with the falling edge of the internal clock. Note that when using an external clock, the rising edge synchronizes the regulator and the falling edge is determined by the internal clock, typically a 25 ns pulse width. The falling edge of the clock starts the cycle by turning on the high-side switch, which produces a positive di/dt current in the inductor. The PWM comparator controls when the high-side switch turns off. The positive input of the comparator monitors the peak inductor current via the SW node.

The negative side of the comparator input voltage is set by the voltage control loop minus the slope compensation. When the high-side switch turns off, the low-side switch turns on for the remainder of the clock period.

While in PWM/PSM mode, the low-side switch turns off when the inductor current reaches zero, operating in discontinuous conduction (DCC) mode. If SYNC is tied high to force the device into PWM only mode, the low-side switch stays on until the next clock cycle or until the inductor current reaches the negative current limit.

PSM OPERATION

The ADP2370/ADP2371 smoothly transition to the variable frequency PSM operation. The ADP2370/ADP2371 select a minimum current value, I_{MIN} , for the peak current of the inductor based on the input and output voltages. The design of the I_{MIN} value is based on the recommended inductor values. Deviating from the recommended inductor value for a particular output voltage results in shifting the PSM to PWM threshold and could result in the device entering DCC mode.

As long as the required peak inductor current is above I_{MIN} , the regulator remains in PWM mode. As the load decreases, the PSM circuitry prevents the peak inductor current from dropping below the PSM peak current value. This circuitry causes the regulator to supply more current to the output filter than the load requires, resulting in the output voltage increasing and the output of the internal compensation node of the error amplifier, V_{COMP} , decreasing.

When the FB pin voltage rises above 1% of the nominal output voltage and the V_{COMP} node voltage is below a predetermined PSM threshold voltage level, the regulator enters sleep mode. While in sleep mode, the high-side and low-side switches and a majority of the circuitry are disabled to allow for a low sleep mode quiescent current as well as high efficiency performance.

During sleep mode, the output voltage decreases as the output capacitor discharges into the load. Fixed frequency operation starts when the FB voltage reaches the nominal output voltage. When the load requirement increases past the I_{MIN} peak current level, the V_{COMP} node rises and the PWM control loop sets the duty cycle. While the part is entering and exiting sleep mode, the PSM voltage ripple is larger than 1% because of the delay in the comparators.

Figure 72 and Figure 73 illustrate how the output voltage and inductor current change with loads and transitions in and out of PSM operation. The output voltage ripple in PSM is ~ 40 mV p-p, and the ripple in PWM is < 10 mV p-p.

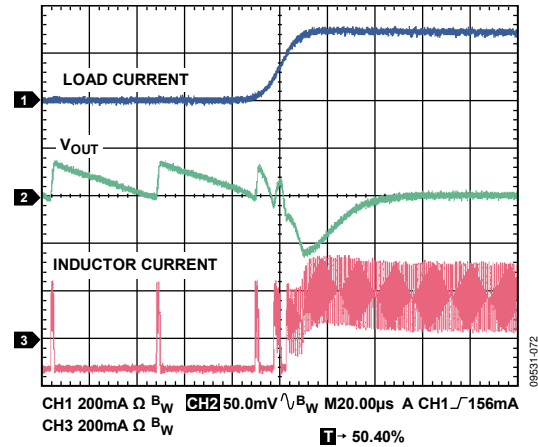


Figure 72. PSM to PWM Transition Waveforms, $V_{OUT} = 1.8$ V, 10 mA Load to 300 mA Load

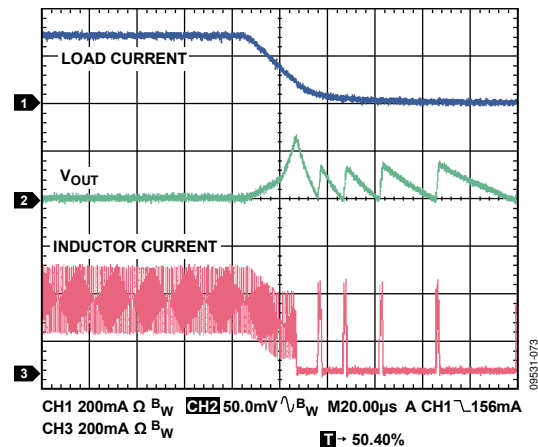


Figure 73. PWM to PSM Transition Waveforms, $V_{OUT} = 1.8$ V, 300 mA Load to 10 mA Load

FEATURES DESCRIPTIONS

PRECISION ENABLE

The enable circuit of the [ADP2370/ADP2371](#) minimizes the input current during shutdown and simultaneously provides an accurate enable threshold. When the enable input voltage is below 400 mV, the regulators are in shutdown mode and the supply current is typically 1.2 μ A. As the enable input voltage rises above the standby enable threshold of 1.0 V, the internal bias currents and voltages are activated, turning on the precision enable circuitry. This allows the precision enable circuitry to detect accurately when the EN pin voltage exceeds the precision enable rising threshold of 1.2 V.

FORCED PWM OR PWM/PSM SELECTION

Connecting the SYNC pin to a voltage greater than 1.2 V forces the device to operate permanently in the PWM mode. This means that the [ADP2370/ADP2371](#) continue to operate at a fixed frequency even when the output current is less than the PWM/PSM threshold. In PWM mode, the efficiency is lower compared to the PSM mode during light loads. The low-side NMOS remains on when the output current drops to less than zero thereby preventing the device from entering discontinuous conduction (DCC) mode.

It is possible to switch from FPWM mode to the power-save mode during operation by pulling the SYNC pin low. The flexible configuration of the SYNC pin during operation of the device allows for efficient power management.

Connecting the SYNC pin to a voltage less than 0.4 V allows the part to operate in either PWM or PSM modes, depending on the output current. Whenever the average output current goes below the PWM/PSM threshold, the [ADP2370/ADP2371](#) enter PSM mode operation. During PSM mode the part operates with reduced switching frequency and with a minimal quiescent current to maintain high efficiency. The low-side NMOS turns off when the output current reaches zero, causing the part to operate in DCC mode.

QUICK OUTPUT DISCHARGE (QOD) FUNCTION

The [ADP2371](#) includes an output discharge resistor that forces the output voltage to zero when the buck is disabled. This ensures that the output of the buck is always in a well-defined state, whether or not it is enabled. The [ADP2370](#) does not include this output discharge function.

SHORT-CIRCUIT PROTECTION

The [ADP2370/ADP2371](#) include frequency foldback to prevent output current runaway on a hard short. When the voltage at the feedback pin falls below 0.3 V, indicating the possibility of a hard short at the output, the switching frequency is reduced to 1/4 of the internal oscillator frequency. The reduction in the switching frequency gives more time for the inductor to discharge, preventing a runaway of output current.

UNDERVOLTAGE LOCKOUT

To protect against battery discharge, an undervoltage lockout (UVLO) circuit is incorporated into the [ADP2370/ADP2371](#). When the input voltage drops below the UVLO threshold, the [ADP2370/ADP2371](#) shuts down, and both the power switch and synchronous rectifier turn off. Once the input voltage rises above the UVLO threshold, the soft start period is initiated and the device is enabled.

THERMAL PROTECTION

In the event that the junction temperature on either the [ADP2370](#) or [ADP2371](#) rises above 150°C, the thermal shutdown protection circuit turns off the regulator. Extreme junction temperature can be the result of high current operation, poor circuit board design, and/or high ambient temperature. A 20°C hysteresis is included in the protection circuit so that when a thermal shutdown occurs, the device does not return to operation until the on-chip temperature drops below 130°C. When exiting a thermal shutdown, soft start is initiated.

SOFT START

The [ADP2370/ADP2371](#) have an internal soft start function that ramps the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the converter. Typical soft start time is 350 μ s. The [ADP2370/ADP2371](#) are also capable of starting up into a precharged output capacitor. If soft start is invoked when the output capacitor charge is greater than zero, the device delays the start of switching until the internal soft start ramp reaches the corresponding FB voltage. This feature prevents discharging the output capacitor at the beginning of soft start.

CURRENT LIMIT

The [ADP2370/ADP2371](#) have protection circuitry that limits the direction and amount of current to 1200 mA that flows through the power switch and synchronous rectifier, cycle by cycle. The positive current limit on the power switch limits the amount of current that can flow from the input to the output. The negative current limit on the synchronous rectifier prevents the inductor current from reversing direction and flowing out of the load.

A negative current limit is provided by the [ADP2370/ADP2371](#) to prevent an excessive reverse inductor current when the switching section sinks current from the load in forced continuous conduction mode. Under negative current-limit conditions, both the high-side and low-side switches are disabled.

100% DUTY CYCLE

The ADP2370/ADP2371 enter and exit 100% duty cycle smoothly. The control loop seeks the next clock cycle while the high-side switch is engaged. When this occurs, the clock signal is masked and the PMOS remains on. When the input voltage increases, the internal V_{COMP} node decreases its signal to the control loop; thus, the device stops skipping clock cycles and exits 100% duty cycle.

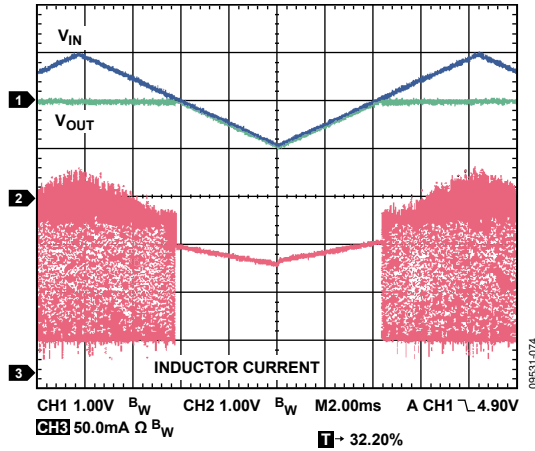


Figure 74. Transition into and out of Dropout in PSM Mode, $V_{OUT} = 5V$, 100 mA Load

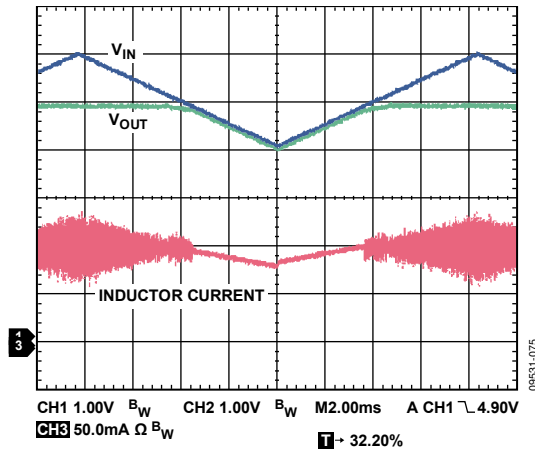


Figure 75. Transition into and out of Dropout in PWM Mode, $V_{OUT} = 5V$, 100 mA Load

SYNCHRONIZING

It is possible to synchronize the ADP2370/ADP2371 to an external clock within a frequency range from 400 kHz to 1.6 MHz. The device automatically detects the rising edge of the first clock and synchronizes to the external clock. When the clock signal stops, the device automatically switches back to the internal clock and continues operating.

The switchover is initiated when no rising edge on the SYNC pin can be detected on the internal clock for a duration of four clock cycles. Therefore, the maximum delay time can be $6.7 \mu s$ if the internal clock is running at its minimum frequency of 600 kHz. During this time, there is no clock signal available. The output stops switching until the ADP2370 circuitry switches to the internal clock signal.

If the device is synchronized to an external clock, the PSM mode is disabled and the device stays in forced PWM mode. Connect FSEL to ground when synchronizing to a frequency range from 400 kHz to 800 kHz, and connect FSEL to the input voltage when the external frequency is in the range of 800 kHz to 1600 kHz. FSEL has an internal pull-down resistor and defaults to the 600 kHz mode when FSEL is unconnected.

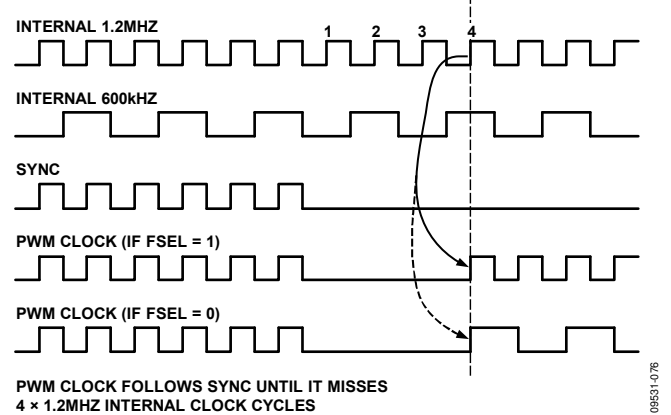


Figure 76. Typical SYNC Timing

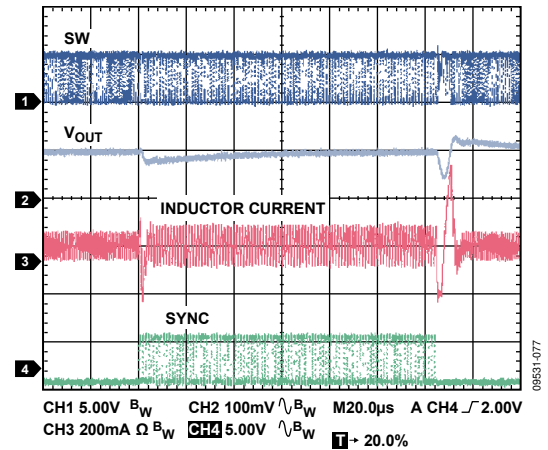


Figure 77. Typical SYNC Transient, 1.2 MHz to 800 kHz to 1.2 MHz

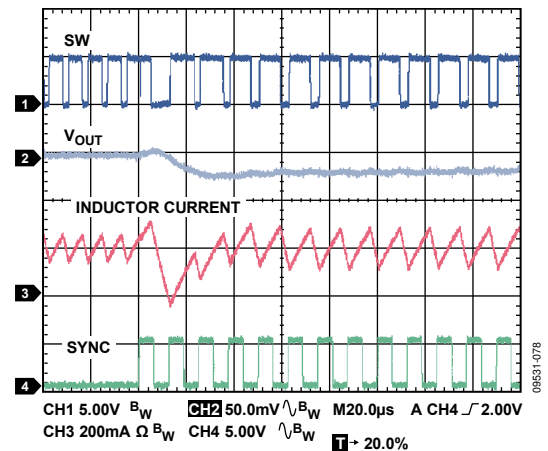


Figure 78. SYNC Transient 1.2 MHz to 800 kHz

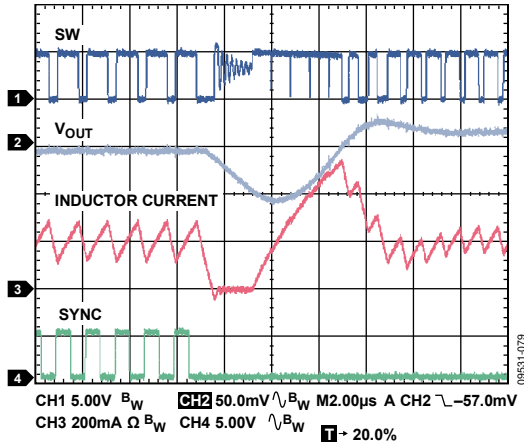


Figure 79. SYNC Transient 800 kHz to 1.2 MHz

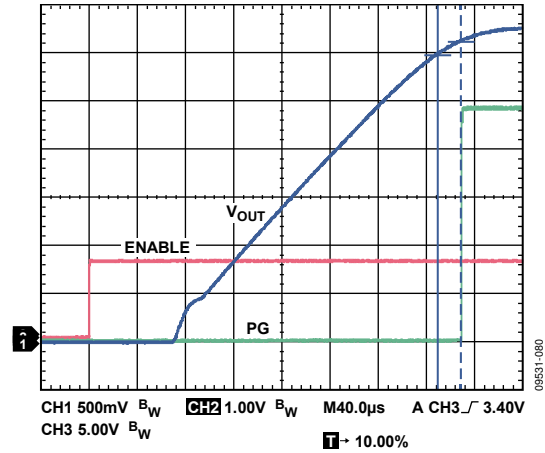


Figure 80. Typical PG Timing at Startup

POWER GOOD

The ADP2370/ADP2371 power-good (PG) output indicates the state of the monitored output voltage. The PG function is an active high, open-drain output, requiring an external pull-up resistor that is typically supplied from the I/O supply rail, as shown in Figure 1.

When the sensed output voltage is below 87% of its nominal value, the PG pin is held low. When the sensed output voltage rises above 92% of the nominal level, the PG line is pulled high after t_{RESET} . The PG pin remains high when the sensed output voltage is above 92% of the nominal output voltage level.

The typical PG delay when the buck is in PWM mode is 20 μ s. Figure 80 shows the typical PG operation during startup. Figure 81 shows the PG operation when there is a large load transient that causes the output voltage to fall just below the PG threshold.

When not using the PG function, remove the pull-up resistor and leave the PG pin either open or shorted to ground.

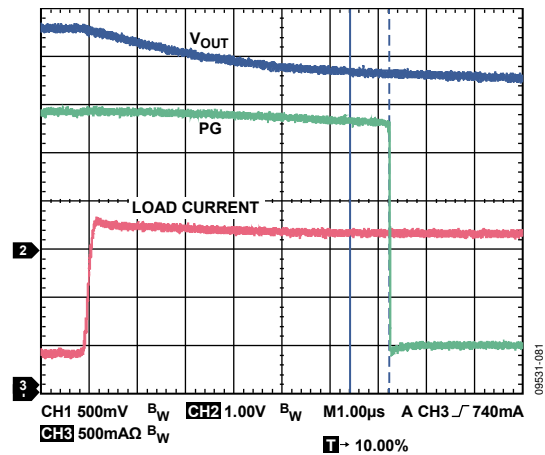


Figure 81. Typical PG Timing with 200 mA to 1100 mA Load Transient

APPLICATIONS INFORMATION

ADIsimPower DESIGN TOOL

ADP2370/ADP2371 are supported by the ADIsimPower™ design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about, and to obtain ADIsimPower design tools, visit www.analog.com/ADIsimPower. Users can also request an unpopulated board through the ADIsimPower tool.

EXTERNAL COMPONENT SELECTION

Table 6 and Table 7 list external component selections for the ADP2370/ADP2371 application circuit shown in Figure 82. The selection of components is dependent on the input voltage, output voltage, and load current requirements. Additionally, trade-offs among performance parameters, such as efficiency and transient response, are made by varying the choice of external components.

SELECTING THE INDUCTOR

The high frequency switching of the ADP2370/ADP2371 allows for the use of small surface-mount power inductors. The inductor value affects the transition from PWM to PSM, efficiency, output ripple, and current-limit values. Use the following equation to calculate the ideal inductance, which is derived from the inductor current slope compensation, for a given output voltage and switching frequency:

$$L = \frac{1.2 \times V_{OUT}}{0.478 \times f_{SW}}$$

The ripple current is calculated as follows:

$$\Delta I_L = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where:

f_{SW} is the switching frequency in MHz (1.2 MHz typical).

L is the inductor value in μH .

The dc resistance (DCR) value of the selected inductor affects efficiency; however, a decrease in this value typically means an increase in root mean square (rms) losses in the core and skin. A minimum requirement of the dc current rating of the inductor is for it to be equal to the maximum load current plus half of the inductor current ripple, as shown by the following equation:

$$I_{PK} = I_{LOAD(MAX)} + \left(\frac{\Delta I_L}{2}\right)$$

OUTPUT CAPACITOR

Output capacitance is required to minimize the voltage overshoot, voltage undershoot, and the ripple voltage present on the output. Capacitors with low equivalent series resistance (ESR) values produce the lowest output ripple; therefore, use capacitors such as the X5R dielectric. Do not use Y5V and Z5U capacitors. Y5V and Z5U capacitors are unsuitable choices because of their large capacitance variation over temperature and their dc bias voltage changes. Because ESR is important, select the capacitor using the following equation:

$$ESR_{COUT} \leq \frac{V_{RIPPLE}}{\Delta I_L}$$

where:

ESR_{COUT} is the ESR of the chosen capacitor.

V_{RIPPLE} is the peak-to-peak output voltage ripple.

Use the following equations to determine the output capacitance:

$$C_{OUT} \geq \frac{V_{IN}}{(2\pi \times f_{SW}) \times 2 \times L \times V_{RIPPLE}}$$

$$C_{OUT} \geq \frac{\Delta I_L}{8 \times f_{SW} \times V_{RIPPLE}}$$

Increasing the output capacitor value has no effect on stability and may reduce output ripple and enhance load transient response. When choosing the output capacitor value, it is important to account for the loss of capacitance due to output voltage dc bias.

INPUT CAPACITOR

An input capacitor is required to reduce input voltage ripple, input ripple current, and source impedance. Place the input capacitor as close as possible to the VIN pin. A low ESR X7R- or X5R-type capacitor is highly recommended to minimize the input voltage ripple. Use the following equation to determine the rms input current:

$$I_{CIN} \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

$$I_{rms} \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

ADJUSTABLE OUTPUT VOLTAGE PROGRAMMING

The ADP2370/ADP2371 feature an adjustable output voltage range from 0.8 V to 12 V. The output voltage is set by the ratio of two external resistors, R2 and R3, as shown in Figure 83. The device servos the output to maintain the voltage at the FB pin at 0.8 V, referenced to ground; the current in R2 is then equal to 0.8 V/R3 plus the FB pin bias current. The bias current of the FB pin, 10 nA at 25°C, flows through R2 into the FB pin.

The output voltage is calculated using the equation

$$V_{OUT} = 0.8 \text{ V} (1 + R2/R3) + (FB_{I-BIAS})(R2)$$