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8-Bit Programmable 2- to 4-Phase Synchronous Buck Controller

ADP3192A

FEATURES

- Selectable 2-, 3-, or 4-phase operation at up to 1 MHz per phase
- ±7.7 mV worst-case differential sensing error over temperature
- Logic-level PWM outputs for interface to external high power drivers
- Fast enhanced PWM (FEPWM) flex mode for excellent load transient performance
- Active current balancing between all output phases
- Built-in power-good/crowbar blanking supports on-the-fly VID code changes
- Digitally programmable 0.5 V to 1.6 V output supports both VR10.x and VR11 specifications
- Programmable short-circuit protection with programmable latch-off delay

APPLICATIONS

- Desktop PC power supplies for next generation Intel® processors
- VRM modules

FUNCTIONAL BLOCK DIAGRAM

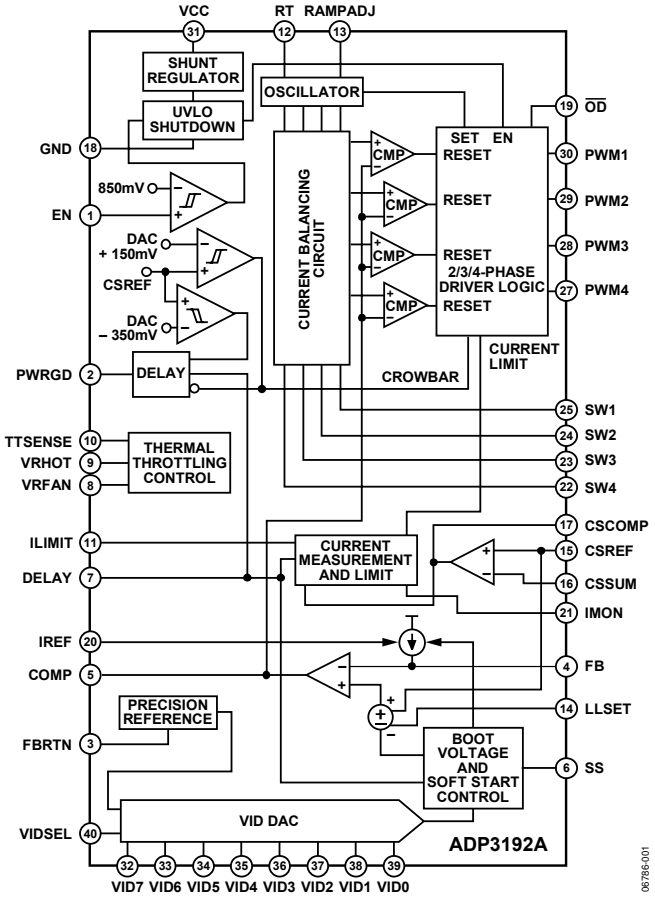

Figure 1.

GENERAL DESCRIPTION

The ADP3192A[1] is a highly efficient, multiphase, synchronous buck-switching regulator controller optimized for converting a 12 V main supply into the core supply voltage required by high performance Intel processors. It uses an internal 8-bit DAC to read a voltage identification (VID) code directly from the processor, which is used to set the output voltage between 0.5 V and 1.6 V.

This device uses a multimode PWM architecture to drive the logic-level outputs at a programmable switching frequency that can be optimized for VR size and efficiency. The phase relationship of the output signals can be programmed to provide 2-, 3-, or 4-phase operation, allowing for the construction of up to four complementary buck-switching stages.

The ADP3192A also includes programmable no load offset and slope functions to adjust the output voltage as a function of the load current, optimally positioning it for a system transient. In addition, the ADP3192A provides accurate and reliable short-circuit protection, adjustable current limiting, and a delayed power-good output that accommodates on-the-fly output voltage changes requested by the CPU.

The ADP3192A has a built-in shunt regulator that allows the part to be connected to the 12 V system supply through a series resistor.

The ADP3192A is specified over the extended commercial temperature range of 0°C to 85°C and is available in a 40-lead LFCSP.

[1] Protected by U.S. Patent Number 6,683,441; other patents pending.

Rev. 0

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REVISION HISTORY

5/07—Revision 0: Initial Version

SPECIFICATIONS

VCC = 5 V, FBRTN = GND, T_A = 0°C to 85°C, unless otherwise noted.[1]

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
REFERENCE CURRENT						
Reference Bias Voltage	V_{IREF}			1.5		V
Reference Bias Current	I_{IREF}	R_{IREF} = 100 kΩ	14.25	15	15.75	µA
ERROR AMPLIFIER						
Output Voltage Range[2]	V_{COMP}		0		4.4	V
Accuracy	V_{FB}	Relative to nominal DAC output, referenced to FBRTN, LLSET = CSREF (see Figure 2)	−7.7		+7.7	mV
	$V_{FB(BOOT)}$	In startup	1.092	1.1	1.108	V
Load Line Positioning Accuracy		CSREF − LLSET = 80 mV	−78	−80	−82	mV
Differential Nonlinearity			−1		+1	LSB
Input Bias Current	I_{FB}	$I_{FB} = I_{IREF}$	13.5	15	16.5	µA
FBRTN Current	I_{FBRTN}			65	200	µA
Output Current	I_{COMP}	FB forced to V_{OUT} − 3%		500		µA
Gain Bandwidth Product	$GBW_{(ERR)}$	COMP = FB		20		MHz
Slew Rate		COMP = FB		25		V/µs
LLSET Input Voltage Range	V_{LLSET}	Relative to CSREF	−250		+250	mV
LLSET Input Bias Current	I_{LLSET}		−10		+10	nA
Boot Voltage Hold Time	t_{BOOT}	C_{DELAY} = 10 nF		2		ms
VID INPUTS						
Input Low Voltage	$V_{IL(VID)}$	VID(X), VIDSEL			0.4	V
Input High Voltage	$V_{IH(VID)}$	VID(X), VIDSEL	0.8			V
Input Current	$I_{IN(VID)}$			−1		µA
VID Transition Delay Time[2]		VID code change to FB change	400			ns
No CPU Detection Turn-Off Delay Time[2]		VID code change to PWM going low	5			µs
OSCILLATOR						
Frequency Range[2]	f_{OSC}		0.25		4	MHz
Frequency Variation	f_{PHASE}	T_A = 25°C, R_T = 205 kΩ, 4-phase	180	200	220	kHz
		T_A = 25°C, R_T = 118 kΩ, 4-phase		400		kHz
		T_A = 25°C, R_T = 55 kΩ, 4-phase		800		kHz
Output Voltage	V_{RT}	R_T = 205 kΩ to GND	1.9	2.0	2.1	V
RAMPADJ Output Voltage	$V_{RAMPADJ}$	RAMPADJ − FB	−50		+50	mV
RAMPADJ Input Current Range	$I_{RAMPADJ}$		1		50	µA
CURRENT SENSE AMPLIFIER						
Offset Voltage	$V_{OS(CSA)}$	CSSUM − CSREF (see Figure 3)	−1.0		+1.0	mV
Input Bias Current	$I_{BIAS(CSSUM)}$		−10		+10	nA
Gain Bandwidth Product	$GBW_{(CSA)}$	CSSUM = CSCOMP		10		MHz
Slew Rate		C_{CSCOMP} = 10 pF		10		V/µs
Input Common-Mode Range		CSSUM and CSREF	0		3.5	V
Output Voltage Range			0.05		3.5	V
Output Current	I_{CSCOMP}			500		µA
Current Limit Latch-Off Delay Time	$t_{OC(DELAY)}$	C_{DELAY} = 10 nF		8		ms
IMON Output	IMON	10 × (CSREF − CSCOMP) > 50 mV	−6		+6	%
CURRENT BALANCE AMPLIFIER						
Common-Mode Range	$V_{SW(X)CM}$		−600		+200	mV
Input Resistance	$R_{SW(X)}$	SW(X) = 0 V	10	17	26	kΩ
Input Current	$I_{SW(X)}$	SW(X) = 0 V	8	12	20	µA
Input Current Matching	$\Delta I_{SW(X)}$	SW(X) = 0 V	−4		+4	%
CURRENT-LIMIT COMPARATOR						
ILIMIT Bias Current	I_{ILIMIT}	$I_{ILIMIT} = 2/3 \times I_{IREF}$	9	10	11	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ILIMIT Voltage	V_{ILIMIT}	R_{ILIMIT} = 121 kΩ (V_{ILIMIT} = (I_{ILIMIT} × R_{ILIMIT}))	1.09	1.21	1.33	V
Maximum Output Voltage			3			V
Current-Limit Threshold Voltage	V_{CL}	V_{CSREF} − V_{CSCOMP}, R_{ILIMIT} = 121 kΩ	80	100	125	mV
Current-Limit Setting Ratio		V_{CL}/V_{ILIMIT}		82.6		mV/V
DELAY TIMER						
Normal Mode Output Current	I_{DELAY}	I_{DELAY} = I_{IREF}	12	15	18	µA
Output Current in Current Limit	$I_{DELAY(CL)}$	$I_{DELAY(CL)}$ = 0.25 × I_{IREF}	3.0	3.75	4.5	µA
Threshold Voltage	$V_{DELAY(TH)}$		1.6	1.7	1.8	V
SOFT START						
Output Current	I_{SS}	During startup, I_{SS} = I_{IREF}	12	15	18	µA
ENABLE INPUT						
Threshold Voltage	$V_{TH(EN)}$		800	850	900	mV
Hysteresis	$V_{HYS(EN)}$		80	100	125	mV
Input Current	$I_{IN(EN)}$			−1		µA
Delay Time	$t_{DELAY(EN)}$	EN > 950 mV, C_{DELAY} = 10 nF		2		ms
$\overline{OD}$ OUTPUT						
Output Low Voltage	$V_{OL(\overline{OD})}$			160	500	mV
Output High Voltage	$V_{OH(\overline{OD})}$		4	5		V
$\overline{OD}$ Pull-Down Resistor				60		kΩ
THERMAL THROTTLING CONTROL						
TTSENSE Voltage Range		Internally limited	0		5	V
TTSENSE Bias Current			−133	−123	−113	µA
TTSENSE VRFAN Threshold Voltage			1.06	1.105	1.15	V
TTSENSE VRHOT Threshold Voltage			765	810	855	mV
TTSENSE Hysteresis				50		mV
VRFAN Output Low Voltage	$V_{OL(VRFAN)}$	$I_{VRFAN(SINK)}$ = −4 mA		150	300	mV
VRHOT Output Low Voltage	$V_{OL(VRHOT)}$	$I_{VRHOT(SINK)}$ = −4 mA		150	300	mV
POWER-GOOD COMPARATOR						
Undervoltage Threshold	$V_{PWRGD(UV)}$	Relative to nominal DAC output	−400	−350	−300	mV
Overvoltage Threshold	$V_{PWRGD(OV)}$	Relative to nominal DAC output	100	150	200	mV
Output Low Voltage	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = −4 mA		150	300	mV
Power-Good Delay Time						
During Soft Start[2]		C_{DELAY} = 10 nF		2		ms
VID Code Changing			100	250		µs
VID Code Static				200		ns
Crowbar Trip Point	$V_{CROWBAR}$	Relative to nominal DAC output	100	150	200	mV
Crowbar Reset Point		Relative to FBRTN	320	375	430	mV
Crowbar Delay Time	$t_{CROWBAR}$	Overvoltage to PWM going low				
VID Code Changing			100	250		µs
VID Code Static				400		ns
PWM OUTPUTS						
Output Low Voltage	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = −400 µA		160	500	mV
Output High Voltage	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ = 400 µA	4.0	5		V
SUPPLY		V_{SYSTEM} = 12 V, R_{SHUNT} = 340 Ω (see Figure 2)				
VCC[2]	VCC		4.65	5	5.55	V
DC Supply Current	I_{VCC}	V_{SYSTEM} = 13.2 V, R_{SHUNT} = 340 Ω			25	mA
UVLO Turn-On Current				6.5	11	mA
UVLO Threshold Voltage	V_{UVLO}	VCC rising	9			V
UVLO Turn-Off Voltage		VCC falling		4.1		V

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
[2] Guaranteed by design or bench characterization, not tested in production.

TEST CIRCUITS

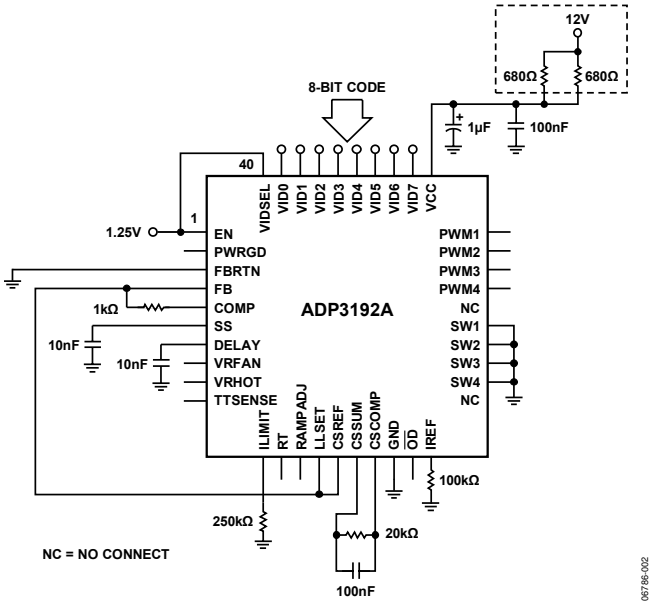

Figure 2. Closed-Loop Output Voltage Accuracy

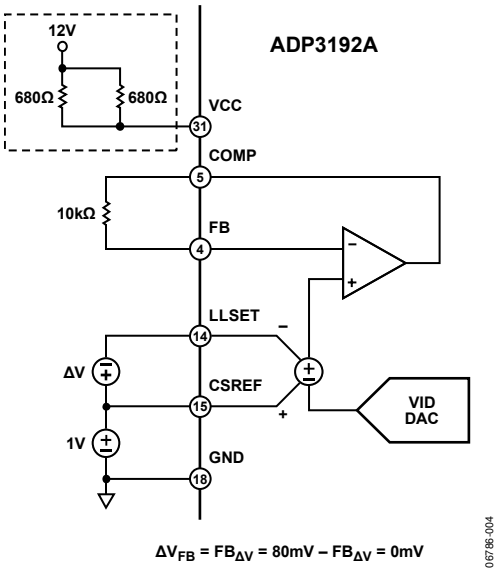

Figure 4. Positioning Voltage

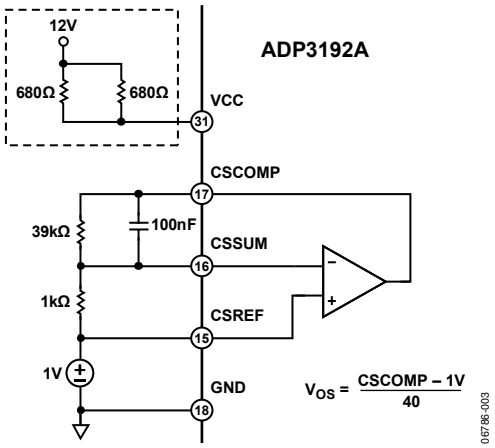

Figure 3. Current Sense Amplifier V_{OS}

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC	−0.3 V to +6 V
FBRTN	−0.3 V to +0.3 V
PWM3 to PWM4, RAMPADJ	−0.3 V to VCC + 0.3 V
SW1 to SW4	−5 V to +25 V
<200 ns	−10 V to +25 V
All Other Inputs and Outputs	−0.3 V to VCC + 0.3 V
Storage Temperature Range	−65°C to +150°C
Operating Ambient Temperature Range	0°C to 85°C
Operating Junction Temperature	125°C
Thermal Impedance (θ_{JA})	39°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Infrared (15 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages referenced to GND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

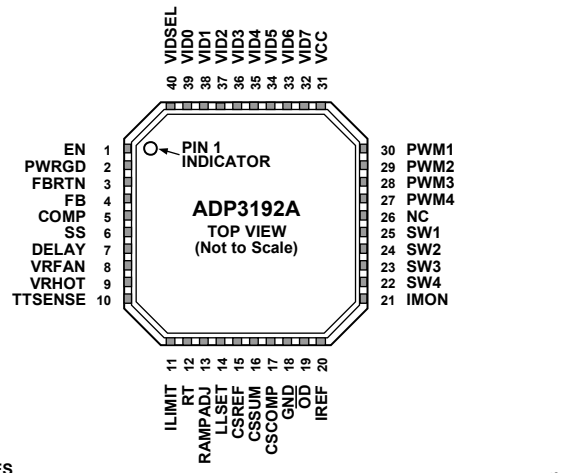

Figure 5. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low.
2	PWRGD	Power-Good Output. Open-drain output that signals when the output voltage is outside of the proper operating range.
3	FBRTN	Feedback Return. VID DAC and error amplifier reference for remote sensing of the output voltage.
4	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage. An external resistor between this pin and the output voltage sets the no load offset point.
5	COMP	Error Amplifier Output and Compensation Point.
6	SS	Soft Start Delay Setting Input. An external capacitor connected between this pin and GND sets the soft start ramp-up time.
7	DELAY	Delay Timer Setting Input. An external capacitor connected between this pin and GND sets the overcurrent latch-off delay time, boot voltage hold time, EN delay time, and PWRGD delay time.
8	VRFAN	VR Fan Activation Output. Open-drain output that signals when the temperature at the monitoring point connected to TTSENSE exceeds the programmed VRFAN temperature threshold.
9	VRHOT	VR Hot Output. Open-drain output that signals when the temperature at the monitoring point connected to TTSENSE exceeds the programmed VRHOT temperature threshold.
10	TTSENSE	VR Hot Thermal Throttling Sense Input. An NTC thermistor between this pin and GND is used to remotely sense the temperature at the desired thermal monitoring point.
11	ILIMIT	Current-Limit Setpoint. An external resistor from this pin to GND sets the current-limit threshold of the converter.
12	RT	Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device.
13	RAMPADJ	PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp.
14	LLSET	Output Load Line Programming Input. This pin can be directly connected to CSCOMP, or it can be connected to the center point of a resistor divider between CSCOMP and CSREF. Connecting LLSET to CSREF disables positioning.
15	CSREF	Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier and the power-good and crowbar functions. This pin should be connected to the common point of the output inductors.
16	CSSUM	Current Sense Summing Node. External resistors from each switch node to this pin sum the average inductor currents together to measure the total output current.
17	CSCOMP	Current Sense Compensation Point. A resistor and capacitor from this pin to CSSUM determines the gain of the current sense amplifier and the positioning loop response time.
18	GND	Ground. All internal biasing and the logic output signals of the device are referenced to this ground.

Pin No.	Mnemonic	Description
19	$\overline{OD}$	Output Disable Logic Output. This pin is actively pulled low when the EN input is low or when VCC is below its UVLO threshold to signal to the driver IC that the driver high-side and low-side outputs should go low.
20	IREF	Current Reference Input. An external resistor from this pin to ground sets the reference current for I_{FB}, I_{DELAY}, I_{SS}, I_{ILIMIT}, and $I_{TTSENSE}$.
21	IMON	Analog Output. Represents the total load current.
22 to 25	SW4 to SW1	Current Balance Inputs. Inputs for measuring the current level in each phase. The SW pins of unused phases should be left open.
26	NC	No Connection.
27 to 30	PWM4 to PWM1	Logic-Level PWM Outputs. Each output is connected to the input of an external MOSFET driver such as the ADP3120A. Connecting the PWM4 and PWM3 outputs to VCC causes that phase to turn off, allowing the ADP3192A to operate as a 2-, 3-, or 4-phase controller.
31	VCC	Supply Voltage for the Device. A 340 Ω resistor should be placed between the 12 V system supply and the VCC pin. The internal shunt regulator maintains VCC = 5 V.
32 to 39	VID7 to VID0	Voltage Identification DAC Inputs. These eight pins are pulled down to GND, providing a Logic 0 if left open. When in normal operation mode, the DAC output programs the FB regulation voltage from 0.5 V to 1.6 V (see Table 4).
40	VIDSEL	VID DAC Selection Pin. The logic state of this pin determines whether the internal VID DAC decodes VID0 to VID7 as extended VR10 or VR11 inputs.

TYPICAL PERFORMANCE CHARACTERISTICS

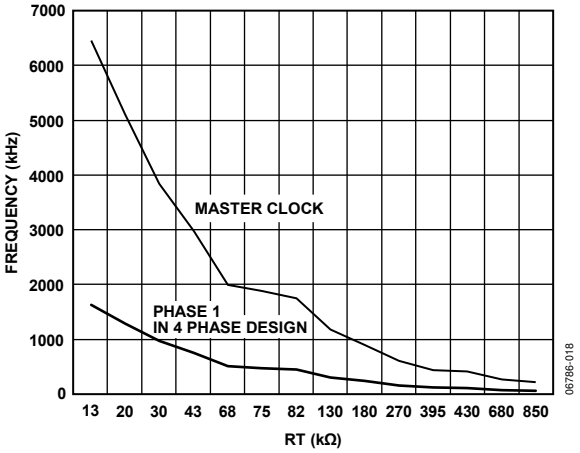

Figure 6. Master Clock Frequency vs. RT

THEORY OF OPERATION

The ADP3192A combines a multimode, fixed frequency, PWM control with multiphase logic outputs for use in 2-, 3-, and 4-phase synchronous buck CPU core supply power converters. The internal VID DAC is designed to interface with the Intel 8-bit VRD/VRM 11-compatible CPU and 7-bit VRD/VRM 10×-compatible CPU. Multiphase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling the high currents in a single-phase converter places high thermal demands on the components in the system, such as the inductors and MOSFETs.

The multimode control of the ADP3192A ensures a stable, high performance topology for the following:

- Balancing currents and thermals between phases
- High speed response at the lowest possible switching frequency and output decoupling
- Minimizing thermal switching losses by using lower frequency operation
- Tight load line regulation and accuracy
- High current output due to 4-phase operation
- Reduced output ripple due to multiphase cancellation
- PC board layout noise immunity
- Ease of use and design due to independent component selection
- Flexibility in operation for tailoring design to low cost or high performance

START-UP SEQUENCE

The ADP3192A follows the VR11 start-up sequence shown in Figure 7. After both the EN and UVLO conditions are met, the DELAY pin goes through one cycle (TD1). The first four clock cycles of TD2 are blanked from the PWM outputs and used for phase detection as explained in the Phase Detection Sequence section. Then, the soft start ramp is enabled (TD2), and the output comes up to the boot voltage of 1.1 V. The boot hold time is determined by the DELAY pin as it goes through a second cycle (TD3). During TD3, the processor VID pins settle to the required VID code. When TD3 is over, the ADP3192A soft starts either up or down to the final VID voltage (TD4). After TD4 is complete and the PWRGD masking time (equal to VID on-the-fly masking) is complete, a third ramp on the DELAY pin sets the PWRGD blanking (TD5).

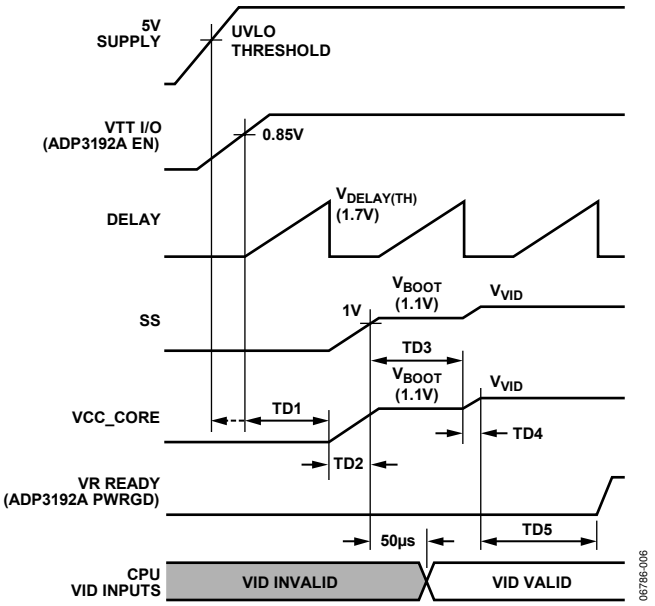

Figure 7. System Start-Up Sequence

PHASE DETECTION SEQUENCE

During startup, the number of operational phases and their phase relationship is determined by the internal circuitry that monitors the PWM outputs. Normally, the ADP3192A operates as a 4-phase PWM controller. Connecting the PWM4 pin to VCC programs 3-phase operation and connecting the PWM4 and PWM3 pins to VCC programs 2-phase operation.

Prior to soft start, while EN is low, the PWM3 and PWM4 pins sink approximately 100 µA. An internal comparator checks each pin's voltage vs. a threshold of 3 V. If the pin is tied to VCC, it is above the threshold. Otherwise, an internal current sink pulls the pin to GND, which is below the threshold. PWM1 and PWM2 are low during the phase detection interval that occurs during the first four clock cycles of TD2. After this time, if the remaining PWM outputs are not pulled to VCC, the 100 µA current sink is removed, and they function as normal PWM outputs. If they are pulled to VCC, the 100 µA current source is removed, and the outputs are put into a high impedance state.

The PWM outputs are logic-level devices intended for driving external gate drivers such as the ADP3120A. Because each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one output can be on at the same time to allow overlapping phases.

MASTER CLOCK FREQUENCY

The clock frequency of the ADP3192A is set with an external resistor connected from the RT pin to GND. The frequency follows the graph in Figure 6. To determine the frequency per phase, the clock is divided by the number of phases in use. If all phases are in use, divide by 4. If PWM4 is tied to VCC, divide the master clock by 3 for the frequency of the remaining phases. If PWM3 and PWM4 are tied to VCC, divide by 2.

OUTPUT VOLTAGE DIFFERENTIAL SENSING

The ADP3192A combines differential sensing with a high accuracy VID DAC and reference, and a low offset error amplifier. This maintains a worst-case specification of ±7.7 mV differential sensing error over its full operating output voltage and temperature range. The output voltage is sensed between the FB pin and FBRTN pin. FB should be connected through a resistor to the regulation point, usually the remote sense pin of the microprocessor. FBRTN should be connected directly to the remote sense ground point. The internal VID DAC and precision reference are referenced to FBRTN, which has a minimal current of 65 μA to allow accurate remote sensing. The internal error amplifier compares the output of the DAC to the FB pin to regulate the output voltage.

OUTPUT CURRENT SENSING

The ADP3192A provides a dedicated current-sense amplifier (CSA) to monitor the total output current for proper voltage positioning vs. load current and for current-limit detection. Sensing the load current at the output gives the total average current being delivered to the load. This is an inherently more accurate method than peak current detection or sampling the current across a sense element such as the low-side MOSFET. This amplifier can be configured several ways, depending on the objectives of the system, as follows:

- Output inductor DCR sensing without a thermistor for lowest cost
- Output inductor DCR sensing with a thermistor for improved accuracy with tracking of inductor temperature
- Sense resistors for highest accuracy measurements

The positive input of the CSA is connected to the CSREF pin, which is connected to the output voltage. The inputs to the amplifier are summed together through resistors from the sensing element, such as the switch node side of the output inductors, to the inverting input CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the feedback resistor.

An additional resistor divider connected between CSREF and CSCOMP (with the midpoint connected to LLSET) can be used to set the load line required by the microprocessor. The current information is then given as CSREF − LLSET. This difference signal is used internally to offset the VID DAC for voltage positioning. The difference between CSREF and CSCOMP is then used as a differential input for the current-limit comparator. This allows the load line to be set independently of the current-limit threshold. In the event that the current-limit threshold and load line are not independent, the resistor divider between CSREF and CSCOMP can be removed, and the CSCOMP pin can be directly connected to LLSET. To disable voltage positioning entirely (that is, no load line), connect LLSET to CSREF.

To provide the best accuracy for sensing current, the CSA is designed to have a low offset input voltage. Also, the sensing gain is determined by external resistors to make it extremely accurate.

ACTIVE IMPEDANCE CONTROL MODE

For controlling the dynamic output voltage droop as a function of output current, a signal proportional to the total output current at the LLSET pin can be scaled to equal the regulator droop impedance multiplied by the output current. This droop voltage is then used to set the input control voltage to the system. The droop voltage is subtracted from the DAC reference input voltage to tell the error amplifier where the output voltage should be. This allows enhanced feed-forward response.

CURRENT CONTROL MODE AND THERMAL BALANCE

The ADP3192A has individual inputs (SW1 to SW4) for each phase that are used for monitoring the current of each phase. This information is combined with an internal ramp to create a current balancing feedback system that has been optimized for initial current balance accuracy and dynamic thermal balancing during operation. This current balance information is independent of the average output current information used for positioning as described in the Output Current Sensing section.

The magnitude of the internal ramp can be set to optimize the transient response of the system. It also monitors the supply voltage for feed-forward control for changes in the supply. A resistor connected from the power input voltage to the RAMPADJ pin determines the slope of the internal PWM ramp. External resistors can be placed in series with individual phases to create an intentional current imbalance if desired, such as when one phase has better cooling and can support higher currents. Resistor R_{SW1} through Resistor R_{SW4} (see Figure 10) can be used for adjusting thermal balance in this 4-phase example. It is best to have the ability to add these resistors during the initial design; therefore, ensure that placeholders are provided in the layout.

To increase the current in any given phase, enlarge R_{SW} for that phase (make R_{SW} = 0 for the hottest phase and do not change it during balancing). Increasing R_{SW} to only 500 Ω makes a substantial increase in phase current. Increase each R_{SW} value by small amounts to achieve balance, starting with the coolest phase first.

VOLTAGE CONTROL MODE

A high gain, high bandwidth, voltage mode error amplifier is used for the voltage mode control loop. The control input voltage to the positive input is set via the VID logic according to the voltages listed in Table 4.

This voltage is also offset by the droop voltage for active positioning of the output voltage as a function of current, commonly known as active voltage positioning. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (FB) is tied to the output sense location with Resistor R_B and is used for sensing and controlling the output voltage at this point. A current source (equal to IREF) from the FB pin flowing through R_B is used for setting the no load offset voltage from the VID voltage. The no load voltage is negative with respect to the VID DAC. The main loop compensation is incorporated into the feedback network between FB and COMP.

CURRENT REFERENCE

The IREF pin is used to set an internal current reference. This reference current sets I_{FB}, I_{DELAY}, I_{SS}, I_{LIMIT}, and $I_{TTSENSE}$. A resistor to ground programs the current based on the 1.5 V output.

$$IREF = \frac{1.5\,V}{R_{IREF}}$$

Typically, R_{IREF} is set to 100 kΩ to program $IREF$ = 15 μA. The following currents are then equal to

$I_{FB} = IREF = 15\ \mu A$

$I_{DELAY} = IREF = 15\ \mu A$

$I_{SS} = IREF = 15\ \mu A$

$I_{LIMIT} = 2/3\ (IREF) = 10\ \mu A$

FAST ENHANCED PWM MODE

Fast enhanced PWM mode (FEPWM) is intended to improve the transient response of the ADP3192A to a load setup. In previous generations of controllers, when a load step-up occurred, the controller had to wait until the next turn-on of the PWM signal to respond to the load change. Enhanced PWM mode allows the controller to immediately respond when a load step-up occurs. This allows the phases to respond more quickly when a load increase takes place.

DELAY TIMER

The delay times for the start-up timing sequence are set with a capacitor from the DELAY pin to GND. In UVLO, or when EN is logic low, the DELAY pin is held at GND. After the UVLO and EN signals are asserted, the first delay time (TD1 in Figure 7) is initiated. A current flows out of the DELAY pin to charge C_{DLY}. This current is equal to IREF, which is typically 15 μA. A comparator monitors the DELAY voltage with a threshold of 1.7 V. The delay time is therefore set by the IREF current charging a capacitor from 0 V to 1.7 V. This DELAY pin is used for multiple delay timings (TD1, TD3, and TD5) during the start-up sequence. In addition, DELAY is used for timing the current-limit latch off, as explained in the Current-Limit, Short-Circuit, and Latch-Off Protection section.

SOFT START

The soft start times for the output voltage are set with a capacitor from the SS pin to GND. After TD1 and the phase detection cycle are complete, the SS time (TD2 in Figure 7) starts. The SS pin is disconnected from GND, and the capacitor is charged up to the 1.1 V boot voltage by the SS amplifier, which has an output current equal to IREF (typically 15 μA). The voltage at the FB pin follows the ramping voltage on the SS pin, limiting the inrush current during startup. The soft start time depends on the value of the boot voltage and C_{SS}.

Once the SS voltage is within 100 mV of the boot voltage, the boot voltage delay time (TD3 in Figure 7) is started. The end of the boot voltage delay time signals the beginning of the second soft start time (TD4 in Figure 7). The SS voltage now changes from the boot voltage to the programmed VID DAC voltage (either higher or lower) using the SS amplifier with the output current equal to IREF. The voltage of the FB pin follows the ramping voltage of the SS pin, limiting the inrush current during the transition from the boot voltage to the final DAC voltage. The second soft start time depends on the boot voltage, the programmed VID DAC voltage, and C_{SS}.

If EN is taken low or if VCC drops below UVLO, DELAY and SS are reset to ground to be ready for another soft start cycle. Figure 8 shows typical start-up waveforms for the ADP3192A.

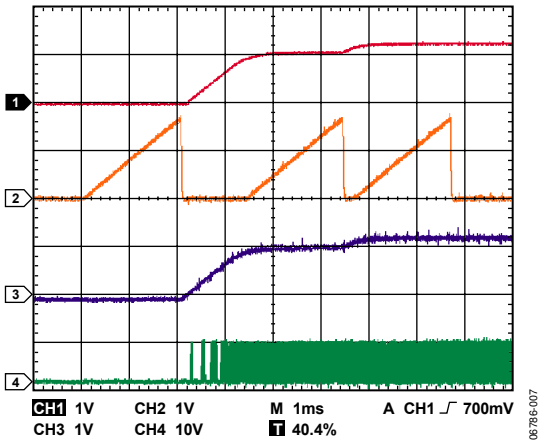

Figure 8. Typical Start-Up Waveforms (Channel 1: CSREF, Channel 2: DELAY, Channel 3: SS, Channel 4: Phase 1 Switch Node)

CURRENT-LIMIT, SHORT-CIRCUIT, AND LATCH-OFF PROTECTION

The ADP3192A compares a programmable current-limit setpoint to the voltage from the output of the current-sense amplifier. The level of current limit is set with the resistor from the ILIMIT pin to GND. During operation, the current from ILIMIT is equal to 2/3 of IREF, giving 10 µA typically. This current through the external resistor sets the ILIMIT voltage, which is internally scaled to give a current-limit threshold of 82.6 mV/V. If the difference in voltage between CSREF and CSCOMP rises above the current-limit threshold, the internal current-limit amplifier controls the internal COMP voltage to maintain the average output current at the limit.

If the limit is reached and TD5 in Figure 7 is complete, a latch-off delay time starts, and the controller shuts down if the fault is not removed. The current-limit delay time shares the DELAY pin timing capacitor with the start-up sequence timing. However, during current limit, the DELAY pin current is reduced to IREF/4. A comparator monitors the DELAY voltage and shuts off the controller when the voltage reaches 1.7 V. Therefore, the current-limit latch-off delay time is set by the current of IREF/4 charging the delay capacitor from 0 V to 1.7 V. This delay is four times longer than the delay time during the start-up sequence.

The current-limit delay time starts only after the TD5 is complete. If there is a current limit during startup, the ADP3192A goes through TD1 to TD5, and then starts the latch-off time. Because the controller continues to cycle the phases during the latch-off delay time, the controller returns to normal operation and the DELAY capacitor is reset to GND if the short is removed before the 1.7 V threshold is reached.

The latch-off function can be reset by either removing and reapplying the supply voltage to the ADP3192A or by toggling the EN pin low for a short time. To disable the short-circuit latch-off function, an external resistor should be placed in parallel with C_{DLY}. This prevents the DELAY capacitor from charging up to the 1.7 V threshold. The addition of this resistor causes a slight increase in the delay times.

During startup, when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot go below GND. This secondary current limit controls the internal COMP voltage to the PWM comparators to 1.5 V. This limits the voltage drop across the low-side MOSFETs through the current balance circuitry. An inherent per-phase current limit protects individual phases if one or more phases stop functioning because of a faulty component. This limit is based on the maximum normal mode COMP voltage. Typical overcurrent latch-off waveforms are shown in Figure 9.

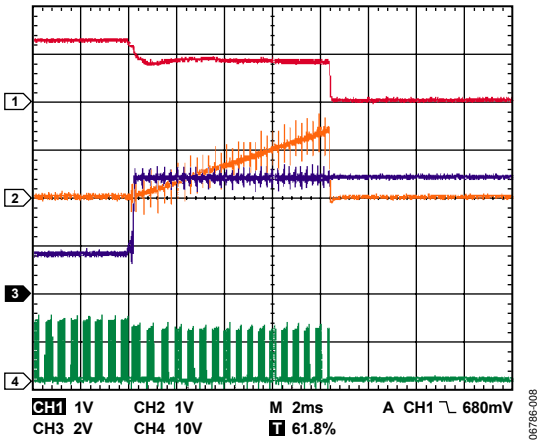

Figure 9. Overcurrent Latch-Off Waveforms (Channel 1: CSREF, Channel 2: DELAY, Channel 3: COMP, Channel 4: Phase 1 Switch Node)

DYNAMIC VID

The ADP3192A has the ability to dynamically change the VID inputs while the controller is running. This allows the output voltage to change while the supply is running and supplying current to the load, which is commonly referred to as VID on-the-fly (OTF). A VID OTF can occur under light or heavy load conditions. The processor signals the controller by changing the VID inputs in multiple steps from the start code to the finish code. This change can be positive or negative.

When a VID input changes state, the ADP3192A detects the change and ignores the DAC inputs for a minimum of 400 ns. This time prevents a false code due to logic skew while the eight VID inputs are changing. Additionally, the first VID change initiates the PWRGD and crowbar blanking functions for a minimum of 100 µs to prevent a false PWRGD or crowbar event. Each VID change resets the internal timer.

POWER-GOOD MONITORING

The power-good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open-drain output whose high level, when connected to a pull-up resistor, indicates that the output voltage is within the specified nominal limits based on the VID voltage setting. PWRGD goes low if the output voltage is outside of this specified range, if the VID DAC inputs are in no CPU mode, or if the EN pin is pulled low. PWRGD is blanked during a VID OTF event for a period of 200 µs to prevent false signals during the time the output is changing.

The PWRGD circuitry also incorporates an initial turn-on delay time (TD5) based on the DELAY timer. Prior to the SS voltage reaching the programmed VID DAC voltage and the PWRGD masking-time finishing, the PWRGD pin is held low. Once the SS pin is within 100 mV of the programmed DAC voltage, the capacitor on the DELAY pin begins to charge. A comparator monitors the DELAY voltage and enables PWRGD when the voltage reaches 1.7 V. The PWRGD delay time is set, therefore, by a current of IREF, charging a capacitor from 0 V to 1.7 V.

OUTPUT CROWBAR

To protect the load and output components of the supply, the PWM outputs are driven low, which turns on the low-side MOSFETs when the output voltage exceeds the upper crowbar threshold. This crowbar action stops once the output voltage falls below the release threshold of approximately 375 mV.

Turning on the low-side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output overvoltage is due to a short in the high-side MOSFET, this action current limits the input supply or blows its fuse, protecting the microprocessor from being destroyed.

OUTPUT ENABLE AND UVLO

For the ADP3192A to begin switching, the input supply (VCC) to the controller must be higher than the UVLO threshold and the EN pin must be higher than its 0.85 V threshold. This initiates a system start-up sequence. If either UVLO or EN is less than their respective thresholds, the ADP3192A is disabled. This holds the PWM outputs at ground, shorts the DELAY capacitor to ground, and forces PWRGD and $\overline{OD}$ signals low.

In the application circuit (see Figure 10), the $\overline{OD}$ pin should be connected to the $\overline{OD}$ inputs of the ADP3120A drivers. Grounding $\overline{OD}$ disables the drivers such that both DRVH and DRVL are grounded. This feature is important in preventing the discharge of the output capacitors when the controller is shut off. If the driver outputs are not disabled, a negative voltage can be generated during output due to the high current discharge of the output capacitors through the inductors.

THERMAL MONITORING

The ADP3192A includes a thermal monitoring circuit to detect when a point on the VR has exceeded two different user-defined temperatures. The thermal monitoring circuit requires an NTC thermistor to be placed between TTSENSE and GND.

A fixed current of 8 × IREF (typically giving 123 µA) is sourced out of the TTSENSE pin and into the thermistor. The current source is internally limited to 5 V. An internal circuit compares the TTSENSE voltage to a 1.105 V and a 0.81 V threshold, and outputs an open-drain signal at the VRFAN and VRHOT outputs, respectively. Once the voltage on the TTSENSE pin drops below its respective threshold, the open-drain outputs assert high to signal the system that an overtemperature event has occurred. Because the TTSENSE voltage changes slowly with respect to time, 50 mV of hysteresis is built into these comparators. The thermal monitoring circuitry does not depend on EN and is active when UVLO is above its threshold. When UVLO is below its threshold, VRFAN and VRHOT are forced low.

Table 4.VR11 and VR10.x VID Codes for the ADP3192A

	VR11 DAC CODES: VIDSEL = HIGH								VR10.x DAC CODES: VIDSEL = LOW						
OUTPUT	**VID7**	**VID6**	**VID5**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID5**	**VID6**
OFF	0	0	0	0	0	0	0	0	N/A						
OFF	0	0	0	0	0	0	0	1	N/A						
1.60000	0	0	0	0	0	0	1	0	0	1	0	1	0	1	1
1.59375	0	0	0	0	0	0	1	1	0	1	0	1	0	1	0
1.58750	0	0	0	0	0	1	0	0	0	1	0	1	1	0	1
1.58125	0	0	0	0	0	1	0	1	0	1	0	1	1	0	0
1.57500	0	0	0	0	0	1	1	0	0	1	0	1	1	1	1
1.56875	0	0	0	0	0	1	1	1	0	1	0	1	1	1	0
1.56250	0	0	0	0	1	0	0	0	0	1	1	0	0	0	1
1.55625	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0
1.55000	0	0	0	0	1	0	1	0	0	1	1	0	0	1	1
1.54375	0	0	0	0	1	0	1	1	0	1	1	0	0	1	0
1.53750	0	0	0	0	1	1	0	0	0	1	1	0	1	0	1
1.53125	0	0	0	0	1	1	0	1	0	1	1	0	1	0	0
1.52500	0	0	0	0	1	1	1	0	0	1	1	0	1	1	1
1.51875	0	0	0	0	1	1	1	1	0	1	1	0	1	1	0

	VR11 DAC CODES: VIDSEL = HIGH								VR10.x DAC CODES: VIDSEL = LOW						
OUTPUT	**VID7**	**VID6**	**VID5**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID5**	**VID6**
1.51250	0	0	0	1	0	0	0	0	0	1	1	1	0	0	1
1.50625	0	0	0	1	0	0	0	1	0	1	1	1	0	0	0
1.50000	0	0	0	1	0	0	1	0	0	1	1	1	0	1	1
1.49375	0	0	0	1	0	0	1	1	0	1	1	1	0	1	0
1.48750	0	0	0	1	0	1	0	0	0	1	1	1	1	0	1
1.48125	0	0	0	1	0	1	0	1	0	1	1	1	1	0	0
1.47500	0	0	0	1	0	1	1	0	0	1	1	1	1	1	1
1.46875	0	0	0	1	0	1	1	1	0	1	1	1	1	1	0
1.46250	0	0	0	1	1	0	0	0	1	0	0	0	0	0	1
1.45625	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0
1.45000	0	0	0	1	1	0	1	0	1	0	0	0	0	1	1
1.44375	0	0	0	1	1	0	1	1	1	0	0	0	0	1	0
1.43750	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1
1.43125	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0
1.42500	0	0	0	1	1	1	1	0	1	0	0	0	1	1	1
1.41875	0	0	0	1	1	1	1	1	1	0	0	0	1	1	0
1.41250	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1
1.40625	0	0	1	0	0	0	0	1	1	0	0	1	0	0	0
1.40000	0	0	1	0	0	0	1	0	1	0	0	1	0	1	1
1.39375	0	0	1	0	0	0	1	1	1	0	0	1	0	1	0
1.38750	0	0	1	0	0	1	0	0	1	0	0	1	1	0	1
1.38125	0	0	1	0	0	1	0	1	1	0	0	1	1	0	0
1.37500	0	0	1	0	0	1	1	0	1	0	0	1	1	1	1
1.36875	0	0	1	0	0	1	1	1	1	0	0	1	1	1	0
1.36250	0	0	1	0	1	0	0	0	1	0	1	0	0	0	1
1.35625	0	0	1	0	1	0	0	1	1	0	1	0	0	0	0
1.35000	0	0	1	0	1	0	1	0	1	0	1	0	0	1	1
1.34375	0	0	1	0	1	0	1	1	1	0	1	0	0	1	0
1.33750	0	0	1	0	1	1	0	0	1	0	1	0	1	0	1
1.33125	0	0	1	0	1	1	0	1	1	0	1	0	1	0	0
1.32500	0	0	1	0	1	1	1	0	1	0	1	0	1	1	1
1.31875	0	0	1	0	1	1	1	1	1	0	1	0	1	1	0
1.31250	0	0	1	1	0	0	0	0	1	0	1	1	0	0	1
1.30625	0	0	1	1	0	0	0	1	1	0	1	1	0	0	0
1.30000	0	0	1	1	0	0	1	0	1	0	1	1	0	1	1
1.29375	0	0	1	1	0	0	1	1	1	0	1	1	0	1	0
1.28750	0	0	1	1	0	1	0	0	1	0	1	1	1	0	1
1.28125	0	0	1	1	0	1	0	1	1	0	1	1	1	0	0
1.27500	0	0	1	1	0	1	1	0	1	0	1	1	1	1	1
1.26875	0	0	1	1	0	1	1	1	1	0	1	1	1	1	0
1.26250	0	0	1	1	1	0	0	0	1	1	0	0	0	0	1
1.25625	0	0	1	1	1	0	0	1	1	1	0	0	0	0	0
1.25000	0	0	1	1	1	0	1	0	1	1	0	0	0	1	1
1.24375	0	0	1	1	1	0	1	1	1	1	0	0	0	1	0
1.23750	0	0	1	1	1	1	0	0	1	1	0	0	1	0	1
1.23125	0	0	1	1	1	1	0	1	1	1	0	0	1	0	0
1.22500	0	0	1	1	1	1	1	0	1	1	0	0	1	1	1
1.21875	0	0	1	1	1	1	1	1	1	1	0	0	1	1	0
1.21250	0	1	0	0	0	0	0	0	1	1	0	1	0	0	1
1.20625	0	1	0	0	0	0	0	1	1	1	0	1	0	0	0
1.20000	0	1	0	0	0	0	1	0	1	1	0	1	0	1	1
1.19375	0	1	0	0	0	0	1	1	1	1	0	1	0	1	0
1.18750	0	1	0	0	0	1	0	0	1	1	0	1	1	0	1
1.18125	0	1	0	0	0	1	0	1	1	1	0	1	1	0	0
1.17500	0	1	0	0	0	1	1	0	1	1	0	1	1	1	1
1.16875	0	1	0	0	0	1	1	1	1	1	0	1	1	1	0
1.16250	0	1	0	0	1	0	0	0	1	1	1	0	0	0	1
1.15625	0	1	0	0	1	0	0	1	1	1	1	0	0	0	0
1.15000	0	1	0	0	1	0	1	0	1	1	1	0	0	1	1

	VR11 DAC CODES: VIDSEL = HIGH								VR10.x DAC CODES: VIDSEL = LOW						
OUTPUT	**VID7**	**VID6**	**VID5**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID5**	**VID6**
1.14375	0	1	0	0	1	0	1	1	1	1	1	0	0	1	0
1.13750	0	1	0	0	1	1	0	0	1	1	1	0	1	0	1
1.13125	0	1	0	0	1	1	0	1	1	1	1	0	1	0	0
1.12500	0	1	0	0	1	1	1	0	1	1	1	0	1	1	1
1.11875	0	1	0	0	1	1	1	1	1	1	1	0	1	1	0
1.11250	0	1	0	1	0	0	0	0	1	1	1	1	0	0	1
1.10625	0	1	0	1	0	0	0	1	1	1	1	1	0	0	0
1.10000	0	1	0	1	0	0	1	0	1	1	1	1	0	1	1
1.09375	0	1	0	1	0	0	1	1	1	1	1	1	0	1	0
OFF	N/A								1	1	1	1	1	0	1
OFF	N/A								1	1	1	1	1	0	0
OFF	N/A								1	1	1	1	1	1	1
OFF	N/A								1	1	1	1	1	1	0
1.08750	0	1	0	1	0	1	0	0	0	0	0	0	0	0	1
1.08125	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0
1.07500	0	1	0	1	0	1	1	0	0	0	0	0	0	1	1
1.06875	0	1	0	1	0	1	1	1	0	0	0	0	0	1	0
1.06250	0	1	0	1	1	0	0	0	0	0	0	0	1	0	1
1.05625	0	1	0	1	1	0	0	1	0	0	0	0	1	0	0
1.05000	0	1	0	1	1	0	1	0	0	0	0	0	1	1	1
1.04375	0	1	0	1	1	0	1	1	0	0	0	0	1	1	0
1.03750	0	1	0	1	1	1	0	0	0	0	0	1	0	0	1
1.03125	0	1	0	1	1	1	0	1	0	0	0	1	0	0	0
1.02500	0	1	0	1	1	1	1	0	0	0	0	1	0	1	1
1.01875	0	1	0	1	1	1	1	1	0	0	0	1	0	1	0
1.01250	0	1	1	0	0	0	0	0	0	0	0	1	1	0	1
1.00625	0	1	1	0	0	0	0	1	0	0	0	1	1	0	0
1.00000	0	1	1	0	0	0	1	0	0	0	0	1	1	1	1
0.99375	0	1	1	0	0	0	1	1	0	0	0	1	1	1	0
0.98750	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
0.98125	0	1	1	0	0	1	0	1	0	0	1	0	0	0	0
0.97500	0	1	1	0	0	1	1	0	0	0	1	0	0	1	1
0.96875	0	1	1	0	0	1	1	1	0	0	1	0	0	1	0
0.96250	0	1	1	0	1	0	0	0	0	0	1	0	1	0	1
0.95625	0	1	1	0	1	0	0	1	0	0	1	0	1	0	0
0.95000	0	1	1	0	1	0	1	0	0	0	1	0	1	1	1
0.94375	0	1	1	0	1	0	1	1	0	0	1	0	1	1	0
0.93750	0	1	1	0	1	1	0	0	0	0	1	1	0	0	1
0.93125	0	1	1	0	1	1	0	1	0	0	1	1	0	0	0
0.92500	0	1	1	0	1	1	1	0	0	0	1	1	0	1	1
0.91875	0	1	1	0	1	1	1	1	0	0	1	1	0	1	0
0.91250	0	1	1	1	0	0	0	0	0	0	1	1	1	0	1
0.90625	0	1	1	1	0	0	0	1	0	0	1	1	1	0	0
0.90000	0	1	1	1	0	0	1	0	0	0	1	1	1	1	1
0.89375	0	1	1	1	0	0	1	1	0	0	1	1	1	1	0
0.88750	0	1	1	1	0	1	0	0	0	1	0	0	0	0	1
0.88125	0	1	1	1	0	1	0	1	0	1	0	0	0	0	0
0.87500	0	1	1	1	0	1	1	0	0	1	0	0	0	1	1
0.86875	0	1	1	1	0	1	1	1	0	1	0	0	0	1	0
0.86250	0	1	1	1	1	0	0	0	0	1	0	0	1	0	1
0.85625	0	1	1	1	1	0	0	1	0	1	0	0	1	0	0
0.85000	0	1	1	1	1	0	1	0	0	1	0	0	1	1	1
0.84375	0	1	1	1	1	0	1	1	0	1	0	0	1	1	0
0.83750	0	1	1	1	1	1	0	0	0	1	0	1	0	0	1
0.83125	0	1	1	1	1	1	0	1	0	1	0	1	0	0	0
0.82500	0	1	1	1	1	1	1	0	N/A						
0.81875	0	1	1	1	1	1	1	1	N/A						
0.81250	1	0	0	0	0	0	0	0	N/A						
0.80625	1	0	0	0	0	0	0	1	N/A						

	VR11 DAC CODES: VIDSEL = HIGH								VR10.x DAC CODES: VIDSEL = LOW						
OUTPUT	**VID7**	**VID6**	**VID5**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID5**	**VID6**
0.80000	1	0	0	0	0	0	1	0				N/A			
0.79375	1	0	0	0	0	0	1	1				N/A			
0.78750	1	0	0	0	0	1	0	0				N/A			
0.78125	1	0	0	0	0	1	0	1				N/A			
0.77500	1	0	0	0	0	1	1	0				N/A			
0.76875	1	0	0	0	0	1	1	1				N/A			
0.76250	1	0	0	0	1	0	0	0				N/A			
0.75625	1	0	0	0	1	0	0	1				N/A			
0.75000	1	0	0	0	1	0	1	0				N/A			
0.74375	1	0	0	0	1	0	1	1				N/A			
0.73750	1	0	0	0	1	1	0	0				N/A			
0.73125	1	0	0	0	1	1	0	1				N/A			
0.72500	1	0	0	0	1	1	1	0				N/A			
0.71875	1	0	0	0	1	1	1	1				N/A			
0.71250	1	0	0	1	0	0	0	0				N/A			
0.70625	1	0	0	1	0	0	0	1				N/A			
0.70000	1	0	0	1	0	0	1	0				N/A			
0.69375	1	0	0	1	0	0	1	1				N/A			
0.68750	1	0	0	1	0	1	0	0				N/A			
0.68125	1	0	0	1	0	1	0	1				N/A			
0.67500	1	0	0	1	0	1	1	0				N/A			
0.66875	1	0	0	1	0	1	1	1				N/A			
0.66250	1	0	0	1	1	0	0	0				N/A			
0.65625	1	0	0	1	1	0	0	1				N/A			
0.65000	1	0	0	1	1	0	1	0				N/A			
0.64375	1	0	0	1	1	0	1	1				N/A			
0.63750	1	0	0	1	1	1	0	0				N/A			
0.63125	1	0	0	1	1	1	0	1				N/A			
0.62500	1	0	0	1	1	1	1	0				N/A			
0.61875	1	0	0	1	1	1	1	1				N/A			
0.61250	1	0	1	0	0	0	0	0				N/A			
0.60625	1	0	1	0	0	0	0	1				N/A			
0.60000	1	0	1	0	0	0	1	0				N/A			
0.59375	1	0	1	0	0	0	1	1				N/A			
0.58750	1	0	1	0	0	1	0	0				N/A			
0.58125	1	0	1	0	0	1	0	1				N/A			
0.57500	1	0	1	0	0	1	1	0				N/A			
0.56875	1	0	1	0	0	1	1	1				N/A			
0.56250	1	0	1	0	1	0	0	0				N/A			
0.55625	1	0	1	0	1	0	0	1				N/A			
0.55000	1	0	1	0	1	0	1	0				N/A			
0.54375	1	0	1	0	1	0	1	1				N/A			
0.53750	1	0	1	0	1	1	0	0				N/A			
0.53125	1	0	1	0	1	1	0	1				N/A			
0.52500	1	0	1	0	1	1	1	0				N/A			
0.51875	1	0	1	0	1	1	1	1				N/A			
0.51250	1	0	1	1	0	0	0	0				N/A			
0.50625	1	0	1	1	0	0	0	1				N/A			
0.50000	1	0	1	1	0	0	1	0				N/A			
OFF	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0
OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

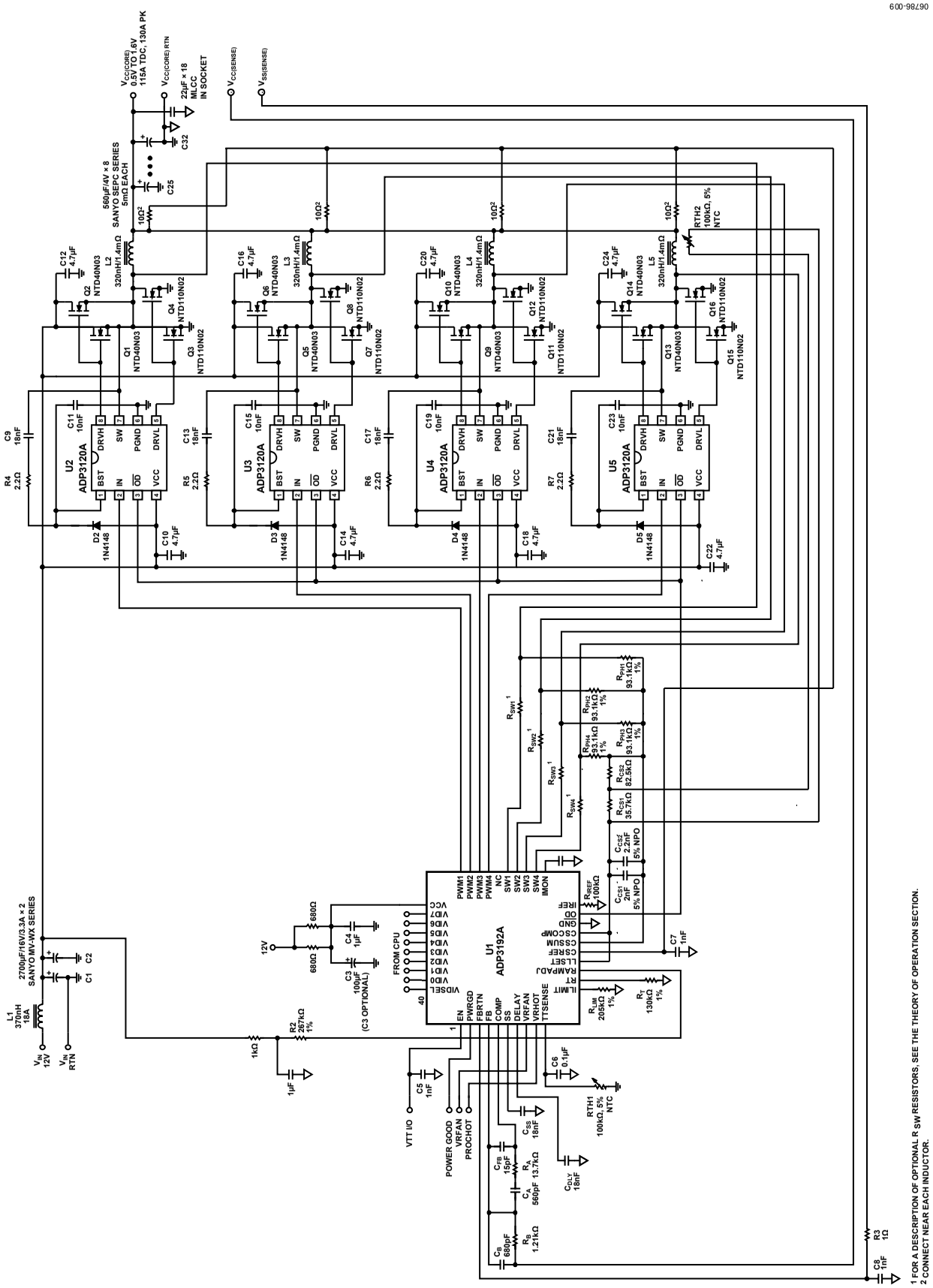

Figure 10. Typical 4-Phase Application Circuit

APPLICATION INFORMATION

The design parameters for a typical Intel VRD 11-compliant CPU application are as follows:

- Input voltage (V_{IN}) = 12 V
- VID setting voltage (V_{VID}) = 1.300 V
- Duty cycle (D) = 0.108
- Nominal output voltage at no load (V_{ONL}) = 1.285 V
- Nominal output voltage at 115 A load (V_{OFL}) = 1.170 V
- Static output voltage drop based on a 1.0 mΩ load line (R_O) from no load to full load (V_D) = V_{ONL} − V_{OFL} = 1.285 V − 1.170 V = 115 mV
- Maximum output current (I_O) = 130 A
- Maximum output current step (ΔI_O) = 100 A
- Maximum output current slew rate (S_R) = 200 A/µs
- Number of phases (n) = 4
- Switching frequency per phase (f_{SW}) = 330 kHz

SETTING THE CLOCK FREQUENCY

The ADP3192A uses a fixed frequency control architecture. The frequency is set by an external timing resistor (R_T). The clock frequency and the number of phases determine the switching frequency per phase, which relates directly to switching losses as well as the sizes of the inductors, the input capacitors, and output capacitors. With n = 4 for four phases, a clock frequency of 1.32 MHz sets the switching frequency (f_{SW}) of each phase to 330 kHz, which represents a practical trade-off between the switching losses and the sizes of the output filter components. Figure 6 shows that to achieve a 1.32 MHz oscillator frequency, the correct value for R_T is 130 kΩ. Alternatively, the value for R_T can be calculated using

$$R_T = \frac{1}{n \times f_{SW} \times 6\ \text{pF}} \quad (1)$$

where 6 pF is the internal IC component values. For good initial accuracy and frequency stability, a 1% resistor is recommended.

SOFT START DELAY TIME

The value of C_{SS} sets the soft start time. The ramp is generated with a 15 µA internal current source. The value for C_{SS} can be found using

$$C_{SS} = 15\,\mu\text{A} \times \frac{TD2}{V_{BOOT}} \quad (2)$$

where:

TD2 is the desired soft start time.
V_{BOOT} is internally set to 1.1 V.

Assuming a desired TD2 time of 3 ms, C_{SS} is 41 nF. The closest standard value for C_{SS} is 39 nF. Although C_{SS} also controls the time delay for TD4 (determined by the final VID voltage), the minimum specification for TD4 is 0 ns. This means that as long as the TD2 time requirement is met, TD4 is within the specification.

CURRENT-LIMIT LATCH-OFF DELAY TIMES

The start-up and current-limit delay times are determined by the capacitor connected to the DELAY pin. The first step is to set C_{DLY} for the TD1, TD3, and TD5 delay times (see Figure 7). The DELAY ramp (I_{DELAY}) is generated using a 15 µA internal current source. The value for C_{DLY} can be approximated using

$$C_{DLY} = I_{DELAY} \times \frac{TD(x)}{V_{DELAY(TH)}} \quad (3)$$

where:

TD(x) is the desired delay time for TD1, TD3, and TD5.
$V_{DELAY(TH)}$, the DELAY threshold voltage, is given as 1.7 V.

In this example, 2 ms is chosen for all three delay times, which meets Intel specifications. Solving for C_{DLY} gives a value of 17.6 nF. The closest standard value for C_{DLY} is 18 nF.

When the ADP3192A enters current limit, the internal current source changes from 15 µA to 3.75 µA. This makes the latch-off delay time four times longer than the start-up delay time. Longer latch-off delay times can be achieved by placing a resistor in parallel with C_{DLY}.

INDUCTOR SELECTION

The choice of inductance for the inductor determines the ripple current in the inductor. Less inductance leads to more ripple current, which increases the output ripple voltage and conduction losses in the MOSFETs. However, using smaller inductors allows the converter to meet a specified peak-to-peak transient deviation with less total output capacitance. Conversely, a higher inductance means lower ripple current and reduced conduction losses, but more output capacitance is required to meet the same peak-to-peak transient deviation.

In any multiphase converter, a practical value for the peak-to-peak inductor ripple current is less than 50% of the maximum dc current in the same inductor. Equation 4 shows the relationship between the inductance, oscillator frequency, and peak-to-peak ripple current in the inductor.

$$I_R = \frac{V_{VID} \times (1 - D)}{f_{SW} \times L} \quad (4)$$

Equation 5 can be used to determine the minimum inductance based on a given output ripple voltage.

$$L \geq \frac{V_{VID} \times R_O \times (1 - (n \times D))}{f_{SW} \times V_{RIPPLE}} \quad (5)$$

Solving Equation 5 for an 8 mV p-p output ripple voltage yields

$$L \geq \frac{1.3\ \text{V} \times 1.0\ \text{m}\Omega \times (1 - 0.432)}{330\ \text{kHz} \times 8\ \text{mV}} = 280\ \text{nH}$$

If the resulting ripple voltage is less than what is designed for, the inductor can be made smaller until the ripple value is met. This allows optimal transient response and minimum output decoupling.

The smallest possible inductor should be used to minimize the number of output capacitors. For this example, choosing a 320 nH inductor is a good starting point and gives a calculated ripple current of 11 A. The inductor should not saturate at the peak current of 35.5 A and should be able to handle the sum of the power dissipation caused by the average current of 30 A in the winding and core loss.

Another important factor in the inductor design is the dc resistance (DCR), which is used for measuring the phase currents. A large DCR can cause excessive power loss, though too small a value can lead to increased measurement error. A good rule is to have the DCR (R_L) be about 1 to 1½ times the droop resistance (R_O). This example uses an inductor with a DCR of 1.4 mΩ.

Designing an Inductor

Once the inductance and DCR are known, the next step is to either design an inductor or find a standard inductor that comes as close as possible to meeting the overall design goals. It is also important to have the inductance and DCR tolerance specified to control the accuracy of the system. Reasonable tolerances most manufacturers can meet are 15% inductance and 7% DCR at room temperature. The first decision in designing the inductor is choosing the core material. Several possibilities for providing low core loss at high frequencies include the powder cores (from Micrometals, Inc., for example, or Kool Mu® from MAGNETICS®) and the gapped soft ferrite cores (for example, 3F3 or 3F4 from Philips®). Low frequency powdered iron cores should be avoided due to their high core loss, especially when the inductor value is relatively low, and the ripple current is high.

The best choice for a core geometry is a closed-loop type, such as a potentiometer core (PQ, U, or E core) or toroid. A good compromise between price and performance is a core with a toroidal shape.

Many useful magnetics design references are available for quickly designing a power inductor, such as

- Intusoft Magnetics Designer Software
- *Designing Magnetic Components for High Frequency dc-dc Converters*, by Colonel Wm. T. McLyman, Kg Magnetics, Inc., ISBN 1883107008

Selecting a Standard Inductor

The following power inductor manufacturers can provide design consultation and deliver power inductors optimized for high power applications upon request:

- Coilcraft®
- Coiltronics®
- Sumida Corporation®

CURRENT SENSE AMPLIFIER

Most designs require the regulator output voltage, measured at the CPU pins, to drop when the output current increases. The specified voltage drop corresponds to a dc output resistance (R_O), also referred to as a load line. The ADP3192A has the flexibility of adjusting R_O, independent of current-limit or compensation components, and it can also support CPUs that do not require a load line.

For designs requiring a load line, the impedance gain of the CS amplifier (R_{CSA}) must be to be greater than or equal to the load line. All designs, whether they have a load line or not, should keep $R_{CSA} \geq 1$ mΩ.

The output current is measured by summing the voltage across each inductor and passing the signal through a low-pass filter. This summer filter is the CS amplifier configured with resistors $R_{PH(X)}$ (summers), and R_{CS} and C_{CS} (filter). The impedance gain of the regulator is set by the following equations, where R_L is the DCR of the output inductors:

$$R_{CSA} = \frac{R_{CS}}{R_{PH(X)}} \times R_L \quad (6)$$

$$C_{CS} = \frac{L}{R_L \times R_{CS}} \quad (7)$$

The user has the flexibility to choose either R_{CS} or $R_{PH(X)}$. However, it is best to select R_{CS} equal to 100 kΩ, and then solve for $R_{PH(X)}$ by rearranging Equation 6. Here, $R_{CSA} = R_O = 1$ mΩ because this is equal to the design load line.

$$R_{PH(X)} = \frac{R_L}{R_{CSA}} \times R_{CS}$$

$$R_{PH(X)} = \frac{1.4\ \text{m}\Omega}{1.0\ \text{m}\Omega} \times 100\ \text{k}\Omega = 140\ \text{k}\Omega$$

Next, use Equation 7 to solve for C_{CS}.

$$C_{CS} = \frac{320\ \text{nH}}{1.4\ \text{m}\Omega \times 100\ \text{k}\Omega} = 2.28\ \text{nF}$$

It is best to have a dual location for C_{CS} in the layout so that standard values can be used in parallel to get as close to the desired value. For best accuracy, C_{CS} should be a 5% or 10% NPO capacitor. This example uses a 5% combination for C_{CS} of two 1 nF capacitors in parallel. Recalculating R_{CS} and $R_{PH(X)}$ using this capacitor combination yields 114 kΩ and 160 kΩ, respectively. The closest standard 1% value for $R_{PH(X)}$ is 158 kΩ.

INDUCTOR DCR TEMPERATURE CORRECTION

When the inductor DCR is used as the sense element and copper wire is used as the source of the DCR, the user needs to compensate for temperature changes of the inductor's winding. Fortunately, copper has a well-known temperature coefficient (TC) of 0.39%/°C.

If R_{CS} is designed to have an opposite and equal percentage change in resistance to that of the wire, it cancels the temperature variation of the inductor DCR. Due to the nonlinear nature of NTC thermistors, Resistor R_{CS1} and Resistor R_{CS2} are needed. Refer to Figure 11 to linearize the NTC and produce the desired temperature tracking.

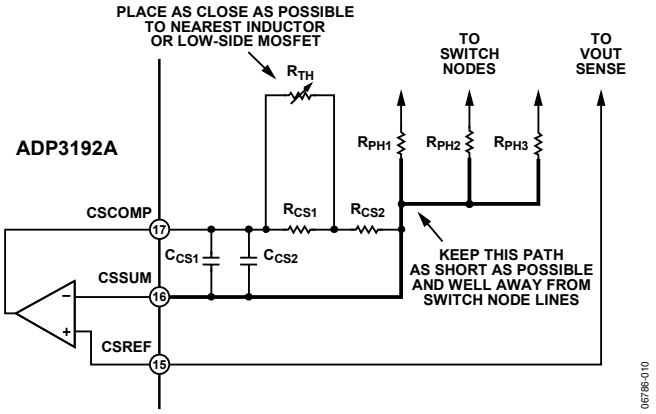

Figure 11. Temperature Compensation Circuit Values

The following procedure and equations yield values to use for R_{CS1}, R_{CS2}, and R_{TH} (the thermistor value at 25°C) for a given R_{CS} value:

1. Select an NTC based on type and value. Because the value is unknown, use a thermistor with a value close to R_{CS}. The NTC should also have an initial tolerance of better than 5%.
2. Based on the type of NTC, find its relative resistance value at two temperatures. Temperatures that work well are 50°C and 90°C. These resistance values are called A ($R_{TH(50°C)}$)/$R_{TH(25°C)}$) and B ($R_{TH(90°C)}$)/$R_{TH(25°C)}$). The relative value of the NTC is always 1 at 25°C.
3. Find the relative value of R_{CS} required for each of these temperatures. This is based on the percentage change needed, which in this example is initially 0.39%/°C. These temperatures are called r_1 (1/(1 + TC × (T_1 − 25°C))) and r_2 (1/(1 + TC × (T_2 − 25°C))), where TC = 0.0039 for copper, T_1 = 50°C, and T_2 = 90°C. From this, r_1 = 0.9112 and r_2 = 0.7978.
4. Compute the relative values for R_{CS1}, R_{CS2}, and R_{TH} using

$$r_{CS2} = \frac{(A-B)\times r_1 \times r_2 - A\times(1-B)\times r_2 + B\times(1-A)\times r_1}{A\times(1-B)\times r_1 - B\times(1-A)\times r_2 - (A-B)} \quad (8)$$

$$r_{CS1} = \frac{(1-A)}{\frac{1}{1-r_{CS2}} - \frac{A}{r_1 - r_{CS2}}} \quad (9)$$

$$r_{TH} = \frac{1}{\frac{1}{1-r_{CS2}} - \frac{1}{r_{CS1}}} \quad (10)$$

5. Calculate $R_{TH} = r_{TH} \times R_{CS}$, then select the closest value of thermistor available. Also, compute a scaling factor (k) based on the ratio of the actual thermistor value used relative to the computed one.

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} \quad (11)$$

6. Calculate values for R_{CS1} and R_{CS2} using Equation 12 and Equation 13.

$$R_{CS1} = R_{CS} \times k \times r_{CS1} \quad (12)$$

$$R_{CS2} = R_{CS} \times \left((1-k) + \left(k \times r_{CS2}\right)\right) \quad (13)$$

In this example, R_{CS} is calculated to be 114 kΩ. Look for an available 100 kΩ thermistor, 0603 size. One such thermistor is the Vishay NTHS0603N01N1003JR NTC thermistor with A = 0.3602 and B = 0.09174. From these values, r_{CS1} = 0.3795, r_{CS2} = 0.7195, and r_{TH} = 1.075.

Solving for R_{TH} yields 122.55 kΩ, so 100 kΩ is chosen, making k = 0.816. Next, find R_{CS1} and R_{CS2} to be 35.3 kΩ and 87.9 kΩ. Finally, choose the closest 1% resistor value, which yields a choice of 35.7 kΩ and 88.7 kΩ.

Load Line Setting

For load line values greater than 1 mΩ, R_{CSA} can be set equal to R_O, and the LLSET pin can be directly connected to the CSCOMP pin. When the load line value needs to be less than 1 mΩ, two additional resistors are required. Figure 12 shows the placement of these resistors.

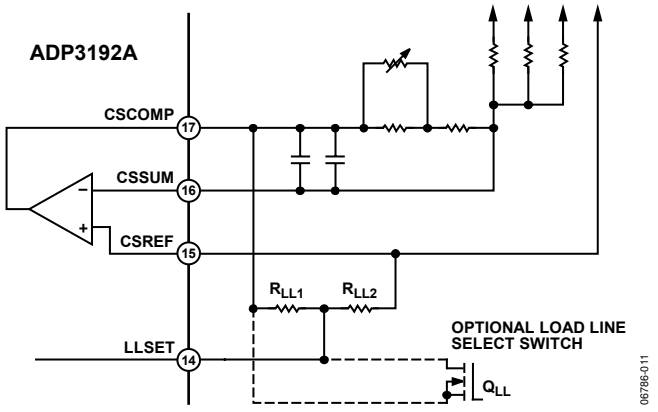

Figure 12. Load Line Setting Resistors

The two resistors R_{LL1} and R_{LL2} set up a divider between the CSCOMP pin and CSREF pin. This resistor divider is input into the LLSET pin to set the load line slope R_O of the VR according to the following equation:

$$R_O = \frac{R_{LL2}}{R_{LL1} + R_{LL2}} \times R_{CSA} \quad (14)$$

The resistor values for R_{LL1} and R_{LL2} are limited by two factors.

- The minimum value is based upon the loading of the CSCOMP pin. This pin's drive capability is 500 µA, and the majority of this should be allocated to the CSA feedback. If the current through R_{LL1} and R_{LL2} is limited to 10% of this drive capability (50 µA), the following limit can be placed on the minimum value for R_{LL1} and R_{LL2}:

$$R_{LL1} + R_{LL2} \geq \frac{I_{LIM} \times R_{CSA}}{50 \times 10^{-6}} \quad (15)$$

  Here, I_{LIM} is the current-limit current, which is the maximum signal level that the CSA responds to.

- The maximum value is based upon minimizing induced dc offset errors based on the bias current of the LLSET pin. To keep the induced dc error less than 1 mV, which makes this error statistically negligible, place the following limit on the parallel combination of R_{LL1} and R_{LL2}:

$$\frac{R_{LL1} \times R_{LL2}}{R_{LL1} + R_{LL2}} \leq \frac{1 \times 10^{-3}}{120 \times 10^{-9}} = 8.33\ \text{k}\Omega \quad (16)$$

Select minimum value resistors to reduce the noise and parasitic susceptibility of the feedback path.

By combining Equation 16 with Equation 14 and selecting minimum values for the resistors, the following equations result:

$$R_{LL2} = \frac{I_{LIM} \times R_O}{50\ \mu\text{A}} \quad (17)$$

$$R_{LL1} = \left(\frac{R_{CSA}}{R_O} - 1 \right) \times R_{LL2} \quad (18)$$

Therefore, both R_{LL1} and R_{LL2} need to be in parallel and less than 8.33 kΩ.

Another useful feature for some VR applications is the ability to select different load lines. Figure 12 shows an optional MOSFET switch that allows this feature. Here, design for $R_{CSA} = R_{O(MAX)}$ (selected with Q_{LL} on), and then use Equation 14 to set $R_O = R_{O(MIN)}$ (selected with Q_{LL} off).

For this design, $R_{CSA} = R_O = 1$ mΩ. As a result, connect LLSET directly to CSCOMP; the R_{LL1} and R_{LL2} resistors are not needed.

OUTPUT OFFSET

The Intel specification requires that at no load, the nominal output voltage of the regulator be offset to a value lower than the nominal voltage corresponding to the VID code. The offset is set by a constant current source flowing out of the FB pin (I_{FB}) and flowing through R_B. The value of R_B can be found using Equation 19.

$$R_B = \frac{V_{VID} - V_{ONL}}{I_{FB}}$$

$$R_B = \frac{1.3\ \text{V} - 1.285\ \text{V}}{15\ \mu\text{A}} = 1.00\ \text{k}\Omega \quad (19)$$

The closest standard 1% resistor value is 1.00 kΩ.

C_{OUT} SELECTION

The required output decoupling for the regulator is typically recommended by Intel for various processors and platforms. Use some simple design guidelines to determine the requirements. These guidelines are based on having both bulk capacitors and ceramic capacitors in the system.

First, select the total amount of ceramic capacitance. This is based on the number and type of capacitor to be used. The best location for ceramic capacitors is inside the socket with 12 to 18, 1206 size being the physical limit. Other capacitors can be placed along the outer edge of the socket as well.

To determine the minimum amount of ceramic capacitance required, start with a worst-case load step occurring right after a switching cycle stops. The ceramic capacitance then delivers the charge to the load while the load is ramping up and until the VR has responded with the next switching cycle.

Equation 20 gives the designer a rough approximation for determining the minimum ceramic capacitance. Due to the complexity of the PCB parasitics and bulk capacitors, the actual amount of ceramic capacitance required can vary.

$$C_{Z(MIN)} \geq \frac{1}{R_O} \times \left[\frac{1}{f_{SW}} \times \left(\frac{1}{n} - D \right) - \frac{\Delta I_O}{2\ S_R} \right] \quad (20)$$

The typical ceramic capacitors consist of multiple 10 µF or 22 µF capacitors. For this example, Equation 20 yields 180.8 µF, therefore, 18, 10 µF ceramic capacitors suffice.

Next, an upper limit is imposed on the total amount of bulk capacitance (C_X) when the user considers the VID on-the-fly voltage stepping of the output (voltage step V_V in time t_V with error of V_{ERR}).

A lower limit is based on meeting the capacitance for load release for a given maximum load step (ΔI_O) and a maximum allowable overshoot. The total amount of load release voltage is given as $\Delta V_O = \Delta I_O \times R_O + \Delta V_{rl}$, where ΔV_{rl} is the maximum allowable overshoot voltage.

$$C_{X(MIN)} \geq \left(\frac{L \times \Delta I_O}{n \times \left(R_O + \frac{\Delta V_{rl}}{\Delta I_O} \right) \times V_{VID}} - C_Z \right) \quad (21)$$

$$C_{X(MAX)} \leq \frac{L}{nK^2 R_O^2} \times \frac{V_V}{V_{VID}} \times \left(\sqrt{1 + \left(t_V \frac{V_{VID}}{V_V} \times \frac{nKR_O}{L} \right)^2} - 1 \right) - C_Z \quad (22)$$

where $K = -1n\left(\frac{V_{ERR}}{V_V}\right)$.

To meet the conditions of these equations and transient response, the ESR of the bulk capacitor bank (R_X) should be less than two times the droop resistance (R_O). If the $C_{X(MIN)}$ is larger than $C_{X(MAX)}$, the system cannot meet the VID on-the-fly specification and may require the use of a smaller inductor or more phases (and may have to increase the switching frequency to keep the output ripple the same).

This example uses 18, 10 µF 1206 MLC capacitors (C_Z = 180 µF). The VID on-the-fly step change is 450 mV in 230 µs with a settling error of 2.5 mV. The maximum allowable load release overshoot for this example is 50 mV. Therefore, solving for the bulk capacitance yields the following:

$$C_{X(MIN)} \leq \left(\frac{320\text{ nH} \times 100\text{ A}}{4 \times \left(1.0\text{ m}\Omega + \frac{50\text{ mV}}{100\text{ A}} \right) \times 1.3\text{ V}} - 180\text{ µF} \right) = 3.92\text{ mF}$$

$$C_{X(MAX)} \leq \frac{320\text{ nH} \times 450\text{ mV}}{4 \times 5.2^2 \times (1.0\text{ m}\Omega)^2 \times 1.3\text{ V}} \times \left(\sqrt{1 + \left(\frac{230\text{ µs} \times 1.3\text{ V} \times 4 \times 5.2 \times 1.0\text{ m}\Omega}{450\text{ mV} \times 320\text{ nH}} \right)^2} - 1 \right) - 180\text{ µF} = 43.0\text{ mF}$$

where K = 5.2.

Using 10, 560 µF Al-Poly capacitors with a typical ESR of 6 mΩ each yields C_X = 5.6 mF with an R_X = 0.6 mΩ.

One last check should be made to ensure that the ESL of the bulk capacitors (L_X) is low enough to limit the high frequency ringing during a load change.

This is tested using

$$L_X \leq C_Z \times R_O{}^2 \times Q^2$$
$$L_X \leq 180\text{ µF} \times (1\text{ m}\Omega)^2 \times \frac{4}{3} = 240\text{ pH} \quad (23)$$

where Q^2 is limited to 4/3 to ensure a critically damped system.

In this example, L_X is approximately 240 pH for the 10, Al-Poly capacitors, which satisfies this limitation. If the L_X of the chosen bulk capacitor bank is too large, the number of ceramic capacitors needs to be increased, or lower ESL bulks need to be used if there is excessive undershoot during a load transient.

For this multimode control technique, all ceramic designs can be used providing the conditions of Equation 20 through Equation 23 are satisfied.

POWER MOSFETS

For this example, the N-channel power MOSFETs have been selected for one high-side switch and two low-side switches per phase. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, Q_G, C_{ISS}, C_{RSS}, and $R_{DS(ON)}$. The minimum gate drive voltage (the supply voltage to the ADP3120A) dictates whether standard threshold or logic-level threshold MOSFETs must be used. With V_{GATE} ~10 V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5 V) are recommended.

The maximum output current (I_O) determines the $R_{DS(ON)}$ requirement for the low-side (synchronous) MOSFETs. With the ADP3192A, currents are balanced between phases, thus, the current in each low-side MOSFET is the output current divided by the total number of MOSFETs (n_{SF}). With conduction losses being dominant, Equation 24 shows the total power that is dissipated in each synchronous MOSFET in terms of the ripple current per phase (I_R) and average total output current (I_O).

$$P_{SF} = (1-D) \times \left[\left(\frac{I_O}{n_{SF}} \right)^2 + \frac{1}{12} \times \left(\frac{n I_R}{n_{SF}} \right)^2 \right] \times R_{DS(SF)} \quad (24)$$

Knowing the maximum output current being designed for and the maximum allowed power dissipation, the user can find the required $R_{DS(ON)}$ for the MOSFET. For D-PAK MOSFETs up to an ambient temperature of 50°C, a safe limit for P_{SF} is 1 W to 1.5 W at a 120°C junction temperature. Therefore, for this example (119 A maximum), $R_{DS(SF)}$ (per MOSFET) < 7.5 mΩ. This $R_{DS(SF)}$ is also at a junction temperature of about 120°C. As a result, users need to account for this when making this selection. This example uses two lower-side MOSFETs at 4.8 mΩ, each at 120°C.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of the feedback to input needs to be small (less than 10% is recommended) to prevent accidental turn-on of the synchronous MOSFETs when the switch node goes high.

Also, the time to switch the synchronous MOSFETs off should not exceed the nonoverlap dead time of the MOSFET driver (40 ns typical for the ADP3120A). The output impedance of the driver is approximately 2 Ω, and the typical MOSFET input gate resistances are about 1 Ω to 2 Ω. Therefore, a total gate capacitance of less than 6000 pF should be adhered to. Because two MOSFETs are in parallel, the input capacitance for each synchronous MOSFET should be limited to 3000 pF.

The high-side (main) MOSFET has to be able to handle two main power dissipation components: conduction and switching losses. The switching loss is related to the amount of time it takes for the main MOSFET to turn on and off, and to the current and voltage that are being switched. Basing the switching speed on the rise and fall time of the gate driver impedance and MOSFET input capacitance, Equation 25 provides an approximate value for the switching loss per main MOSFET.

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{CC} \times I_O}{n_{MF}} \times R_G \times \frac{n_{MF}}{n} \times C_{ISS} \quad (25)$$

where:

n_{MF} is the total number of main MOSFETs.
R_G is the total gate resistance (2 Ω for the ADP3120A and about 1 Ω for typical high speed switching MOSFETs, making R_G = 3 Ω).
C_{ISS} is the input capacitance of the main MOSFET.

Adding more main MOSFETs (n_{MF}) does not help the switching loss per MOSFET because the additional gate capacitance slows switching. Use lower gate capacitance devices to reduce switching loss.

The conduction loss of the main MOSFET is given by

$$P_{C(MF)} = D \times \left[\left(\frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{MF}} \right)^2 \right] \times R_{DS(MF)} \quad (26)$$

where $R_{DS(MF)}$ is the on resistance of the MOSFET.

Typically, for main MOSFETs, the highest speed (low C_{ISS}) device is preferred, but these usually have higher on resistance. Select a device that meets the total power dissipation (about 1.5 W for a single D-PAK) when combining the switching and conduction losses.

For this example, an NTD40N03 is selected as the main MOSFET (eight total; n_{MF} = 8), with C_{ISS} = 584 pF (maximum) and $R_{DS(MF)}$ = 19 mΩ (maximum at T_J = 120°C). An NTD110N02is selected as the synchronous MOSFET (eight total; n_{SF} = 8), with C_{ISS} = 2710 pF (maximum) and $R_{DS(SF)}$ = 4.8 mΩ (maximum at T_J = 120°C). The synchronous MOSFET C_{ISS} is less than 3000 pF, satisfying this requirement.

Solving for the power dissipation per MOSFET at I_O = 119 A and I_R = 11 A yields 958 mW for each synchronous MOSFET and 872 mW for each main MOSFET. A guideline to follow is to limit the MOSFET power dissipation to 1 W. The values calculated in Equation 25 and Equation 26 comply with this guideline.

Finally, consider the power dissipation in the driver for each phase. This is best expressed as Q_G for the MOSFETs and is given by Equation 27.

$$P_{DRV} = \left[\frac{f_{SW}}{2 \times n} \times \left(n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF} \right) + I_{CC} \right] \times V_{CC} \quad (27)$$

where:

Q_{GMF} is the total gate charge for each main MOSFET.
Q_{GSF} is the total gate charge for each synchronous MOSFET.

Also shown is the standby dissipation factor ($I_{CC} \times V_{CC}$) of the driver. For the ADP3120A, the maximum dissipation should be less than 400 mW. In this example, with I_{CC} = 7 mA, Q_{GMF} = 5.8 nC, and Q_{GSF} = 48 nC, there is 297 mW in each driver, which is below the 400 mW dissipation limit. See the ADP3120A data sheet for more details.

RAMP RESISTOR SELECTION

The ramp resistor (R_R) is used for setting the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. Equation 28 is used for determining the optimum value.

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R} \quad (28)$$

$$R_R = \frac{0.2 \times 320 \text{ nH}}{3 \times 5 \times 2.4 \text{ m}\Omega \times 5 \text{ pF}} = 356 \text{ k}\Omega$$

where:

A_R is the internal ramp amplifier gain.
A_D is the current balancing amplifier gain.
R_{DS} is the total low-side MOSFET on resistance.
C_R is the internal ramp capacitor value.

The internal ramp voltage magnitude can be calculated by using

$$V_R = \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} \quad (29)$$

$$V_R = \frac{0.2 \times (1 - 0.108) \times 1.3 \text{ V}}{357 \text{ k}\Omega \times 5 \text{ pF} \times 330 \text{ kHz}} = 394 \text{ mV}$$

The size of the internal ramp can be made larger or smaller. If it is made larger, stability and noise rejection improves, but transient degrades. Likewise, if the ramp is made smaller, transient response improves at the sacrifice of noise rejection and stability.

The factor of 3 in the denominator of Equation 28 sets a ramp size that gives an optimal balance for good stability, transient response, and thermal balance.

COMP PIN RAMP

A ramp signal on the COMP pin is due to the droop voltage and output voltage ramps. This ramp amplitude adds to the internal ramp to produce the following overall ramp signal at the PWM input:

$$V_{RT} = \frac{V_R}{\left(1 - \frac{2 \times \left(1 - n \times D\right)}{n \times f_{SW} \times C_X \times R_O}\right)} \quad (30)$$

In this example, the overall ramp signal is 0.46 V. However, if the ramp size is smaller than 0.5 V, increase the ramp size to be at least 0.5 V by decreasing the ramp resistor for noise immunity. Because there is only 0.46 V initially, a ramp resistor value of 332 kΩ is chosen for this example, yielding an overall ramp of 0.51 V.

CURRENT-LIMIT SETPOINT

To select the current-limit setpoint, first find the resistor value for R_{LIM}. The current-limit threshold for the ADP3192A is set with a constant current source flowing out of the ILIMIT pin, which sets up a voltage (V_{LIM}) across R_{LIM} with a gain of 82.6 mV/V (A_{LIM}). Thus, increasing R_{LIM} now increases the current limit. R_{LIM} can be found using

$$R_{LIM} = \frac{V_{CL}}{A_{LIM} \times I_{ILIMIT}} = \frac{I_{LIM} \times R_{CSA}}{82.6\ \text{mV}} \times R_{REF} \quad (31)$$

Here, I_{LIM} is the peak average current limit for the supply output. The peak average current is the dc current limit plus the output ripple current. In this example, choosing a dc current limit of 159 A and having a ripple current of 11 A gives an I_{LIM} of 170 A. This results in an R_{LIM} = 205.8 kΩ, for which 205 kΩ is chosen as the nearest 1% value.

The per-phase initial duty cycle limit and peak current during a load step are determined by

$$D_{MAX} = D \times \frac{V_{COMP(MAX)} - V_{BIAS}}{V_{RT}} \quad (32)$$

$$I_{PHMAX} \cong \frac{D_{MAX}}{f_{SW}} \times \frac{\left(V_{IN} - V_{VID}\right)}{L} \quad (33)$$

For the ADP3192A, the maximum COMP voltage ($V_{COMP(MAX)}$) is 4.0 V, and the COMP pin bias voltage (V_{BIAS}) is 1.1 V. In this example, the maximum duty cycle is 0.61 and the peak current is 62 A.

The limit of the peak per-phase current described earlier during the secondary current limit is determined by

$$I_{PHLIM} \cong \frac{V_{COMP(CLAMPED)} - V_{BIAS}}{A_D \times R_{DS(MAX)}} \quad (34)$$

For the ADP3192A, the current balancing amplifier gain (A_D) is 5 and the clamped COMP pin voltage is 2 V. Using an $R_{DS(MAX)}$ of 2.8 mΩ (low-side on resistance at 150°C) results in a per-phase peak current limit of 64 A. This current level can be reached only with an absolute short at the output and only if the current-limit latch-off function shuts down the regulator before overheating can occur.

FEEDBACK LOOP COMPENSATION DESIGN

Optimized compensation of the ADP3192A allows the best possible response of the regulator output to a load change.

The basis for determining the optimum compensation is to make the regulator and output decoupling appear as an output impedance that is entirely resistive over the widest possible frequency range, including dc, and equal to the droop resistance (R_O). With the resistive output impedance, the output voltage droops in proportion to the load current at any load current slew rate. This ensures optimal positioning and minimizes the output decoupling.

Because of the multimode feedback structure of the ADP3192A, the feedback compensation must be set to make the converter output impedance work in parallel with the output decoupling to make the load look entirely resistive. Compensation is needed for several poles and zeros created by the output inductor and the decoupling capacitors (output filter).

A type three compensator on the voltage feedback is adequate for proper compensation of the output filter. Equation 35 to Equation 39 are intended to yield an optimal starting point for the design; some adjustments may be necessary to account for PCB and component parasitic effects (see the Tuning the ADP3192A section).