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# 7-Bit, Programmable, Dual-Phase, Mobile, CPU, Synchronous Buck Controller

## ADP3208A

### FEATURES

**Single-chip solution**

- Fully compatible with the Intel® IMVP-6+™ specifications
- Integrated MOSFET drivers
- Selectable 1- or 2-phase operation with up to 1 MHz per phase switching frequency
- Guaranteed  $\pm 8$  mV worst-case differentially sensed core voltage error over temperature
- Automatic power-saving mode maximizes efficiency with light load during deeper sleep operation
- Soft transient control reduces inrush current and audio noise
- Active current balancing between output phases
- Independent current limit and load line setting inputs for additional design flexibility
- Built-in power good blanking supports voltage identification (VID) on-the-fly transients
- 7-bit, digitally programmable DAC with 0.3 V to 1.5 V output
- Short-circuit protection with programmable latch-off delay
- Clock enable output delays the CPU clock until the core voltage is stable
- Output power or current monitor options
- 48-lead LFCSP
- ADP3208A version has 1.0V Boot voltage

### APPLICATIONS

Notebook power supplies for next-generation Intel processors

### General Description

The ADP3208 is a highly efficient, multiphase, synchronous buck switching regulator controller. With its integrated drivers, the ADP3208 is optimized for converting the notebook battery voltage into the core supply voltage required by high performance Intel processors. An internal 7-bit DAC is used to read a VID code directly from the processor and to set the CPU core voltage to a value within the range of 0.3 V to 1.5 V. The phase relationship of the output signals ensures interleaved 2-phase operation.

The ADP3208 uses a multimode architecture run at a programmable switching frequency and optimized for efficiency depending on the output current requirement. The ADP3208 switches between single- and dual-phase operation to maximize efficiency with all load conditions. The chip includes a programmable load line slope function to adjust the output voltage as a function of the load current so that the core voltage is always optimally positioned for a load transient. The ADP3208 also provides accurate and reliable short-circuit protection, adjustable current limiting, and a delayed power good output. The IC supports on-the-fly output voltage changes requested by the CPU.

ADP3208 is specified over the extended commercial temperature range of 0°C to 100°C and is available in a 48-lead LFCSP

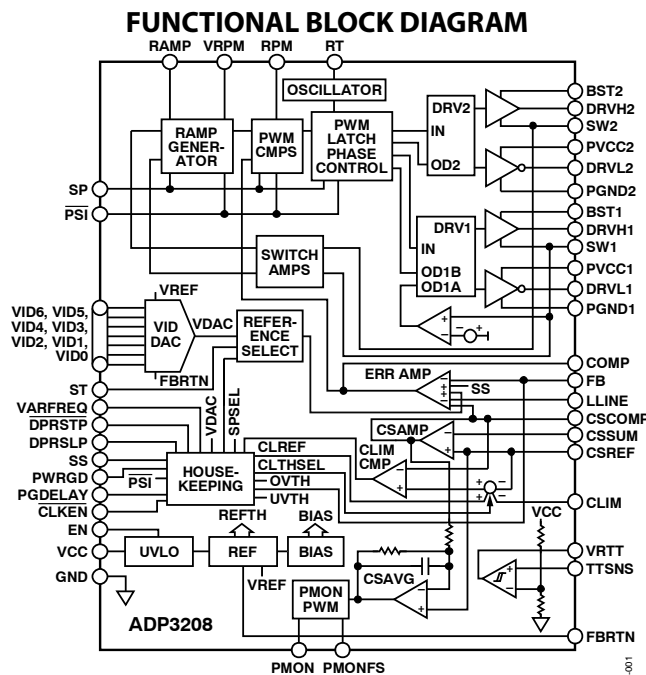


Figure 1.

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## REVISION HISTORY

01/08—Rev 2: Conversion to ON Semiconductor

08/07—Rev Sp1: Changed to ADP3208A

10/05—Rev Sp0: Initial Version

## SPECIFICATIONS

VCC = PVCC1 = PVCC2 = BST1 = BST2 = high = 5 V, FBRTN = GND = SW1 = SW2 = PGND1 = PGND2 = low = 0 V, EN = VARFREQ = high, DPRSLP = 0 V, PSI = 1.05 V, DPRSTP = 0 V, V<sub>VID</sub> = 1.2000 V, T<sub>A</sub> = 0°C to 100°C, unless otherwise noted.<sup>1</sup> Current entering a pin (sunk by the device) has a positive sign.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>VOLTAGE ERROR AMPLIFIER</b>						
Output Voltage Range	V <sub>COMP</sub>		0.8		3.6	V
DC Accuracy	V <sub>FB</sub>	Relative to nominal V <sub>VID</sub> , LLINE = CSREF V <sub>VID</sub> = 0.5000 V to 1.5000 V	-8		+8	mV
		V <sub>VID</sub> = 0.3000 V to 0.4875 V	-10		+10	mV
Boot Voltage	V <sub>BOOT(FB)</sub>	Start-up	0.992	1.0	1.008	V
LLINE Positioning Accuracy	ΔV <sub>FB</sub>	LLINE – CSREF = -80 mV	78	80	82	mV
		LLINE – CSREF = -200 mV	180	200	220	mV
LLINE Input Bias Current	I <sub>LLINE</sub>		-80		+80	nA
Differential Nonlinearity <sup>2</sup>			-1		+1	LSB
Line Regulation	ΔV <sub>FB</sub>	VCC = 4.75 V to 5.25 V		0.005		%
Input Bias Current	I <sub>FB</sub>		-1		+1	μA
FBRTN Current	I <sub>FBRTN</sub>			60	400	μA
Output Current	I <sub>COMP</sub>	FB forced to V <sub>VID</sub> - 3%		-4		mA
		FB forced to V <sub>VID</sub> + 3%		900		μA
Gain Bandwidth Product <sup>2</sup>	GBW	COMP = FB		20		MHz
Slew Rate <sup>2</sup>		C <sub>COMP</sub> = 10 pF		25		V/μs
<b>VID DAC INPUTS</b>						
Input Low Voltage	V <sub>IL</sub>	VID(x)		0.52	0.3	V
Input High Voltage	V <sub>IH</sub>	VID(x)	0.7	0.52		V
Input Current	I <sub>IN(VID)</sub>	Sink current		1		μA
VID Transition Delay Time <sup>2</sup>		VID code change to FB change	400			ns
<b>PWM OSCILLATOR</b>						
Frequency Range <sup>2</sup>		PSI = DPRSTP = 1.05 V, DPRSLP = 0 V	0.3		3	MHz
Frequency	f <sub>OSC</sub>	T <sub>A</sub> = 25°C, RT = 250 kΩ, PWM mode, VARFREQ = high, V <sub>VID</sub> = 1.5000 V		400		kHz
		T <sub>A</sub> = 25°C, RT = 125 kΩ, PWM mode, VARFREQ = high, V <sub>VID</sub> = 1.5000 V		750		kHz
RT Voltage	V <sub>RT</sub>	RT = 250 kΩ to GND, V <sub>VID</sub> = 1.5000 V VARFREQ = low	1.08	1.25	1.32	V
VRPM Reference Voltage	V <sub>VRPM</sub>	I <sub>VRPM</sub> = 0	0.95	1	1.05	V
		I <sub>VRPM</sub> = 120 μA	0.95	1	1.16	V
RPM Output Current	I <sub>RPM</sub>	V <sub>VID</sub> = 1.5000 V, RT = 250 kΩ		-5		μA
RPM Comparator Offset	V <sub>OS(RPM)</sub>	V <sub>COMP</sub> - V <sub>RPM</sub>  , PSI = 0 V	-20	-1	+15	mV
RAMP Input Voltage	V <sub>RAMP</sub>		0.9	1.0	1.1	V
RAMP Input Current Range	I <sub>RAMP</sub>	EN = high	1		50	μA
RAMP Input Current in Shutdown		EN = low or UVLO, RAMP = 19 V		1		μA
<b>CURRENT SENSE AMPLIFIER</b>						
Offset Voltage	V <sub>OS(CSA)</sub>	CSSUM – CSREF	-2.0		+2.0	mV
Input Bias Current	I <sub>CSSUM</sub>		-65		+65	nA
Input Common-Mode Range <sup>2</sup>		CSSUM and CSREF	0		3.5	V
Output Voltage Range	V <sub>CSCOMP</sub>		0.05		2.7	V
Output Current	I <sub>CSCOMP</sub>	Sink current		1		mA
		Source current		-15		mA

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Gain Bandwidth Product <sup>2</sup>	GBW <sub>CSA</sub>			10		MHz
Slew Rate <sup>2</sup>		C <sub>CSCOMP</sub> = 10 pF		10		V/μs
<b>CURRENT BALANCE AMPLIFIER</b>						
Common-Mode Voltage Range <sup>2</sup>	V <sub>SW(x)</sub>		-600		+200	mV
Input Resistance	R <sub>SW(x)</sub>		30	50	60	kΩ
Input Current	I <sub>SW(x)</sub>	SW(x) = 0 V		-3.5		μA
Input Current Matching	ΔI <sub>SW(x)</sub>	SW(x) = 0 V	-5		+5	%
Zero Current Switching Threshold Voltage	V <sub>ZCS(SW1)</sub>	DPRSLP = 3.3 V, DCM		-6		mV
DCM Minimum Off Time Masking	t <sub>OFFMASK</sub>	DPRSLP = 3.3 V, SW1 falling		450		ns
<b>CURRENT LIMIT COMPARATOR</b>						
Output Current	I <sub>CLIM</sub>	R <sub>CLIM</sub> = 125 kΩ		10		μA
Current Limit Threshold Voltage	V <sub>CLTH</sub>	V <sub>CSREF</sub> - V <sub>CSCOMP</sub> , R <sub>CLIM</sub> = 125 kΩ, SP = low (2-phase), PSI = 1.05 V	111	125	139	mV
		V <sub>CSREF</sub> - V <sub>CSCOMP</sub> , R <sub>CLIM</sub> = 125 kΩ, SP = low (2-phase), PSI = 0 V or DPRSLP = low	54	62.5	74	mV
		V <sub>CSREF</sub> - V <sub>CSCOMP</sub> , R <sub>CLIM</sub> = 125 kΩ, SP = high (1-phase)	111	125	139	mV
Current Limit Setting Ratio		V <sub>CL</sub> /V <sub>ILIM</sub> , PSI = 1.05 V		0.1		
		V <sub>CL</sub> /V <sub>ILIM</sub> , PSI = low, SP = low		0.05		
<b>SOFT START/LATCH-OFF TIMER</b>						
Output Current	I <sub>SS</sub>	V <sub>SS</sub> < 1.7 V, start-up	-10	-8	-6	μA
		V <sub>SS</sub> > 1.7 V, normal mode		-48		μA
		V <sub>SS</sub> > 1.7 V, current limit	-2.5	-2	-1.5	μA
Termination Threshold Voltage	V <sub>TH(SS)</sub>	Start-up, SS rising	1.6	1.7	1.8	V
Normal Mode Operating Voltage		CLKEN = low		2.9		V
Current Limit Latch-Off Voltage	V <sub>LOFF(SS)</sub>	Current limit or PWRGD failure, SS falling	1.55	1.65	1.8	V
<b>SOFT TRANSIENT CONTROL</b>						
ST Sourcing Current	I <sub>SOURCE(ST)</sub>	Fast exit from deeper sleep mode, DPRSLP = 0 V, ST = V <sub>DAC</sub> - 0.3 V		-9		μA
		Slow exit from deeper sleep mode, DPRSLP = 3.3 V, DPRSTP = 0, ST = V <sub>DAC</sub> - 0.3 V		-2.5		μA
ST Sinking Current	I <sub>SINK(ST)</sub>	Slow entry to deeper sleep, DPRSLP = 3.3 V, ST = V <sub>DAC</sub> + 0.3 V		2.5		μA
ST Offset Voltage	V <sub>OS(ST)</sub>	ST - V <sub>VID</sub>   at the end of PWRGD masking	-25		+25	mV
Minimum Capacitance <sup>2</sup>	C <sub>ST</sub>		100			pF
Extended PWRGD Masking Comparator Voltage Threshold	V <sub>TH(ST)</sub>	ST - V <sub>VID</sub>  , DPRSLP = 3.3 V, ST falling		170		mV
<b>DIGITAL CONTROL INPUTS</b>						
Input Low Voltage	V <sub>IL</sub>	PSI, DPRSTP			0.3	V
		VARFREQ, SP			0.7	V
		DPRSLP, EN			1.0	V
Input High Voltage	V <sub>IH</sub>	PSI, DPRSTP	0.7			V
		VARFREQ, SP	4			V
		DPRSLP, EN	2.3			V
Input Current	I <sub>IN</sub>	DPRSTP, VARFREQ, DPRSLP, SP		20		nA
		EN = low or EN = high		20		nA
		EN = V <sub>TH(EN)</sub> , high-to-low or low-to-high transition		60		μA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		DPRSTP = high, PSI = high		1		$\mu\text{A}$
		PSI = low		-100		nA
<b>THERMAL THROTTLING/CROWBAR DISABLE CONTROL</b>						
TTSNS Voltage Range <sup>2</sup>		Temperature sensing	0.4		5	V
TTSNS VR TT Threshold Voltage	$V_{VRTT(TTSNS)}$	Crowbar disable threshold disable	0		50	mV
TTSNS VR TT Threshold Hysteresis		VCC = 5 V, TTSNS falling	2.45	2.5	2.55	V
TTSNS Crowbar Disable Threshold Voltage	$V_{CBDIS(TTSNS)}$		50	95		mV
TTSNS Input Current		TTSNS > 1.0 V, temperature sensing	-1		+1	$\mu\text{A}$
		TTSNS = 0 V, disabling overvoltage protection		-3		$\mu\text{A}$
VRTT Output Low Voltage	$V_{OL(VRTT)}$	$I_{SINK(VRTT)} = 400 \mu\text{A}$		50	100	mV
VRTT Output High Voltage	$V_{OH(VRTT)}$	$I_{SOURCE(VRTT)} = -400 \mu\text{A}$	4	5		V
<b>POWER GOOD</b>						
CSREF Undervoltage Threshold	$V_{UV(CSREF)}$	Relative to $V_{VID} = 0.5 \text{ V to } 1.5 \text{ V}$		-300		mV
		Relative to $V_{VID} = 0.3125 \text{ V to } 0.4875 \text{ V}$	-160			mV
CSREF Overvoltage Threshold	$V_{OV(CSREF)}$	Relative to $V_{VID} = 0.5 \text{ V to } 1.5 \text{ V}$	150	200	250	mV
CSREF Crowbar (Overvoltage Protection) Threshold	$V_{CB(CSREF)}$	Relative to FBRTN	1.65	1.7	1.75	V
CSREF Reverse Voltage Detection Threshold	$V_{RVP(CSREF)}$	Relative to FBRTN				
		CSREF falling	-400	-300		mV
		CSREF rising		-60	-5	mV
PWRGD Output Low Voltage	$V_{OL(PWRGD)}$	$I_{SINK(PWRGD)} = 4 \text{ mA}$		70	200	mV
PWRGD Output Leakage Current		$V_{PWRGD} = 5 \text{ V}$		0.03	3	$\mu\text{A}$
Power Good Delay Timer						
PGDELAY Voltage Detection Threshold	$V_{TH(PGDELAY)}$			2.9		V
PGDELAY Charge Current	$I_{PGDELAY}$	$V_{PGDELAY} = 2.0 \text{ V}$		-3		$\mu\text{A}$
PGDELAY Discharge Resistance	$R_{PGDELAY}$	$V_{PGDELAY} = 0.2 \text{ V}$		600		$\Omega$
PWRGD Masking Time				130		$\mu\text{s}$
<b>CLOCK ENABLE</b>						
Output Low Voltage		$I_{SINK} = 4 \text{ mA}$		100	400	mV
Output Leakage Current		CLKEN = 5 V, $V_{SS} = \text{GND}$			1	$\mu\text{A}$
<b>POWER MONITOR</b>						
PMON Output Resistance		$I_{SINK} = 2 \text{ mA}$		16		$\Omega$
PMON Leakage Current		PMON = 5 V			1	$\mu\text{A}$
PMON Oscillator Frequency		PMONFS = 2 V		320		kHz
PMONFS Voltage Range <sup>2</sup>			1.5		4	V
PMONFS Output Current		PMONFS = 2.5 V		-10		$\mu\text{A}$
<b>HIGH-SIDE MOSFET DRIVERS</b>						
DRVH Output Resistance, Sourcing Current		BST – SW = 4.6 V		1.9	3.3	$\Omega$
DRVH Output Resistance, Sinking Current		BST – SW = 4.6 V		1.5	3	$\Omega$
Transition Times	$t_{rDRVH}$	BST – SW = 4.6 V, $C_L = 3 \text{ nF}$ , see Figure 2		10	30	ns
	$t_{fDRVH}$	BST – SW = 4.6 V, $C_L = 3 \text{ nF}$ , see Figure 2		8	25	ns
Propagation Delay Time	$t_{pdhDRVH}$	BST – SW = 4.6 V, see Figure 2		16	70	ns
BST Quiescent Current		EN = low, shutdown		5		$\mu\text{A}$

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		EN = high, no switching		120		μA
<b>LOW-SIDE MOSFET DRIVERS</b>						
Output Resistance, Sourcing Current				1.8	3.3	Ω
Output Resistance, Sinking Current				1.4	2.5	Ω
Transition Times	$t_{rDRVL}$	$C_L = 3 \text{ nF}$ , see Figure 2		11	30	ns
	$t_{fDRVL}$	$C_L = 3 \text{ nF}$ , see Figure 2		9	25	ns
Propagation Delay Time	$tpd_{DRVL}$	$C_L = 3 \text{ nF}$ , see Figure 2		13	30	ns
SW Transition Timeout	$t_{TO(SW)}$	BST – SW = 4.6 V	80	130	300	ns
Zero Voltage Switching Detection Threshold	$V_{ZVS(SW)}$			2.2		V
PVCC Quiescent Current		EN = low, shutdown		13		μA
		EN = high, no switching		180		μA
<b>SUPPLY</b>						
Supply Voltage Range <sup>2</sup>	$V_{CC}$		4.5		5.5	V
Supply Current		EN = high, normal mode		5.5	10	mA
		EN = low, shutdown		32	150	μA
VCC OK Threshold Voltage	$V_{CCOK}$	VCC rising		4.4	4.5	V
VCC UVLO Threshold Voltage	$V_{CCUVLO}$	VCC falling	4.0	4.2		V
UVLO Hysteresis <sup>2</sup>			150			mV

<sup>1</sup> All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

<sup>2</sup> Guaranteed by design or characterization, not production tested.

## TIMING DIAGRAM

Timing is referenced to the 90% and 10% points, unless otherwise noted.

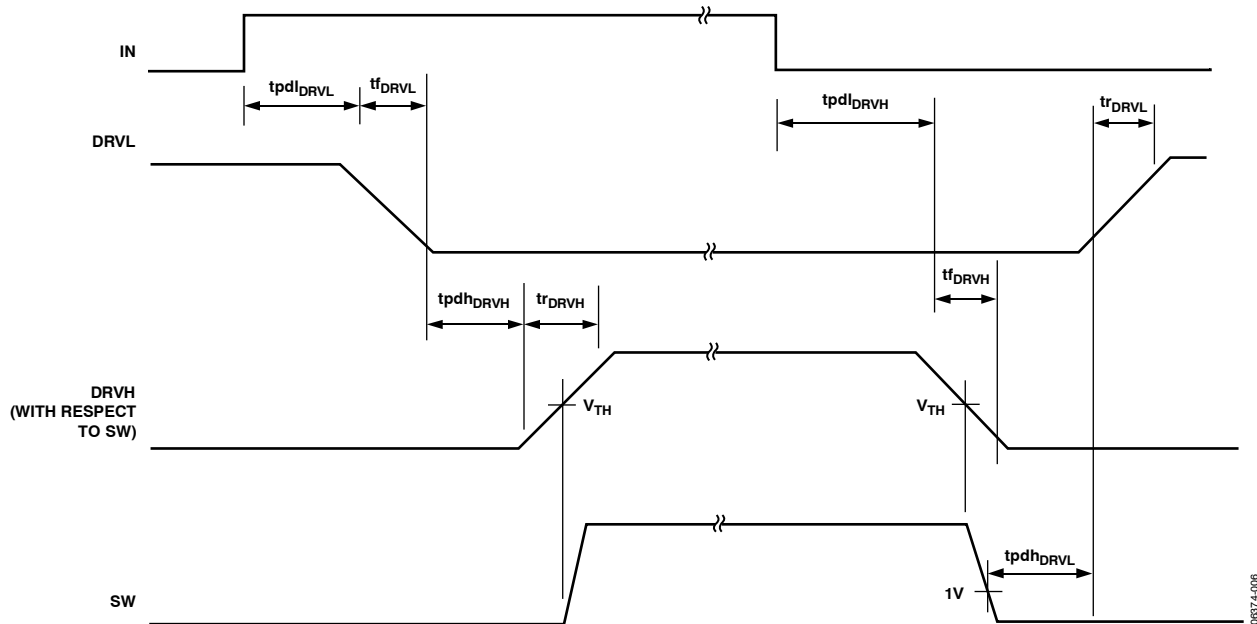


Figure 2. Timing Diagram

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## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC, PVCC1, PVCC2	-0.3 V to +6 V
FBRTN, PGND1, PGND2	-0.3 V to +0.3 V
BST1, BST2	
DC	-0.3 V to +25 V
t < 200 ns	-0.3 V to +30 V
BST1 to SW1, BST2 to SW2	-0.3 V to +6 V
DRVH1, DRVH2, SW1, SW2	
DC	-5 V to +20 V
t < 200 ns	-10 V to +25 V
DRVH1 to SW1, DRVH2 to SW2,	-0.3 V to +6 V
DRVL1 to PGND1, DRVL2 to PGND2	
DC	-0.3 V to +6 V
T < 200 ns	-5V to +6V
RAMP (in Shutdown)	
DC	-0.3 V to +20 V
t < 200 ns	-0.3 V to +25 V
All Other Inputs and Outputs	-0.3 V to +6 V
Storage Temperature	-65°C to +150°C
Operating Ambient Temperature Range	0°C to 100°C
Operating Junction Temperature	125°C
Thermal Impedance ( $\theta_{JA}$ ) 2-Layer Board	40°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Infrared (15 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

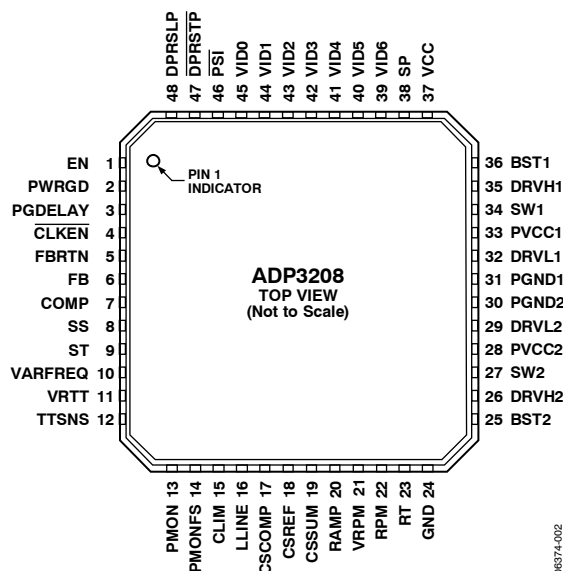


Figure 3. LFCSP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	EN	Enable Input. Driving the pin low shuts down the chip, disables the driver outputs, pulls PWRGD and VRTT low, and pulls CLKEN high.
2	PWRGD	Power Good Output. Open-drain output. A low logic state means that the output voltage is outside of the VID DAC defined range.
3	PGDELAY	Power Good Delay Setting Input/Output. A capacitor connected from this pin to GND sets the power good delay time.
4	CLKEN	Clock Enable Output. Open-drain output. A low logic state enables the CPU internal PLL clock to lock to the external clock.
5	FBRTN	Feedback Return Input/Output. This pin remotely senses the CPU core voltage. It is also used as the ground return for the VID DAC and the voltage error amplifier blocks.
6	FB	Voltage Error Amplifier Feedback Input. The inverting input of the voltage error amplifier.
7	COMP	Voltage Error Amplifier Output and Frequency Compensation Point.
8	SS	Soft Start and Latch-Off Delay Setting Input/Output. An external capacitor from this pin to GND sets the soft start ramp-up time and the current limit latch-off delay ramp-down time.
9	ST	Soft Transient Slew Rate Timing Input/Output. A capacitor from this pin to GND sets the slew rate of the output voltage when it transitions from one VID setting to another, including boot-to-active VID, VID on the fly, and deeper sleep entry and exit transients.
10	VARFREQ	Variable Frequency Enable Input. A high logic state enables the PWM clock frequency to vary with VID code.
11	VRTT	Voltage Regulator Thermal Throttling Output. Logic high state indicates that the voltage regulator temperature at the remote sensing point exceeded a set alarm threshold level.
12	TTSNS	Thermal Throttling Sense and Crowbar Disable Input. A resistor divider where the upper resistor is connected to VCC, the lower resistor (NTC thermistor) is connected to GND, and the center point is connected to this pin and acts as a temperature sensor half bridge. Connecting TTSNS to GND disables the thermal throttling function and disables the crowbar, or overvoltage protection (OVP), feature of the chip.
13	PMON	Power Monitor Output. Open-drain output. A pull-up resistor from PMON to CSREF provides a duty cycle modulated power output signal. An external RC network can be used to convert the digital signal stream to an averaged power analog output voltage.
14	PMONFS	Power Monitor Full-Scale Setting Input/Output. A resistor from this pin to GND sets the full-scale value of the PMON output signal.
15	CLIM	Current Limit Setting Input/Output. An external resistor from this pin to GND sets the current limit threshold of the converter.

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Pin No.	Mnemonic	Description
16	LLINE	Load Line Programming Input. The center point of a resistor divider connected between CSREF and CSSUM can be tied to this pin to set the load line slope.
17	CSCOMP	Current Sense Amplifier Output and Frequency Compensation Point.
18	CSREF	Current Sense Reference Input. This pin must be connected to the common point of the output inductors. The node is shorted to GND through an internal switch when the chip is disabled to provide soft stop transient control of the converter output voltage.
19	CSSUM	Current Sense Summing Input. External resistors from each switch node to this pin sum the inductor currents to provide total current information.
20	RAMP	PWM Ramp Slope Setting Input. An external resistor from the converter input voltage node to this pin sets the slope of the internal PWM stabilizing ramp used for phase-current balancing.
21	VRPM	RPM Mode Reference Voltage Output.
22	RPM	Ramp Pulse Modulation Current Source Output. A resistor between this pin and VRPM sets the RPM comparator upper threshold.
23	RT	PWM Oscillator Frequency Setting Input. An external resistor from this pin to GND sets the PWM oscillator frequency.
24	GND	Analog and Digital Signal Ground.
25	BST2	High-Side Bootstrap Supply for Phase 2. A capacitor from this pin to SW2 holds the bootstrapped voltage while the high-side MOSFET is on.
26	DRVH2	High-Side Gate Drive Output for Phase 2.
27	SW2	Current Balance Input for Phase 2 and Current Return for High-Side Gate Drive.
28	PVCC2	Power Supply Input/Output of Low-side Gate Driver for Phase 2.
29	DRVL2	Low-Side Gate Drive Output for Phase 2.
30	PGND2	Low-Side Driver Power Ground for Phase 2.
31	PGND1	Low-Side Driver Power Ground for Phase 1.
32	DRVL1	Low-Side Gate Drive Output for Phase 1.
33	PVCC1	Power Supply Input/Output of Low-Side Gate Driver for Phase 1.
34	SW1	Current Balance Input for Phase 1 and Current Return For High-Side Gate Drive.
35	DRVH1	High-Side Gate Drive Output for Phase 1.
36	BST1	High-Side Bootstrap Supply for Phase 1. A capacitor from this pin to SW1 holds the bootstrapped voltage while the high-side MOSFET is on.
37	VCC	Power Supply Input/Output of the Controller.
38	SP	Single-Phase Select Input. Logic high state sets single-phase configuration.
39 to 45	VID6 to VID0	Voltage Identification DAC Inputs. A 7-bit word (the VID code) programs the DAC output voltage, the reference voltage of the voltage error amplifier without a load (see the VID code table, Table 6).
46	PSI	Power State Indicator Input. Driving this pin low forces the controller to operate in single-phase mode.
47	DPRSTP	Deeper Stop Control Input. The logic state of this pin is usually complementary to the state of the DPRSLP pin; however, during slow deeper sleep exit, both pins are logic low.
48	DPRSLP	Deeper Sleep Control Input.

TEST CIRCUITS

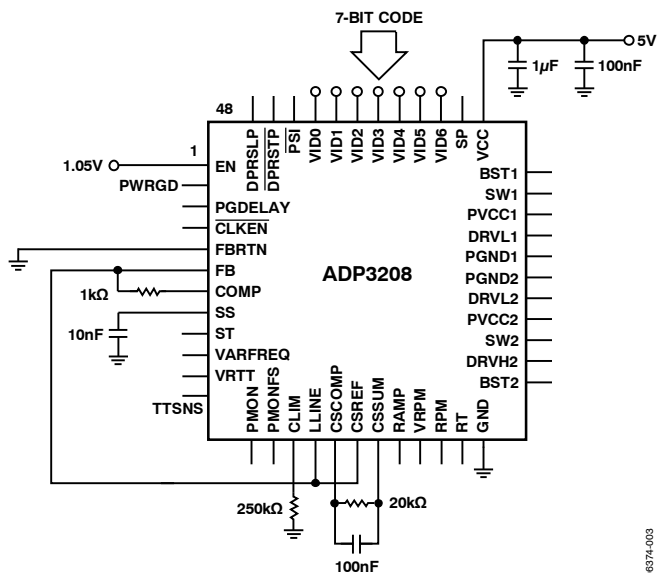
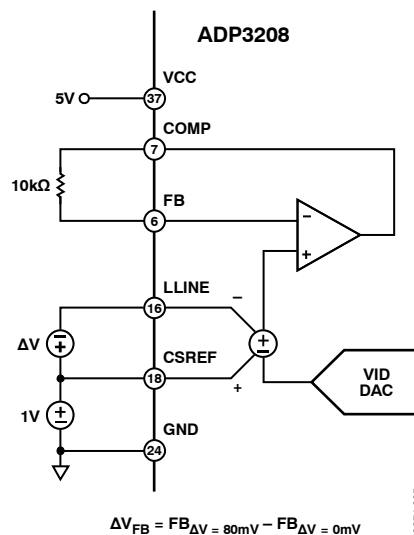


Figure 4. Closed-Loop Output Voltage Accuracy

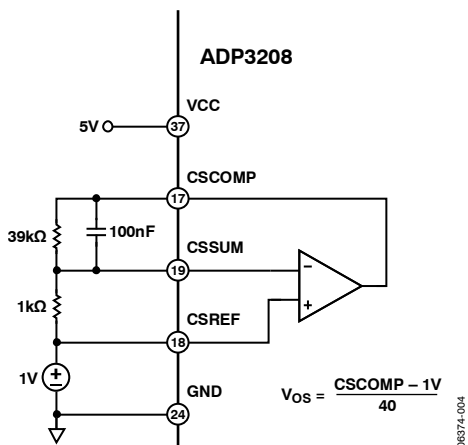
06374-003



$$\Delta V_{FB} = FB_{\Delta V} = 80mV - FB_{\Delta V} = 0mV$$

Figure 6. Positioning Accuracy

06374-005



$$V_{os} = \frac{CSCOMP - 1V}{40}$$

Figure 5. Current Sense Amplifier,  $V_{os}$

06374-004

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{VID} = 1.5\text{ V}$ ,  $T_A = 20^\circ\text{C}$  to  $100^\circ\text{C}$ , unless otherwise noted.

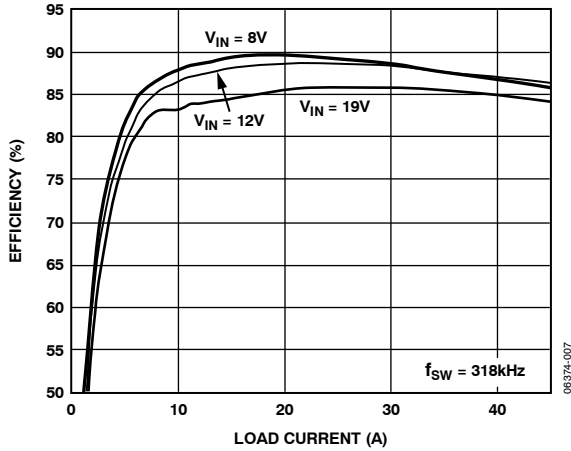


Figure 7. PWM Mode Efficiency vs. Load Current

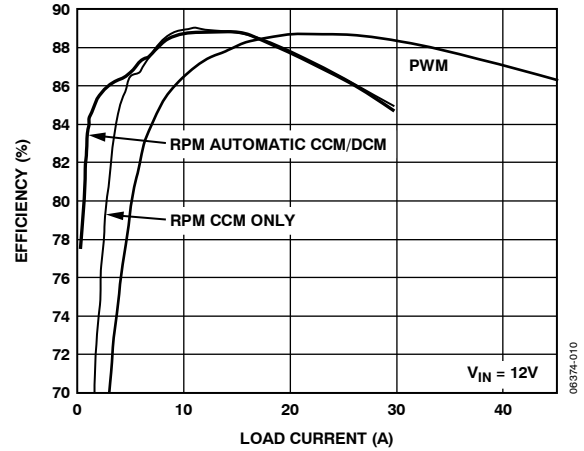


Figure 10. Efficiency vs. Load Current in All Modes

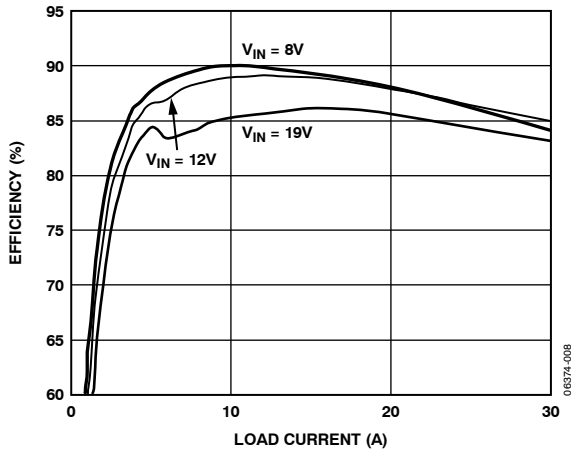


Figure 8. RPM Mode Efficiency vs. Load Current in CCM Only

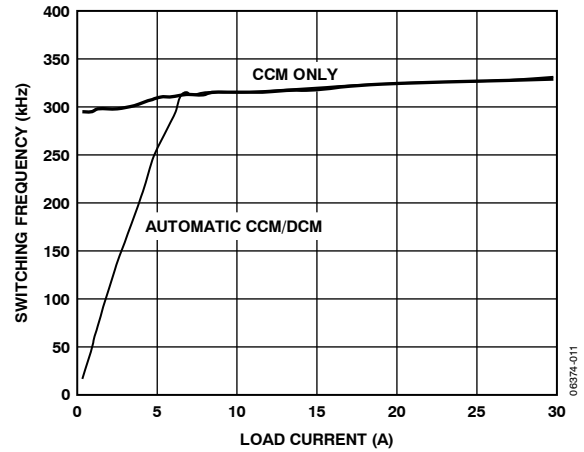


Figure 11. Switching Frequency vs. Load Current in RPM

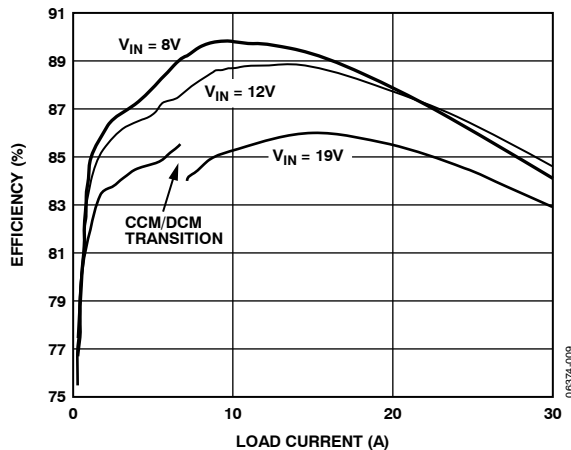


Figure 9. RPM Mode Efficiency vs. Load Current Automatic in CCM/DCM

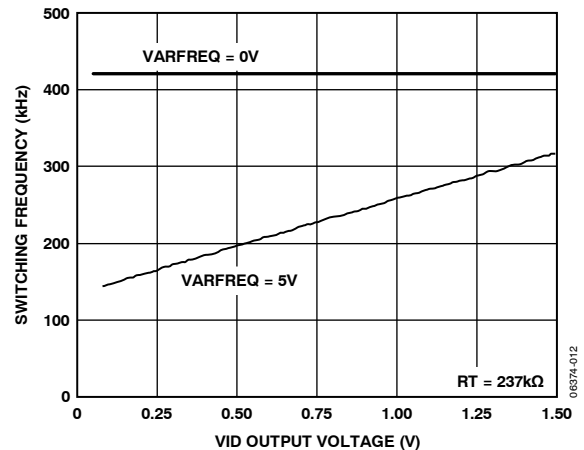


Figure 12. Switching Frequency vs. VID Output Voltage in PWM

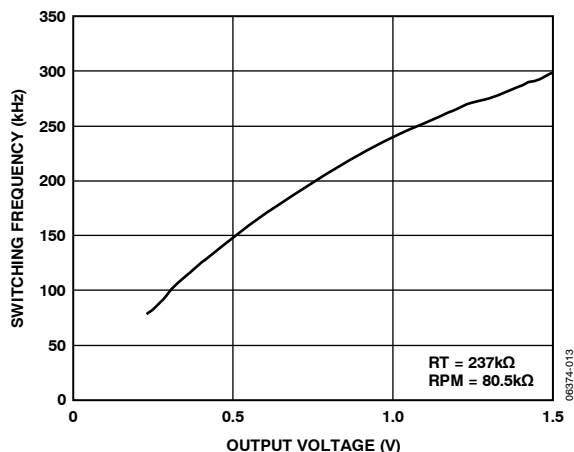


Figure 13. Switching Frequency vs. Output Voltage in RPM

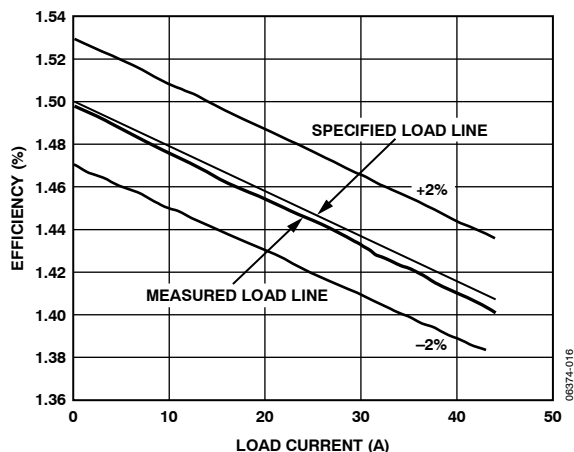


Figure 16. Load Line Accuracy

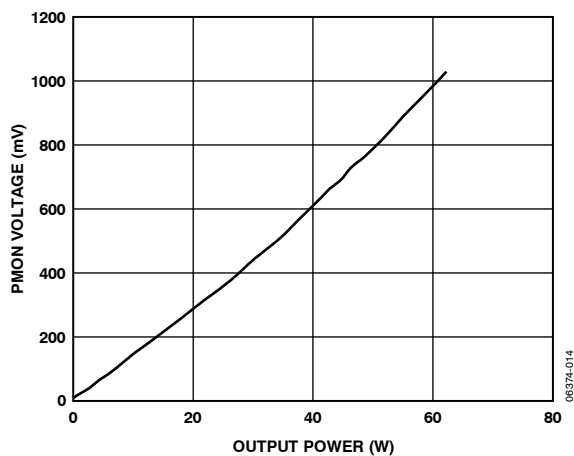


Figure 14. PMON Voltage vs. Output Power

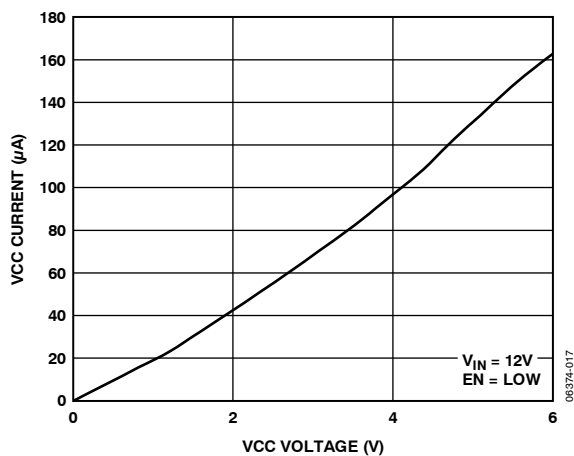


Figure 17. VCC Current vs. VCC Voltage with Enable Low

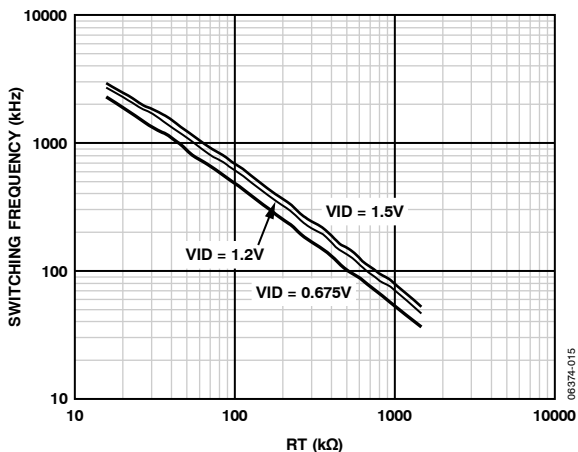


Figure 15. Per Phase Switching Frequency vs. RT Resistor

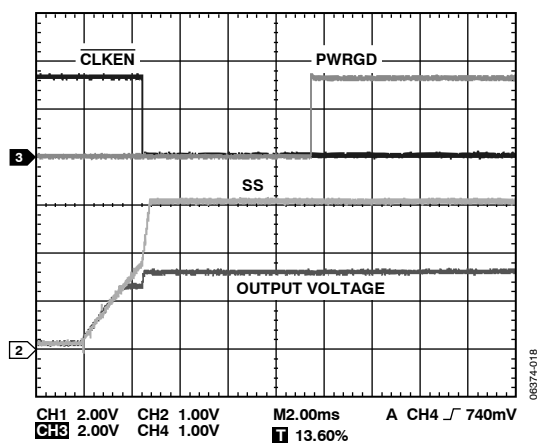


Figure 18. Start-Up Waveforms

# ADP3208A

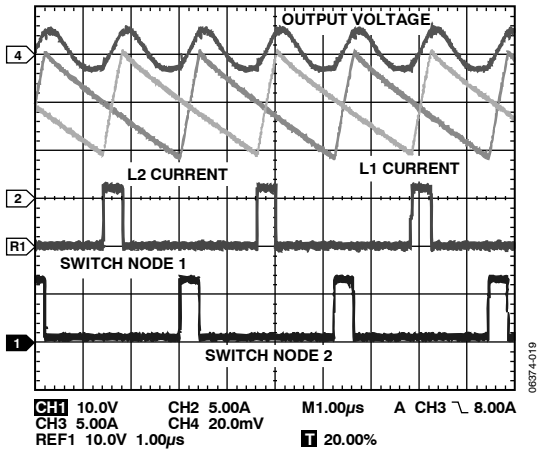


Figure 19. Dual-Phase, Interleaved PWM Waveform, 20 A Load

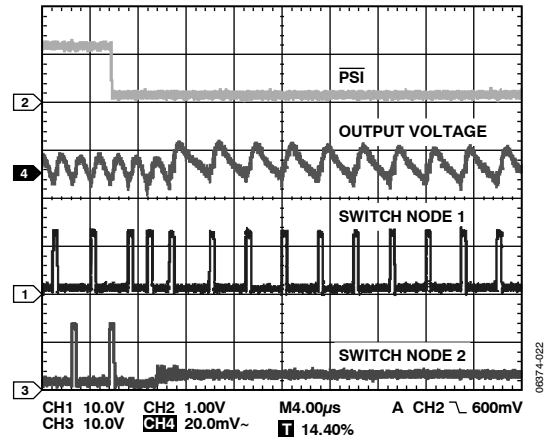


Figure 22. PDI Transition

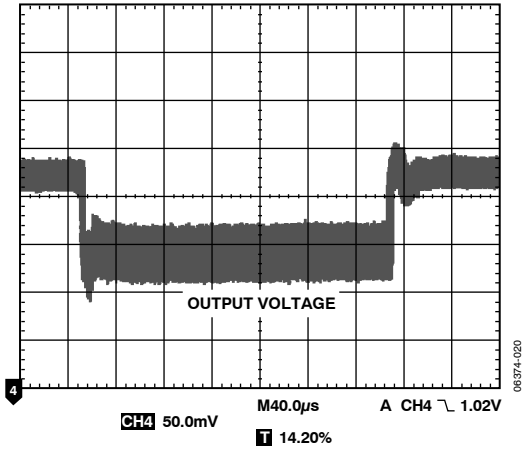


Figure 20. Load Transient 9 A to 44 A

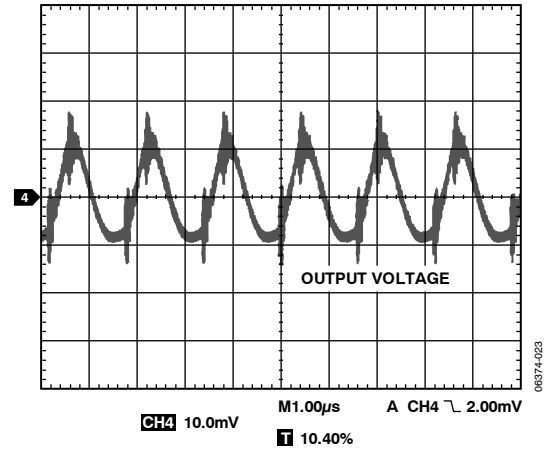


Figure 23. PWM Mode Output Ripple, 40 A Load,  $V_{IN} = 12 V$

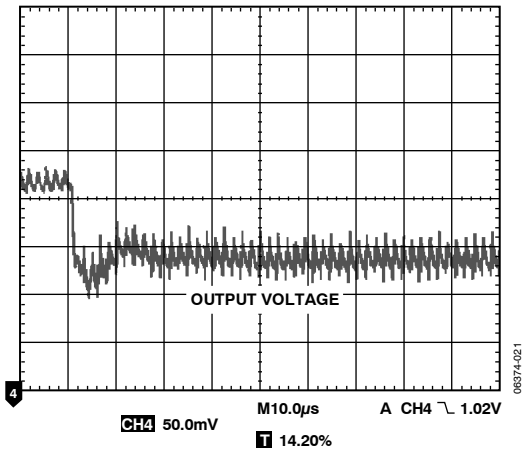


Figure 21. Load Transient 9 A to 44 A

## THEORY OF OPERATION

The ADP3208 combines multimode pulse width modulated (PWM) control and ramp pulse modulated (RPM) control with multiphase logic outputs for use in single- and dual-phase synchronous buck CPU core supply power converters. The internal 7-bit VID DAC conforms to the Intel IMVP-6+ specifications.

Multiphase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling high currents in a single-phase converter would put too high of a thermal stress on system components such as the inductors and MOSFETs.

The multimode control of the ADP3208 is a stable, high performance architecture that includes

- Current and thermal balance between phases
- High speed response at the lowest possible switching frequency and minimal count of output decoupling capacitors
- Minimized thermal switching losses due to lower frequency operation
- High accuracy load line regulation
- High current output by supporting 2-phase operation
- Reduced output ripple due to multiphase ripple cancellation
- High power conversion efficiency with heavy and light loads
- Increased immunity from noise introduced by PC board layout constraints
- Ease of use due to independent component selection
- Flexibility in design by allowing optimization for either low cost or high performance

### NUMBER OF PHASES

The number of operational phases can be set by the user. Tying the SP pin to the VCC pin forces the chip into single-phase operation; otherwise, dual-phase operation is automatically selected and the chip switches between single- and dual-phase modes as the load changes to optimize power conversion efficiency.

In dual-phase configuration, SP is low and the timing relationship between the two phases is determined by internal circuitry that monitors the PWM outputs. Because each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one output can be active at a time, permitting overlapping phases.

### OPERATION MODES

The number of phases can be static (see the Number of Phases section) or dynamically controlled by system signals to optimize the power conversion efficiency with heavy and light loads.

If SP is set low (user-selected dual-phase mode) during a VID transient or with a heavy load condition (indicated by DPRSLP being low and PSI being high), the ADP3208 runs in 2-phase, interleaved PWM mode to achieve minimal  $V_{CORE}$  output voltage ripple and the best transient performance possible. If the load becomes light (indicated by PSI being low or DPRSLP being high), ADP3208 switches to single-phase mode to maximize the power conversion efficiency.

In addition to changing the number of phases, the ADP3208 is also capable of dynamically changing the control method. In dual-phase operation, the ADP3208 runs in PWM mode, where the switching frequency is controlled by the master clock. In single-phase operation (commanded by the PSI low state), the ADP3208 runs in RPM mode, where the switching frequency is controlled by the ripple voltage appearing on the COMP pin. In RPM mode, the DRVH1 pin is driven high each time the COMP pin voltage rises to a voltage limit set by the VID voltage and an external resistor connected between the VRPM and RPM pins. If the device is in single-phase mode and the system signal DPRSLP is asserted high during the deeper sleep mode of CPU operation, the ADP3208 continues running in RPM mode but offers the option of turning off the low-side (synchronous rectifier) MOSFET when the inductor current drops to 0. Turning off the low-side MOSFETs at the zero current crossing prevents reversed inductor current build up and breaks synchronous operation of high- and low-side switches. Due to the asynchronous operation, the switching frequency becomes slower as the load current decreases, resulting in good power conversion efficiency with very light loads.

Table 4 summarizes how the ADP3208 dynamically changes the number of active phases and transitions the operation mode based on system signals and operating conditions.



# ADP3208A

**Table 4. Phase Number and Operation Modes<sup>1</sup>**

PSI No.	DPRSLP	VID Transition <sup>2</sup>	Current Limit	No. of Phases Selected by the User	No. of Phases in Operation	Operation Modes <sup>3</sup>
*	*	Yes	*	N [2 or 1]	N	PWM, CCM only
1	0	No	*	N [2 or 1]	N	PWM, CCM only
0	0	No	No	*	1	RPM, CCM only
0	0	No	Yes	*	1	PWM, CCM only
*	1	No	No	*	1	RPM, automatic CCM/DCM
*	1	No	Yes	*	1	PWM, CCM only

<sup>1</sup> \* = don't care.

<sup>2</sup> VID transient period is the time following any VID change, including entry into and exit from deeper sleep mode. The duration of VID transient period is the same as that of PWRGD masking time.

<sup>3</sup> CCM stands for continuous current mode, and DCM stands for discontinuous current mode.

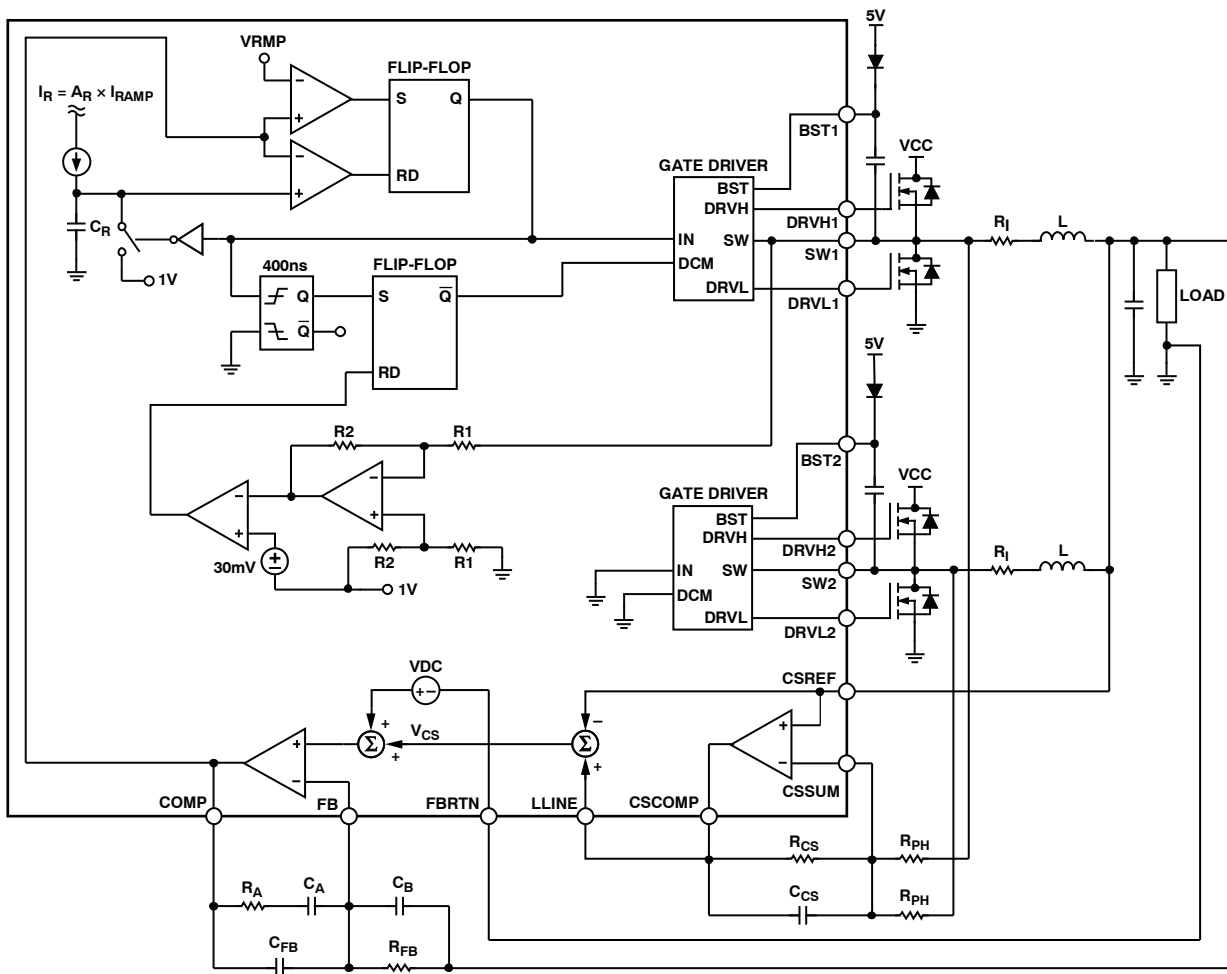


Figure 24. Single-Phase RPM Mode

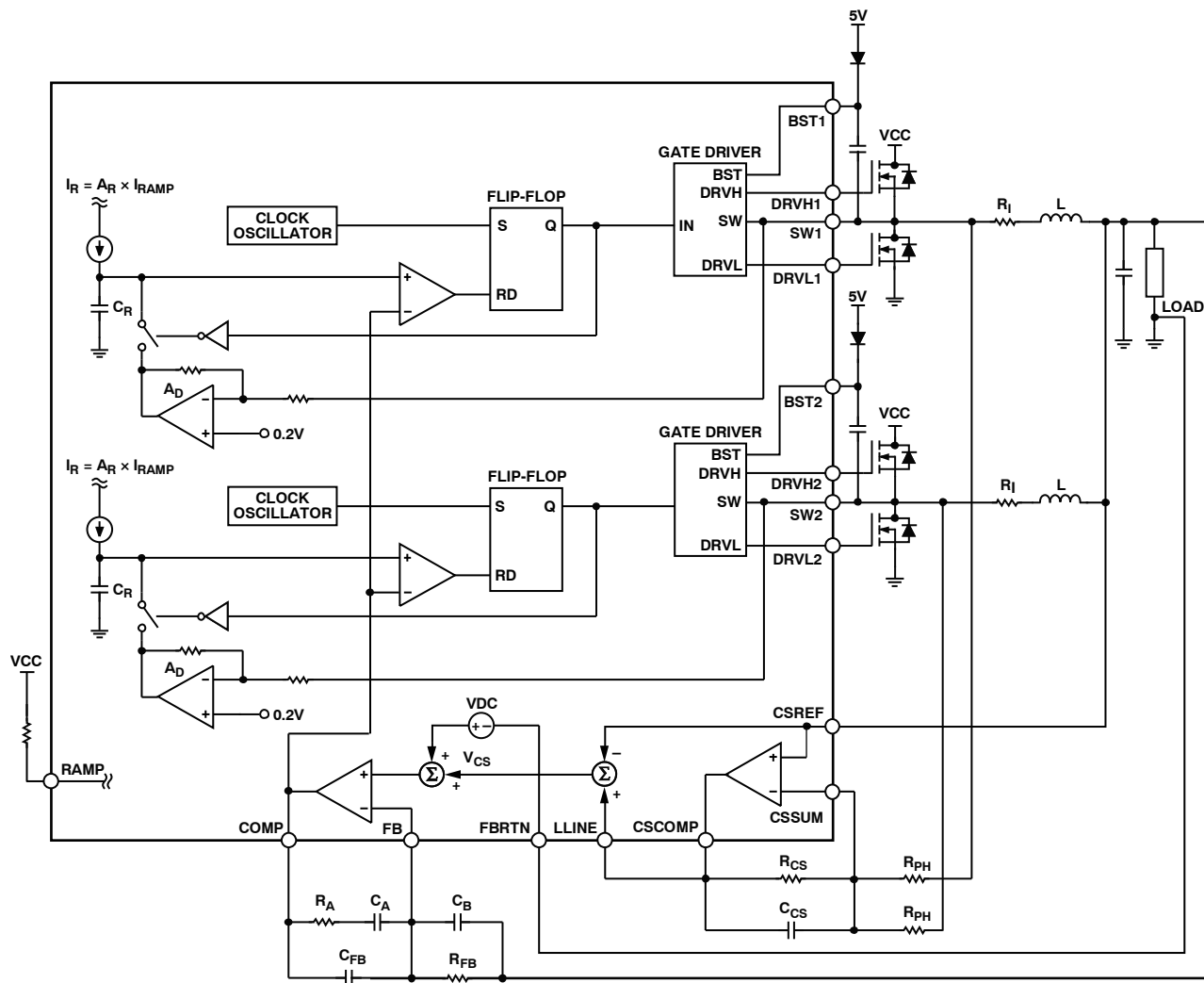


Figure 25. Dual-Phase PWM Mode

## Setting Switch Frequency

### Master Clock Frequency in PWM Mode

When the ADP3208 runs in PWM, the clock frequency of the ADP3208 is set by an external resistor connected from the RT pin to GND. The frequency is constant at a given VID code but varies with the VID voltage: The lower the VID voltage, the lower the clock frequency. The variation of clock frequency with VID voltage maintains constant  $V_{\text{CORE}}$  ripple and improves power conversion efficiency at lower VID voltages. Figure 15 shows the relationship between clock frequency and VID voltage, parameterized by RT resistance.

To determine the switching frequency per phase, divide the clock by the number of phases in use.

### Switching Frequency in RPM Mode— Single-Phase Operation

In single-phase RPM mode, the switching frequency is controlled by the ripple voltage on the COMP pin, rather than by the master clock. Each time the COMP pin voltage exceeds the RPM pin voltage threshold level determined by the VID voltage and the external resistor connected between RPM and VRPM, an internal ramp signal is started and DRVH1 is driven high. The slew rate of the internal ramp is programmed by the current entering the RAMP pin. One-third of the RAMP current charges an internal ramp capacitor (5 pF typical) and creates a ramp. When the internal ramp signal intercepts the COMP voltage, the DRVH1 pin is reset low.

In continuous current mode, the switching frequency of RPM operation is almost constant. While in discontinuous current conduction mode, the switching frequency is reduced as a function of the load current.

## DIFFERENTIAL SENSING OF OUTPUT VOLTAGE

The ADP3208 combines differential sensing with a high accuracy VID DAC, referenced by a precision band gap source and a low offset error amplifier, to meet the rigorous accuracy requirement of the Intel IMVP-6+ specification. In steady-state mode, the combination of the VID DAC and error amplifier maintain the output voltage for a worst-case scenario within  $\pm 8$  mV of the full operating output voltage and temperature range.

The CPU core output voltage is sensed between the FB and FBRTN pins. FB should be connected through a resistor to the positive regulation point—the VCC remote sensing pin of the microprocessor. FBRTN should be connected directly to the negative remote sensing point—the  $V_{\text{SS}}$  sensing point of the CPU. The internal VID DAC and precision voltage reference are referenced to FBRTN and have a maximum current of 200  $\mu\text{A}$  for guaranteed accurate remote sensing.

## OUTPUT CURRENT SENSING

The ADP3208 includes a dedicated current sense amplifier (CSA) to monitor the total output current of the converter for

proper voltage positioning vs. load current and for over current detection. Sensing the current delivered to the load is an inherently more accurate method than detecting peak current or sampling the current across a sense element, such as the low-side MOSFET. The current sense amplifier can be configured several ways, depending on system optimization objectives, and the current information can be obtained by

- Output inductor ESR sensing without the use of a thermistor for the lowest cost
- Output inductor ESR sensing with the use of a thermistor that tracks inductor temperature to improve accuracy
- Discrete resistor sensing for the highest accuracy

At the positive input of the CSA, the CSREF pin is connected to the output voltage. At the negative input (that is, the CSSUM pin of the CSA), signals from the sensing element (in the case of inductor DCR sensing, signals from the switch node side of the output inductors) are summed together by series summing resistors. The feedback resistor between the CSCOMP and CSSUM pins sets the gain of the current sense amplifier, and a filter capacitor is placed in parallel with this resistor. The current information is then given as the voltage difference between the CSCOMP and CSREF pins. This signal is used internally as a differential input for the current limit comparator.

An additional resistor divider connected between the CSCOMP and CSREF pins with the midpoint connected to the LLINE pin can be used to set the load line required by the microprocessor specification. The current information to set the load line is then given as the voltage difference between the LLINE and CSREF pins. This configuration allows the load line slope to be set independently from the current limit threshold. If the current limit threshold and load line do not have to be set independently, the resistor divider between the CSCOMP and CSREF pins can be omitted and the CSCOMP pin can be connected directly to LLINE. To disable voltage positioning entirely (that is, to set no load line), LLINE should be tied to CSREF.

To provide the best accuracy for current sensing, the CSA has a low offset input voltage and the sensing gain is set by an external resistor ratio.

## ACTIVE IMPEDANCE CONTROL MODE

To control the dynamic output voltage droop as a function of the output current, the signal that is proportional to the total output current, converted from the voltage difference between LLINE and CSREF, can be scaled to be equal to the required droop voltage. This droop voltage is calculated by multiplying the droop impedance of the regulator by the output current. This value is used as the control voltage of the PWM regulator. The droop voltage is subtracted from the DAC reference output voltage, and the resulting voltage is used as the voltage positioning setpoint. The arrangement results in an enhanced feed-forward response.

## CURRENT CONTROL MODE AND THERMAL BALANCE

The ADP3208 has individual inputs for monitoring the current of each phase. The phase current information is combined with an internal ramp to create a current-balancing feedback system that is optimized for initial current accuracy and dynamic thermal balance. The current balance information is independent from the total inductor current information used for voltage positioning described in the Active Impedance Control Mode section.

The magnitude of the internal ramp can be set so that the transient response of the system is optimal. The ADP3208 monitors the supply voltage to achieve feed-forward control whenever the supply voltage changes. A resistor connected from the power input voltage rail to the RAMP pin determines the slope of the internal PWM ramp. More detail about programming the ramp is provided in the Application Information section.

The ADP3208 should not require external thermal balance circuitry with good layout. However, if mismatch is desired due to uneven cooling in phase, external resistors can be added to individually control phase currents as long as the phase currents are mismatched by less than 30%. If unwanted mismatch exceeds 30%, a new layout that improves phase symmetry should be considered.

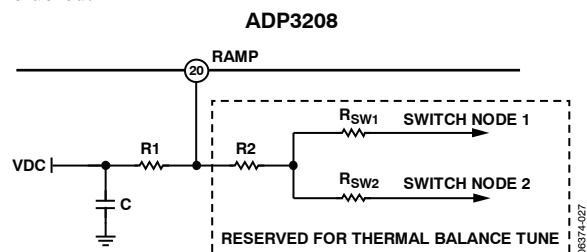


Figure 26. Optional Current Balance Resistors

In 2-phase operation, alternate cycles of the internal ramp control the duty cycle of the separate phases. Figure 26 shows the addition of two resistors from each switch node to the RAMP pin; this modifies the ramp-charging current individually for each phase. During Phase 1, SW Node 1 is high (practically at the input voltage potential) and SW Node 2 is low (practically at the ground potential). As a consequence, the RAMP pin, through the R2 resistor, sees the tap point of a divider connected to the input voltage, where  $R_{SW1}$  is the upper element and  $R_{SW2}$  is the lower element of the divider. During Phase 2, the voltages on SW Node 1 and SW Node 2 switch and the resistors swap functions. Tuning  $R_{SW1}$  and  $R_{SW2}$  allows current to be optimally set for each phase. To increase current for a given phase, decrease  $R_{SW}$  for that phase.

## VOLTAGE CONTROL MODE

A high-gain bandwidth error amplifier is used for the voltage mode control loop. The non-inverting input voltage is set via

the 7-bit VID DAC. The VID codes are listed in Table 6. The non-inverting input voltage is offset by the droop voltage as a function of current, commonly known as active voltage positioning. The output of the error amplifier is the COMP pin, which sets the termination voltage of the internal PWM ramps. At the negative input, the FB pin is tied to the output sense location using  $R_B$ , a resistor for sensing and controlling the output voltage at the remote sensing point. The main loop compensation is incorporated in the feedback network connected between the FB and COMP pins.

## POWER GOOD MONITORING

The power good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open-drain output that can be pulled up through an external resistor to a voltage rail—not necessarily the same VCC voltage rail that is running the controller. A logic high level indicates that the output voltage is within the voltage limits defined by a range around the VID voltage setting. PWRGD goes low when the output voltage is outside of that range.

Following the IMVP-6+ specification, the PWRGD range is defined to be 300 mV less than and 200 mV greater than the actual VID DAC output voltage. For any DAC voltage less than 300 mV, only the upper limit of the PWRGD range is monitored. To prevent a false alarm, the power good circuit is masked during various system transitions, including a VID change and entrance into or exit out of deeper sleep. The duration of the PWRGD mask is set to approximately 130  $\mu$ s by an internal timer. If the voltage drop is greater than 200 mV during deeper sleep entry or slow deeper sleep exit, the duration of PWRGD masking is extended by the internal logic circuit.

## POWER-UP SEQUENCE AND SOFT START

The power-on ramp-up time of the output voltage is set with a capacitor tied from the SS pin to GND. The capacitance on the SS pin also determines the current limit latch-off time, as explained in the Current Limit, Short-Circuit, and Latch-Off Protection section. The power-up sequence, including the soft start is illustrated in Figure 27.

In VCC UVLO or shutdown mode, the SS pin is held at zero potential. When VCC ramps to a value greater than the upper UVLO threshold while EN is asserted high, the ADP3208 enables internal bias and starts a reset cycle of 50  $\mu$ s~60  $\mu$ s. When the initial reset is complete, the chip detects the number of phases set by the user and signals to ramp up the SS voltage. During soft start, the external SS capacitor is charged by an internal 8  $\mu$ A current source. The  $V_{CORE}$  voltage follows the ramping SS voltage up to the  $V_{BOOT}$  voltage level determined by a burnt-in VID code (1.2V according to the IMVP-6+ specification). The ADP3208A version has a  $V_{BOOT}$  of 1.0V. All other parameters for the ADP3208A are identical to ADP3208. While the  $V_{CORE}$  is regulated at the  $V_{BOOT}$  voltage, the SS capacitor continues to rise. When the SS pin

# ADP3208A

voltage reaches 1.7 V, the ADP3208 immediately asserts the CLKEN signal low if the  $V_{CORE}$  voltage is within the power good range defined by  $V_{BOOT}$ . In addition, the chip reads the VID codes provided by the CPU on the VID [0:6] input pins. The  $V_{CORE}$  voltage changes from the  $V_{BOOT}$  voltage to the VID voltage by a well-controlled soft transition slope (see the Soft Transient section). During this transition, the SS capacitor is quickly charged up to about a 2.9 V SS clamp level, controlled by the SS source current, which is increased to 48  $\mu\text{A}$  (typical).

The PWRGD signal is asserted after a  $t_{CPU\_PWRGD}$  delay of 3 ms~10 ms, as specified by IMVP-6+. The power good delay can be programmed by the capacitor connected from the PGDELAY pin to GND. Before the CLKEN signal is asserted low, PGDELAY is reset to 0. Following the assertion of the CLKEN signal, an internal source current of 2  $\mu\text{A}$  starts charging up the external capacitor on the PGDELAY pin. Assuming that the  $V_{CORE}$  voltage has settled within the power good range defined by the VID DAC voltage, the PWRGD signal is asserted high when the PGDELAY voltage reaches the 2.9 V power good delay termination threshold.

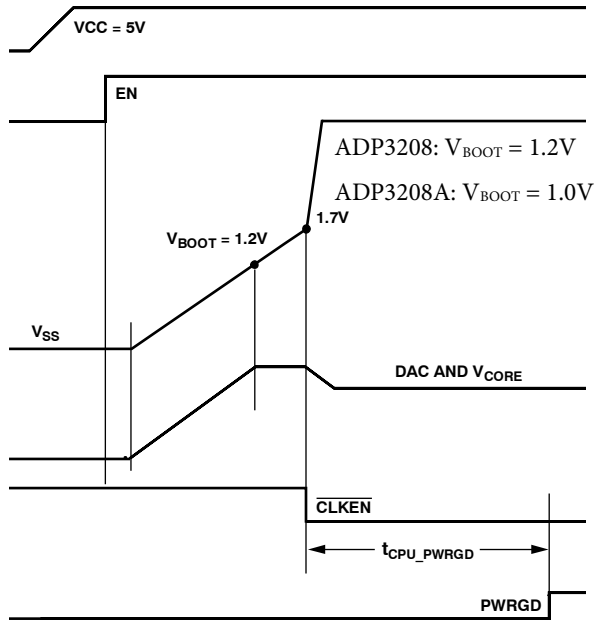


Figure 27. Power-Up Sequence of ADP3208

If EN is taken low or VCC drops below the VCC UVLO threshold, both the SS capacitor and the PGDELAY capacitor are reset to ground to prepare the chip for a subsequent soft start cycle.

## SOFT TRANSIENT

The ADP3208 provides a soft transient function to reduce inrush current during various transitions, including entrance into and exit out of deeper sleep and the transition from  $V_{BOOT}$  to VID voltage. Reducing the inrush current helps decrease the acoustic noise generated by the MLCC input capacitors and inductors.

The soft transient feature is implemented with an ST buffer amplifier that outputs constant sink or source current on the ST pin that is connected to an external capacitor. The capacitor is used to program the slew rate of  $V_{CORE}$  voltage during a VID voltage transient. During steady-state operation, the reference inputs of the voltage error amplifier and the ST amplifier are connected to the VID DAC output. Consequently, the ST voltage is a buffered version of VID DAC output. When system signals trigger a soft transition, the reference input of the voltage error amplifier switches from the DAC output to the ST output while the input of the ST amplifier remains connected to the DAC. The ST buffer input recognizes the almost instantaneous VID voltage change and tries to track it. However, tracking is not instantaneous because the slew rate of the buffer is limited by the source and sink current capabilities of the ST output. Therefore, the  $V_{CORE}$  voltage slew rate is controlled. When the transient period is complete, the reference input of the voltage amplifier reverts to the VID DAC output to improve accuracy.

Table 5 lists the source/sink current on the ST pin for various transitions. Charging/discharging the external capacitor on the ST pin programs the voltage slew rate of the ST pin and consequently of the  $V_{CORE}$  output. For example, a 390 pF ST capacitor results in a +10 mV/ $\mu\text{s}$   $V_{CORE}$  slew rate for fast exit from deeper sleep and a  $\pm 3.3$  mV/ $\mu\text{s}$   $V_{CORE}$  slew rate for slow entry into or exit from deeper sleep.

Table 5. Source/Sink Current of ST Pin

VID Transient	System Signals <sup>1</sup>		ST Pin Current ( $\mu\text{A}$ )
	DPRSLP	DPRSTP	
Slow Entry into Deeper Sleep	High	*	-2.5
Fast Exit from Deeper Sleep	Low	*	+7.5
Slow Exit from Deeper Sleep	High	High	+2.5
Transient from $V_{BOOT}$ to VID	*	*	$\pm 2.5$

<sup>1</sup>\* = do not care.

## CURRENT LIMIT, SHORT-CIRCUIT, AND LATCH-OFF PROTECTION

The ADP3208 compares the differential output of a current sense amplifier to a programmable current limit setpoint to provide the current-limiting function. The current limit threshold is set by the user with a resistor connected from the CLIM pin to GND, utilizing the fixed (10  $\mu\text{A}$  typ) current sourced by the CLIM pin. The ground-referenced CLIM voltage is scaled down inside the chip by a factor of 10 in dual-phase operation and by a factor of 20 in single-phase operation. The scaled-down and level-shifted  $V_{CLTH}$  current limit threshold floats on top of the CSCOMP voltage. The current limit comparator monitors the differential voltage appearing across CSCOMP and CSREF and compares it to the floating  $V_{CLTH}$  threshold. If the sensed current exceeds the threshold, a current

limit alert is released and the control of the internal COMP voltage is transferred from the voltage error amplifier to the current limit amplifier to maintain an average output current determined by the set current limit level.

When the output voltage is less than 200 mV during start-up, a secondary current limit is activated. This is necessary because the voltage swing on the CSCOMP cannot extend below ground. The secondary current limit circuit clamps the internal COMP voltage at around 1.6 V, resulting in duty cycle limited operation. There is also an inherent per phase current limit that protects individual phases in case any of the phases stop functioning due to a faulty component. This limit is based on the maximum normal mode COMP voltage.

If the output current exceeds the current limit threshold or the output voltage is outside the PWRGD range, the SS pin is discharged by an internal sink current of 2  $\mu$ A. A comparator monitors the SS pin voltage and shuts off the controller when the voltage drops to less than about 1.65 V. Because the voltage ramp ( $2.9 \text{ V} - 1.65 \text{ V} = 1.25 \text{ V}$ ) and the discharge current (2  $\mu$ A) are internally fixed, the current limit latch-off delay time is determined by the external SS pin capacitor selection.

Figure 28 shows how the ADP3208 reacts to a current overload.

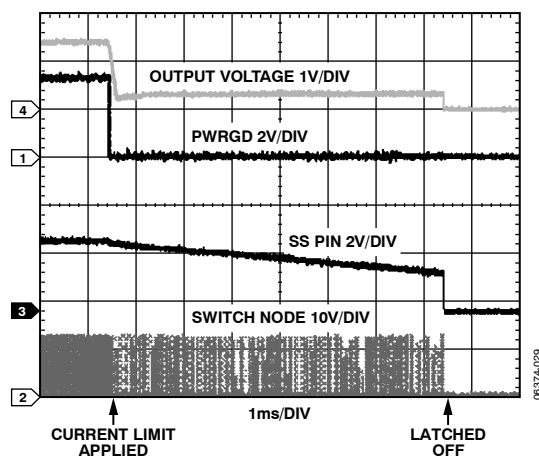


Figure 28. Current Overload

The controller cycles the phases during the latch-off delay time. If the current overload is removed and the PWRGD is recovered before the 1.65 V threshold is reached, the controller resumes normal operation and the SS pin voltage recovers to a 2.9 V clamp level.

The latch off can be reset by either removing and reapplying VCC or by briefly cycling the EN pin low and high. To disable the current limit latch-off function, an external pull-up resistor can be tied from the SS pin to the VCC rail. The pull-up current must override the 2  $\mu$ A sink current of the SS pin to prevent the SS capacitor from discharging to a voltage level that is less than the 1.65 V latch-off threshold.

## CHANGING VID ON THE FLY

The ADP3208 is designed to track dynamically changing VID code. As a consequence, the CPU VCC voltage can change without the need to reset the controller or the CPU. This concept is commonly referred to as VID on-the-fly (VID OTF) transient. A VID OTF can occur with either light or heavy load conditions. The processor alerts the controller that a VID change is occurring by changing the VID inputs in LSB incremental steps from the start code to the finish code. The change can be either upwards or downwards steps.

When a VID input changes, the ADP3208 detects the change but ignores new code for a minimum of 400 ns. This delay is required to prevent the device from reacting to digital signal skew while the 7-bit VID input code is in transition. Additionally, the VID change triggers a PWRGD masking timer to prevent a PWRGD failure. Each VID change resets and retriggers the internal PWRGD masking timer.

As listed in Table 6, during a VID transient, the ADP3208 forces PWM mode regardless of the state of the system input signals. For example, this means that if the chip is configured as a dual-phase controller but is running in single-phase mode due to a light load condition, a current overload event causes the chip to switch to dual-phase mode to share the excessive load until the delayed current limit latch-off cycle terminates.

In user-set single-phase mode, the ADP3208 usually runs in RPM mode. When a VID transition occurs, however, the ADP3208 switches to dual-phase PWM mode.

### Light Load RPM DCM Operation

In single-phase normal mode, DPRSLP is pulled low and the ADP3208 operates in continuous conduction mode (CCM) over the entire load range. The upper and lower MOSFETs are always running synchronously and in complementary phase. See Figure 29 for the typical waveforms of the ADP3208 running in CCM with a 7 A load current.

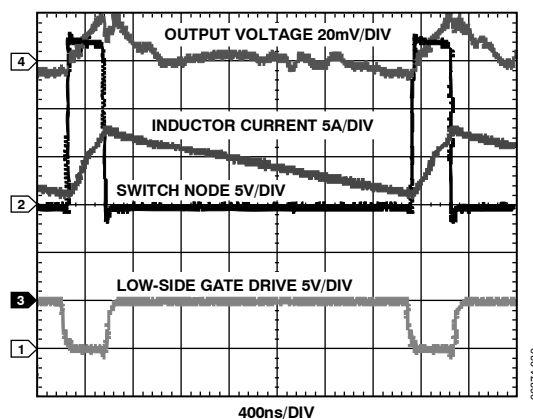


Figure 29. Single-Phase Waveforms in CCM

If DPRSLP is pulled high, the ADP3208 operates in RPM mode. If the load condition is light, the chip enters discontinuous conduction mode (DCM). Figure 30 shows a typical single-phase

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buck with one upper FET, one lower FET, an output inductor, an output capacitor, and a load resistor. Figure 37 shows the path of the inductor current with the upper FET on and the lower FET off. In Figure 32 the high-side FET is off and the low-side FET is on. In CCM, if one FET is on, its complementary FET must be off; however, in DCM, both high- and low-side FETs are off and no current flows into the inductor (see Figure 7). Figure 34 shows the inductor current and switch node voltage in DCM.

In DCM with a light load, the ADP3208 monitors the switch node voltage to determine when to turn off the low-side FET. Figure 35 shows a typical waveform in DCM with a 1 A load current. Between  $t_1$  and  $t_2$  the inductor current ramps down. The current flows through the source drain of the low-side FET and creates a voltage drop across the FET with a slightly negative switch node. As the inductor current ramps down to 0 A, the switch voltage approaches 0 V, as seen just before  $t_2$ . When the switch voltage is approximately  $-6$  mV, the low-side FET is turned off.

Figure 34 shows a small, dampened ringing at  $t_2$ . This is caused by the LC created from capacitance on the switch node, including the  $C_{DS}$  of the FETs and the output inductor. This ringing is normal.

The ADP3208 automatically goes into DCM with a light load. Figure 35 shows the typical DCM waveform of the ADP3208. As the load increases, the ADP3208 enters into CCM. In DCM, frequency decreases with load current. Figure 36 shows switching frequency vs. load current for a typical design. In DCM, switching frequency is a function of the inductor, load current, input voltage, and output voltage.

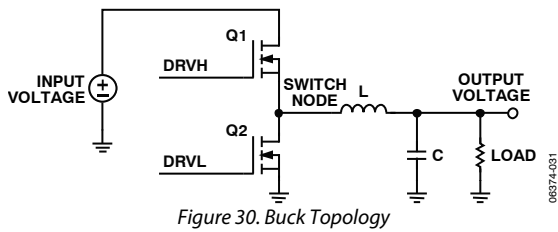


Figure 30. Buck Topology

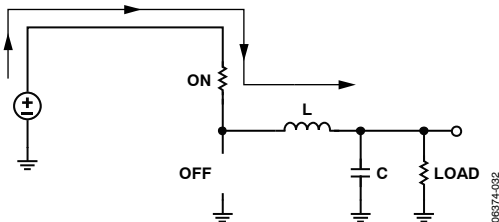


Figure 31. Buck Topology Inductor Current During  $t_0$  and  $t_1$

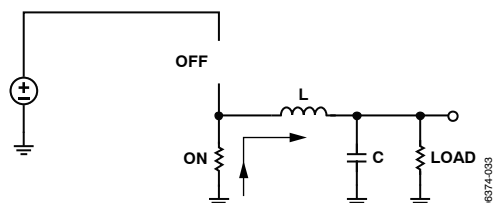


Figure 32. Buck Topology Inductor Current During  $t_1$  and  $t_2$

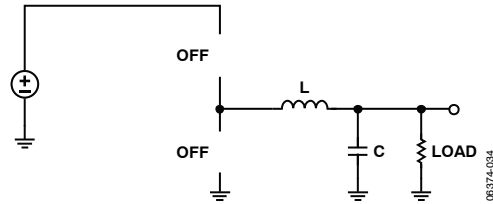


Figure 33. Buck Topology Inductor Current During  $t_2$  and  $t_3$

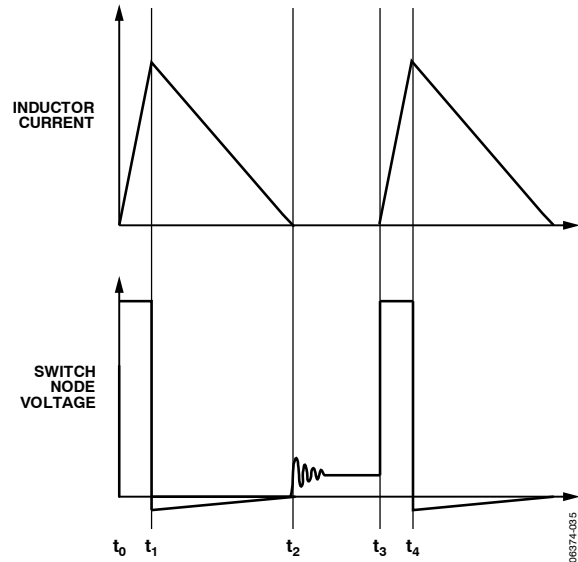


Figure 34. Inductor Current and Switch Node in DCM

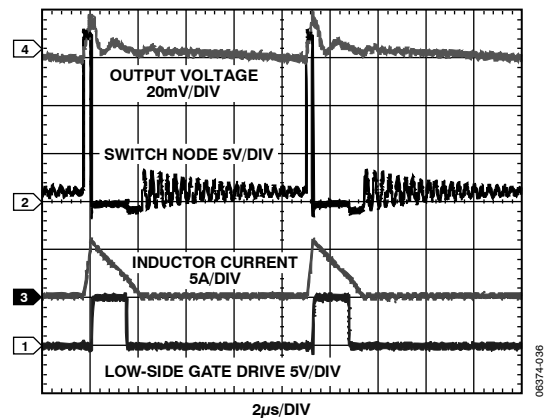


Figure 35. Single-Phase Waveforms in DCM with 1 A Load Current

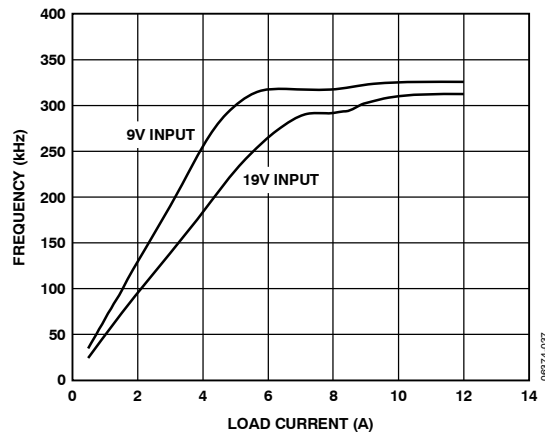


Figure 36. Single-Phase CCM/DCM Frequency vs. Load Current

## **OUTPUT CROWBAR**

To prevent the CPU and other external components from damage due to overvoltage, the ADP3208 turns off the DRVH1 and DRVH2 outputs and turns on the DRVL1 and DRVL2 outputs when the output voltage exceeds the OVP threshold (1.7 V typical). Turning on the low-side MOSFETs forces the output capacitor to discharge and the current to reverse, due to current build up in the inductors. If the output overvoltage is due to a drain-source short of the high-side MOSFET, turning on the low-side MOSFET results in a crowbar across the input voltage rail. The crowbar action blows the fuse of the input rail, breaking the circuit and thus protecting the microprocessor from destruction.

When the OVP feature is triggered, the ADP3208 is latched off. The latch-off function can be reset by removing and reapplying VCC to the ADP3208 or by briefly pulling the EN pin low.

Pulling TTSNS to less than 1 V disables the overvoltage protection function. In this configuration, VRTT should be tied to ground.

## **REVERSE VOLTAGE PROTECTION**

Very large reverse current in inductors can cause negative VCORE voltage, which is harmful to the CPU and other output components. The ADP3208 provides a reverse voltage protection (RVP) function without additional system cost. The VCORE voltage is monitored through the CSREF pin. When the CSREF pin voltage drops to less than -300 mV, the ADP3208 triggers the RVP function by disabling all PWM outputs and driving DRVL1 and DRVL2 low, thus turning off all MOSFETs. The reverse inductor currents can be quickly reset to 0 by discharging the built-up energy in the inductor into the input dc voltage source via the forward-biased body diode of the high-side MOSFETs. The RVP function is terminated when the CSREF pin voltage returns to greater than -100 mV.

Sometimes the crowbar feature inadvertently causes output reverse voltage because turning on the low-side MOSFETs results in a very large reverse inductor current. To prevent damage to the CPU caused from negative voltage, the ADP3208 maintains its RVP monitoring function even after OVP latch off. During OVP latch off, if the CSREF pin voltage drops to less than -300 mV, the low-side MOSFETs is turned off. DRVL outputs are allowed to turn back on when the CSREF voltage recovers to greater than -100 mV.

## **OUTPUT ENABLE AND UVLO**

For the ADP3208 to begin switching, the VCC supply voltage to the controller must be greater than the VCCOK threshold and the EN pin must be driven high. If the VCC voltage is less than the VCCUVLO threshold or the EN pin is a logic low, the ADP3208 shuts off. In shutdown mode, the controller holds the PWM outputs low, shorts the capacitors of the SS and PGDELAY pins to ground, and drives the DRVH and DRVL outputs low.

The user must adhere to proper power-supply sequencing during start-up and shutdown of the ADP3208. All input pins must be at ground prior to removing or applying VCC, and all output pins should be left in high impedance state while VCC is off.

## **THERMAL THROTTLING CONTROL**

The ADP3208 includes a thermal monitoring circuit to detect whether the temperature of the VR has exceeded a user-defined thermal throttling threshold. The thermal monitoring circuit requires an external resistor divider connected between the VCC pin and GND. The divider consists of an NTC thermistor and a resistor. To generate a voltage that is proportional to temperature, the midpoint of the divider is connected to the TTSNS pin. An internal comparator circuit compares the TTSNS voltage to half the VCC threshold and outputs a logic level signal at the VRTT output when the temperature trips the user-set alarm threshold. The VRTT output is designed to drive an external transistor that in turn provides the high current, open-drain VRTT signal required by the IMVP-6+ specification. The internal VRTT comparator has a hysteresis of approximately 100 mV to prevent high frequency oscillation of VRTT when the temperature approaches the set alarm point.



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## POWER MONITOR FUNCTION

The ADP3208 includes a power monitor. The circuit creates the product of the output voltage and the output current. The multiplication is done by converting the differential current sense signal from CSCOMP to CSREF into a pulse-modulated periodic signal stream and then scaling that signal with the output voltage. The duty cycle of the pulse-modulated PMON signal is proportional to the current, and the amplitude is proportional to the voltage. The maximum load current that corresponds to the full-scale (100%) modulated signal can be adjusted by a resistor, RPMONFS, tied from PMONFS to GND. RPMONFS also affects the clock frequency of the PWM circuit. An RC low path filter connected to the PMON output demodulates the PWM pulse stream and creates averaged output current or power information, depending on which rail the open-drain PMON output is pulled up to.

If PMON is pulled up to a dc voltage, the RC-filtered voltage is proportional to the averaged load current. Figure 37 shows the PMON configuration used to monitor load current.

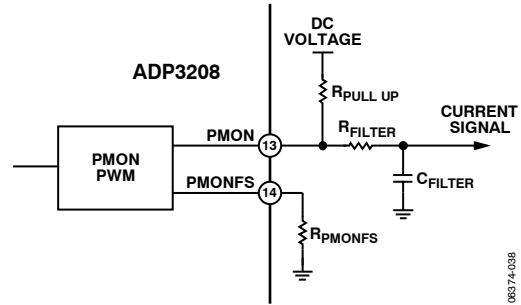


Figure 37. PMON Current Monitor Configuration

If PMON is pulled up to the converter output node, the demodulated voltage becomes proportional to the averaged power (see Figure 38).

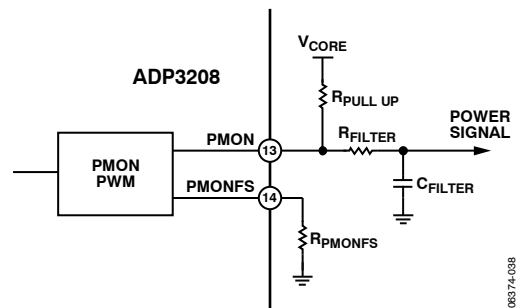


Figure 38. PMON Power Monitor Configuration

Table 6. VID Codes

VID6	VID5	VID4	VID3	VID2	VID1	VID0	OUTPUT	VID6	VID5	VID4	VID3	VID2	VID1	VID0	OUTPUT		
0	0	0	0	0	0	0	1.5000 V	0	1	1	1	1	0	1	0.7375 V		
0	0	0	0	0	0	1	1.4875 V	0	1	1	1	1	1	0	0.7250 V		
0	0	0	0	0	1	0	1.4750 V	0	1	1	1	1	1	1	0.7125 V		
0	0	0	0	0	1	1	1.4625 V	1	0	0	0	0	0	0	0.7000 V		
0	0	0	0	1	0	0	1.4500 V	1	0	0	0	0	0	1	0.6875 V		
0	0	0	0	1	0	1	1.4375 V	1	0	0	0	0	1	0	0.6750 V		
0	0	0	0	1	1	0	1.4250 V	1	0	0	0	0	1	1	0.6625 V		
0	0	0	0	1	1	1	1.4125 V	1	0	0	0	1	0	0	0.6500 V		
0	0	0	1	0	0	0	1.4000 V	1	0	0	0	0	1	0	1	0.6375 V	
0	0	0	1	0	0	1	1.3875 V	1	0	0	0	0	1	1	0	0.6250 V	
0	0	0	1	0	1	0	1.3750 V	1	0	0	0	0	1	1	1	0.6125 V	
0	0	0	1	0	1	1	1.3625 V	1	0	0	1	0	0	0	0	0.6000 V	
0	0	0	1	1	0	0	1.3500 V	1	0	0	1	0	0	1	1	0.5875 V	
0	0	0	1	1	0	1	1.3375 V	1	0	0	1	0	1	0	0	0.5750 V	
0	0	0	1	1	1	0	1.3250 V	1	0	0	1	0	1	1	1	0.5625 V	
0	0	0	1	1	1	1	1.3125 V	1	0	0	1	1	0	0	0	0.5500 V	
0	0	1	0	0	0	0	1.3000 V	1	0	0	1	1	0	1	1	0.5375 V	
0	0	1	0	0	0	1	1.2875 V	1	0	0	1	1	1	0	0	0.5250 V	
0	0	1	0	0	1	0	1.2750 V	1	0	0	1	1	1	1	1	0.5125 V	
0	0	1	0	0	1	1	1.2625 V	1	0	1	0	0	0	0	0	0.5000 V	
0	0	1	0	1	0	0	1.2500 V	1	0	1	0	0	0	1	1	0.4875 V	
0	0	1	0	1	0	1	1.2375 V	1	0	1	0	0	1	0	0	0.4750 V	
0	0	1	0	1	1	0	1.2250 V	1	0	1	0	0	1	1	1	0.4625 V	
0	0	1	0	1	1	1	1.2125 V	1	0	1	0	1	0	0	0	0.4500 V	
0	0	1	1	0	0	0	1.2000 V	1	0	1	0	1	0	1	0	1	0.4375 V
0	0	1	1	0	0	1	1.1875 V	1	0	1	0	1	1	0	0	0.4250 V	
0	0	1	1	0	1	0	1.1750 V	1	0	1	0	1	1	1	1	0.4125 V	
0	0	1	1	0	1	1	1.1625 V	1	0	1	1	0	0	0	0	0.4000 V	
0	0	1	1	1	0	0	1.1500 V	1	0	1	1	0	0	1	1	0.3875 V	
0	0	1	1	1	0	1	1.1375 V	1	0	1	1	0	1	0	0	0.3750 V	
0	0	1	1	1	1	0	1.1250 V	1	0	1	1	0	1	1	1	0.3625 V	
0	0	1	1	1	1	1	1.1125 V	1	0	1	1	1	0	0	0	0.3500 V	
0	1	0	0	0	0	0	1.1000 V	1	0	1	1	1	0	1	0	1	0.3375 V
0	1	0	0	0	0	1	1.0875 V	1	0	1	1	1	1	0	0	0.3250 V	
0	1	0	0	0	1	0	1.0750 V	1	0	1	1	1	1	1	1	0.3125 V	
0	1	0	0	0	1	1	1.0625 V	1	1	0	0	0	0	0	0	0.3000 V	
0	1	0	0	1	0	0	1.0500 V	1	1	0	0	0	0	1	1	0.2875 V	
0	1	0	0	1	0	1	1.0375 V	1	1	0	0	0	1	0	0	0.2750 V	
0	1	0	0	1	1	0	1.0250 V	1	1	0	0	0	1	1	1	0.2625 V	
0	1	0	0	1	1	1	1.0125 V	1	1	0	0	1	0	0	0	0.2500 V	
0	1	0	1	0	0	0	1.0000 V	1	1	0	0	1	0	1	0	1	0.2375 V
0	1	0	1	0	0	1	0.9875 V	1	1	0	0	1	1	0	0	0.2250 V	
0	1	0	1	0	1	0	0.9750 V	1	1	0	0	1	1	1	1	0.2125 V	
0	1	0	1	0	1	1	0.9625 V	1	1	0	1	0	0	0	0	0.2000 V	
0	1	0	1	1	0	0	0.9500 V	1	1	0	1	0	0	1	1	0.1875 V	
0	1	0	1	1	0	1	0.9375 V	1	1	0	1	0	1	0	0	0.1750 V	
0	1	0	1	1	1	0	0.9250 V	1	1	0	1	0	1	1	1	0.1625 V	
0	1	0	1	1	1	1	0.9125 V	1	1	0	1	1	0	0	0	0.1500 V	
0	1	1	0	0	0	0	0.9000 V	1	1	0	1	1	0	1	1	0.1375 V	
0	1	1	0	0	0	1	0.8875 V	1	1	0	1	1	1	0	0	0.1250 V	
0	1	1	0	0	1	0	0.8750 V	1	1	0	1	1	1	1	1	0.1125 V	
0	1	1	0	0	1	1	0.8625 V	1	1	1	0	0	0	0	0	0.1000 V	
0	1	1	0	1	0	0	0.8500 V	1	1	1	0	0	0	1	1	0.0875 V	
0	1	1	0	1	0	1	0.8375 V	1	1	1	0	0	1	0	0	0.0750 V	
0	1	1	0	1	1	0	0.8250 V	1	1	1	0	0	1	1	1	0.0625 V	
0	1	1	0	1	1	1	0.8125 V	1	1	1	0	1	0	0	0	0.0500 V	
0	1	1	1	0	0	0	0.8000 V	1	1	1	0	1	0	1	1	0.0375 V	
0	1	1	1	0	0	1	0.7875 V	1	1	1	0	1	1	0	0	0.0250 V	
0	1	1	1	0	1	0	0.7750 V	1	1	1	0	1	1	1	1	0.0125 V	
0	1	1	1	0	1	1	0.7625 V	1	1	1	1	0	0	0	0	0.0000 V	
0	1	1	1	1	0	0	0.7500 V	1	1	1	1	0	0	1	1	0.0000 V	