Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

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ADP3208C

7-Bit, Programmable, Dual-Phase, Mobile, CPU, Synchronous Buck Controller

The ADP3208C is a highly efficient, multiphase, synchronous buck switching regulator controller. With its integrated drivers, the ADP3208C is optimized for converting the notebook battery voltage into the core supply voltage required by high performance Intel processors. An internal 7−bit DAC is used to read a VID code directly from the processor and to set the CPU core voltage to a value within the range of 0.3 V to 1.5 V. The phase relationship of the output signals ensures interleaved 2−phase operation.

The ADP3208C uses a multi−mode architecture run at a programmable switching frequency and optimized for efficiency depending on the output current requirement. The ADP3208C switches between single− and dual−phase operation to maximize efficiency with all load conditions. The chip includes a programmable load line slope function to adjust the output voltage as a function of the load current so that the core voltage is always optimally positioned for a load transient. The ADP3208C also provides accurate and reliable short−circuit protection, adjustable current limiting, and a delayed power−good output. The IC supports On−The−Fly (OTF) output voltage changes requested by the CPU.

The ADP3208C is specified over the extended commercial temperature range of −10°C to 100°C and is available in a 48−lead LFCSP.

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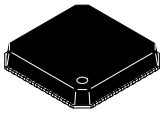

LFCSP48
CASE 932AD

MARKING DIAGRAM

A = Assembly Location
WL = Wafer Lot
YYWW = Date Code
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 36 of this data sheet.

Features

- Single−Chip Solution
- Fully Compatible with the Intel® IMVP−6+™ Specifications
- Integrated MOSFET Drivers
- Input Voltage Range of 3.3 V to 22 V
- Selectable 1− or 2−Phase Operation with Up to 1 MHz per Phase Switching Frequency
- Guaranteed ±8 mV Worst−Case Differentially Sensed Core Voltage Error Overtemperature
- Automatic Power−Saving Mode Maximizes Efficiency with Light Load During Deeper Sleep Operation
- Soft Transient Control Reduces Inrush Current and Audio Noise
- Active Current Balancing Between Output Phases
- Independent Current Limit and Load Line Setting Inputs for Additional Design Flexibility
- Built−In Power−Good Blanking Supports Voltage Identification (VID) OTF Transients
- 7−Bit, Digitally Programmable DAC with 0.3 V to 1.5 V Output
- Short−Circuit Protection with Latchoff Delay
- Clock Enable Output Delays the CPU Clock Until the Core Voltage is Stable
- Output Load Current Monitor
- This is a Pb−Free Device

Applications

- Notebook Power Supplies for Next Generation Intel® Processors

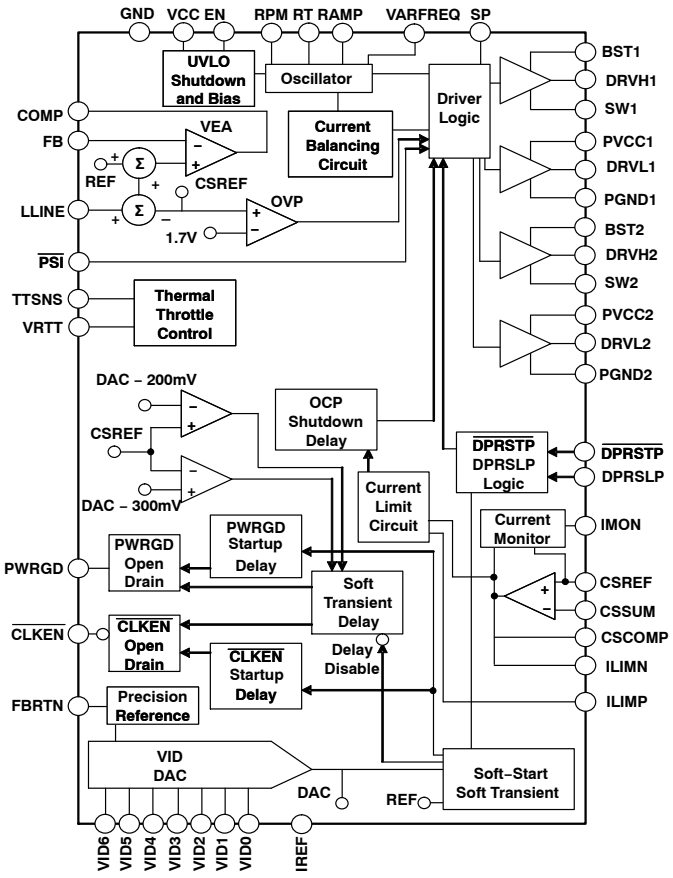

Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
VCC, PVCC1, PVCC2	–0.3 to +6.0	V
FBRTN, PGND1, PGND2	–0.3 to +0.3	V
BST1, BST2 DC t < 200 ns	 –0.3 to +28 –0.3 to +33	V
BST1 to SW1, BST2 to SW2	–0.3 to +6.0	V
SW1, SW2 DC t < 200 ns	 –5.0 to +22 –10 to +28	V
DRVH1 to SW1, DRVH2 to SW2	–0.3 to +6.0	V
DRVL1 to PGND1, DRVL2 to PGND2 DC t < 200 ns	 –0.3 to +6.0 –5.0 to +6.0	V
RAMP (In Shutdown) DC	–0.3 to +22	V
All Other Inputs and Outputs	–0.3 to +6.0	V
Storage Temperature	–65 to +150	°C
Operating Ambient Temperature Range	–10 to 100	°C
Operating Junction Temperature	125	°C
Thermal Impedance (θ_{JA}) 2–Layer Board	40	°C/W
Lead Temperature Soldering (10 sec) Infrared (15 sec)	 300 260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

TEST CIRCUITS

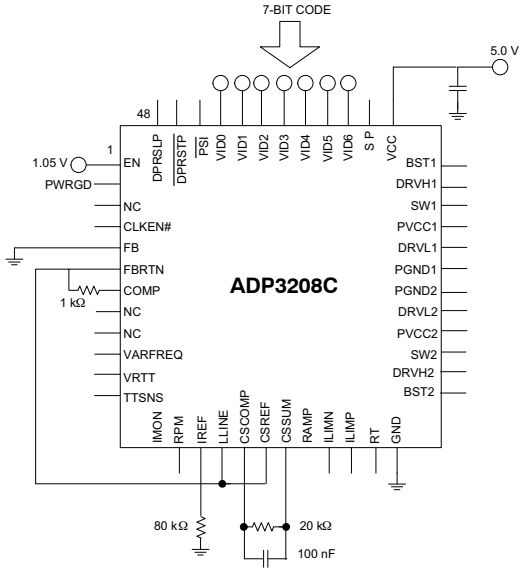

Figure 2. Closed−Loop Output Voltage Accuracy

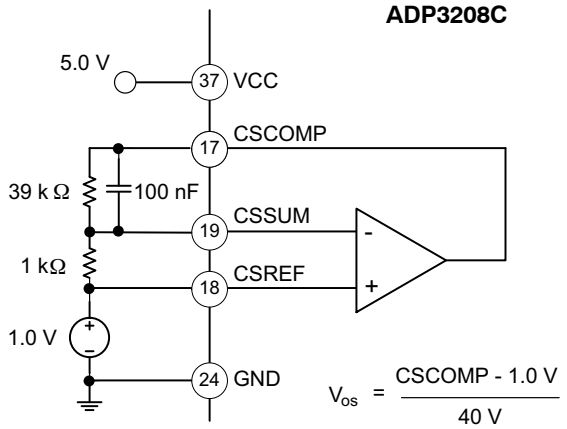

Figure 3. Current Sense Amplifier, V_{OS}

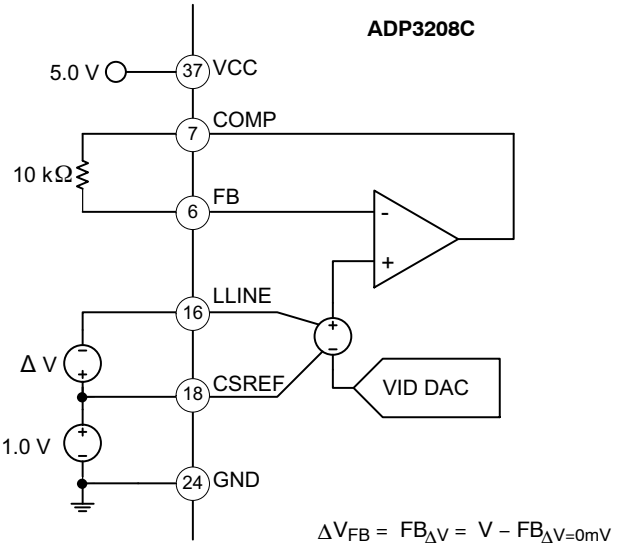

Figure 4. Positioning Accuracy

PIN FUNCTION DESCRIPTIONS

Pin No	Mnemonic	Description
1	EN	Enable Input. Driving this pin low shuts down the chip, disables the driver outputs, pulls PWRGD and VRTT low, and pulls $\overline{\text{CLKEN}}$ high.
2	PWRGD	Power−Good Output. Open−drain output. A low logic state means that the output voltage is outside of the VID DAC defined range.
3	NC	Not Connected.
4	$\overline{\text{CLKEN}}$	Clock Enable Output. Open−drain output. A low logic state enables the CPU internal PLL clock to lock to the external clock.
5	FBRTN	Feedback Return Input/Output. This pin remotely senses the CPU core voltage. It is also used as the ground return for the VID DAC and the voltage error amplifier blocks.
6	FB	Voltage Error Amplifier Feedback Input. The inverting input of the voltage error amplifier.
7	COMP	Voltage Error Amplifier Output and Frequency Compensation Point.
8	NC	Not Connected.
9	IRPM/NC	RPM Mode Timing Control Input. A resistor between this pin or RPM pin to ground sets the RPM mode turn−on threshold voltage. If a resistor is connected between this pin to ground, RPM pin must remain floating and not connected.
10	VARFREQ	Variable Frequency Enable Input. A high logic state enables the PWM clock frequency to vary with VID code.
11	VRTT	Voltage Regulator Thermal Throttling Output. Logic high state indicates that the voltage regulator temperature at the remote sensing point exceeded a set alarm threshold level.
12	TTSNS	Thermal Throttling Sense and Crowbar Disable Input. A resistor divider where the upper resistor is connected to VCC, the lower resistor (NTC thermistor) is connected to GND, and the center point is connected to this pin and acts as a temperature sensor half bridge. Connecting TTSNS to GND disables the thermal throttling function and disables the crowbar, or Overvoltage Protection (OVP), feature of the chip.
13	IMON	Current Monitor Output. This pin sources a current proportional to the output load current. A resistor to FBRTN sets the current monitor gain.
14	RPM	RPM Mode Timing Control Input. A resistor between this pin or IRPM pin to ground sets the RPM mode turn−on threshold voltage. If a resistor is connected between this pin to ground, IRPM pin must remain floating.
15	IREF	This pin sets the internal bias currents. A 80 kΩ resistor is connected from this pin to ground.
16	LLINE	Load Line Programming Input. The center point of a resistor divider connected between CSREF and CSCOMP can be tied to this pin to set the load line slope.
17	CSCOMP	Current Sense Amplifier Output and Frequency Compensation Point.
18	CSREF	Current Sense Reference Input. This pin must be connected to the common point of the output inductors. The node is shorted to GND through an internal switch when the chip is disabled to provide soft stop transient control of the converter output voltage.
19	CSSUM	Current Sense Summing Input. External resistors from each switch node to this pin sum the inductor currents to provide total current information.
20	RAMP	PWM Ramp Slope Setting Input. An external resistor from the converter input voltage node to this pin sets the slope of the internal PWM stabilizing ramp used for phase−current balancing.
21	ILIMN	Current Limit Set. An external resistor from ILIMN to ILIMP sets the current limit threshold of the converter.
22	ILIMP	Current Limit Set. An external resistor from ILIMN to ILIMP sets the current limit threshold of the converter.
23	RT	PWM Oscillator Frequency Setting Input. An external resistor from this pin to GND sets the PWM oscillator frequency.
24	GND	Analog and Digital Signal Ground.
25	BST2	High−Side Bootstrap Supply for Phase 2. A capacitor from this pin to SW2 holds the bootstrapped voltage while the high−side MOSFET is on.
26	DRVH2	High−Side Gate Drive Output for Phase 2.
27	SW2	Current Balance Input for Phase 2 and Current Return for High−Side Gate Drive.
28	PVCC2	Power Supply Input/Output of Low−Side Gate Driver for Phase 2.
29	DRVL2	Low−Side Gate Drive Output for Phase 2.
30	PGND2	Low−Side Driver Power Ground for Phase 2.

Pin No	Mnemonic	Description
31	PGND1	Low−Side Driver Power Ground for Phase 1.
32	DRVL1	Low−Side Gate Drive Output for Phase 1.
33	PVCC1	Power Supply Input/Output of Low−Side Gate Driver for Phase 1.
34	SW1	Current Balance Input for Phase 1 and Current Return For High−Side Gate Drive.
35	DRVH1	High−Side Gate Drive Output for Phase 1.
36	BST1	High−Side Bootstrap Supply for Phase 1. A capacitor from this pin to SW1 holds the bootstrapped voltage while the high−side MOSFET is on.
37	VCC	Power Supply Input/Output of the Controller.
38	SP	Single−Phase Select Input. Logic high state sets single−phase configuration.
39 to 45	VID6 to VID0	Voltage Identification DAC Inputs. A 7−bit word (the VID code) programs the DAC output voltage, the reference voltage of the voltage error amplifier without a load (see the VID code Table 3).
46	$\overline{\text{PSI}}$	Power State Indicator Input. Driving this pin low forces the controller to operate in single−phase mode.
47	$\overline{\text{DPRSTP}}$	Deeper Stop Control Input. The logic state of this pin is usually complementary to the state of the DPRSLP pin; however, during slow deeper sleep exit, both pins are logic low.
48	DPRSLP	Deeper Sleep Control Input.

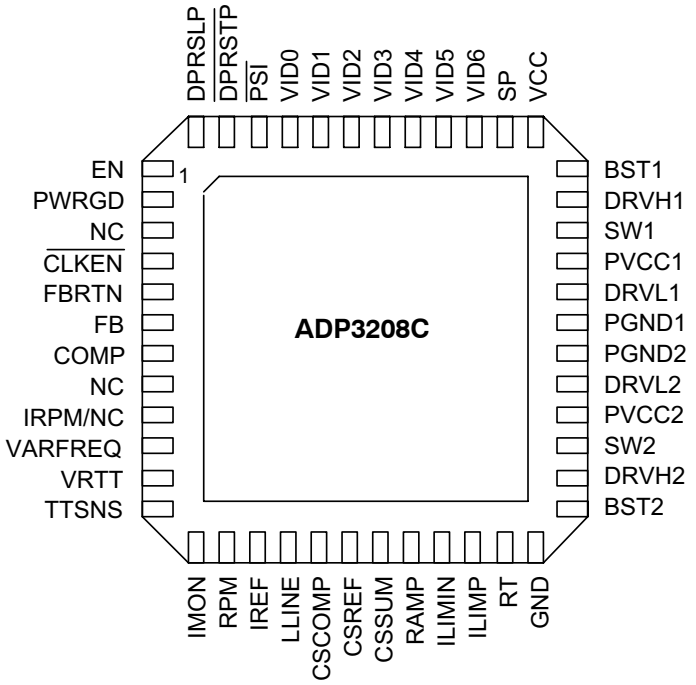

Figure 5. Pin Configuration
(Top View)

ELECTRICAL CHARACTERISTICS V_{CC} = P_{VCC1} = P_{VCC2} = BST1 = BST2 = High = 5.0V, FBRTN = GND = SW1 = SW2 = PGND1 = PGND2 = Low = 0 V, EN = VATFREQ = High, DPRSLP = 0 V, $\overline{PSI}$ = 1.05 V, V_{VID} = 1.2000 V, T_A = −40°C to 100°C, unless otherwise noted (Note 1). Current entering a pin (sunk by the device) has a positive sign. R_{REF} = 80 kΩ.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VOLTAGE CONTROL − Voltage Error Amplifier (VEAMP)						
FB, LLINE Voltage Range (Note 2)	V_{FB}, V_{LLINE}	Relative to CSREF = V_{DAC}	−200		+200	mV
FB, LLINE Offset Voltage (Note 2)	V_{OSVEA}	Relative to CSREF = V_{DAC}	−0.5		+0.5	mV
FB LLINE Bias Current (Note 2)	I_{FB}		−100		100	A
LLINE Positioning Accuracy	V_{FB} − V_{VID}	Measured on FB relative to V_{VID}, LLINE forced 80 mV below CSREF	−78	−80	−82	mV
COMP Voltage Range	V_{COMP}	Operating Range	0.85		4.0	V
COMP Current	I_{COMP}	COMP = 2.0 V, CSREF = V_{DAC} FB forced 200 mV below CSREF FB forced 200 mV above CSREF		 −0.75 6.0		mA
COMP Slew Rate	SR_{COMP}	C_{COMP} = 10 pF, CSREF = V_{DAC}, Open loop configuration FB forced 200 mV below CSREF FB forced 200 mV above CSREF		 15 −20		V/μs
Gain Bandwidth (Note 2)	GBW	Non−inverting unit gain configuration, R_{FB} = 1 kΩ		20		MHz
VID DAC VOLTAGE REFERENCE						
V_{DAC} Voltage Range (Note 3)		See VID Code Table	0		1.5	V
V_{DAC} Accuracy	V_{FB} − V_{VID}	Measured on FB (includes offset), relative to V_{VID}, for VID table see Table 3, V_{VID} = 1.2125 V to 1.5000 V V_{VID} = 0.3000 V to 1.2000 V	 −9.0 −7.5		 +9.0 +7.5	mV
V_{DAC} Differential Non−linearity (Note 2)			−1.0		+1.0	LSB
V_{DAC} Line Regulation	ΔV_{FB}	V_{CC} = 4.75 V to 5.25 V		0.05		%
V_{DAC} Boot Voltage (Note 2)	V_{BOOTFB}	Measured during boot delay period		1.200		V
Soft−Start Delay (Note 2)	t_{DSS}	Measured from EN pos edge to FB = 50 mV		200		μs
Soft−Start Time	t_{SS}	Measured from EN pos edge to FB settles to V_{BOOT} = 1.2 V within −5%		1.7		ms
Boot Delay	t_{BOOT}	Measured from FB settling to V_{BOOT} = 1.2 V within −5% to $\overline{CLKEN}$ neg edge		150		μs
V_{DAC} Slew Rate		Soft−Start Non−LSB VID step, DPRSLP = H, Slow C4 Entry/Exit Non−LSB VID step, DPRSLP = L, Fast C4 Exit		0.0625 0.25 1.0		LSB/μs
FBRTN Current	I_{FBRTN}			90	200	μA
VOLTAGE MONITORING AND PROTECTION − Power Good						
CSREF Undervoltage Threshold	$V_{UVCSREF}$	Relative to DAC Voltage: = 0.5 V to 1.5 V = 0.3 V to 0.4875 V	 −360 −360	 −300 −300	 −240 −160	mV
CSREF Overvoltage Threshold	$V_{OVCSREF}$	Relative to nominal DAC Voltage	150	200	250	mV
CSREF Crowbar Voltage Threshold	$V_{CBCSREF}$	Relative to FBRTN	1.57	1.7	1.78	V
CSREF Reverse Voltage Threshold	$V_{RVCSREF}$	Relative to FBRTN, Latchoff mode: CSREF Falling CSREF Rising	 −350	 −300 −70	 −5.0	mV

1. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).
2. Guaranteed by design or bench characterization, not production tested.
3. Timing is referenced to the 90% and 10% points, unless otherwise noted.

ELECTRICAL CHARACTERISTICS V_{CC} = P_{VCC1} = P_{VCC2} = BST1 = BST2 = High = 5.0V, FBRTN = GND = SW1 = SW2 = PGND1 = PGND2 = Low = 0 V, EN = VATFREQ = High, DPRSLP = 0 V, $\overline{PSI}$ = 1.05 V, V_{VID} = 1.2000 V, T_A = −40°C to 100°C, unless otherwise noted (Note 1). Current entering a pin (sunk by the device) has a positive sign. R_{REF} = 80 kΩ.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VOLTAGE MONITORING AND PROTECTION − Power Good						
PWRGD Low Voltage	V_{PWRGD}	$I_{PWRGD(SINK)}$ = 4 mA		50	150	mV
PWRGD High, Leakage Current	I_{PWRGD}	V_{PWRDG} = 5.0 V			0.1	μA
PWRGD Startup Delay	$T_{SSPWRGD}$	Measured from CLKEN neg edge to PWRGD Pos Edge		8.0		ms
PWRGD Latchoff Delay	$T_{LOFFPWRGD}$	Measured from Out−off−Good−Window event to Latchoff (switching stops)		8.0		ms
PWRGD Propagation Delay (Note 3)	$T_{PDPWRGD}$	Measured from Out−off−Good−Window event to PWRGD neg edge		200		ns
Crowbar Latchoff Delay (Note 2)	T_{LOFFCB}	Measured from Crowbar event to Latchoff (switching stops)		200		ns
PWRGD Masking Time		Triggered by any VID change or OCP event		100		μs
CSREF Soft−Stop Resistance		EN = L or Latchoff condition		70		Ω
CURRENT CONTROL − Current Sense Amplifier (CSAMP)						
CSSUM, CSREF Common−Mode Range (Note 2)		Voltage range of interest	0		2.0	V
CSSUM, CSREF Offset Voltage	V_{OSCSA}	T_A = 25°C CSREF − CSSUM, T_A = −10°C to 85°C CSREF − CSSUM, T_A = −40°C to 85°C	−0.5 −1.7 −1.8		+0.5 +1.7 +1.8	mV
CSSUM Bias Current	I_{BCSSUM}		−50		+50	nA
CSREF Bias Current	I_{BCSREF}		−120		+120	nA
CSCOMP Voltage Range (Note 2)		Operating Range	0.05		2.0	V
CSCOMP Current	$I_{CSCOMPsource}$ $I_{CSCOMPsink}$	CSCOMP = 2.0 V CSSUM forced 200 mV below CSREF CSSUM forced 200 mV above CSREF		−750 1.0		μA mA
CSCOMP Slew Rate		C_{CSCOMP} = 10 pF, Open Loop Configuration CSSUM forced 200 mV below CSREF CSSUM forced 200 mV above CSREF		 10 −10		V/μs
Gain Bandwidth (Note 2)	GBW_{CSA}	Non−inverting unit gain configuration R_{FB} = 1 kΩ		20		MHz
CURRENT MONITORING AND PROTECTION						
Current Reference I_{REF} Voltage	V_{REF}	R_{REF} = 80 kΩ to set I_{REF} = 20 μA	1.55	1.6	1.65	V
Current Limiter (OCP) Current Limit Threshold	V_{LIMTH}	Measured from CSCOMP to CSREF, R_{LIM} = 4.5 kΩ, 2−ph configuration, $\overline{PSI}$ = H 2−ph configuration, $\overline{PSI}$ = L 1−ph configuration Measured from CSCOMP to CSREF, R_{LIM} = 4.5 kΩ, 3−ph configuration, $\overline{PSI}$ = H 3−ph configuration, $\overline{PSI}$ = L 1−ph configuration	 −70 −32 −70 −70 −15 −70	 −95 −47.5 −95 −90 −30 −90	 −115 −65 −115 −115 −50 −115	mV
Current Limit Latchoff Delay		Measured from OCP event to PWRGD deassertion		8.0		ms

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2. Guaranteed by design or bench characterization, not production tested.
3. Timing is referenced to the 90% and 10% points, unless otherwise noted.

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CURRENT MONITOR						
Current Gain Accuracy	I_{MON}/I_{LIM}	Measured from I_{LIMP} to I_{MON} I_{LIM} = −20 μA I_{LIM} = −10 μA I_{LIM} = −5 μA	 9.5 9.3 9.0	 10 10 10	 10.5 10.7 11.0	
I_{MON} Clamp Voltage	V_{MAXMON}	Relative to FBRTN, I_{LIMP} = −30 μA	1.0		1.05	V
PULSE WIDTH MODULATOR – Clock Oscillator						
R_T Voltage	V_{RT}	VARFREQ = High, R_T = 125 kΩ, V_{VID} = 1.5000 V VARFREQ = Low, See also $V_{RT}(V_{VID})$ formula	1.22 0.98	1.25 1.0	1.27 1.02	V
PWM Clock Frequency Range (Note 2)	f_{CLK}	Operating Range	0.3		3.0	MHz
PWM Clock Frequency	f_{CLK}	T_A = 25°C, V_{VID} = 1.2000 V R_T = 73 kΩ R_T = 125 kΩ R_T = 180 kΩ	 1200 680 400	 1470 920 640	 1720 1120 840	kHz
RAMP GENERATOR						
RAMP Voltage	V_{RAMP}	EN = high, I_{RAMP} = 30 μA EN = low	0.9	1.0 V_{IN}	1.1	V
RAMP Current Range (Note 2)	I_{RAMP}	EN = high EN = low, RAMP = 19 V	1.0 −0.5		100 +0.5	μA
PWM COMPARATOR						
PWM Comparator Offset (Note 2)	V_{OSRPM}	V_{RAMP} − V_{COMP}	−3.0		3.0	mV
RPM COMPARATOR						
RPM Current	I_{RPM}	V_{VID} = 1.2 V, R_T = 125 kΩ, VARFREQ = High, See also $I_{RPM}(R_T)$ formula		−8.8		μA
RPM Comparator Offset (Note 2)	V_{OSRPM}	V_{COMP} − (1 +V_{RPM})	−3.0		3.0	mV
EPWM CLOCK SYNC						
Trigger Threshold (Note 2)		Relative to COMP sampled T_{CLK} earlier 2−phase configuration 1−phase configuration		 400 450		mV
SWITCH AMPLIFIER						
SW Common Mode Range (Note 2)	$V_{SW(X)CM}$	Operating Range for current sensing	−600		+200	mV
SW Resistance	$R_{SW\_PGND(X)}$	Measured from SW to PGND		3.0		kΩ
ZERO CURRENT SWITCHING COMPARATOR						
SW ZCS Threshold	$V_{DCM(SW1)}$	DCM mode, DPRSLP = 3.3 V		−6.0		mV
Masked Off Time	$t_{OFFMSKD}$	Measured from DRVH neg edge to DRVH pos edge at max frequency of operation		700		ns
SYSTEM I/O BUFFERS VID[6:0], $\overline{PSI}$ INPUTS						
Input Voltage		Refers to driving signal level Logic low, $I_{sink} \geq$ 1 μA Logic high, $I_{source} \leq$ −5 μA	 0.7		 0.3	V
Input Current		V = 0.2 V VID[6:0], DPRSLP (active pulldown to GND) $\overline{PSI}$ (active pullup to V_{CC})		 −1.0 +1.0		μA
VID Delay Time (Note 2)		Any VID edge to FB change 10%	200			ns

1. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).
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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DPRSLP						
Input Voltage		Refers to driving signal level Logic low, $I_{sink} \geq 1$ μA Logic high, $I_{source} \leq -5$ μA	 2.3		 1.0	V
Input Current		DPRSLP = low DPRSLP = high		−1.0 +2.0		μA
$\overline{\text{DPRSTP}}$						
Input Voltage		Refers to driving signal level Logic low, $I_{sink} \geq 1$ μA Logic high, $I_{source} \leq -5$ μA	 0.7		 0.3	V
Input Current				1.0		μA
VARFREQ, SP						
Input Voltage		Refers to driving signal level Logic low, $I_{sink} \geq 1$ μA Logic high, $I_{source} \leq -5$ μA	 4.0		 0.7	V
Input Current				1.0		μA
EN INPUT						
Input Voltage		Refers to driving signal level Logic low, $I_{sink} \geq 1$ μA Logic high, $I_{source} \leq -5$ μA	 2.3		 1.0	V
Input Current		EN = L or EN = H (Static) 0.8 V < EN < 1.6 V (During Transition)		10 70		nA μA
$\overline{\text{CLKEN}}$ OUTPUT						
Output Low Voltage		Logic low, I_{sink} = 4 mA		50	100	mV
Output High, Leakage Current		Logic high, $V_{CLKEN} = V_{CC}$			1.0	μA
THERMAL MONITORING AND PROTECTION						
TTSNS Voltage Range (Note 2)			0		5.0	V
TTSNS Threshold		V_{CC} = 5.0 V, TTSNS is falling	2.45	2.5	2.55	V
TTSNS Hysteresis			50	110		mV
TTSNS Bias Current		TTSNS = 2.6 V	−2.0		2.0	μA
VRTT Output Voltage	V_{VRTT}	Logic low, $I_{VRTT(SINK)}$ = 400 μA Logic high, $I_{VRTT(SOURCE)}$ = −400 μA	 4.0	10 5.0	100	mV V
SUPPLY						
Supply Voltage Range	V_{CC}		4.5		5.5	V
Supply Current		EN = H EN = 0 V		6.0 15	10 50	mA μA
V_{CC} OK Threshold	V_{CCOK}	V_{CC} is Rising		4.3	4.5	V
V_{CC} UVLO Threshold	V_{CCUVLO}	V_{CC} is Falling	4.0	4.1		V
V_{CC} Hysteresis (Note 2)				210		mV
HIGH−SIDE MOSFET DRIVER						
Pullup Resistance, Sourcing Current		BST = PVCC		1.8	3.3	Ω
Pulldown Resistance, Sinking Current		BST = PVCC		1.0	3.0	Ω

1. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).
2. Guaranteed by design or bench characterization, not production tested.
3. Timing is referenced to the 90% and 10% points, unless otherwise noted.

ELECTRICAL CHARACTERISTICS V_{CC} = P_{VCC1} = P_{VCC2} = BST1 = BST2 = High = 5.0V, FBRTN = GND = SW1 = SW2 = PGND1 = PGND2 = Low = 0 V, EN = VATFREQ = High, DPRSLP = 0 V, $\overline{PSI}$ = 1.05 V, V_{VID} = 1.2000 V, T_A = −40°C to 100°C, unless otherwise noted (Note 1). Current entering a pin (sunk by the device) has a positive sign. R_{REF} = 80 kΩ.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
HIGH−SIDE MOSFET DRIVER						
Transition Times	tr_{DRVH} tf_{DRVH}	BST = PVCC, C_L = 3 nF, Figure 6 BST = PVCC, C_L = 3 nF, Figure 6		15 13	35 31	ns
Dead Delay Times	$tpdh_{DRVH}$	BST = PVCC, Figure 6		39	50	ns
BST Quiescent Current		EN = L (Shutdown) EN = H, no switching		0.6 15	5.0	μA
LOW−SIDE MOSFET DRIVER						
Pullup Resistance, Sourcing Current		BST = PVCC		1.6	3.3	Ω
Pulldown Resistance, Sinking Current		BST = PVCC		0.8	2.5	Ω
Transition Times	tr_{DRVL} tf_{DRVL}	C_L = 3 nF, Figure 6 C_L = 3 nF, Figure 6		15 14	35 35	ns
Progation Delay Times	$tpdh_{DRVL}$	C_L = 3 nF, Figure 6		10	45	ns
SW Transition Times	t_{TOSW}	DRVH = L, SW = 2.5 V	210	250	450	ns
SW Off Threshold	V_{OFFSW}			1.6		V
PVCC Quiescent Current		EN = L (Shutdown) EN = H, no switching		1.0 240	15	μA
BOOTSTRAP RECTIFIER SWITCH						
On Resistance		EN = L or EN = H and DRVL = H	3.0	6.0	1.0	Ω

1. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).
2. Guaranteed by design or bench characterization, not production tested.
3. Timing is referenced to the 90% and 10% points, unless otherwise noted.

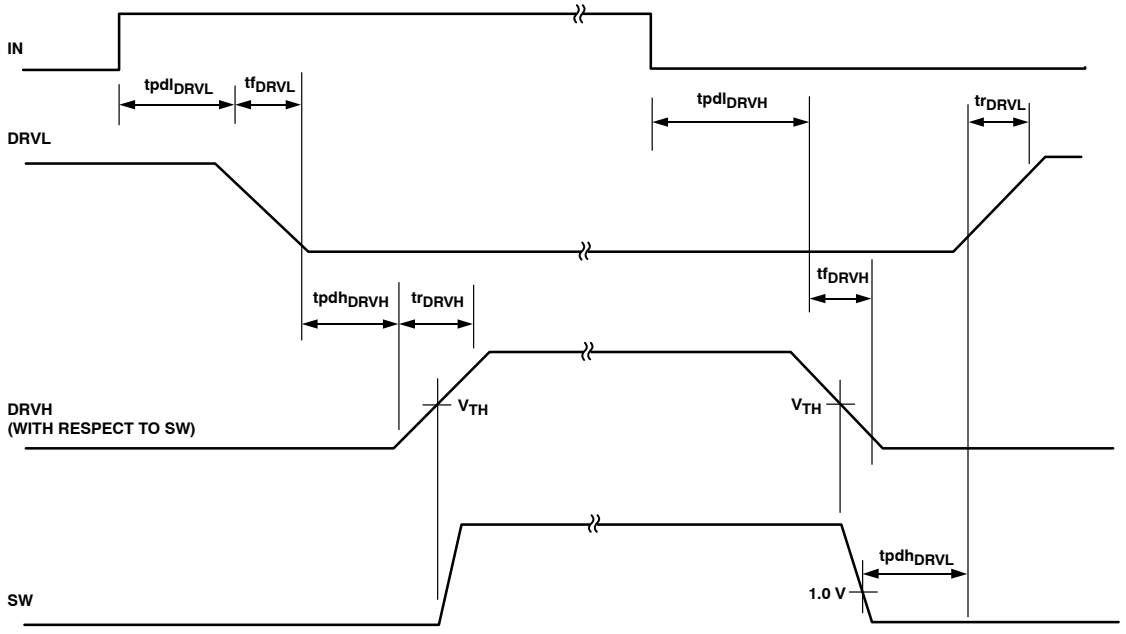

Figure 6. Timing Diagram (Note 3)

TYPICAL PERFORMANCE CHARACTERISTICS

V_{VID} = 1.5 V, T_A = 20°C to 100°C, unless otherwise noted.

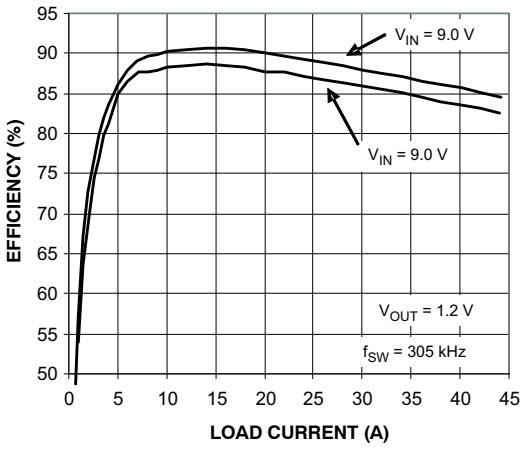

Figure 7. PWM Mode Efficiency vs. Load Current

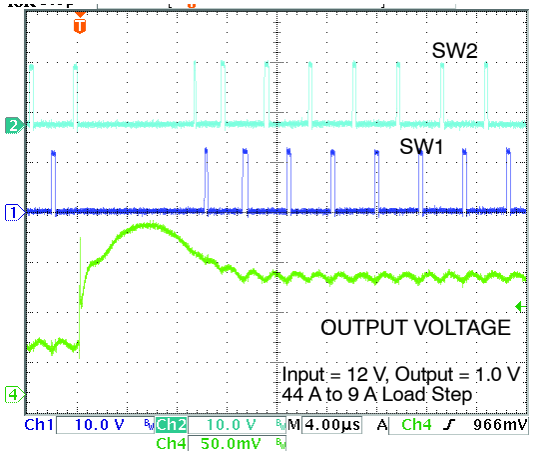

Figure 8. Load Transient with 2−Phases

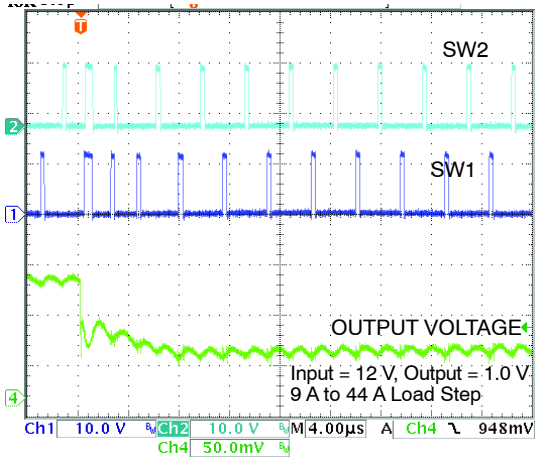

Figure 9. Load Transient with 2 Phases

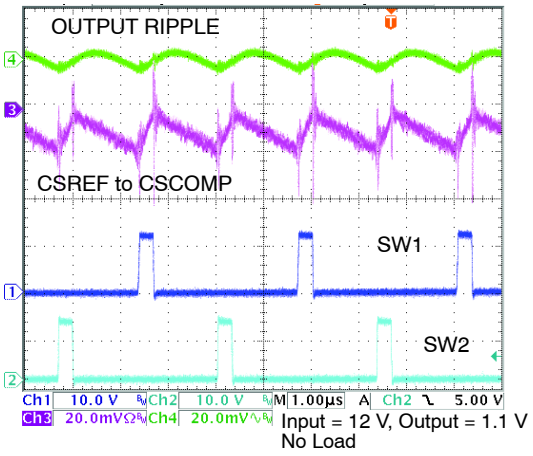

Figure 10. Switching Waveforms in 2 Phase

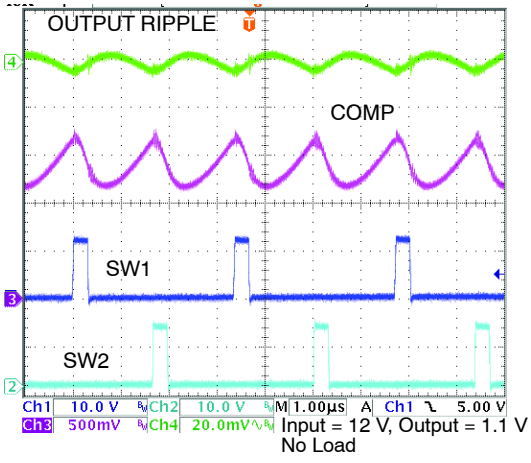

Figure 11. Switching Waveforms in 2−Phase

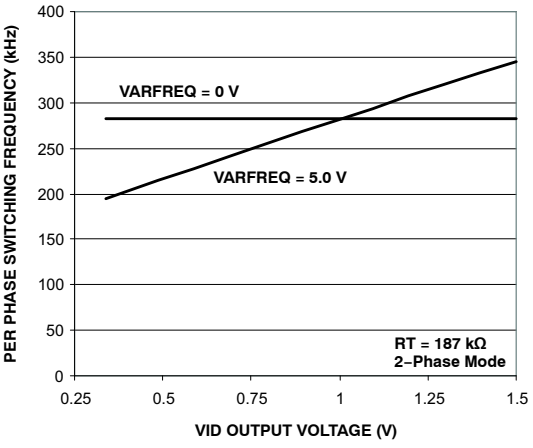

Figure 12. Switching Frequency vs. VID Output Voltage in PWM Mode

TYPICAL PERFORMANCE CHARACTERISTICS

V_{VID} = 1.5 V, T_A = 20°C to 100°C, unless otherwise noted.

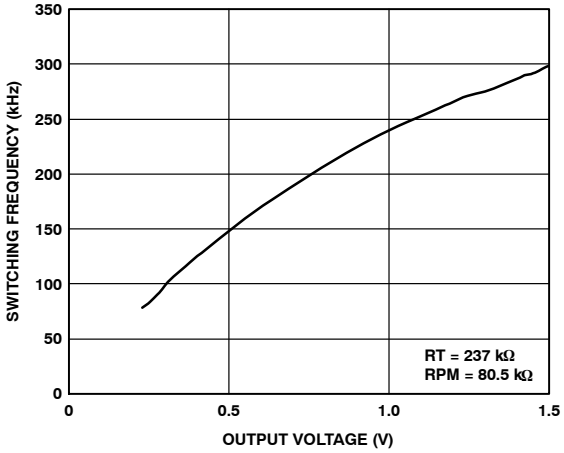

Figure 13. Switching Frequency vs. Output Voltage in RPM Mode

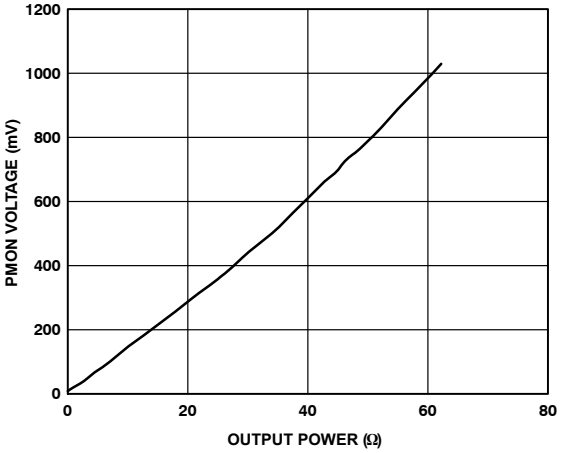

Figure 14. IMON Voltage vs. Output Current

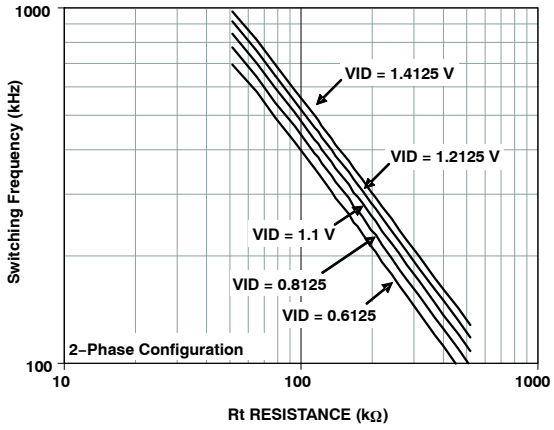

Figure 15. Per Phase Switching Frequency vs. RT Resistance

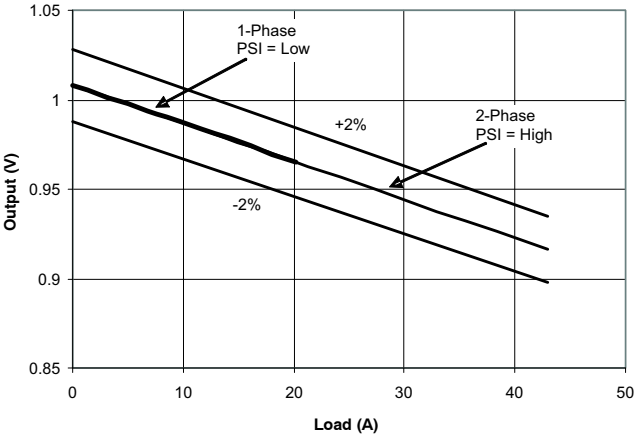

Figure 16. Load Line Accuracy

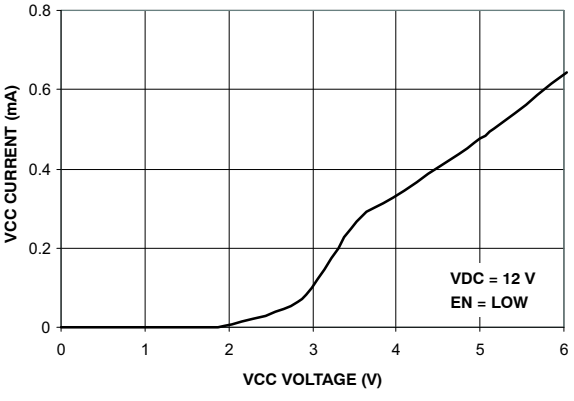

Figure 17. VCC Current vs. VCC Voltage with Enable Low

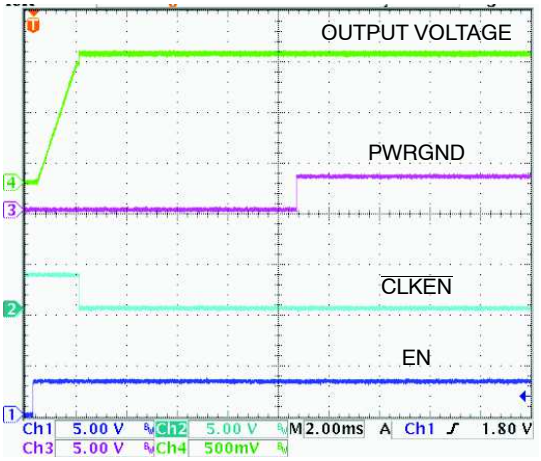

Figure 18. Startup Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS

V_{VID} = 1.5 V, T_A = 20°C to 100°C, unless otherwise noted.

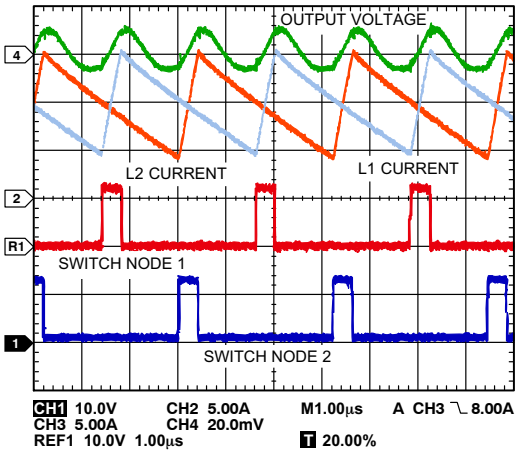

Figure 19. Dual−Phase, Interleaved PWM Waveform, 20 A Load

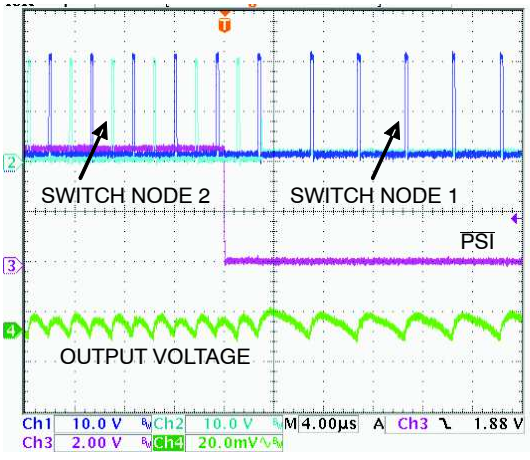

Figure 20. $\overline{\text{PSI}}$ Transition

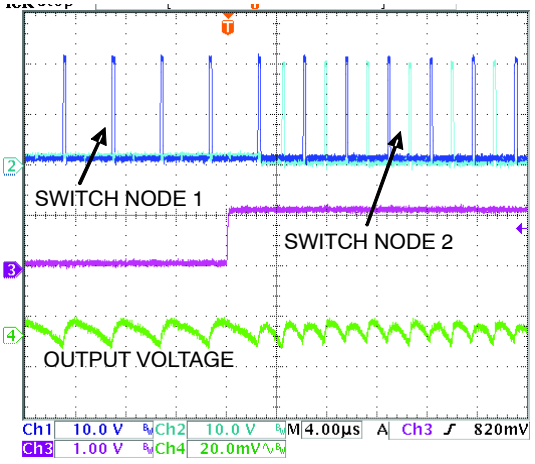

Figure 21. $\overline{\text{PSI}}$ Transition

TYPICAL PERFORMANCE CHARACTERISTICS

V_{VID} = 1.5 V, T_A = 20°C to 100°C, unless otherwise noted.

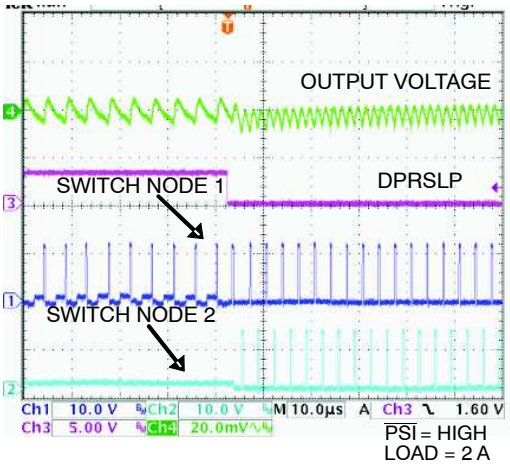

Figure 22. DPRSLP Transition

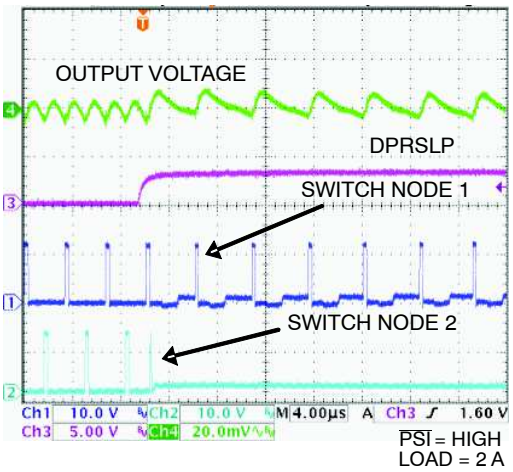

Figure 23. DPRSLP Transition

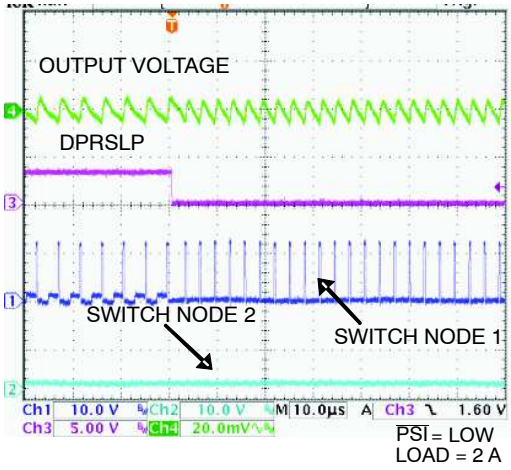

Figure 24. DPRSLP Transition

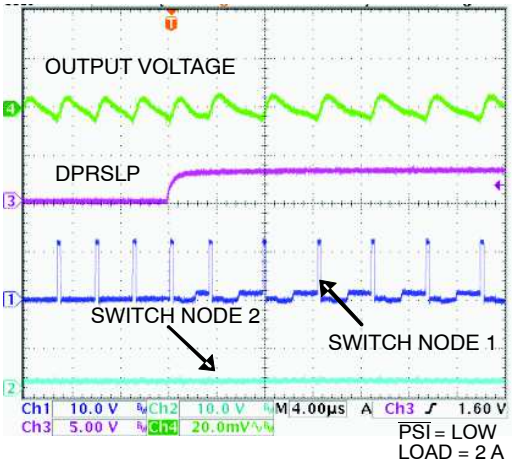

Figure 25. DPRSLP Transition

Theory of Operation

The ADP3208C combines multi−mode Pulse Width Modulated (PWM) control and Ramp Pulse Modulated (RPM) control with multi−phase logic outputs for use in single− and dual−phase synchronous buck CPU core supply power converters. The internal 7−bit VID DAC conforms to the Intel IMVP−6+ specifications.

Multiphase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling high currents in a single−phase converter would put too high of a thermal stress on system components such as the inductors and MOSFETs.

The multi−mode control of the ADP3208C is a stable, high performance architecture that includes

- Current and thermal balance between phases
- High speed response at the lowest possible switching frequency and minimal count of output decoupling capacitors
- Minimized thermal switching losses due to lower frequency operation
- High accuracy load line regulation
- High current output by supporting 2−phase operation
- Reduced output ripple due to multiphase ripple cancellation
- High power conversion efficiency with heavy and light loads
- Increased immunity from noise introduced by PC board layout constraints
- Ease of use due to independent component selection
- Flexibility in design by allowing optimization for either low cost or high performance

Number of Phases

The number of operational phases can be set by the user. Tying the SP pin to the VCC pin forces the chip into single−phase operation. Otherwise, dual−phase operation is automatically selected, and the chip switches between single− and dual−phase modes as the load changes to optimize power conversion efficiency.

In dual−phase configuration, SP is low and the timing relationship between the two phases is determined by internal circuitry that monitors the PWM outputs. Because each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one output can be active at a time, permitting overlapping phases.

Operation Modes

The number of phases can be static (see the Number of Phases section) or dynamically controlled by system signals to optimize the power conversion efficiency with heavy and light loads.

If SP is set low (user−selected dual−phase mode) during a VID transient or with a heavy load condition (indicated by DPRSLP being low and $\overline{\text{PSI}}$ being high), the ADP3208C runs in 2−phase, interleaved PWM mode to achieve minimal V_{CORE} output voltage ripple and the best transient performance possible. If the load becomes light (indicated by $\overline{\text{PSI}}$ being low or DPRSLP being high), ADP3208C switches to single−phase mode to maximize the power conversion efficiency.

In addition to changing the number of phases, the ADP3208C is also capable of dynamically changing the control method. In dual−phase operation, the ADP3208C runs in PWM mode, where the switching frequency is controlled by the master clock. In single−phase operation (commanded by the $\overline{\text{PSI}}$ low state), the ADP3208C runs in RPM mode, where the switching frequency is controlled by the ripple voltage appearing on the COMP pin. In RPM mode, the DRVH1 pin is driven high each time the COMP pin voltage rises to a voltage limit set by the VID voltage and an external resistor connected from the RPM to GND. If the device is in single−phase mode and the system signal DPRSLP is asserted high during the deeper sleep mode of CPU operation, the ADP3208C continues running in RPM mode but offers the option of turning off the low−side (synchronous rectifier) MOSFET when the inductor current drops to 0. Turning off the low−side MOSFETs at the zero current crossing prevents reversed inductor current build up and breaks synchronous operation of high− and low−side switches. Due to the asynchronous operation, the switching frequency becomes slower as the load current decreases, resulting in good power conversion efficiency with very light loads.

Table 1 summarizes how the ADP3208C dynamically changes the number of active phases and transitions the operation mode based on system signals and operating conditions.

Table 1. Phase Number and Operation Modes

$\overline{\text{PSI}}$	DPRSLP	VID Transient (Note 1)	Current Limit	No. of Phases Selected by User	No. of Phases in Operation	Operation Mode (Note 2)
*	*	Yes	*	N [2 or 1]	N	PWM, CCM only
1	0	No	*	N [2 or 1]	N	PWM, CCM only
0	0	No	No	*	1	RPM, CCM only
0	0	No	Yes	*	1	PWM, CCM only
*	1	No	No	*	1	RPM, automatic CCM/DCM
*	1	No	Yes	*	1	PWM, CCM only

* = Don't Care

1. VID transient period is the time following any VID change, including entry into and exit from deeper sleep mode. The duration of VID transient period is the same as that of PWRGD masking time.
2. CCM stands for continuous current mode, and DCM stands for discontinuous current mode.

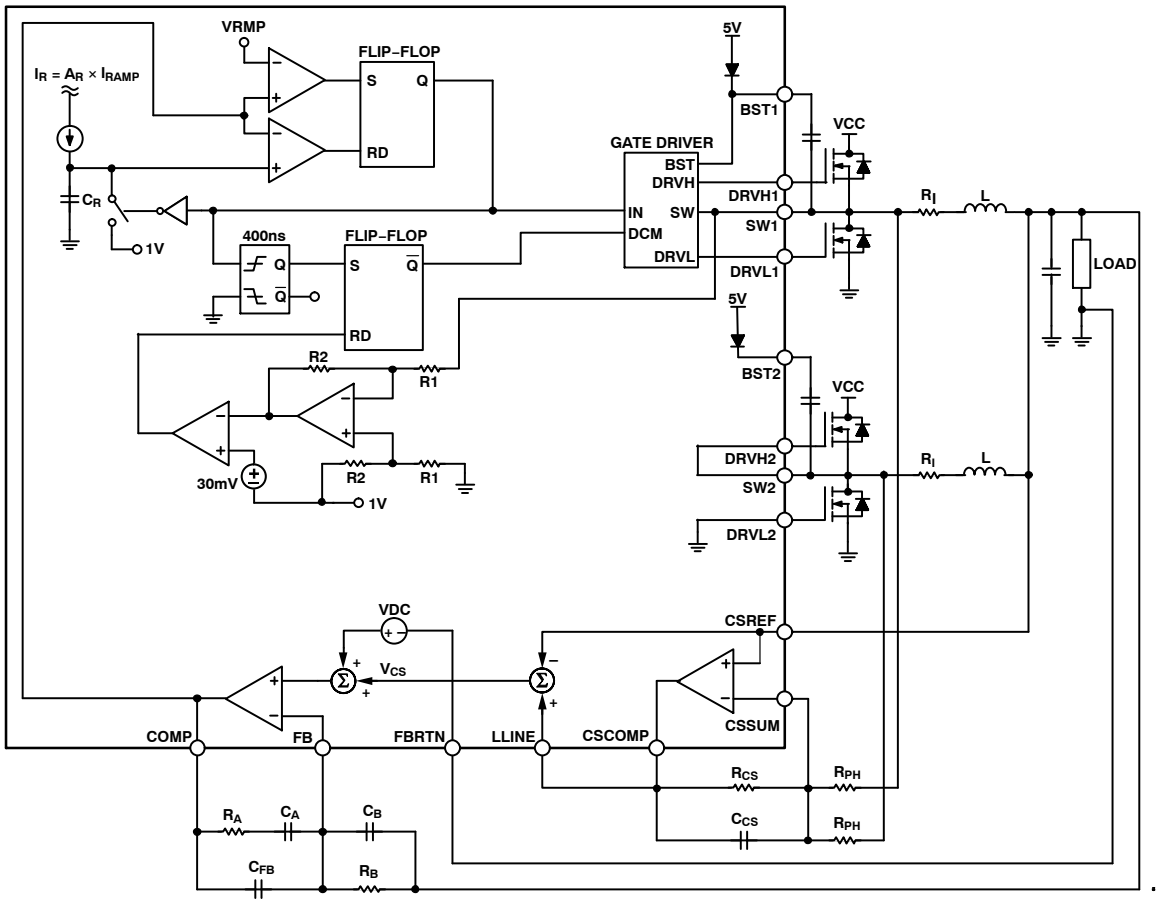

Figure 26. Single−Phase RPM Mode Operation

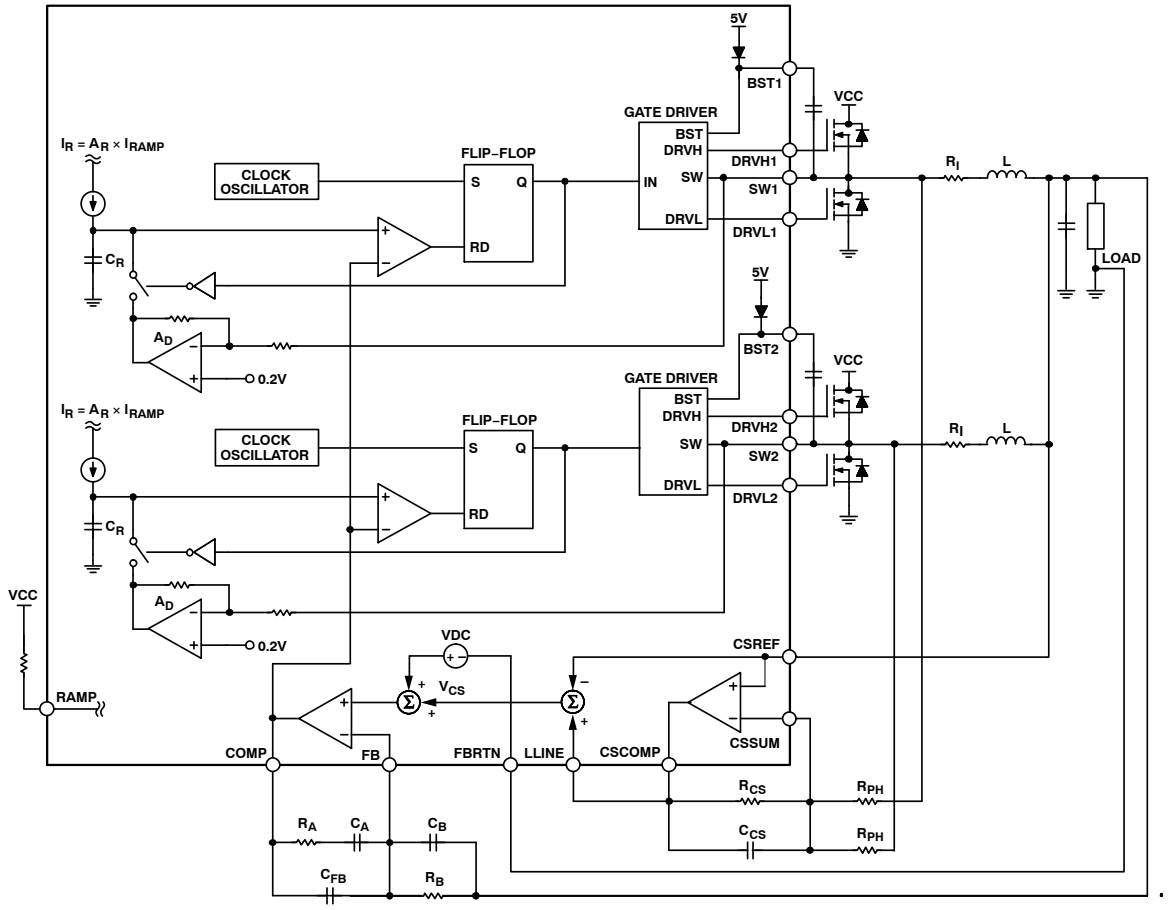

Figure 27. Dual−Phase PWM Mode Operation

Setting Switch Frequency

Master Clock Frequency in PWM Mode

When the ADP3208C runs in PWM, an external resistor connected from the RT pin to GND sets the clock frequency. The frequency is constant at a given VID code but varies with the VID voltage: the lower the VID voltage, the lower the clock frequency. The variation of clock frequency with VID voltage maintains constant V_{CORE} ripple and improves power conversion efficiency at lower VID voltages. Figure 15 shows the relationship between clock frequency and VID voltage, parametrized by RT resistance.

To determine the switching frequency per phase, divide the clock by the number of phases in use.

Switching Frequency in RPM Mode — Single−Phase Operation

In single−phase RPM mode, the switching frequency is controlled by the ripple voltage on the COMP pin, rather than by the master clock. Each time the COMP pin voltage exceeds the RPM pin voltage threshold level determined by the VID voltage and the external resistor connected from RPM to GND, an internal ramp signal is started and DRVH1 is driven high. The slew rate of the internal ramp is programmed by the current entering the RAMP pin. One−third of the RAMP current charges an internal ramp capacitor (5 pF typical) and creates a ramp. When the internal ramp signal intercepts the COMP voltage, the DRVH1 pin is reset low.

In continuous current mode, the switching frequency of RPM operation is almost constant. While in discontinuous current conduction mode, the switching frequency is reduced as a function of the load current.

Differential Sensing of Output Voltage

The ADP3208C combines differential sensing with a high accuracy VID DAC, referenced by a precision band gap source and a low offset error amplifier, to meet the rigorous accuracy requirement of the Intel IMVP−6+ specification. In steady−state mode, the combination of the VID DAC and error amplifier maintain the output voltage for a worst−case scenario within ±8 mV of the full operating output voltage and temperature range.

The CPU core output voltage is sensed between the FB and FBRTN pins. FB should be connected through a resistor to the positive regulation point; the VCC remote sensing pin of the microprocessor. FBRTN should be connected directly to the negative remote sensing point; the V_{SS} sensing point of the CPU. The internal VID DAC and precision voltage reference are referenced to FBRTN and have a maximum current of 200 μA for guaranteed accurate remote sensing.

Output Current Sensing

The ADP3208C includes a dedicated Current Sense Amplifier (CSA) to monitor the total output current of the converter for proper voltage positioning vs. load current and for over current detection. Sensing the current delivered to the load is an inherently more accurate method than detecting peak current or sampling the current across a sense element, such as the low−side MOSFET. The CSA can be configured several ways, depending on system optimization objectives, and the current information can be obtained by:

- Output inductor ESR sensing without the use of a thermistor for the lowest cost
- Output inductor ESR sensing with the use of a thermistor that tracks inductor temperature to improve accuracy
- Discrete resistor sensing for the highest accuracy

At the positive input of the CSA, the CSREF pin is connected to the output voltage. At the negative input (that is, the CSSUM pin of the CSA), signals from the sensing element (in the case of inductor DCR sensing, signals from the switch node side of the output inductors) are summed together by series summing resistors. The feedback resistor between the CSCOMP and CSSUM pins sets the gain of the CSA, and a filter capacitor is placed in parallel with this resistor. The current information is then given as the voltage difference between the CSCOMP and CSREF pins. This signal is used internally as a differential input for the current limit comparator.

An additional resistor divider connected between the CSCOMP and CSREF pins with the midpoint connected to the LLINE pin can be used to set the load line required by the microprocessor specification. The current information to set the load line is then given as the voltage difference between the LLINE and CSREF pins. This configuration allows the load line slope to be set independent from the current limit threshold. If the current limit threshold and load line do not have to be set independently, the resistor divider between the CSCOMP and CSREF pins can be omitted and the CSCOMP pin can be connected directly to LLINE. To disable voltage positioning entirely (that is, to set no load line), LLINE should be tied to CSREF.

To provide the best accuracy for current sensing, the CSA has a low offset input voltage and the sensing gain is set by an external resistor ratio.

Active Impedance Control Mode

To control the dynamic output voltage droop as a function of the output current, the signal that is proportional to the total output current, converted from the voltage difference between LLINE and CSREF, can be scaled to be equal to the required droop voltage. This droop voltage is calculated by multiplying the droop impedance of the regulator by the output current. This value is used as the control voltage of the PWM regulator. The droop voltage is subtracted from the DAC reference output voltage, and the resulting voltage is used as the voltage positioning setpoint. The arrangement results in an enhanced feed−forward response.

Current Control Mode and Thermal Balance

The ADP3208C has individual inputs for monitoring the current of each phase. The phase current information is combined with an internal ramp to create a current−balancing feedback system that is optimized for initial current accuracy and dynamic thermal balance. The current balance information is independent from the total inductor current information used for voltage positioning described in the Active Impedance Control Mode section.

The magnitude of the internal ramp can be set so that the transient response of the system is optimal. The ADP3208C monitors the supply voltage to achieve feed forward control whenever the supply voltage changes. A resistor connected from the power input voltage rail to the RAMP pin determines the slope of the internal PWM ramp. More detail about programming the ramp is provided in the Application Information section.

The ADP3208C should not require external thermal balance circuitry if a good layout is used. However, if mismatch is desired due to uneven cooling in phase, external resistors can be added to individually control phase currents as long as the phase currents are mismatched by less than 30%. If unwanted mismatch exceeds 30%, a new layout that improves phase symmetry should be considered.

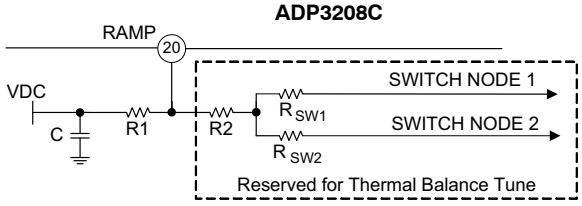

Figure 28. Optional Current Balance Resistors

In 2−phase operation, alternate cycles of the internal ramp control the duty cycle of the separate phases. Figure 28 shows the addition of two resistors from each switch node to the RAMP pin; this modifies the ramp−charging current individually for each phase. During Phase 1, SW Node 1 is high (practically at the input voltage potential) and SW Node 2 is low (practically at the ground potential). As a consequence, the RAMP pin, through the R2 resistor, sees the tap point of a divider connected to the input voltage, where R_{SW1} is the upper element and R_{SW2} is the lower element of the divider. During Phase 2, the voltages on SW Node 1 and SW Node 2 switch and the resistors swap functions. Tuning R_{SW1} and R_{SW2} allows the current to be optimally set for each phase. To increase the current for a given phase, decrease R_{SW} for that phase.

Voltage Control Mode

A high−gain bandwidth error amplifier is used for the voltage mode control loop. The noninverting input voltage

is set via the 7−bit VID DAC. The VID codes are listed in the VID Code table. The noninverting input voltage is offset by the droop voltage as a function of current, commonly known as active voltage positioning. The output of the error amplifier is the COMP pin, which sets the termination voltage of the internal PWM ramps.

At the negative input, the FB pin is tied to the output sense location using R_B, a resistor for sensing and controlling the output voltage at the remote sensing point. The main loop compensation is incorporated in the feedback network connected between the FB and COMP pins.

Power−Good Monitoring

The power−good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open−drain output that can be pulled up through an external resistor to a voltage rail, not necessarily the same VCC voltage rail that is running the controller. A logic high level indicates that the output voltage is within the voltage limits defined by a range around the VID voltage setting. PWRGD goes low when the output voltage is outside of this range.

Following the IMVP−6+ specification, the PWRGD range is defined to be 300 mV less than and 200 mV greater than the actual VID DAC output voltage. For any DAC voltage less than 300 mV, only the upper limit of the PWRGD range is monitored. To prevent a false alarm, the power−good circuit is masked during various system transitions, including a VID change and entrance into or exit out of deeper sleep. The duration of the PWRGD mask is set to approximately 130 μs by an internal timer. If the voltage drop is greater than 200 mV during deeper sleep entry or slow deeper sleep exit, the duration of PWRGD masking is extended by the internal logic circuit.

Powerup Sequence and Soft−Start

The power−on ramp−up time of the output voltage is set internally. The powerup sequence, including the soft−start is illustrated in Figure 29.

After EN is asserted high, the soft−start sequence starts. The core voltage ramps up linearly to the boot voltage. The ADP3208C regulates at the boot voltage for 100 μs. After the boot time is completed, $\overline{\text{CLKEN}}$ is asserted low. After $\overline{\text{CLKEN}}$ is asserted low for 9ms, PWRGD is asserted high.

In VCC UVLO or in shutdown, a small MOSFET turns on connecting the CSREF to GND. The MOSFET on the CSREF pin has a resistance of approximately 100Ω. When VCC ramps above the upper UVLO threshold and EN is asserted high, the ADP3208C enables internal bias and starts a reset cycle that lasts about 50 μs to 60 μs. Next, when initial reset is over, the chip detects the number of phases set by the user, and gives a go signal to start soft−start. The ADP3208C reads the VID codes provided by the CPU on VID0 to VID6 input pins after $\overline{\text{CLKEN}}$ is asserted low. The PWRGD signal is asserted after a t_{CPU_PWRGD} delay of about 9 ms, as specified by IMVP−6+. The power−good delay is programmed internally.

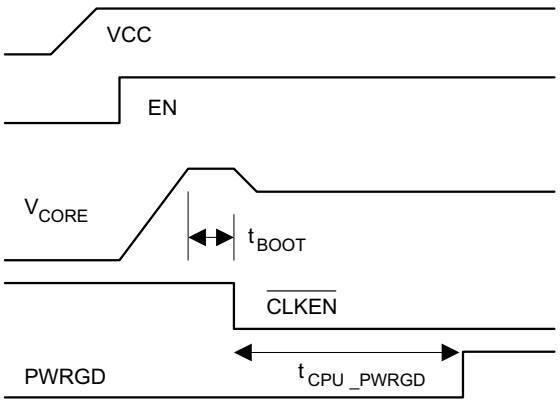

Figure 29. Powerup Sequence of ADP3208C

If EN is taken low or VCC drops below the VCC UVLO threshold, both the SS capacitor and the PGDELAY capacitor are reset to ground to prepare the chip for a subsequent soft−start cycle.

Soft Transient

When a VID input changes, the ADP3208C detects the change but ignores new code for a minimum of 400 ns. This delay is required to prevent the device from reacting to digital signal skew while the 7−bit VID input code is in transition. Additionally, the VID change triggers a PWRGD masking timer to prevent a PWRGD failure. Each VID change resets and retriggers the internal PWRGD masking timer.

The ADP3208C provides a soft transient function to reduce inrush current during VID transitions. Reducing the inrush current helps decrease the acoustic noise generated by the MLCC input capacitors and inductors.

The soft transient feature is implemented internally. When a new VID code is detected, the ADP3208C steps sequentially through each VID voltage to the final VID voltage. There is a PWRGD masking time of 100μs after the last VID code is changed internally. Table 2 lists the soft transient slew rate.

Table 2. Soft Transient Slew Rate

VID Transient	DPRSLP	Slew Rate
Entrance to Deeper Sleep	HIGH	−3.125mV/μs
Fast Exit from Deeper Sleep	LOW	+12.5mV/μs
Slow Exit from Deeper Sleep	HIGH	+3.125mV/μs
Transient from V_{BOOT} to VID	DNC[1]	±3.125mV/μs

1. DNC = Do Not Care.

Current Limit

The ADP3208C compares the differential output of a current sense amplifier to a programmable current limit setpoint to provide current limiting function. The current limit set point is set with a resistor connected from I_{LIM} pin to CSCOMP pin. This is the R_{lim} resistor. During normal

operation, the voltage on the I_{LIM} pin is equal to the CSREF pin. The voltage across R_{LIM} is equal to the voltage across the CSA (from CSREF pin to CSCOMP pin). This voltage is proportional to output current. The current through R_{LIM} is proportional to the output inductor current. The current through R_{LIM} is compared with an internal reference current. When the R_{LIM} current goes above the internal reference current, the ADP3208C goes into current limit. The current limit circuit is shown in Figure 30.

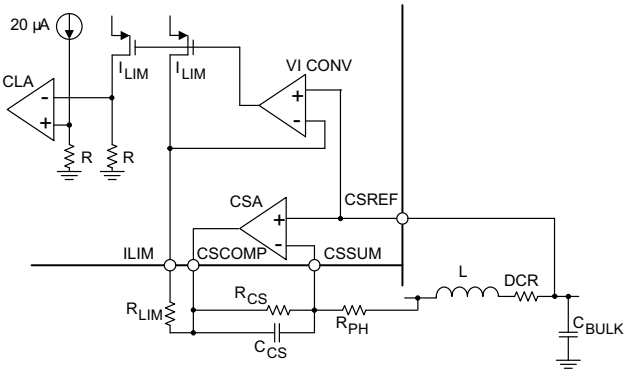

Figure 30. Current Limit Circuit

During startup when the output voltage is below 200 mV, a secondary current limit is activated. This is necessary because the voltage swing on CSCOMP cannot extend below ground. The secondary current limit circuit clamps the internal COMP voltage and sets the internal compensation ramp termination voltage at 1.5 V level. The clamp actually limits voltage drop across the low side MOSFETs through the current balance circuitry.

An inherent per phase current limit protects individual phases in case one or more phases stop functioning because of a faulty component. This limit is based on the maximum normal mode COMP voltage.

After 9 ms in current limit, the ADP3208C will latchoff. The latchoff can be reset by removing and reapplying VCC, or by recycling the EN pin low and high for a short time.

The latchoff can be reset by removing and reapplying VCC, or by recycling the EN pin low and high for a short time.

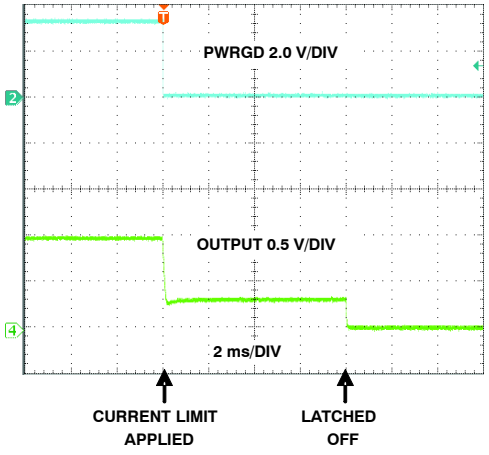

Figure 31. Current Overload

Changing VID OTF

The ADP3208C is designed to track dynamically changing VID code. As a consequence, the CPU VCC voltage can change without the need to reset the controller or the CPU. This concept is commonly referred to as VID OTF transient. A VID OTF can occur with either light or heavy load conditions. The processor alerts the controller that a VID change is occurring by changing the VID inputs in LSB incremental steps from the start code to the finish code. The change can be either upwards or downwards steps.

When a VID input changes, the ADP3208C detects the change but ignores new code for a minimum of 400 ns. This delay is required to prevent the device from reacting to digital signal skew while the 7−bit VID input code is in transition. Additionally, the VID change triggers a PWRGD masking timer to prevent a PWRGD failure. Each VID change resets and retriggers the internal PWRGD masking timer.

As listed in Table 3, during a VID transient, the ADP3208C forces PWM mode regardless of the state of the system input signals. For example, this means that if the chip is configured as a dual−phase controller but is running in single−phase mode due to a light load condition, a current overload event causes the chip to switch to dual−phase mode to share the excessive load until the delayed current limit latchoff cycle terminates.

In user−set single−phase mode, the ADP3208C usually runs in RPM mode. When a VID transition occurs, however, the ADP3208C switches to dual−phase PWM mode.

Light Load RPM DCM Operation

In single−phase normal mode, DPRSLP is pulled low and the APD3208 operates in Continuous Conduction Mode (CCM) over the entire load range. The upper and lower MOSFETs run synchronously and in complementary phase. See Figure 32 for the typical waveforms of the ADP3208C running in CCM with a 7 A load current.

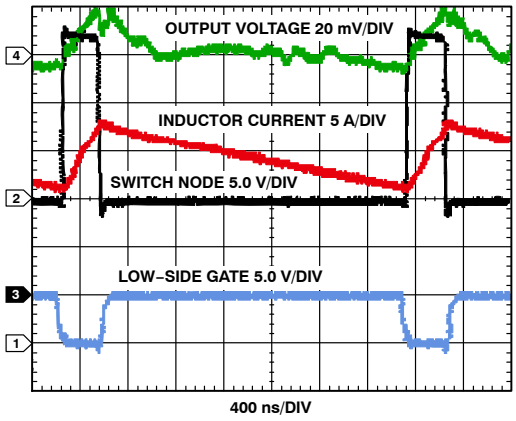

Figure 32. Single−Phase Waveforms in CCM

If DPRSLP is pulled high, the ADP3208C operates in RPM mode. If the load condition is light, the chip enters Discontinuous Conduction Mode (DCM). Figure 33 shows a typical single−phase buck with one upper FET, one lower FET, an output inductor, an output capacitor, and a load resistor. Figure 34 shows the path of the inductor current with the upper FET on and the lower FET off. In Figure 35 the high−side FET is off and the low−side FET is on. In CCM, if one FET is on, its complementary FET must be off; however, in DCM, both high− and low−side FETs are off and no current flows into the inductor (see Figure 36). Figure 37 shows the inductor current and switch node voltage in DCM.

In DCM with a light load, the ADP3208C monitors the switch node voltage to determine when to turn off the low−side FET. Figure 38 shows a typical waveform in DCM with a 1 A load current. Between t_1 and t_2, the inductor current ramps down. The current flows through the source drain of the low−side FET and creates a voltage drop across the FET with a slightly negative switch node. As the inductor current ramps down to 0 A, the switch voltage approaches 0 V, as seen just before t_2. When the switch voltage is approximately −6 mV, the low−side FET is turned off.

Figure 37 shows a small, dampened ringing at t_2. This is caused by the LC created from capacitance on the switch node, including the C_{DS} of the FETs and the output inductor. This ringing is normal.

The ADP3208C automatically goes into DCM with a light load. Figure 38 shows the typical DCM waveform of the ADP3208C. As the load increases, the ADP3208C enters into CCM. In DCM, frequency decreases with load current. Figure 39 shows switching frequency vs. load current for a typical design. In DCM, switching frequency is a function of the inductor, load current, input voltage, and output voltage.

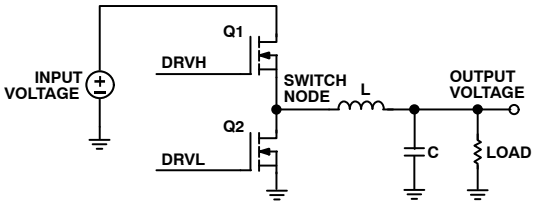

Figure 33. Buck Topology

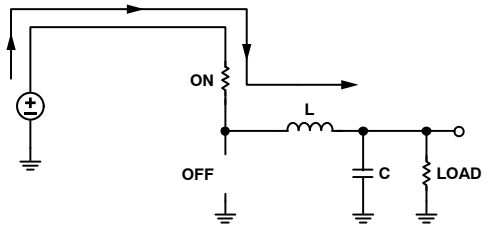

Figure 34. Buck Topology Inductor Current During t_0 and t_1

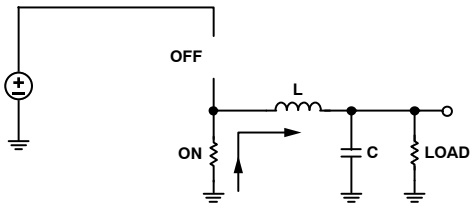

Figure 35. Buck Topology Inductor Current During t_1 and t_2

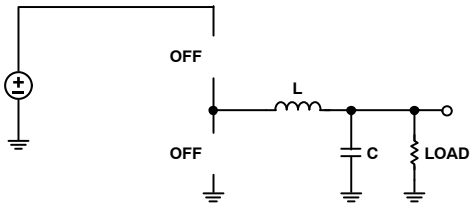

Figure 36. Buck Topology Inductor Current During t_2 and t_3

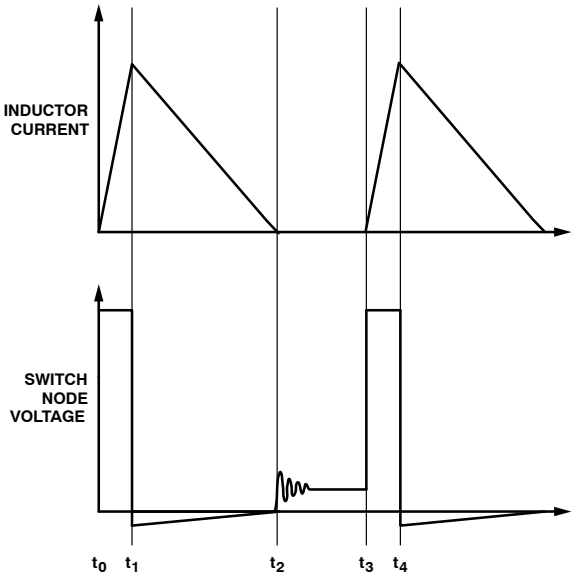

Figure 37. Inductor Current and Switch Node in DCM

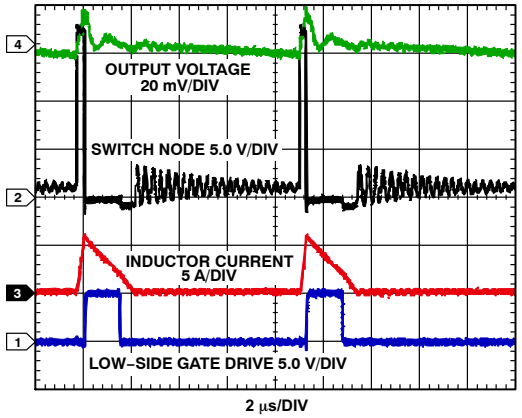

Figure 38. Single−Phase Waveforms in DCM with 1 A Load Current

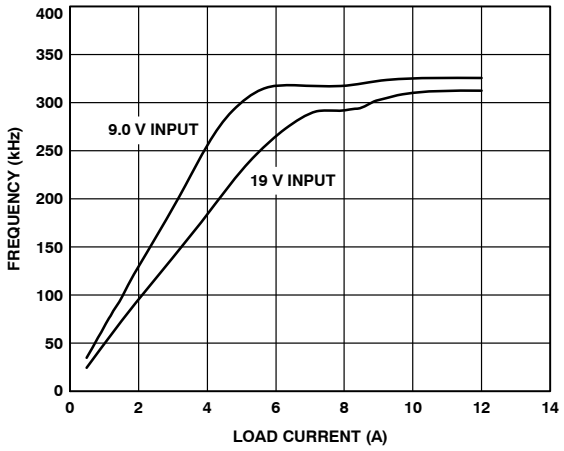

Figure 39. Single−Phase CCM/DCM Frequency vs. Load Current

Output Crowbar

To prevent the CPU and other external components from damage due to overvoltage, the ADP3208C turns off the DRVH1 and DRVH2 outputs and turns on the DRVL1 and DRVL2 outputs when the output voltage exceeds the OVP threshold (1.7 V typical).

Turning on the low−side MOSFETs forces the output capacitor to discharge and the current to reverse due to current build up in the inductors. If the output overvoltage is due to a drain−source short of the high−side MOSFET, turning on the low−side MOSFET results in a crowbar across the input voltage rail. The crowbar action blows the fuse of the input rail, breaking the circuit and thus protecting the microprocessor from destruction.

When the OVP feature is triggered, the ADP3208C is latched off. The latchoff function can be reset by removing and reapplying VCC to the ADP3208C or by briefly pulling the EN pin low.

Pulling TTSNS to less than 1.0 V disables the overvoltage protection function. In this configuration, VRTT should be tied to ground.

Reverse Voltage Protection

Very large reverse current in inductors can cause negative V_{CORE} voltage, which is harmful to the CPU and other output components. The ADP3208C provides a reverse voltage protection (RVP) function without additional system cost. The V_{CORE} voltage is monitored through the CSREF pin. When the CSREF pin voltage drops to less than −300 mV, the ADP3208C triggers the RVP function by disabling all PWM outputs and driving DRVL1 and DRVL2 low, thus turning off all MOSFETs. The reverse inductor currents can be quickly reset to 0 by discharging the built−up energy in the inductor into the input dc voltage source via the forward−biased body diode of the high−side MOSFETs. The RVP function is terminated when the CSREF pin voltage returns to greater than −100 mV.

Sometimes the crowbar feature inadvertently causes output reverse voltage because turning on the low−side MOSFETs results in a very large reverse inductor current. To prevent damage to the CPU caused from negative voltage, the ADP3208C maintains its RVP monitoring function even after OVP latchoff. During OVP latchoff, if the CSREF pin voltage drops to less than −300 mV, the low−side MOSFETs is turned off. DRVL outputs are allowed to turn back on when the CSREF voltage recovers to greater than −100 mV.

Figure 40 shows a typical OVP test. FB pin is shorted to ground causing the control to command a large duty cycle. The output voltage climbs up. When the output voltage is climbs 200 mV above the DAC voltage, the PWRGD signal de−asserts. When the output voltage climbs to 1.7V, OVP is enabled. In OVP, the phase 1 and phase 2 low side drive turns on the low side power MOSFETs. The low side MOSFETs pull the output voltage low through the power inductor. When the output voltage falls below −300 mV, Reverse Voltage Protection is enabled. In Reverse Voltage Protection, all power MOSFETs are turned off. This protects the CPU from seeing a large negative voltage.

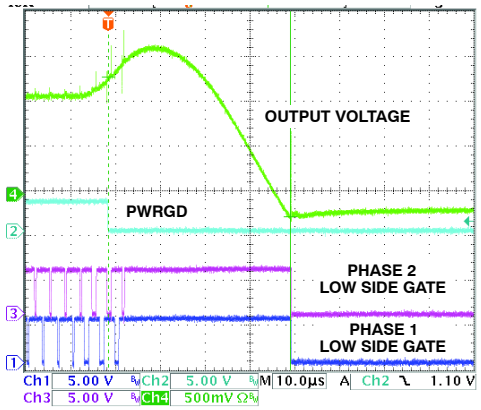

Figure 40. Overvoltage Protection and Reverse Voltage Protection

Output Enable and UVLO

For the ADP3208C to begin switching the VCC supply voltage to the controller must be greater than the V_{CCO} threshold and the EN pin must be driven high. If the VCC voltage is less than the V_{CCUVLO} threshold or the EN pin is a logic low, the ADP3208C shuts off. In shutdown mode, the controller holds the PWM outputs low, shorts the capacitors of the SS and PGDELAY pins to ground, and drives the DRVH and DRVL outputs low.

The user must adhere to proper power supply sequencing during startup and shutdown of the ADP3208C. All input pins must be at ground prior to removing or applying VCC, and all output pins should be left in high impedance state while VCC is off.

Thermal Throttling Control

The ADP3208C includes a thermal monitoring circuit to detect whether the temperature of the VR has exceeded a user−defined thermal throttling threshold. The thermal monitoring circuit requires an external resistor divider connected between the VCC pin and GND. The divider consists of an NTC thermistor and a resistor. To generate a

voltage that is proportional to temperature, the midpoint of the divider is connected to the TTSNS pin. An internal comparator circuit compares the TTSNS voltage to half the VCC threshold and outputs a logic level signal at the VRTT output when the temperature trips the user−set alarm threshold. The VRTT output is designed to drive an external transistor that in turn provides the high current, open−drain VRTT signal required by the IMVP−6+ specification. The internal VRTT comparator has a hysteresis of approximately 100 mV to prevent high frequency oscillation of VRTT when the temperature approaches the set alarm point.

Current Monitor Function

The ADP3208C has an output current monitor. The IMON pin sources a current proportional to the inductor current. A resistor from IMON pin to FBRTN sets the gain. A 0.1 μF is added in parallel with R_{MON} to filter the inductor ripple. The IMON pin is clamped to prevent it from going above 1.15V

Table 3. VID Code Table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500
0	0	1	0	1	0	1	1.2375
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375

Table 3. VID Code Table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500

Table 3. VID Code Table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625
1	1	1	0	1	0	0	0.0500
1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125
1	1	1	1	0	0	0	0.0000
1	1	1	1	0	0	1	0.0000
1	1	1	1	0	1	0	0.0000
1	1	1	1	0	1	1	0.0000
1	1	1	1	1	0	0	0.0000
1	1	1	1	1	0	1	0.0000
1	1	1	1	1	1	0	0.0000
1	1	1	1	1	1	1	0.0000