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ADP3210

7-Bit, Programmable, Multiphase Mobile CPU Synchronous Buck Controller

The ADP3210 is a high efficiency, multiphase, synchronous, buck−switching regulator controller optimized for converting notebook battery voltage into the core supply voltage of high performance Intel processors. The part uses an internal 7−bit DAC to read Voltage Identification (VID) code directly from the processor that sets the output voltage. The phase relationship of the output signals can be configured for 1−, 2−, or 3−phase operation, with interleaved switching.

The ADP3210 uses a multi−mode architecture to drive the logic−level PWM outputs at a switching frequency selected by the user depending on the output current requirement. The part switches between multiphase and single−phase operation according to a system signal provided by the CPU. Shedding phases as function of the load maximizes power conversion efficiency under different load conditions. In addition, the ADP3210 supports programmable load−line resistance adjustment. As a result, the output voltage is always optimally positioned for a load transient.

The chip also provides accurate and reliable short−circuit protection with adjustable current limit threshold and a delayed power−good output that is masked during On−The−Fly (OTF) output voltage changes to eliminate false alarm.

The ADP3210 performance is specified over the extended commercial temperature range of −10°C to 100°C. The chip is available in a 40−lead QFN package.

Features

- 1−, 2−, or 3−Phase Operation at Up to 1 MHz per Phase
- Input Voltage Range of 3.3 V to 22 V
- ±6 mV Worst−Case Differential Sensing Error Overtemperature
- Interleaved PWM Outputs for Driving External High Power MOSFET Drivers
- Automatic Power−Saving Modes Maximize Efficiency During Light Load and Deeper Sleep Operation
- Active Current Balancing Between Output Phases
- Independent Current Limit and Load Line Setting Inputs for Additional Design Flexibility
- 7−Bit Digitally Programmable 0 V to 1.5 V Output
- Overload and Short−Circuit Protection with Latchoff Delay
- Built−In Clock Enable Output for Delaying CPU Clock Synchronization Until CPU Supply Voltage Stabilizes
- Output Current Monitor
- This is a Pb−Free Device

Applications

- Notebook Power Supplies for Next Generation Intel® Processors

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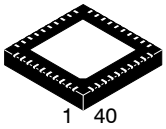
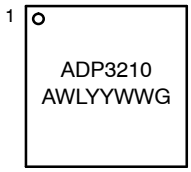


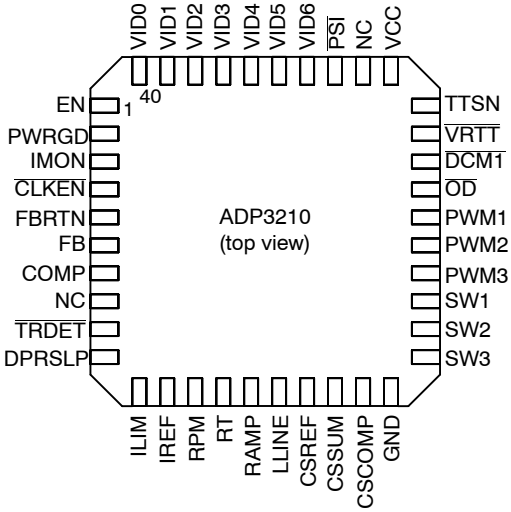
QFN40
MN SUFFIX
CASE 488AR

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 31 of this data sheet.

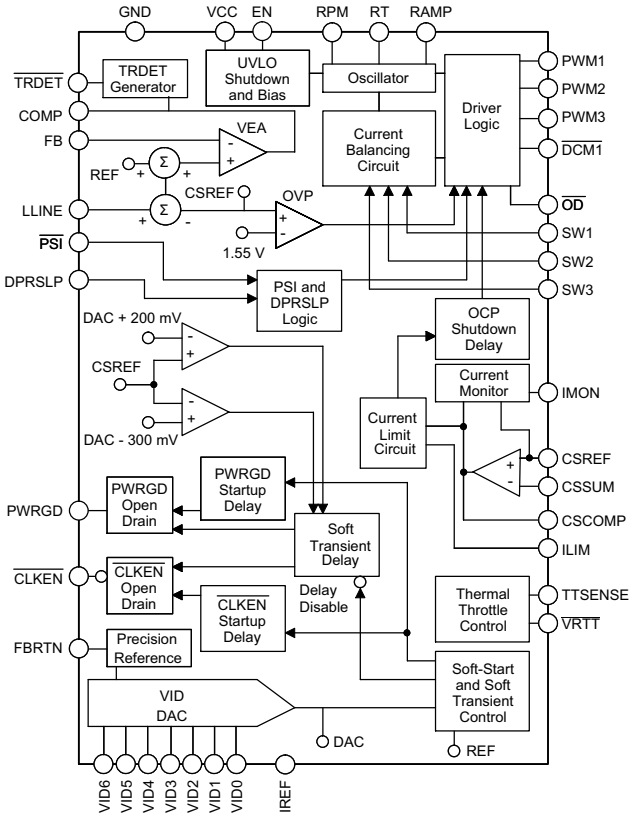


Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
V_{CC}	−0.3 to +6.0	V
FBRTN	−0.3 to +0.3	V
SW1 to SW3 DC t < 200 ns	 −1.0 to +22 −6.0 to +28	V
RAMPADJ (in Shutdown)	−0.3 to +22	V
All Other Inputs and Outputs	−0.3 to V_{CC} to +22	V
Storage Temperature Range	−65 to +150	°C
Operating Ambient Temperature Range	−10 to 100	°C
Operating Junction Temperature	125	°C
Thermal Impedance (θ_{JA})	98	°C/W
Lead Temperature Soldering (10 sec) Infrared (15 sec)	 300 260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low.
2	PWRGD	Power−Good Output. Open drain output that signals when the output voltage is outside of the proper operating range. The pull−high voltage on this pin cannot be higher than VCC.
3	IMON	Current Monitor Output. This pin sources a current proportional to the output load current. A resistor to FBRTN sets the current monitor gain.
4	$\overline{\text{CLKEN}}$	Clock Enable Output. The pull−high voltage on this pin cannot be higher than VCC.
5	FBRTN	Feedback Return. VID DAC and error amplifier reference for remote sensing of the output voltage.
6	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage.
7	COMP	Error Amplifier Output and Compensation Point.
8	NC	Not Connected.
9	$\overline{\text{TRDET}}$	Transient Detect Output. This pin is pulled low when a load release transient is detected. A capacitor to ground is connected to $\overline{\text{TRDET}}$ pin and a resistor from FB pin to $\overline{\text{TRDET}}$ is connected. During repetitive load transients at high frequencies, this circuit optimally positions the maximum and minimum output voltage into a specified load−line window.
10	DPRSLP	Deeper Sleep Control Input.
11	ILIM	Current Limit Set−point. An external resistor from this pin to CSCOMP sets the current limit threshold of the converter.
12	IREF	This pin sets the internal bias currents. A 80kΩ resistor is connected from this pin to ground.
13	RPM	RPM Mode Timing Control Input. A resistor between this pin to ground sets the RPM mode turn−on threshold voltage.
14	RT	Multiphase Frequency Setting Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device when operating in multiphase PWM mode.
15	RAMP	PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp.
16	LLINE	Output Load Line Programming Input. The center point of a resistor divider between CSREF and CSCOMP is connected to this pin to set the load line slope.
17	CSREF	Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier and the power−good and crowbar functions. This pin should be connected to the common point of the output inductors.
18	CSSUM	Current Sense Summing Node. External resistors from each switch node to this pin sum the inductor currents together to measure the total output current.
19	CSCOMP	Current Sense Compensation Point. A resistor and capacitor from this pin to CSSUM determine the gain of the current sense amplifier and the positioning loop response time.
20	GND	Ground. All internal biasing and the logic output signals of the device are referenced to this ground.
21 to 23	SW3 to SW1	Current Balance Inputs. Inputs for measuring the current level in each phase. The SW pins of unused phases should be left open.
24 to 26	PWM3 to PWM1	Logic−Level PWM Outputs. Each output is connected to the input of an external MOSFET driver such as the ADP3419. Connecting the PWM2 and/or PWM3 outputs to VCC causes that phase to turn off, allowing the ADP3210 to operate as a 1−, 2−, or 3−phase controller.
27	$\overline{\text{OD}}$	Multiphase Output Disable Logic Output. This pin is actively pulled low when the ADP3210 enters single−phase mode or during shutdown. Connect this pin to the SD inputs of the Phase−2 and Phase−3 MOSFET drivers.
28	$\overline{\text{DCM1}}$	Discontinuous Current Mode Enable Output 1. This pin actively pulled low when the single−phase inductor current crosses zero.
29	$\overline{\text{VRTT}}$	Voltage Regulator Thermal Throttling Logic Output. This pin goes high if the temperature at the monitoring point connected to TTSN exceeds the programmed $\overline{\text{VRTT}}$ temperature threshold.
30	TTSN	Thermal Throttling Sense Input. The center point of a resistor divider (where the lower resistor is an NTC thermistor) between VCC and GND is connected to this pin to remotely sense the temperature at the desired thermal monitoring point. Connect TTSN to VCC if this function is not used.
31	VCC	Supply Voltage for the Device.
32	NC	Not Connected.
33	$\overline{\text{PSI}}$	Power State Indicator Input. Pulling this pin to GND forces the ADP3210 to operate in single−phase mode.
34 to 40	VID6 to VID0	Voltage Identification DAC Inputs. When in normal operation mode, the DAC output programs the FB regulation voltage from 0.3 V to 1.5 V.

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0 V, FBRTN = GND, EN = V_{CC}, V_{VID} = 1.20 V to 1.500 V, $\overline{PSI}$ = 1.1 V, DPRSLP = GND, LLINE = CSREF, Current going into pin is positive. T_A = −10°C to 100°C, unless otherwise noted. (Note 1) R_{REF} = 80 kΩ

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VOLTAGE CONTROL − Voltage Error Amplifier (VEAMP)						
FB, LLINE Voltage Range (Note 2)	V_{FB}, V_{LLINE}	Relative to CSREF = V_{DAC}	−200		+200	mV
FB, LLINE Offset Voltage (Note 2)	V_{OSVEA}	Relative to CSREF = V_{DAC}	−0.5		+0.5	mV
FB Bias Current	I_{FB}		−1.0		1.0	μA
LLINE Bias Current	I_{LL}		−50		50	nA
LLINE Positioning Accuracy	V_{FB} − V_{VID}	Measured on FB relative to V_{VID}, LLINE forced 80 mV below CSREF	−82	−80	−78	mV
COMP Voltage Range (Note 2)	V_{COMP}		0.85		4.0	V
COMP Current (Note 2)	I_{COMP}	COMP = 2.0 V, CSREF = V_{DAC} FB forced 80 mV below CSREF FB forced 80 mV above CSREF		 −0.75 10		mA
COMP Slew Rate (Note 2)	SR_{COMP}	C_{COMP} = 10 pF, CSREF = V_{DAC} FB forced 200 mV below CSREF FB forced 200 mV above CSREF		 15 −20		V/μs
Gain Bandwidth (Note 2)	GBW	Inverting unit gain configuration, R = 1 kΩ		20		MHz
VID DAC VOLTAGE REFERENCE						
V_{DAC} Voltage Range (Note 2)		See VID Code Table	0		1.5	V
V_{DAC} Accuracy	V_{FB} − V_{VID}	Measured on FB (includes offset), relative to V_{VID}: V_{VID} = 0.3000 V to 1.2000 V V_{VID} = 1.2125 V to 1.5000 V	 −6.0 −7.0		 +6.0 +7.0	mV
V_{DAC} Differential Non−linearity (Note 2)			−1.0		+1.0	LSB
V_{DAC} Line Regulation (Note 2)	ΔV_{FB}	V_{CC} = 4.75 V to 5.25 V		0.05		%
V_{DAC} Boot Voltage	V_{BOOTFB}	Measured during boot delay period		1.100		V
Soft−Start Delay	t_{SS}	Measured from EN pos edge to FB settles to V_{BOOT} = 1.1 V within 5%		1.4		ms
Boot Delay	t_{BOOT}	Measured from FB settling to V_{BOOT} = 1.1 V within 5% to $\overline{CLKEN}$ neg edge		100		μs
V_{DAC} Slew Rate		Soft−Start Non−LSB VID step D_{VID} transition (LSB VID step)		0.0625 1.0 0.4		LSB/μs
FBRTN Current	I_{FBRTN}			−90	200	μA
VOLTAGE MONITORING AND PROTECTION − Power Good						
CSREF Undervoltage Threshold	$V_{UVCSREF}$	Relative to nominal DAC Voltage	−360	−300	−240	mV
CSREF Overvoltage Threshold	$V_{OVCSREF}$	Relative to nominal DAC Voltage	135	200	250	mV
CSREF Crowbar Voltage Threshold	$V_{CBCSREF}$	Relative to FBRTN	1.5	1.55	1.6	V
CSREF Reverse Voltage Threshold	$V_{RVCSREF}$	Relative to FBRTN CSREF Falling CSREF Rising	 −350	 −300 −75	 −10	mV
PWRGD Low Voltage	V_{PWRGD}	$I_{PWRGD(SINK)}$ = 4 mA		85	250	mV
PWRGD Leakage Current	I_{PWRGD}	V_{PWRDG} = 5.0 V			1.0	μA
PWRGD Startup Delay	$T_{SSPWRGD}$	Measured from CLKEN neg edge to PWRGD Pos Edge		8.0		ms
PWRGD Propagation Delay (Note 2)	$T_{PDPWRGD}$	Measured from Out−off−Good−Window event to PWRGD neg edge		200		ns

1. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).
2. Guaranteed by design or bench characterization, not production tested.

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0 V, FBRTN = GND, EN = V_{CC}, V_{VID} = 1.20 V to 1.500 V, $\overline{PSI}$ = 1.1 V, DPRSLP = GND, LLINE = CSREF, Current going into pin is positive. T_A = −10°C to 100°C, unless otherwise noted. (Note 1) R_{REF} = 80 kΩ

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VOLTAGE MONITORING AND PROTECTION − Power Good						
PWRGD Masking Time		Triggered by any VID change or OCP event		100		μs
CSREF Soft−Stop Resistance		EN = L or Latchoff condition		50		Ω
CURRENT CONTROL − Current Sense Amplifier (CSAMP)						
CSSUM, CSREF Common−Mode Range (Note 2)			0.05		3.5	V
CSSUM, CSREF Offset Voltage	V_{OSCSA}	CSREF − CSSUM, T_A = 25°C T_A = −10°C to 85°C	−0.3 −1.2		+0.3 +1.2	mV
CSSUM Bias Current	I_{BCSSUM}		−50		+50	nA
CSREF Bias Current	I_{BCSREF}		−1.0		+1.0	μA
CSCOMP Voltage Range (Note NO TAG)			0.05		2.0	V
CSCOMP Current	$I_{CSCOMPsource}$ $I_{CSCOMPsink}$	CSCOMP = 2.0 V CSSUM forced 200 mV below CSREF CSSUM forced 200 mV above CSREF		−660 1.0		μA mA
CSCOMP Slew Rate (Note 2)		C_{CSCOMP} = 10 pF CSSUM forced 200 mV below CSREF CSSUM forced 200 mV above CSREF		 10 −10		V/μs
Gain Bandwidth (Note 2)	GBW_{CSA}	Inverting unit gain configuration R = 1 kΩ		20		MHz
CURRENT MONITORING AND PROTECTION						
Current Reference I_{REF} Voltage	V_{REF}	R_{REF} = 80 kΩ to set I_{REF} = 20 μA	1.55	1.6	1.65	V
Current Limiter (OCP) Current Limit Threshold	V_{LIMTH}	CSCOMP relative to CSREF, R_{LIM} = 4.5 kΩ, 3−ph configuration, $\overline{PSI}$ = H 3−ph configuration, $\overline{PSI}$ = L 2−ph configuration, $\overline{PSI}$ = H 2−ph configuration, $\overline{PSI}$ = L 1−ph configuration	 −70 −15 −70 −30 −70	 −90 −30 −90 −45 −90	 −110 −50 −110 −65 −110	mV
Current Limit Latchoff Delay				8.0		ms
CURRENT MONITOR						
Current Gain Accuracy	I_{MON}/I_{LIM}	Measured from I_{LIM} to I_{MON} I_{LIM} = −20 μA I_{LIM} = −10 μA I_{LIM} = −5 μA (Note 2)	 9.4 9.1 8.9	 10 10 10	 10.7 11.0 11.4	−
I_{MON} Clamp Voltage	V_{MAXMON}	Relative to FBRTN, I_{LIM} = −30 μA	1.0		1.15	V
PULSE WIDTH MODULATOR − Clock Oscillator						
R_T Voltage	V_{RT}	R_T = 125 kΩ, V_{VID} = 1.4000 V See also $V_{RT}(V_{VID})$ formula	1.08	1.2	1.32	V
PWM Clock Frequency Range (Note 2)	f_{CLK}		0.3		3.0	MHz
PWM Clock Frequency	f_{CLK}	T_A = +25°C, V_{VID} = 1.2000 V R_T = 73 kΩ (Note 2) R_T = 125 kΩ (Note 2) R_T = 180 kΩ	 1000 700 500	 1300 800 600	 1600 900 780	kHz
RAMP GENERATOR						
RAMP Voltage	V_{RAMP}	EN = High, I_{RAMP} = 60 μA EN = Low	0.9	1.0 V_{IN}	1.1	V
RAMP Current Range (Note 2)	I_{RAMP}	EN = High EN = Low, RAMP = 19 V	1.0 −0.5		100 +0.5	μA
PWM COMPARATOR						
PWM Comparator Offset (Note 2)	V_{OSRPM}	$V_{OSRPM} = V_{RAMP} - V_{COMP}$	−3.0		3.0	mV

1. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).
2. Guaranteed by design or bench characterization, not production tested.

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0 V, FBRTN = GND, EN = V_{CC}, V_{VID} = 1.20 V to 1.500 V, $\overline{PSI}$ = 1.1 V, DPRSLP = GND, LLINE = CSREF, Current going into pin is positive. T_A = −10°C to 100°C, unless otherwise noted. (Note 1) R_{REF} = 80 kΩ

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RPM COMPARATOR						
RPM Current	I_{RPM}	V_{VID} = 1.2 V, R_T = 180 kΩ See also $I_{RPM}(R_T)$ formula		6.1		μA
RPM Comparator Offset (Note 2)	V_{OSRPM}	$V_{OSRPM} = V_{COMP} - (1 + V_{RPMTH})$	−3.0		3.0	mV
CLOCK SYNC						
Trigger Threshold (Note 2)		Relative to COMP sampled T_{CLK} earlier 3−phase configuration 2−phase configuration 1−phase configuration		 350 400 450		mV
$\overline{TRDET}$						
Trigger Threshold (Note 2)		Relative to COMP sampled T_{CLK} earlier 3−phase configuration 2−phase configuration 1−phase configuration		 −450 −500 −600		mV
$\overline{TRDET}$ Low Voltage (Note 2)	V_{LTRDET}	Logic Low, $I_{CLKENsink}$ = 4 mA		30	300	mV
$\overline{TRDET}$ Leakage Current (Note 2)	V_{HTRDET}	Logic High, $V_{\overline{TRDET}} = V_{CC}$			3.0	μA
SWITCH AMPLIFIER						
SW Common Mode Range (Note 2)	$V_{SW(X)CM}$		−600		+200	mV
SW Input Resistance	$R_{SW(X)}$	SW_X = 0 V	20	35	50	kΩ
ZERO CURRENT SWITCHING COMPARATOR						
SW ZCS Threshold	$V_{DCM(SW1)}$	DCM mode, DPRSLP = 3.3 V		−6.0		mV
Masked Off Time	$t_{OFFMSKD}$	Measured from PWM neg edge to Pos Edge		650		ns
SYSTEM I/O BUFFERS VID[6:0], DPRSLP, $\overline{PSI}$ INPUTS						
Input Voltage		Refers to input (driving) signal level Logic Low, $I_{sink} \geq$ 1 μA Logic High, $I_{source} \leq$ −5 μA	 0.7		0.3	V
Input Current		V = 0.2 V VID[6:0], DPRSLP (active pulldown to GND) $\overline{PSI}$ (active pullup to V_{CC})		 −1.0 +2.0		μA
VID Delay Time (Note 2)		VID any edge to FB change 10%	200			ns
EN INPUT						
Input Voltage		Refers to input (driving) signal level Logic Low, $I_{sink} \geq$ 1 μA Logic High, $I_{source} \leq$ −5 μA	 1.8		0.3	V
Input Current		EN = L or EN = H (Static) 0.8 V < EN < 1.6 V (During Transition)		10 70		nA μA
$\overline{CLKEN}$ OUTPUT						
Output Low Voltage		Logic Low, I_{sink} = 4 mA		10	200	mV
Output High, Leakage Current		Logic High, $V_{CLKEN} = V_{CC}$			1.0	μA
PWM, $\overline{OD}$, AND $\overline{DCM1}$ OUTPUT						
Output Low Voltage		Logic Low, I_{SINK} = 400 μA Logic High, I_{SOURCE} = −400 μA	 4.05	10 5.0	100	mV V
Phase Protection Threshold		Logic Low during first 3 CLK = Phase active Logic High during first 3 CLK = Phase active	 3.0		0.6	V
Phase Protection Current		PWM = 0.2 V or higher		50		μA
THERMAL MONITORING AND PROTECTION						
TTSENSE Voltage Range (Note 2)			0		5.0	V

1. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).
2. Guaranteed by design or bench characterization, not production tested.

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0 V, FBRTN = GND, EN = V_{CC}, V_{VID} = 1.20 V to 1.500 V, $\overline{PSI}$ = 1.1 V, DPRSLP = GND, LLINE = CSREF, Current going into pin is positive. T_A = −10°C to 100°C, unless otherwise noted. (Note 1) R_{REF} = 80 kΩ

Parameter	Symbol	Conditions	Min	Typ	Max	Units
THERMAL MONITORING AND PROTECTION						
TTSENSE Threshold		V_{CC} = 5.0 V, TTSNS is falling	2.45	2.5	2.55	V
TTSENSE Hysteresis			50	95		mV
TTSENSE Bias Current		TTSENSE = 2.6 V	−2.0		2.0	μA
VRTT Output Voltage	V_{VRTT}	Logic Low, $I_{VRTT(SINK)}$ = 400 μA Logic High, $I_{VRTT(SOURCE)}$ = −400 μA	 4.0	10 5.0	100	mV V
SUPPLY						
Supply Voltage Range	V_{CC}		4.5		5.5	V
Supply Current		EN = H EN = 0 V		8.0 10	11 50	mA μA
V_{CC} OK Threshold	V_{CCOK}	V_{CC} is Rising		4.4	4.5	V
V_{CC} UVLO Threshold	V_{CCUVLO}	V_{CC} is Falling	4.0	4.15		V
V_{CC} Hysteresis (Note 2)				150		mV

1. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).
2. Guaranteed by design or bench characterization, not production tested.

TEST CIRCUITS

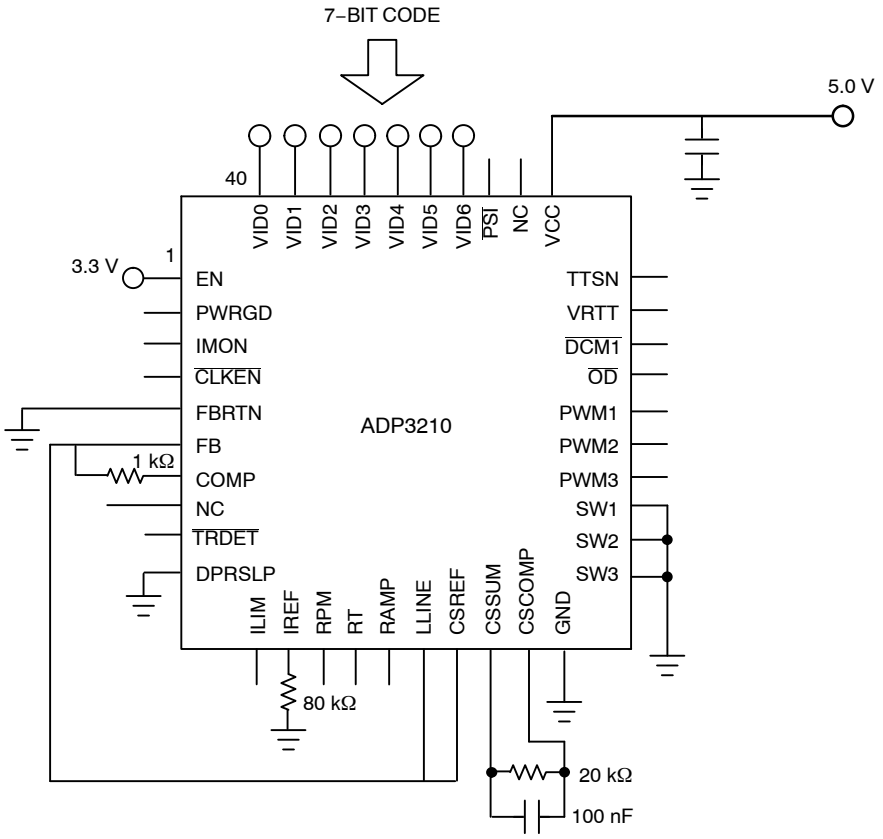


Figure 2. Closed−Loop Output Voltage Accuracy

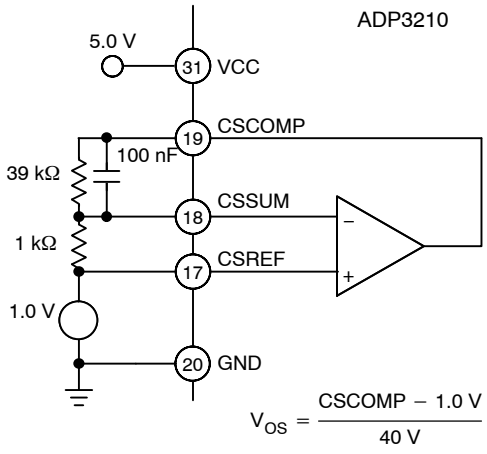


Figure 3. Current Sense Amplifier V_{OS}

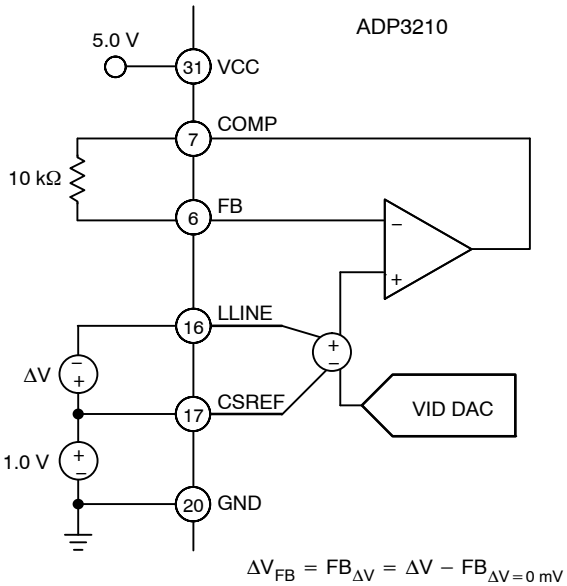


Figure 4. Positioning Accuracy

TYPICAL CHARACTERISTICS

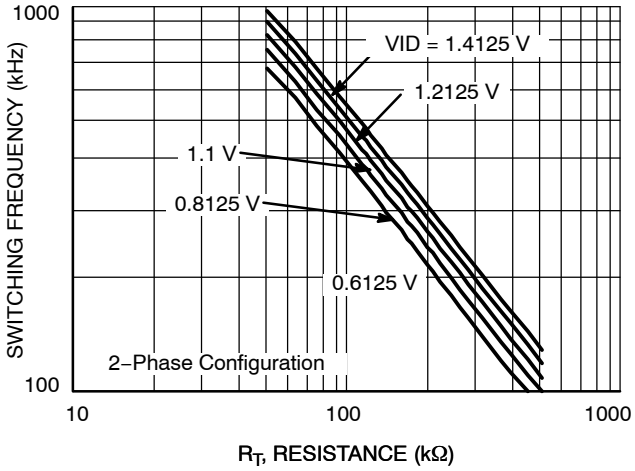


Figure 5. Master Clock Frequency vs. R_T

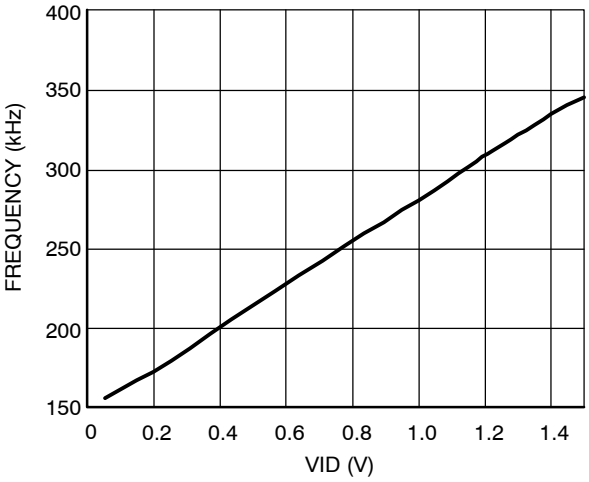


Figure 6. Master Clock vs. VID

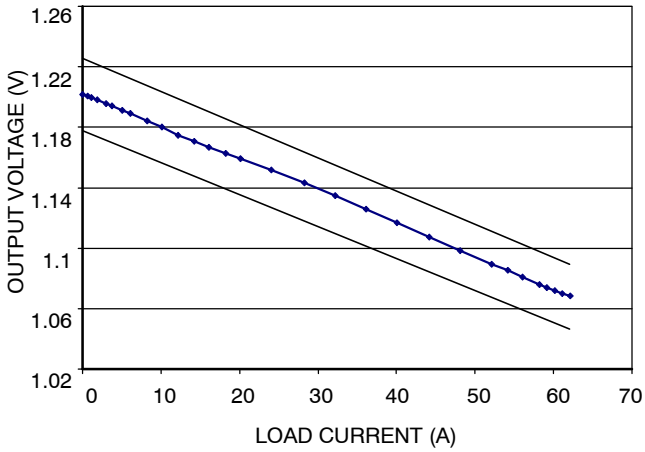
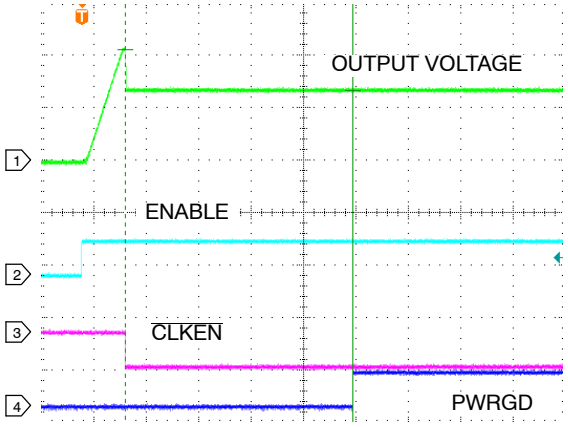
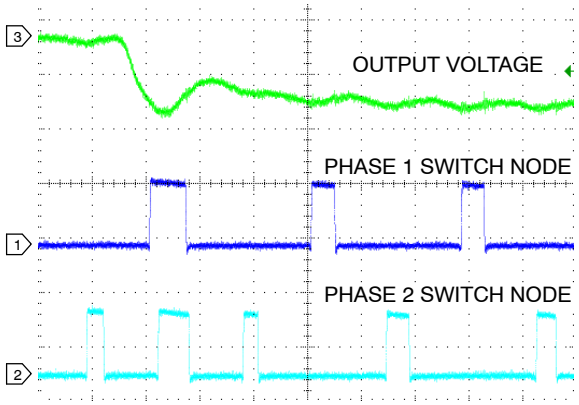


Figure 7. Load Line Accuracy



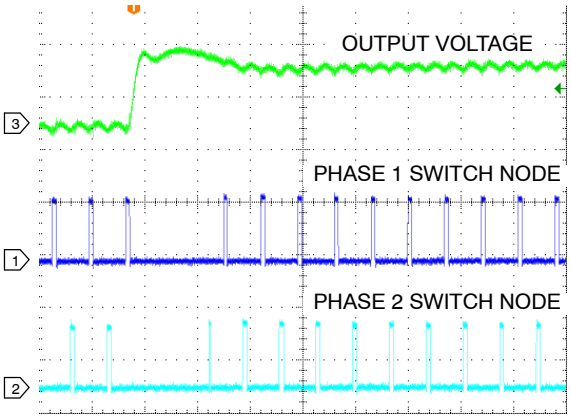
1: 500 mV / div **3:** 5.0 V / div 2 ms / div
2: 5.0 V / div **4:** 5.0 V / div

Figure 8. Startup Waveforms



1: 10 V / div **2:** 10 V / div **3:** 50 mV / div 1μs / div
Input = 12 V, Output = 1.0 V
15 A to 50 A Load Step

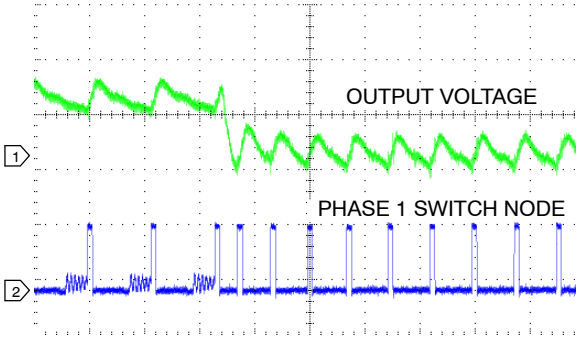
Figure 9. Load Transient with 2−Phases



1: 10 V / div **2:** 10 V / div **3:** 50 mV / div 1μs / div
Input = 12 V, Output = 1.0 V
50 A to 15 A Load Step

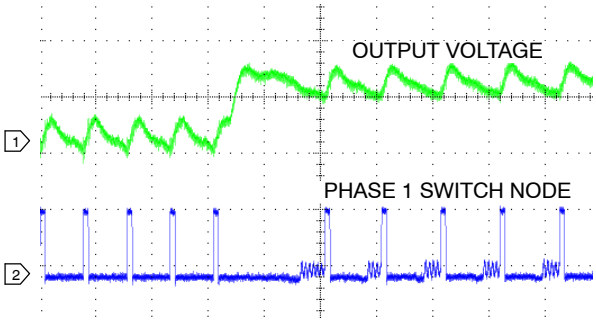
Figure 10. Load Transient with 2−Phases

TYPICAL CHARACTERISTICS



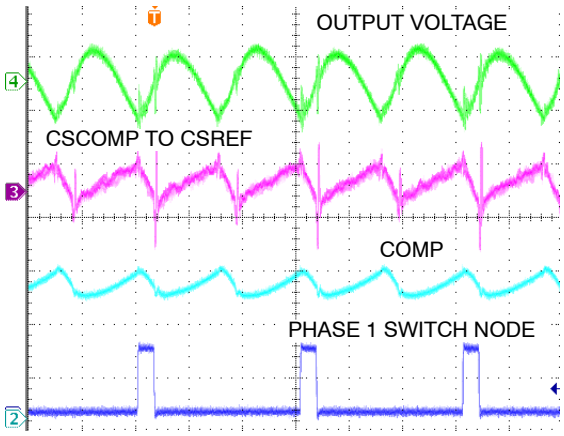
1: 50 mV / div **2:** 10 V / div 4 μs / div
Input = 12 V, Output = 1.0 V
3.0 A to 15 A Load Step

Figure 11. Load Transient with 1−Phase



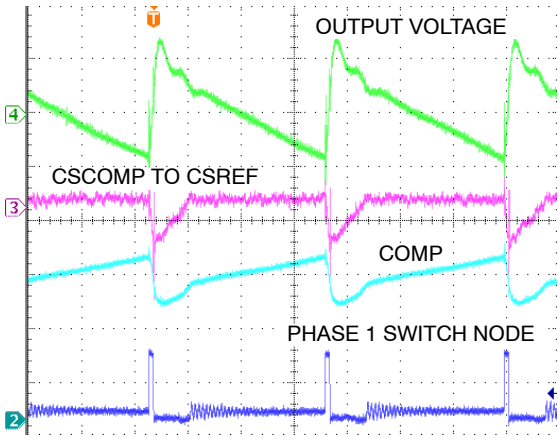
1: 50 mV / div **2:** 10 V / div 4 μs / div
Input = 12 V, Output = 1.0 V
15 A to 3.0 A Load Step

Figure 12. Load Transient with 1−Phase



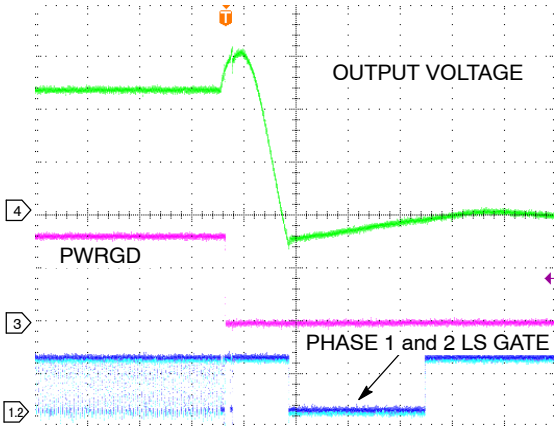
1: 10 V / div **3:** 20 mV / div 1 μs / div
2: 0.5 V / div **4:** 5.0 mV / div
Input = 12 V, Output = 1.0 V
2−Phase

Figure 13. Switching Waveforms



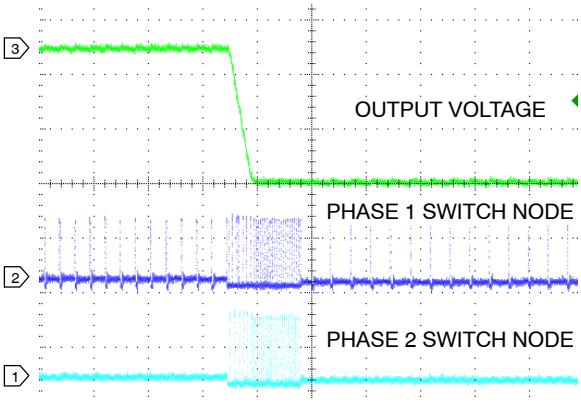
1: 10 V / div **3:** 20 mV / div 4 μs / div
2: 0.5 V / div **4:** 5.0 mV / div
Input = 12 V, Output = 1.0 V
Single−Phase DCM, 1.0 A

Figure 14. Switching Waveforms



1: 5.0 V / div **3:** 2.0 V / div 40 μs / div
2: 5.0 V / div **4:** 0.5 V / div
Input = 12 V, Output = 1.0 V
FB shortened to GND

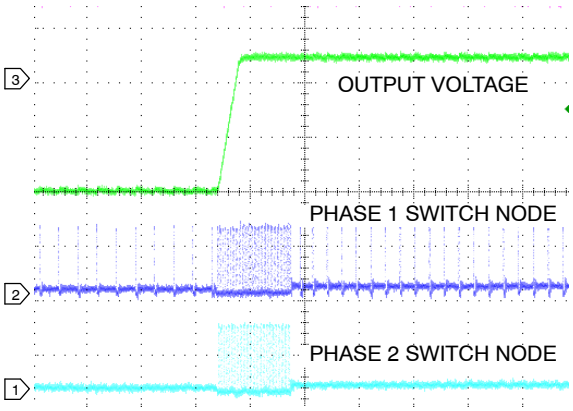
Figure 15. OVP and RVP Test



1: 10 V / div **2:** 10 V / div **3:** 200 mV / div 100 μs / div
Input = 12 V, Output = 0.5 A
1.2 V to 0.7 V VID Step
$\overline{\text{PSI}}$ = High, DPRSLP = High

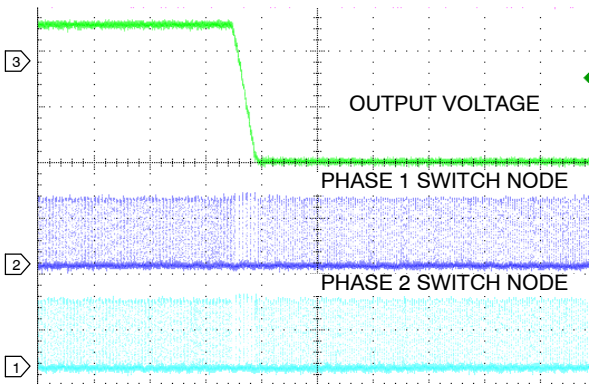
Figure 16. VID Step

TYPICAL CHARACTERISTICS



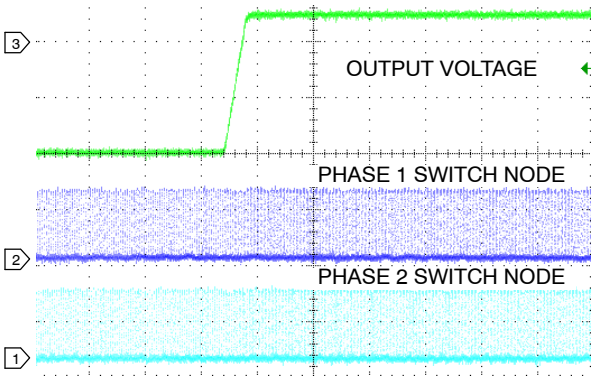
1: 10 V / div **2:** 10 V / div **3:** 200 mV / div 100μs / div
Input = 12 V, Output = 0.5 A
0.7 V to 1.2 V VID Step
$\overline{PSI}$ = High, DPRSLP = High

Figure 17. VID Step



1: 10 V / div **2:** 10 V / div **3:** 200 mV / div 100μs / div
Input = 12 V, Output = 0.5 A
1.2 V to 0.7 V VID Step
$\overline{PSI}$ = High, DPRSLP = Low

Figure 18. VID Step



1: 10 V / div **2:** 10 V / div **3:** 200 mV / div 100μs / div
Input = 12 V, Output = 0.5 A
0.7 V to 1.2 V VID Step
$\overline{PSI}$ = High, DPRSLP = Low

Figure 19. VID Step

Theory of Operation

The ADP3210 combines a multi−mode PWM Ramp Pulse Modulated (RPM) control with multiphase logic outputs for use in 1−, 2−, and 3−phase synchronous buck CPU core supply power converters. The internal 7−bit VID DAC conforms to Intel IMVP−6.5 specifications. Multiphase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling high currents in a single−phase converter puts high thermal stress on the system components such as the inductors and MOSFETs.

The multi−mode control of the ADP3210 ensures a stable high performance topology for:

- Balancing currents and thermals between phases
- High speed response at the lowest possible switching frequency and minimal output decoupling
- Minimizing thermal switching losses due to lower frequency operation
- Tight load line regulation and accuracy
- High current output by supporting up to 3−phase operation
- Reduced output ripple due to multiphase ripple cancellation
- High power conversion efficiency both at heavy load and light load
- PC board layout noise immunity
- Ease of use and design due to independent component selection
- Flexibility in operation by allowing optimization of design for low cost or high performance

Number of Phases

The number of operational phases and their phase relationship is determined by internal circuitry that monitors the PWM outputs. Normally, the ADP3210 operates as a 3−phase controller. For 2−phase operation, the PWM3 pin is connected to V_{CC} 5.0 V, and for 1−phase operation, the PWM3 and PWM2 pins are connected to V_{CC} 5.0 V.

When the ADP3210 is initially enabled, the controller sinks 50 μA on the PWM2 and PWM3 pins. An internal comparator checks the voltage of each pin against a high threshold of 3.0 V. If the pin voltage is high due to pullup to the V_{CC} 5.0 V rail, then the phase is disabled. The phase detection is made during the first three clock cycles of the internal oscillator. After phase detection, the 50 μA current sink is removed. The pins that are not connected to the V_{CC} 5.0 V rail function as normal PWM outputs. The pins that are connected to V_{CC} enter into high impedance state.

The PWM outputs are 5.0 V logic−level signals intended for driving external gate drivers such as the ADP3611. Because each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one output can operate at a time to allow overlapping phases.

Operation Modes

For ADP3210, the number of phases can be selected by the user as described in the Number of Phases section, or they can dynamically change based on system signals to optimize the power conversion efficiency at heavy and light CPU loads.

During a VID transient or at a heavy load condition, indicated by DPRSLP going low and $\overline{PSI}$ going high, the ADP3210 runs in full−phase mode. All user selected phases operate in interleaved PWM mode that results in minimal V_{CORE} ripple and best transient performance. While in light load mode, indicated by either $\overline{PSI}$ going low or DPRSLP going high, only Phase 1 of ADP3210 is in operation to maximize power conversion efficiency.

In addition to the change of phase number, the ADP3210 dynamically changes operation modes. In multiphase operation, the ADP3210 runs in PWM mode, with switching frequency controlled by the master clock. In single−phase mode based on $\overline{PSI}$ signal, the ADP3210 switches to RPM mode, where the switching frequency is no longer controlled by the master clock, but by the ripple voltage appearing on the COMP pin. The PWM1 pin is set to high each time the COMP pin voltage rises to a limit determined by the VID voltage and programmed by the external resistor connected from Pin RPM to ground. In single−phase mode based on the DPRSLP signal, the ADP3210 runs in RPM mode, with the synchronous rectifier (low−side) MOSFETs of Phase 1 being controlled by the $\overline{DCM1}$ pin to prevent any reverse inductor current. Thus, the switch frequency varies with the load current, resulting in maximum power conversion efficiency in deeper sleep mode of CPU operation. In addition, during any VID transient, system transient (entry/exit of deeper sleep), or current limit, the ADP3210 goes into full phase mode, regardless of DPRSLP and $\overline{PSI}$ signals, eliminating current stress to Phase 1.

Table 1 summarizes how the ADP3210 dynamically changes phase number and operation modes based on system signals and operating conditions.

Table 1. Phase Number and Operation Modes

$\overline{PSI}$	DPRSLP	VID Transient Period (Note 1)	Hit Current Limit	No. of Phases Selected by User	No. of Phases in Operation	Operation Mode
DNC	DNC	Yes	DNC	N 3, 2, or 1	N	PWM, CCM Only
1	0	No	DNC	N 3, 2, or 1	N	PWM, CCM Only
0	0	No	No	DNC	Phase 1 only	RPM, CCM Only
0	0	No	Yes	DNC	N	PWM, CCM Only
DNC	1	No	No	DNC	Phase 1 only	RPM, Automatic CCM / DCM
DNC	1	No	Yes	DNC	N	PWM, CCM Only

1. VID transient period is the time following any VID change, including entrance and exit of deeper sleep mode. The duration of VID transient period is the same as that of PWRGD masking time.
2. DNC = Do Not Care.
3. CCM = Continuous Conduction Mode.
4. DCM = Discontinuous Conduction Mode.

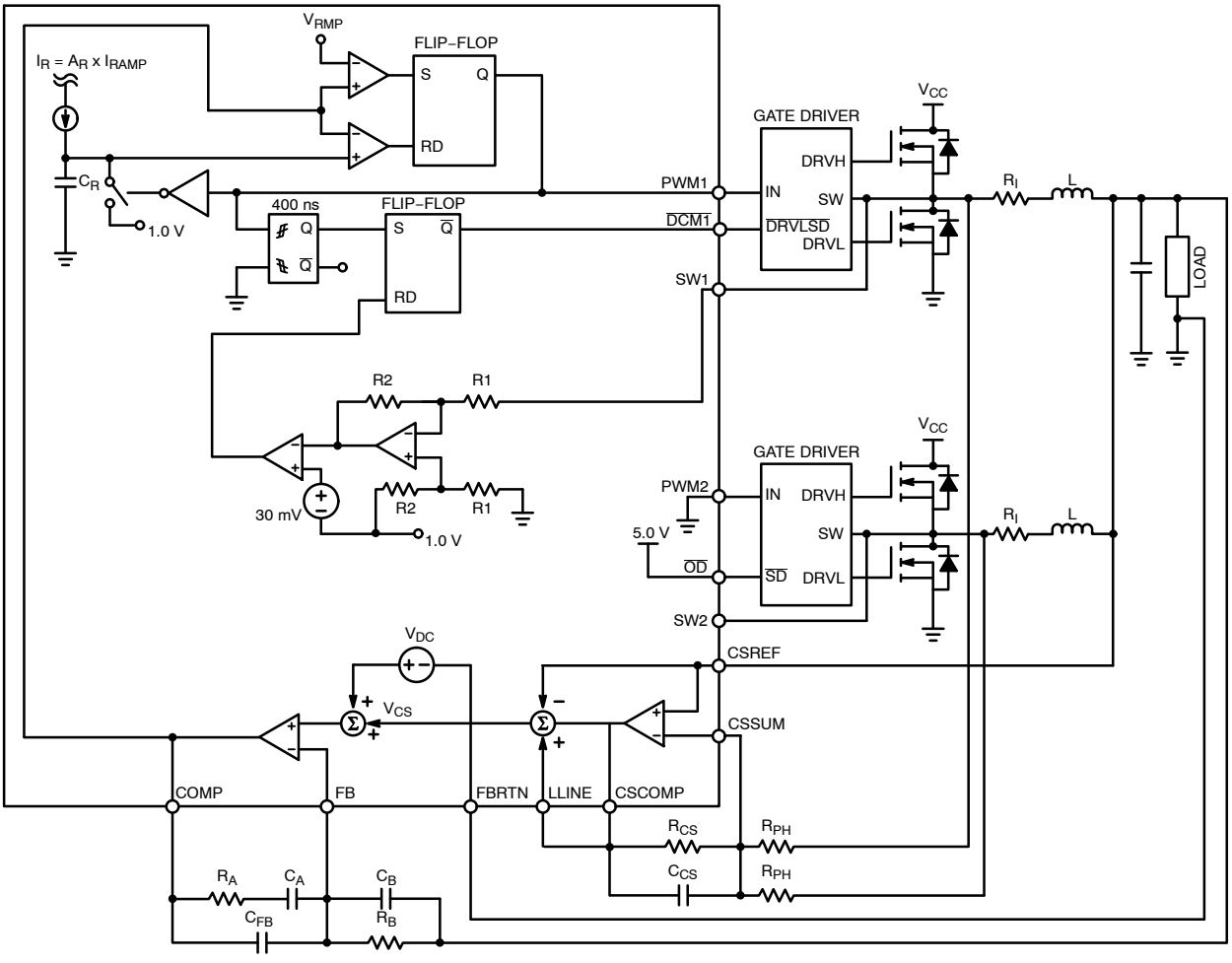


Figure 20. Single−Phase RPM Mode Operation

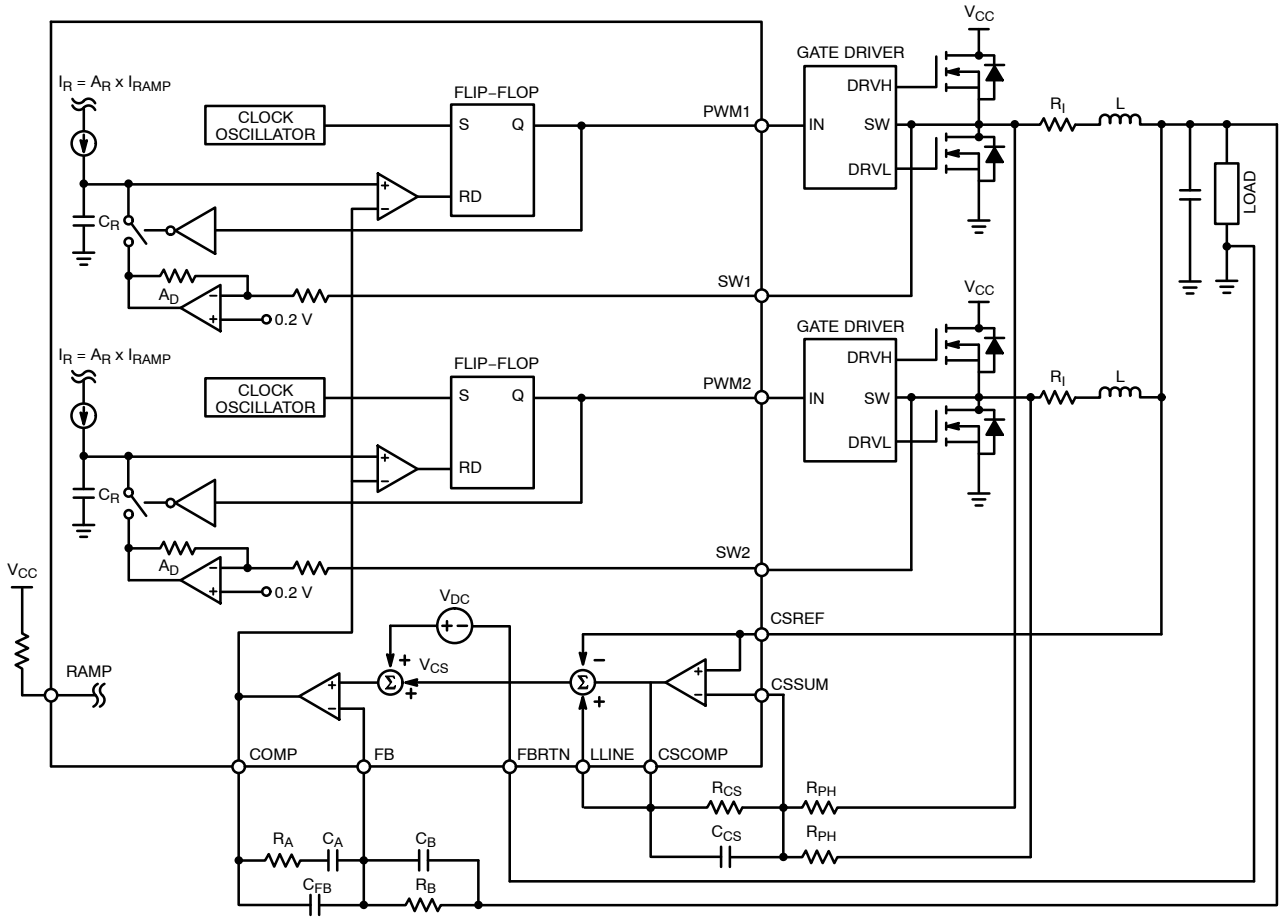


Figure 21. Dual−Phase PWM Mode Operation

Switch Frequency Setting

Master Clock Frequency for PWM Mode

The clock frequency of the ADP3210 is set by an external resistor connected from the RT pin to ground. The frequency varies with the VID voltage: the lower the VID voltage, the lower the clock frequency. The variation of clock frequency with VID voltage makes V_{CORE} ripple remain constant and improves power conversion efficiency at a lower VID voltage. Figure 5 shows the relationship between clock frequency and VID voltage, parametrized by RT resistance.

To determine the switching frequency per phase, the clock is divided by the number of phases in use. If PWM3 is pulled up to V_{CC}, then the master clock is divided by 2 for the frequency of the remaining phases. If PWM2 and PWM3 are pulled up to V_{CC}, then the switching frequency of a Phase 1 equals the master clock frequency. If all phases are in use, divide by 3.

Switching Frequency for RPM Mode−Phase 1

When ADP3210 operates in single−phase RPM mode, its switching frequency is not controlled by the master clock, but by the ripple voltage on the COMP pin. The PWM1 pin is set high each time the COMP pin voltage rises to a voltage limit determined by the VID voltage and the external resistance connected from Pin RPM to ground. Whenever PWM1 pin is high, an internal ramp signal rises at a slew rate programmed by the current flowing into the RAMP pin. Once this internal ramp signal hits the COMP pin voltage, the PWM1 pin is reset to low.

In continuous current mode, the switching frequency of RPM operation is maintained almost constantly. While in discontinuous current mode, the switching frequency reduces with the load current.

Output Voltage Differential Sensing

The ADP3210 combines differential sensing with a high accuracy, VID DAC, precision REF output and a low offset error amplifier to meet the rigorous accuracy requirement of the Intel IMVP−6.5 specification. In steady−state, the VID DAC and error amplifier meet the worst−case error specification of ±10 mV over the full operating output voltage and temperature range.

The CPU core output voltage is sensed between the FB and FBRTN pins. Connect FB through a resistor to the positive regulation point, usually the V_{CC} remote sense pin of the microprocessor. Connect FBRTN directly to the negative remote sense point, the VSS sense point of the CPU. The internal VID DAC and precision voltage reference are referenced to FBRTN, and have a maximum current of 200 μA to guarantee accurate remote sensing.

Output Current Sensing

The ADP3210 provides a dedicated Current Sense Amplifier (CSA) to monitor the total output current of the converter for proper voltage positioning vs. load current, and for current limit detection. Sensing the load current being delivered to the load is inherently more accurate than detecting peak current or sampling the current across a sense element, such as the low−side MOSFET. The CSA can be configured several ways depending on system requirements.

- Output inductor DCR sensing without use of a thermistor for lowest cost
- Output inductor DCR sensing with use of a thermistor that tracks inductor temperature to improve accuracy
- Discrete resistor sensing for highest accuracy

The positive input of the CSA is connected to the CSREF pin, which is connected to the output voltage. At the negative input CSSUM pin of the CSA, signals from the sensing element (that is, in case of inductor DCR sensing, signals from the switch node side of the output inductors) are summed together by using series summing resistors. The feedback resistor between CSCOMP and CSSUM sets the gain of the current sense amplifier, and a filter capacitor is placed in parallel with this resistor. The current information is then given as the voltage difference between CSREF and CSCOMP. This signal is used internally as a differential input for the current limit comparator.

An additional resistor divider connected between CSREF and CSCOMP with the midpoint connected to LLINE can be used to set the load line required by the microprocessor specification. The current information for load line setting is then given as the voltage difference of CSREF − LLINE. The configuration in the previous paragraph makes it possible for the load line slope to be set independently of the current limit threshold. In the event that the current limit threshold and load line do not have to be independent, the resistor divider between CSREF and CSCOMP can be omitted and the CSCOMP pin can be connected directly to LLINE. To disable voltage positioning entirely (that is, to set no load line), tie LLINE to CSREF.

To provide the best accuracy for current sensing, the CSA is designed to have a low offset input voltage. In addition, the sensing gain is set by an external resistor ratio.

Active Impedance Control Mode

To control the dynamic output voltage droop as a function of the output current, the signal proportional to the total output current is converted to a voltage that appears between CSREF and LLINE. This voltage can be scaled to equal the droop voltage, which is calculated by multiplying the droop impedance of the regulator with the output current. The droop voltage is then used as the control voltage of the PWM regulator. The droop voltage is subtracted from the DAC reference output voltage and determines the voltage positioning set−point. The setup results in an enhanced feed−forward response.

Current Control Mode and Thermal Balance

The ADP3210 has individual inputs for monitoring the current in each phase. The phase current information is combined with an internal ramp to create a current balancing feedback system that is optimized for initial current accuracy and dynamic thermal balance. The current balance information is independent of the total inductor current information used for voltage positioning described in the Active Impedance Control Mode section.

The magnitude of the internal ramp can be set so the transient response of the system becomes optimal. The ADP3210 also monitors the supply voltage to achieve feed−forward control whenever the supply voltage changes. A resistor connected from the power input voltage rail to the RAMP pin determines the slope of the internal PWM ramp. Detailed information about programming the ramp is given in the Ramp Resistor Selection section.

External resistors are placed in series with the SW1, SW2 and SW3 pins to create an intentional current imbalance, if desired. Such a condition can exist when one phase has better cooling and supports higher currents than the other phase. Resistor RSW2 and Resistor RSW3 (see the Typical Application Circuit in Figure 24.) can be used to adjust thermal balance. It is recommended to add these resistors during the initial design to make sure placeholders are provided in the layout.

To increase the current in any given phase, users should make RSW for that phase larger (that is, make RSW = 1 kΩ for the hottest phase and do not change it during balance optimization). Increasing RSW to 1.5 kΩ makes a substantial increase in phase current. Increase each RSW value by small amounts to achieve thermal balance starting with the coolest phase.

If adjusting current balance between phases is not needed, switch resistors should be 1 kΩ for all phases.

Voltage Control Mode

A high gain bandwidth error amplifier is used for the voltage−mode control loop. The non−inverting input voltage is set via the 7−bit VID DAC. The VID codes are listed in Table 2. The non−inverting input voltage is offset by the droop voltage as a function of current, commonly known as active voltage positioning. The output of the error amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input, FB, is tied to the output sense location through a resistor, RB, for sensing and controlling the output voltage at the remote sense point. The main loop compensation is incorporated in the feedback network connected between FB and COMP.

Power−Good Monitoring

The power−good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open drain output that can be pulled up through an external resistor to a voltage rail that is not necessarily the same V_{CC} voltage rail of the

controller. Logic high level indicates that the output voltage is within the voltage limits defined by a window around the VID voltage setting. PWRGD goes low when the output voltage is outside of that window.

Following the IMVP−6.5 specification, PWRGD window is defined as −300 mV below and +200 mV above the actual VID DAC output voltage. For any DAC voltage below 300 mV, only the upper limit of the PWRGD window is monitored. To prevent false alarm, the power−good circuit is masked during various system transitions, including any VID change and entrance/exit out of deeper sleep. The duration of the PWRGD mask time is set by an internal clock to approximately 100 μs.

During a VID change, the PWRGD signal is masked to prevent false PWRGD glitches. The PWRGD is masked for approximately 100 μs after a VID change.

Powerup Sequence and Soft−Start

The power−on ramp−up time of the output voltage is set internally. During startup, the ADP3210 steps sequentially through each VID code until it reaches the boot voltage. The whole powerup sequence, including soft−start, is illustrated in Figure 22.

After EN is asserted high, the soft−start sequence starts. The core voltage ramps up linearly to the boot voltage. The ADP3210 regulates at the boot voltage for 100 μs. After the boot time is completed, $\overline{\text{CLKEN}}$ is asserted low. After $\overline{\text{CLKEN}}$ is asserted low for 9 ms, PWRGD is asserted high.

In V_{CC} UVLO or in shutdown, a small MOSFET turns on connecting the CSREF to GND. The MOSFET on the CSREF pin has a resistance of approximately 100 Ω. When V_{CC} ramps above the upper UVLO threshold and EN is asserted high, the ADP3210 enables internal bias and starts a reset cycle that lasts about 50 μs to 60 μs. Next, when initial reset is over, the chip detects the number of phases set by the user, and gives a go signal to start soft−start. The ADP3210 reads the VID codes provided by the CPU on VID0 to VID6 input pins after $\overline{\text{CLKEN}}$ is asserted low.

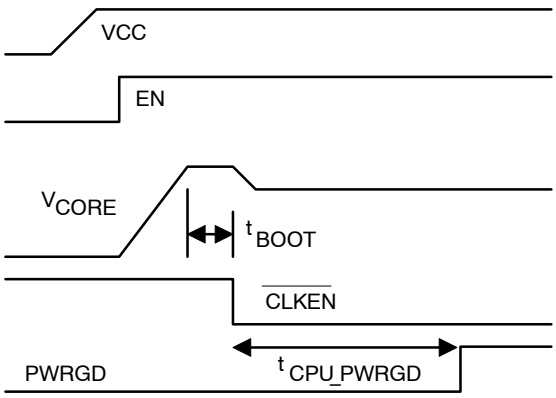


Figure 22. Powerup Sequence

Soft Transient

The IMVP−6.5 specification requires the CPU to step through the VID codes in 12.5mV steps when transitioning from one VID code to another. This reducing the inrush current and helps decrease the acoustic noise generated by the MLCC input capacitors and inductors.

The ADP3210 also offers soft transient control for large VID step changes. When the VID is changed, the ADP3210 changes the output voltage 1 LSB every 1 μs. The output voltage slew rate is controlled to 12.5 mV/μs.

Current Limit, Short−Circuit, and Latchoff Protection

The ADP3210 compares the differential output of a current sense amplifier to a programmable current limit set−point to provide current limiting function. The current limit set point is set with a resistor connected from I_{LIM} pin to CSCOMP pin. This is the R_{LIM} resistor. During normal operation, the voltage on the I_{LIM} pin is equal to the CSREF pin. The voltage across R_{LIM} is equal to the voltage across the current sense amplifier (from CSREF pin to CSCOMP pin). This voltage is proportional to output current. The current through R_{LIM} is proportional to the output inductor current. The current through R_{LIM} is compared with an internal reference current. When the R_{LIM} current goes above the internal reference current, the ADP3210 goes into current limit. The current limit circuit is shown in Figure 23.

In 3 phase configuration with all 3 phase switching, current limit occurs when the current in the R_{LIM} resistor is 20 μA. In 3 phase configuration with only phase 1 switching, current limit occurs when the current in the R_{LIM} resistor is 6.7 μA. In 2 phase configuration with both phases switching, current limit occurs when the current in the R_{LIM} resistor is 20 μA. In 2 phase configuration with only phase 1 switching, current limit occurs when the current in the R_{LIM} resistor is 10 μA. In single phase configuration, current limit occurs when the current in the R_{LIM} resistor is 20 μA.

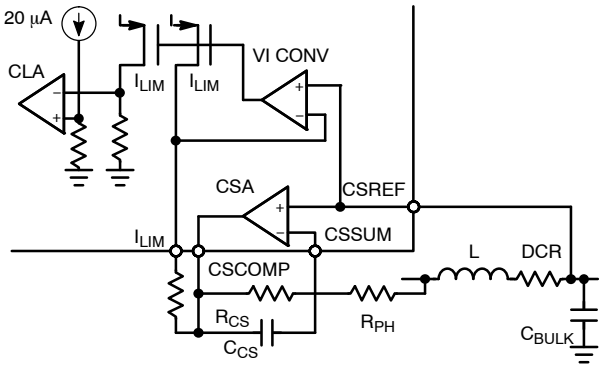


Figure 23. Current Limit Circuit

During startup when the output voltage is below 200 mV, a secondary current limit is activated. This is necessary because the voltage swing on CSCOMP cannot extend below ground. The secondary current limit circuit clamps the internal COMP voltage and sets the internal compensation ramp termination voltage at 1.5 V level. The clamp actually limits voltage drop across the low side MOSFETs through the current balance circuitry.

An inherent per phase current limit protects individual phases in case one or more phases stop functioning because of a faulty component. This limit is based on the maximum normal−mode COMP voltage.

After 9 ms in current limit, the ADP3210 will latchoff. The latchoff can be reset by removing and reapplying V_{CC}, or by recycling the EN pin low and high for a short time.

Changing VID OTF

The ADP3210 is designed to track dynamically changing VID code. As a result, the converter output voltage, that is, the CPU V_{CC} voltage, can change without the need to reset either the controller or the CPU. This concept is commonly referred to as VID OTF transient. A VID OTF can occur either under light load or heavy load conditions. The processor signals the controller by changing the VID inputs in LSB incremental steps from the start code to the finish code. The change can be either upwards or downwards steps.

When a VID input changes state, the ADP3210 detects the change but ignores the new code for a minimum of time of 400 ns. This keep out is required to prevent reaction to false code that can occur by a skew in the VID code while the 7−bit VID input code is in transition. Additionally, the VID change triggers a PWRGD masking timer to prevent a PWRGD failure. Each VID change resets and re−triggers the internal PWRGD masking timer. As listed in Table 2, during any VID transient, the ADP3210 forces a multiphase PWM mode regardless of system input signals.

Output Crowbar

To protect the CPU load and output components of the converter, the PWM outputs are driven low, $\overline{\text{DCM1}}$ and $\overline{\text{OD}}$ are driven high (that is, commanded to turn on the low−side MOSFETs of all phases) when the output voltage exceeds an OVP threshold of 1.55 V as specified by IMVP−6.5.

Turning on the low−side MOSFETs discharges the output capacitor as soon as reverse current builds up in the inductors. If the output overvoltage is due to a short of the high−side MOSFET, then this crowbar action current limits the input supply or causes the input rail fuse to blow, protecting the microprocessor from destruction.

Once overvoltage protection (OVP) is triggered, the ADP3210 is latched off. The latchoff function can be reset by removing and reapplying V_{CC}, or by recycling EN low and high for a short time.

Reverse Voltage Protection

Very large reverse currents in inductors can cause negative V_{CORE} voltage, which is harmful to the CPU and other output components. ADP3210 provides Reverse Voltage Protection (RVP) function without additional system cost. The V_{CORE} voltage is monitored through the CSREF pin. Any time the CSREF pin voltage is below −300 mV, the ADP3210 triggers its RVP function by disabling all PWM outputs and setting both $\overline{\text{DCM1}}$ and $\overline{\text{OD}}$ pins low. Thus, all the MOSFETs are turned off. The reverse inductor current can be quickly reset to zero by dumping the energy built up in the inductor into the input dc voltage source via the forward−biased body diode of the high−side MOSFETs. The RVP function is terminated when the CSREF pin voltage returns above −100 mV.

Occasionally, overvoltage crowbar protection results in negative V_{CORE} voltage, because turn−on of all low−side MOSFETs leads to very large reverse inductor current. To prevent damage of the CPU by negative voltage, ADP3210 keeps its RVP monitoring function alive even after OVP latchoff. During OVP latchoff, if the CSREF pin voltage drops below −300mV, then all low−side MOSFETs are turned off by setting both $\overline{\text{DCM1}}$ and $\overline{\text{OD}}$ low. $\overline{\text{DCM1}}$ and $\overline{\text{OD}}$ pins are set high again when CSREF voltage recovers above −100 mV.

Output Enable and UVLO

The V_{CC} supply voltage to the controller must be higher than the UVLO upper threshold, and the EN pin must be higher than its logic threshold so the ADP3210 can begin switching. If the V_{CC} voltage is less than the UVLO threshold, or the EN pin is logic low, then the ADP3210 is in shutdown. In shutdown, the controller holds the PWM outputs at ground, shorts the SS pin and PGDELAY pin capacitors to ground, and drives $\overline{\text{DCM1}}$ and $\overline{\text{OD}}$ pins low.

Proper power supply sequencing during startup and shutdown of the ADP3210 must be adhered to. All input pins must be at ground prior to applying or removing V_{CC}. All output pins should be left in high impedance state while V_{CC} is off.

Output Current Monitor

The ADP3210 has an output current monitor. The I_{MON} pin sources a current proportional to the inductor current. A resistor from I_{MON} pin to FBRTN sets the gain. A 0.1 μF is added in parallel with R_{MON} to filter the inductor ripple. The I_{MON} pin is clamped to prevent it from going above 1.15 V.

Thermal Throttling Control

The ADP3210 includes a thermal monitoring circuit to detect if the temperature of the variable resistor (VR) has exceeded a user−defined thermal throttling threshold. The thermal monitoring circuit requires an external resistor divider connected between the V_{CC} pin and GND. The divider consists of an NTC thermistor and a resistor. To generate a voltage that is proportional to temperature, the midpoint of the divider is connected to the TTSN pin. Whenever the temperature trips the set alarm threshold, an internal comparator circuit compares the TTSN voltage to a half V_{CC} threshold and outputs a logic level signal at the $\overline{\text{VRTT}}$ output. The $\overline{\text{VRTT}}$ output is designed to drive an external transistor that, in turn, provides the high current, open drain $\overline{\text{VRTT}}$ signal that is required by the IMVP−6.5 specification. When the temperature is around the set alarm point, the internal $\overline{\text{VRTT}}$ comparator has a hysteresis of about 100 mV to prevent high frequency oscillation of $\overline{\text{VRTT}}$.

Table 2. VID Code Table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500
0	0	1	0	1	0	1	1.2375
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625

Table 2. VID Code Table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125

Table 2. VID Code Table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625
1	1	1	0	1	0	0	0.0500
1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125
1	1	1	1	0	0	0	0.0000
1	1	1	1	0	0	1	0.0000
1	1	1	1	0	1	0	0.0000
1	1	1	1	0	1	1	0.0000
1	1	1	1	1	0	0	0.0000
1	1	1	1	1	0	1	0.0000
1	1	1	1	1	1	0	0.0000
1	1	1	1	1	1	1	0.0000

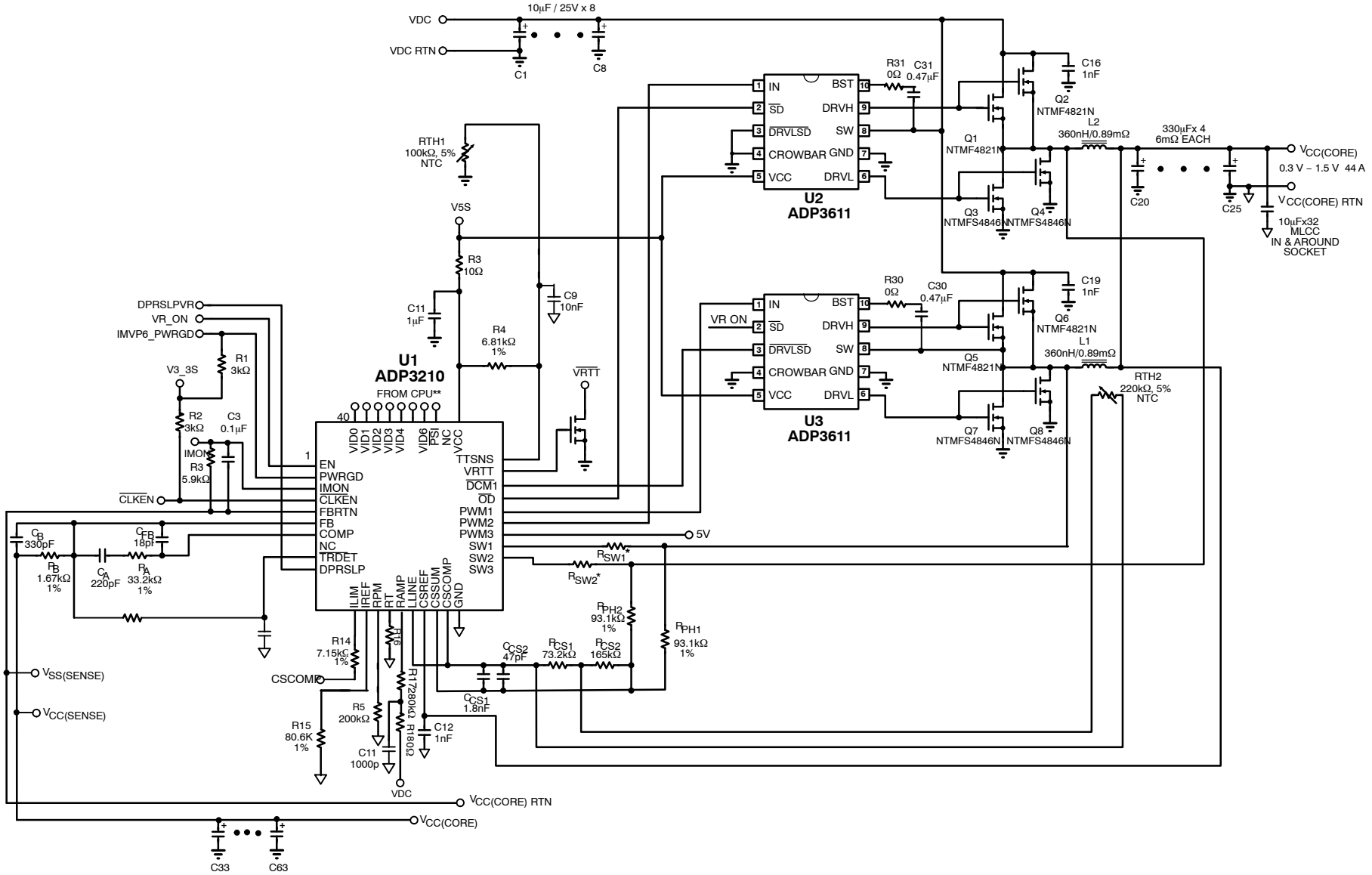


Figure 24. Typical Application Circuit

Application Information

The design parameters for a typical Intel IMVP6.5−compliant CPU Core VR application are as follows:

- Maximum input voltage (V_{INMAX}) = 19 V
- Minimum input voltage (V_{INMIN}) = 7.0 V
- Output voltage by VID setting (V_{VID}) = 1.150 V
- Maximum output current (I_O) = 55 A
- Load line slope (R_O) = 2.1 mΩ
- Maximum output current step (ΔI_O) = 34.5 A
- Maximum output thermal current (I_{OTDC}) = 32 A
- Number of phases (n) = 3
- Switching frequency per phase (f_{SW}) = 280 kHz
- Duty cycle at maximum input voltage (D_{MIN}) = 0.061
- Duty cycle at minimum input voltage (D_{MAX}) = 0.164

Setting the Clock Frequency for PWM Mode

In PWM mode operation, The ADP3210 uses a fixed−frequency control architecture. The frequency is set by an external timing resistor (R_T). The clock frequency and the number of phases determine the switching frequency per phase, which directly relates to switching losses, and the sizes of the inductors and input and output capacitors. In a 2−phase design, a clock frequency of 560 kHz sets the switching frequency to 280 kHz per phase. This selection represents a trade−off between the switching losses and the minimum sizes of the output filter components. To achieve a 560 kHz oscillator frequency at VID voltage 1.150 V, R_T has to be 196 kΩ. Alternatively, the value for R_T can be calculated using:

$$R_T = \frac{V_{VID} + 1.0\ V}{n \times 2 \times f_{SW} \times 9\ pF} - 16\ k\Omega \qquad \text{(eq. 1)}$$

where 9 pF and 16 kΩ are internal IC component values. For good initial accuracy and frequency stability, it is recommended to use a 1% resistor.

Inductor Selection

The choice of inductance determines the ripple current in the inductor. Less inductance leads to more ripple current, which increases the output ripple voltage and conduction losses in the MOSFETs. However, this allows the use of smaller−size inductors, and for a specified peak−to−peak transient deviation, it allows less total output capacitance. Conversely, a higher inductance means lower ripple current and reduced conduction losses, but requires larger size inductors and more output capacitance for the same peak−to−peak transient deviation. In a multiphase converter, the practical peak−to−peak inductor ripple current is less than 50% of the maximum dc current in the same inductor. Equation 2 shows the relationship between the inductance, oscillator frequency, and peak−to−peak ripple current. Equation 3 can be used to determine the minimum inductance based on a given output ripple voltage.

$$I_R = \frac{V_{VID} \times \left(1 - D_{MIN}\right)}{f_{SW} \times L} \qquad \text{(eq. 2)}$$

$$L \geq \frac{V_{VID} \times R_O \times (1 - (n \times D_{MIN})) \times (1 - D_{MIN})}{f_{SW} \times V_{RIPPLE}} \qquad \text{(eq. 3)}$$

Solving Equation 3 for a 20 mV peak−to−peak output ripple voltage yields:

$$L \geq \frac{1.150\ V \times 2.1\ m\Omega \times (1 - (2 \times 0.061)) \times (1 - 0.061)}{280\ kHz \times 20\ mV}$$

$$= 356\ nH \qquad \text{(eq. 4)}$$

If the ripple voltage ends up being less than the initially selected value, then the inductor can be changed to a smaller value until the ripple value is met. This iteration allows optimal transient response and minimum output decoupling.

The smallest possible inductor should be used to minimize the number of output capacitors. For this example, choosing a 360 nH inductor is a good starting point, and gives a calculated ripple current of 10.7 A. The inductor should not saturate at the peak current of 27.4 A, and should be able to handle the sum of the power dissipation caused by the average current of 16 A in the winding and core loss.

Another important factor in the inductor design is the DCR, which is used to measure phase currents. A large DCR causes excessive power losses, though too small a value leads to increased measurement error. This example uses an inductor with a DCR of 0.89 mΩ.

Selecting a Standard Inductor

Once the inductance and DCR are known, the next step is to either design an inductor or select a standard inductor that comes as close as possible to meeting the overall design goals. It is also important to have the inductance and DCR tolerance specified to keep the accuracy of the system controlled; 20% inductance and 15% DCR (at room temperature) are reasonable assumptions that most manufacturers can meet.

Power Inductor Manufacturers

The following companies provide surface mount power inductors optimized for high power applications upon request:

- Vishay Dale Electronics, Inc. – http://www.vishay.com
- Panasonic – http://www.panasonic.com
- Sumida Corporation – http://www.sumida.com
- NEC Tokin Corporation – http://www.nec−tokin.com

Output Droop Resistance

The inductor design requires that the regulator output voltage measured at the CPU pins drops when the output current increases. The specified voltage drop corresponds to a dc output resistance (R_O).

The output current is measured by summing the currents of the resistors monitoring the voltage across each inductor and by passing the signal through a low−pass filter. This summer−filter is implemented by the CS amplifier that is configured with resistors $R_{PH(X)}$ (summer), and R_{CS} and C_{CS} (filter). The output resistance of the regulator is set by the following equations, where R_L is the DCR of the output inductors:

$$R_O = \frac{R_{CS}}{R_{PH(x)}} \times R_L \quad \text{(eq. 5)}$$

$$C_{CS} = \frac{L}{R_L \cdot R_{CS}} \quad \text{(eq. 6)}$$

Users have the flexibility of choosing either R_{CS} or $R_{PH(X)}$. Due to the current drive ability of the CSCOMP pin, the R_{CS} resistance should be larger than 100 kΩ. For example, users should initially select R_{CS} to be equal to 220 kΩ, then use Equation 6 to solve for C_{CS}:

$$C_{CS} = \frac{360\ \text{nH}}{0.89\ \text{m}\Omega \times 220\ \text{k}\Omega} = 1.84\ \text{nF} \quad \text{(eq. 7)}$$

Because C_{CS} is not the standard capacitance, it is implemented with two standard capacitors in parallel: 1.8 nF and 47 pF. For the best accuracy, C_{CS} should be a 5% NPO capacitor. Next, solve $R_{PH(X)}$ by rearranging Equation 5.

$$R_{PH(X)} \geq \frac{0.89\ \text{m}\Omega}{2.1\ \text{m}\Omega} \cdot 220\ \text{k}\Omega = 93.2\ \text{k}\Omega \quad \text{(eq. 8)}$$

The standard 1% resistor for $R_{PH(X)}$ is 93.1 kΩ.

Inductor DCR Temperature Correction

With the inductor DCR used as a sense element, and copper wire being the source of the DCR, users need to compensate for temperature changes in the inductor's winding. Fortunately, copper has a well−known temperature coefficient (TC) of 0.39%/°C.

If R_{CS} is designed to have an opposite sign but equal percentage change in resistance, then it cancels the temperature variation of the inductor DCR. Due to the nonlinear nature of NTC thermistors, series resistors, R_{CS1} and R_{CS2} (see Figure 25) are needed to linearize the NTC and produce the desired temperature coefficient tracking.

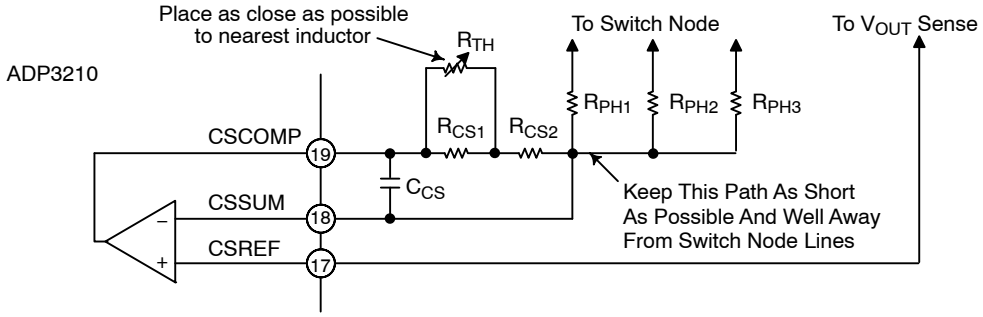


Figure 25. Temperature−Compensation Circuit Values

The following procedure and equations yield values for R_{CS1}, R_{CS2}, and R_{TH} (the thermistor value at 25°C) for a given R_{CS} value:

1. Select an NTC to be used based on type and value. Because there is no value yet, start with a thermistor with a value close to R_{CS}. The NTC should also have an initial tolerance of better than 5%.
2. Based on the type of NTC, find its relative resistance value at two temperatures. Temperatures that work well are 50°C and 90°C. These are called Resistance Value A (A is $R_{TH}(50°C)/R_{TH}(25°C)$) and Resistance Value B (B is $R_{TH}(90°C)/R_{TH}(25°C)$). Note that the relative value of NTC is always 1 at 25°C.
3. Next, find the relative value of R_{CS} that is required for each of these temperatures. This is based on the percentage of change needed, which is initially 0.39%/°C. These are called r_1 and r_2.

$$r_1 = \frac{1}{1 + TC \times (T_1 - 25)}$$

$$r_2 = \frac{1}{1 + TC \times (T_2 - 25)} \quad \text{(eq. 9)}$$

where:
TC = 0.0039
T_1 = 50°C
T_2 = 90°C.

4. Compute the relative values for r_{CS1}, r_{CS2}, and r_{TH} using:

$$r_{CS2} = \frac{(A - B) \times r_1 \times r_2 - A \times (1 - B) \times r_2 + B \times (1 - A) \times r_1}{A \times (1 - B) \times r_1 - B \times (1 - A) \times r_2 - (A - B)}$$

$$r_{CS1} = \frac{(1 - A)}{\frac{1}{1 - r_{CS2}} - \frac{1}{r_1 - r_{CS2}}}$$

$$r_{TH} = \frac{1}{\frac{1}{1 - r_{CS2}} - \frac{1}{r_{CS1}}} \quad \text{(eq. 10)}$$

5. Calculate $R_{TH} = R_{TH} \times R_{CS}$, then select the closest value of thermistor that is available. Also, compute a scaling factor k based on the ratio of the actual thermistor value relative to the computed one.

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} \quad \text{(eq. 11)}$$

6. Finally, calculate values for R_{CS1} and R_{CS2} using:

$$R_{CS1} = R_{CS} \times k \times r_{CS1}$$
$$R_{CS2} = R_{CS} \times ((1 - k) + (k \times r_{CS2})) \quad \text{(eq. 12)}$$

This example starts with a thermistor value of 100 kΩ and uses a Vishay NTHS0603N04 NTC thermistor (a 0603 size thermistor) with A = 0.3359 and B = 0.0771. From this data, r_{CS1} = 0.359, r_{CS2} = 0.729 and r_{TH} = 1.094. Solving for R_{TH} yields 240 kΩ, so 220 kΩ is chosen, making k = 0.914. Finally, R_{CS1} and R_{CS2} are 72.3 kΩ and 166 kΩ. Choosing the closest 1% resistor values yields a choice of 71.5 kΩ and 165 kΩ.

C_{OUT} Selection

The required output decoupling for processors and platforms is typically recommended by Intel. The following guidelines can also be used if both bulk and ceramic capacitors in the system:

- Select the total amount of ceramic capacitance. This is based on the number and type of capacitors to be used. The best location for ceramics is inside the socket; 20 pieces of Size 0805 being the physical limit. Additional capacitors can be placed along the outer edge of the socket.
- Select the number of ceramics and find the total ceramic capacitance (C_Z). Combined ceramic values of 200 μF to 300 μF are recommended and are usually made up of multiple 10 μF or 22 μF capacitors.
- Note that there is an upper limit imposed on the total amount of bulk capacitance (C_X) when considering the VID OTF output voltage stepping (voltage step V_V in time t_V with error of V_{ERR}), and also a lower limit based on meeting the critical capacitance for load release at a given maximum load step ΔI_O. For a step−off load current, the current version of the IMVP−6 specification allows a maximum V_{CORE} overshoot (V_{OSMAX}) of 10 mV, plus 1.5% of the VID voltage. For example, if the VID is 1.150 V, then the largest overshoot allowed is 27 mV.

$$C_{x(MIN)} \geq \left(\frac{L \times \Delta I_O}{n \times \left(R_O + \frac{V_{OSMAX}}{\Delta I_O} \right) \times V_{VID}} - C_z \right) \quad \text{(eq. 13)}$$

$$C_{X(MAX)} \leq \frac{L}{nK^2 R_O{}^2} \times \frac{V_v}{V_{VID}} \times \left(\sqrt{1 + \left(t_v \frac{V_{VID}}{V_v} \times \frac{nKR_O}{L} \right)^2} - 1 \right) - C_z \quad \text{(eq. 14)}$$

where:

$$K = -1n\left(\frac{V_{ERR}}{V_V}\right) \quad \text{(eq. 15)}$$

To meet the conditions of these equations and transient response, the ESR of the bulk capacitor bank (R_X) should be less than two times the droop resistance, R_O. If the $C_{X(MIN)}$ is larger than $C_{X(MAX)}$, the system does not meet the VID OTF and/or deeper sleep exit specification and can require a smaller inductor or more phases (the switching frequency can also have to be increased to keep the output ripple the same).

For example, if using 32 pieces of 10 μF 0805 MLC capacitors (C_Z = 320 μF), the fastest VID voltage change is the exit of deeper sleep, and V_{CORE} change is 220 mV in 22 μs with a setting error of 10 mV. Where K = 3.1, solving for the bulk capacitance yields:

$$C_{X(MIN)} \geq \left(\frac{360\ \text{nH} \times 34.5\ \text{A}}{2 \times \left(2.1\ \text{m}\Omega + \frac{50\ \text{mV}}{34.5\ \text{A}}\right) \times 1.150\ \text{V}} - 320\ \mu\text{F} \right) = 0.8\ \text{mF}$$

$$C_{X(MAX)} \leq \frac{360\ \text{nH} \times 220\ \text{mV}}{2 \times 3.1^2 \times (2.1\ \text{m}\Omega)^2 \times 1.150\ \text{V}} \left(\sqrt{1 + \left(\frac{22\ \mu\text{s} \times 1.150\ \text{V} \times 2 \times 3.1 \times 2.1\ \text{m}\Omega}{220\ \text{mV} \times 360\ \text{nH}} \right)^2} - 1 \right) - 320\ \mu\text{F} = 2.3\ \text{mF} \quad \text{(eq. 16)}$$

Using four 330 μF Panasonic SP capacitors with a typical ESR of 6 mΩ each yields C_X = 1.32 mF with an R_X = 1.5 mΩ.

One last check should be made to ensure that the ESL of the bulk capacitors (L_X) is low enough to limit the high frequency ringing during a load change. This is tested using:

$$L_X \leq C_2 \times R_O{}^2 \times Q^2$$
$$L_X \leq C_{320\ \mu\text{F}} \times (2.1\ \text{m}\Omega)^2 \times 2 = 2\ \text{nH} \quad \text{(eq. 17)}$$

where:

Q is limited to the square root of 2 to ensure a critically damped system.

In this example, L_X is about 250 pH for the four SP capacitors, which satisfies this limitation. If the L_X of the chosen bulk capacitor bank is too large, the number of ceramic capacitors may need to be increased if there is excessive ringing.

Note that for this multi−mode control technique, an all−ceramic capacitor design can be used as long as the conditions of Equation(s) 13, 14, and 15 are satisfied.

Power MOSFETs

For normal 20 A per phase application, the N−channel power MOSFETs are selected for two high−side switches and two low−side switches per phase. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, Q_G, C_{ISS}, C_{RSS} and $R_{DS(ON)}$. Because the gate drive voltage (the supply voltage to the ADP3611) is 5.0 V, logic−level threshold MOSFETs must be used.

The maximum output current I_O determines the $R_{DS(ON)}$ requirement for the low−side (synchronous) MOSFETs. In the ADP3210, currents are balanced between phases; the current in each low−side MOSFET is the output current divided by the total number of MOSFETs (n_{SF}). With conduction losses being dominant, the following equation shows the total power dissipated in each synchronous MOSFET in terms of the ripple current per phase (I_R) and average total output current (I_O):

$$P_{SF} = (1 - D) \times \left[\left(\frac{I_O}{n_{SF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{SF}} \right)^2 \right] \times R_{DS(SF)} \quad \text{(eq. 18)}$$

Knowing the maximum output thermal current and the maximum allowed power dissipation, users can find the required $R_{DS(ON)}$ for the MOSFET. For 8−lead SOIC or 8−lead SOIC compatible packaged MOSFETs, the junction to ambient (PCB) thermal impedance is 50°C/W. In the worst case, the PCB temperature is 90°C during heavy load operation of the notebook; a safe limit for P_{SF} is 0.6 W at 120°C junction temperature. Thus, for this example (32 A maximum thermal current), $R_{DS(SF)}$ (per MOSFET) is less than 9.6 mΩ for two pieces of low−side MOSFET. This $R_{DS(SF)}$ is also at a junction temperature of about 120°C; therefore, the $R_{DS(SF)}$ (per MOSFET) should be lower than 6.8 mΩ at room temperature, giving 9.6 mΩ at high temperature.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of feedback to input needs to be small (less than 10% is recommended) to prevent accidental turn−on of the synchronous MOSFETs when the switch node goes high.

The high−side (main) MOSFET has to be able to handle two main power dissipation components, conduction and switching losses. The switching loss is related to the amount of time it takes for the main MOSFET to turn on and off, and to the current and voltage that are being switched. Basing the switching speed on the rise and fall time of the gate driver impedance and MOSFET input capacitance, Equation 19 provides an approximate value for the switching loss per main MOSFETs:

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{CC} \times I_O}{n_{MF}} \times R_G \times \frac{n_{MF}}{n} \times C_{ISS} \quad \text{(eq. 19)}$$

where:

n_{MF} is the total number of main MOSFETs.

R_G is the total gate resistance (1.5 Ω for the ADP3419 and about 0.5 Ω for two pieces of typical high speed switching MOSFETs, making R_G = 2 Ω).

C_{ISS} is the input capacitance of the main MOSFET. The best thing to reduce switching loss is to use lower gate capacitance devices.

The conduction loss of the main MOSFET is given by:

$$P_{C(MF)} = D \times \left[\left(\frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{MF}} \right)^2 \right] \times R_{DS(MF)} \quad \text{(eq. 20)}$$

where:

$R_{DS(MF)}$ is the on−resistance of the MOSFET.

Typically, for main MOSFETs, users want the highest speed (low C_{ISS}) device, but these usually have higher on−resistance. Users must select a device that meets the total power dissipation (0.6 W for a single 8−lead SOIC package) when combining the switching and conduction losses.

For example, using an IRF7821 device as the main MOSFET (four in total; that is, n_{MF} = 4), with about C_{ISS} = 1010 pF (max) and $R_{DS(MF)}$ = 18 mΩ (max at T_J = 120°C) and an IR7832 device as the synchronous MOSFET (four in total; that is, n_{SF} = 4), $R_{DS(SF)}$ = 6.7 mΩ (max at T_J = 120°C). Solving for the power dissipation per MOSFET at I_O = 32 A and I_R = 10.7 A yields 420 mW for each synchronous MOSFET and 410 mW for each main MOSFET.

One last consideration is the power dissipation in the driver for each phase. This is best described in terms of the QG for the MOSFETs and is given by the following equation:

$$P_{DRV} = \left[\frac{f_{SW}}{2 \times n} \times \left(n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF} \right) + I_{CC} \right] \times V_{CC} \quad \text{(eq. 21)}$$

where:

Q_{GMF} is the total gate charge for each main MOSFET.

Q_{GSF} is the total gate charge for each synchronous MOSFET.

Also shown is the standby dissipation (I_{CC} x V_{CC}) of the driver. For the ADP3419, the maximum dissipation should be less than 300 mW, considering its thermal impedance is 220°C/W and the maximum temperature increase is 50°C. For this example, with I_{CC} = 2 mA, Q_{GMF} = 14 nC and Q_{GSF} = 51 nC, there is 120 mW dissipation in each driver, which is below the 300 mW dissipation limit. See the ADP3419 data sheet for more details.

Ramp Resistor Selection

The ramp resistor (R_R) is used for setting the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. Use this equation to determine a starting value:

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R} \quad \text{(eq. 22)}$$

$$R_R = \frac{0.5 \times 360\ \text{nH}}{3 \times 5 \times 5.2\ \text{m}\Omega \times 5\ \text{pF}} = 462\ \text{k}\Omega$$