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# ADP3211, ADP3211A

## 7-Bit, Programmable, Single-Phase, Synchronous Buck Controller

The ADP3211 is a highly efficient, single-phase, synchronous buck switching regulator controller. With its integrated driver, the ADP3211 is optimized for converting the notebook battery voltage to the supply voltage required by high performance Intel chipsets. An internal 7-bit DAC is used to read a VID code directly from the chip-set or the CPU and to set the GMCH render voltage or the CPU core voltage to a value within the range of 0 V to 1.5 V.

The ADP3211 uses a multi-mode architecture. It provides programmable switching frequency that can be optimized for efficiency depending on the output current requirement. In addition, the ADP3211 includes a programmable load line slope function to adjust the output voltage as a function of the load current so that the core voltage is always optimally positioned for a load transient. The ADP3211 also provides accurate and reliable current overload protection and a delayed power-good output. The IC supports On-The-Fly (OTF) output voltage changes requested by the chip-set.

The ADP3211 has a boot voltage of 1.1 V for IMVP-6.5 applications in CPU mode. The ADP3211A has a boot voltage of 1.2 V in CPU mode.

The ADP3211 is specified over the extended commercial temperature range of -40°C to 100°C and is available in a 32-lead QFN.

### Features

- Single-Chip Solution
  - ◆ Fully Compatible with the Intel® IMVP-6.5™ CPU and GMCH Chipset Voltage Regulator Specifications Integrated MOSFET Drivers
- Input Voltage Range of 3.3 V to 22 V
- ±7 mV Worst-Case Differentially Sensed Core Voltage Error Overtemperature
- Automatic Power-Saving Modes Maximize Efficiency During Light Load Operation
- Soft Transient Control Reduces Inrush Current and Audio Noise
- Independent Current Limit and Load Line Setting Inputs for Additional Design Flexibility
- Built-in Power-Good Masking Supports Voltage Identification (VID) OTF Transients
- 7-Bit, Digitally Programmable DAC with 0 V to 1.5 V Output
- Short-Circuit Protection
- Current Monitor Output Signal
- This is a Pb-Free Device
- Fully RoHS Compliant
- 32-Lead QFN

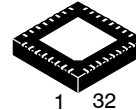
### Applications

- Notebook Power Supplies for Next Generation Intel Chipsets
- Intel Netbook Atom Processors



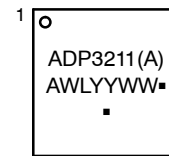
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QFN32  
MN SUFFIX  
CASE 488AM

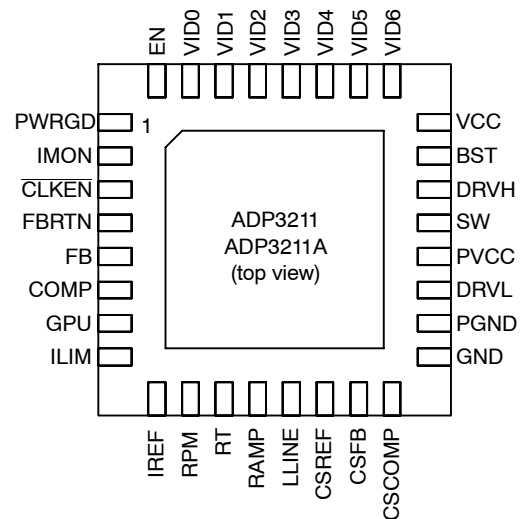
### MARKING DIAGRAM



(A) = ADP3211A Device Only  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

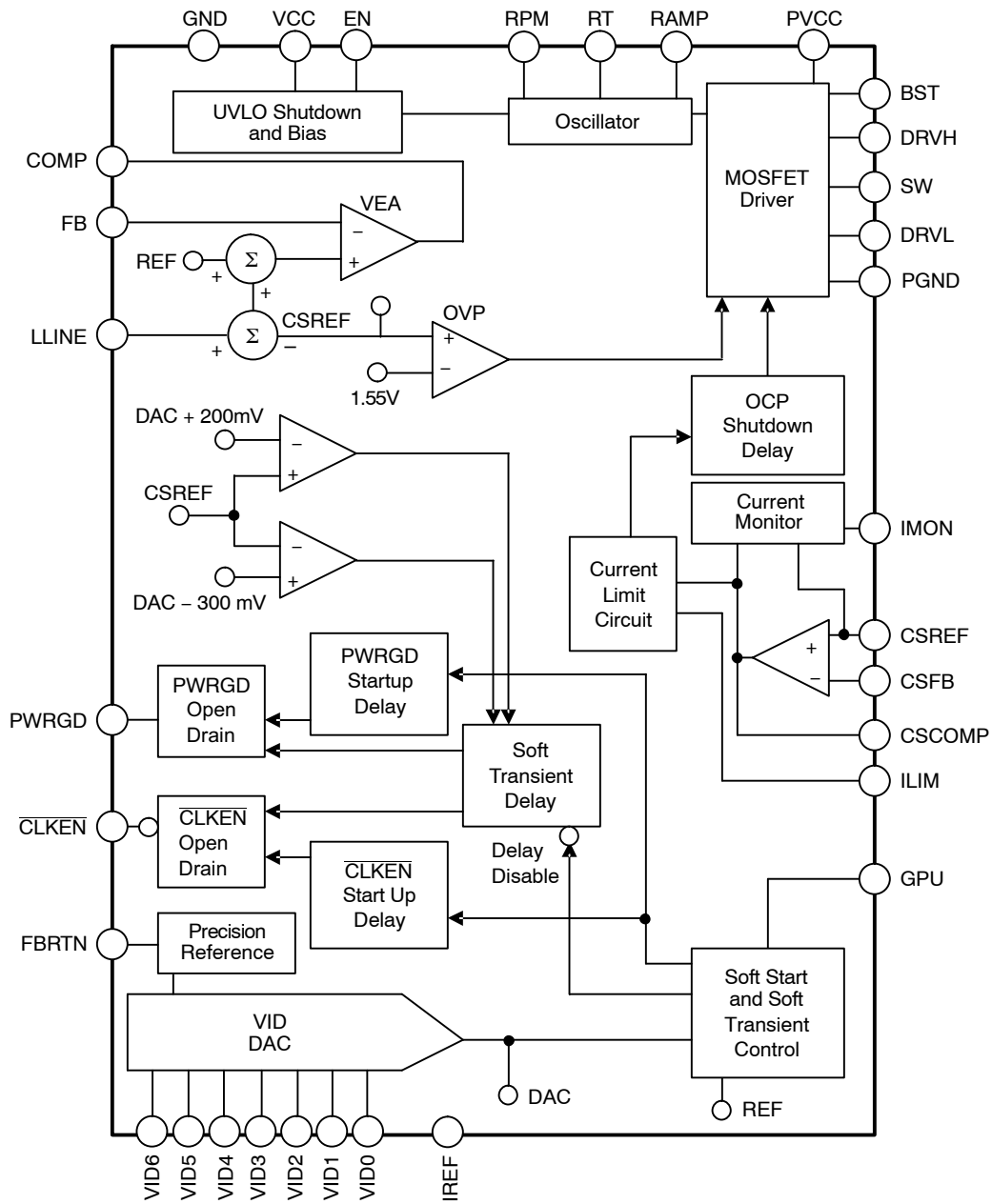
### PIN ASSIGNMENT



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 31 of this data sheet.

# ADP3211, ADP3211A



**Figure 1: Functional Block Diagram**

## ADP3211, ADP3211A

### ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
V <sub>CC</sub>	-0.3 to +6.0	V
FBRN, PGND	-0.3 to +0.3	V
BST, DRVH DC t < 200 ns	-0.3 to +28 -0.3 to +33	V
BST to PV <sub>CC</sub> DC t < 200 ns	-0.3 to +22 -0.3 to +28	V
BST to SW	-0.3 to +6.0	V
SW DC t < 200 ns	-1.0 to +22 -6.0 to +28	V
DRVH to SW	-0.3 to +6.0	V
DRVL to PGND DC t < 200 ns	-0.3 to +6.0 -5.0 to +6.0	V
RAMP (in Shutdown) DC t < 200 ns	-0.3 to +22 -0.3 to +26	V
All Other Inputs and Outputs	-0.3 to +6.0	V
Storage Temperature Range	-65 to +150	°C
Operating Ambient Temperature Range	-40 to 100	°C
Operating Junction Temperature	125	°C
Thermal Impedance ( $\theta_{JA}$ ) 2-Layer Board	32.6	°C/W
Lead Temperature Soldering (10 sec) Infrared (15 sec)	300 260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

## ADP3211, ADP3211A

### PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	PWRGD	Power-Good Output. Open-drain output. A low logic state means that the output voltage is outside of the VID DAC defined range.
2	IMON	Current Monitor Output. This pin sources current proportional to the output load current. A resistor connected to FBRTN sets the current monitor gain.
3	CLKEN	Clock Enable Output. Open drain output. The pull-high voltage on this pin cannot be higher than VCC.
4	FBRTN	Feedback Return Input/Output. This pin remotely senses the GMCH voltage. It is also used as the ground return for the VID DAC and the voltage error amplifier blocks.
5	FB	Voltage Error Amplifier Feedback Input. The inverting input of the voltage error amplifier.
6	COMP	Voltage Error Amplifier Output and Frequency Compensation Point.
7	GPU	GMCH/CPU select pin. Connect to ground when powering the CPU. Connect to 5.0 V when powering the GMCH. When GPU is connected to ground, the boot voltage is 1.1 V for the ADP3211 and 1.2 V for the ADP3211A. When GPU is connected to 5.0 V, there is no boot voltage.
8	ILIM	Current Limit Set pin. Connect a resistor between ILIM and CSCOMP to the current limit threshold.
9	IREF	This pin sets the internal bias currents. A 80 k $\Omega$ is connected from IREF to ground.
10	RPM	RPM Mode Timing Control Input. A resistor is connected from RPM to ground sets the RPM mode turn-on threshold voltage.
11	RT	PWM Oscillator Frequency Setting Input. An external resistor from this pin to GND sets the PWM oscillator frequency.
12	RAMP	PWM Ramp Slope Setting Input. An external resistor from the converter input voltage node to this pin sets the slope of the internal PWM stabilizing ramp.
13	LLINE	Load Line Programming Input. The center point of a resistor divider connected between CSREF and CSCOMP tied to this pin sets the load line slope.
14	CSREF	Current Sense Reference Input. This pin must be connected to the opposite side of the output inductor.
15	CSFB	Non-inverting Input of the Current Sense Amplifier. The combination of a resistor from the switch node to this pin and the feedback network from this pin to the CSCOMP pin sets the gain of the current sense amplifier.
16	CSCOMP	Current Sense Amplifier Output and Frequency Compensation Point.
17	GND	Analog and Digital Signal Ground.
18	PGND	Low-Side Driver Power Ground. This pin should be connected close to the source of the lower MOSFET(s).
19	DRVL	Low-Side Gate Drive Output.
20	PVCC	Power Supply Input/Output of Low-Side Gate Driver.
21	SW	Current Return For High-Side Gate Drive.
22	DRVH	High-Side Gate Drive Output.
23	BST	High-Side Bootstrap Supply. A capacitor from this pin to SW holds the bootstrapped voltage while the high-side MOSFET is on.
24	VCC	Power Supply Input/Output of the Controller.
25 to 31	VID6 to VID0	Voltage Identification DAC Inputs. A 7-bit word (the VID Code) programs the DAC output voltage, the reference voltage of the voltage error amplifier without a load (see the VID Code Table, Table NO TAG). In normal operation mode, the VID DAC output programs the output voltage to a value within the 0 V to 1.5 V range. The input is actively pulled down.
32	EN	Enable Input. Driving this pin low shuts down the chip, disables the driver outputs, and pulls PWRGD low.

## ADP3211, ADP3211A

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = PV_{CC} = 5.0\text{ V}$ ,  $FBRTN = GND = PGND = 0\text{ V}$ ,  $H = 5.0\text{ V}$ ,  $L = 0\text{ V}$ ,  $V_{VID} = V_{DAC} = 1.2\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $100^\circ\text{C}$ , unless otherwise noted. (Note 1) Current entering a pin (sunk by the device) has a positive sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>VOLTAGE CONTROL – Voltage Error Amplifier (VEAMP)</b>						
FB, LLINE Voltage Range (Note 2)	$V_{FB}, V_{LLINE}$	Relative to CSREF = $V_{DAC}$	-200		+200	mV
FB, LLINE Offset Voltage (Note 2)	$V_{OSVEA}$	Relative to CSREF = $V_{DAC}$	-0.5		+0.5	mV
FB Bias Current	$I_{FB}$		-1.0		+1.0	$\mu\text{A}$
LLINE Bias Current	$I_{LL}$		-50		+50	nA
LLINE Positioning Accuracy	$V_{FB} - V_{DAC}$	Measured on FB relative to nominal $V_{DAC}$ LLINE forced 80 mV below CSREF -10°C to 100°C -40°C to 100°C	-78 -77	-80 -80	-82 -83	mV
COMP Voltage Range	$V_{COMP}$	Voltage range of interest	0.85		4.0	V
COMP Current	$I_{COMP}$	COMP = 2.0 V, CSREF = $V_{DAC}$ FB forced 200 mV below CSREF FB forced 200 mV above CSREF		-650 2.0		$\mu\text{A}$ mA
COMP Slew Rate	$SR_{COMP}$	$C_{COMP} = 10\text{ pF}$ , CSREF = $V_{DAC}$ , Open loop configuration FB forced 200 mV below CSREF FB forced 200 mV above CSREF		10 -10		V/ $\mu\text{s}$
Gain Bandwidth (Note 2)	GBW	Non-inverting unit gain configuration, $R_{FB} = 1\text{ k}\Omega$		20		MHz

### VID DAC VOLTAGE REFERENCE

$V_{DAC}$ Voltage Range (Note 2)		See VID Code Table	0		1.5	V
$V_{DAC}$ Accuracy	$V_{FB} - V_{DAC}$	Measured on FB (includes offset), relative to nominal $V_{DAC}$ $V_{DAC} = 0.3000\text{ V}$ to $1.2000\text{ V}$ , -10°C to 100°C $V_{DAC} = 0.3000\text{ V}$ to $1.2000\text{ V}$ , -40°C to 100°C $V_{DAC} = 1.2125\text{ V}$ to $1.5000\text{ V}$ , -40°C to 100°C	-7.0 -9.0 -9.0		+7.0 +9.0 +9.0	mV
$V_{DAC}$ Differential Non-linearity (Note 2)			-1.0		+1.0	LSB
$V_{DAC}$ Line Regulation	$\Delta V_{FB}$	$V_{CC} = 4.75\text{ V}$ to $5.25\text{ V}$		0.05		%
$V_{DAC}$ Boot Voltage	$V_{BOOTFB}$	Measured during boot delay period, GPU = 0 V ADP3211 ADP3211A		1.100 1.200		V
Soft-Start Delay (Note 2)	$t_{DSS}$	Measured from EN pos edge to FB = 50 mV		200		$\mu\text{s}$
Soft-Start Time	$t_{SS}$	Measured from EN pos edge to FB settles to $V_{boot} = 1.1\text{ V}$ within -5%		1.4		ms
Boot Delay	$t_{BOOT}$	Measured from FB settling to $V_{boot} = 1.1\text{ V}$ within -5% to $\overline{CLKEN}$ neg edge		100		$\mu\text{s}$
$V_{DAC}$ Slew Rate		Soft-Start Arbitrary VID step		0.0625 1.0		LSB/ $\mu\text{s}$
FBRTN Current	$I_{FBRTN}$			70	200	$\mu\text{A}$

### VOLTAGE MONITORING and PROTECTION – Power Good

CSREF Undervoltage Threshold	$V_{UVCSREF} - V_{DAC}$	Relative to nominal $V_{DAC}$ Voltage	-360	-300	-240	mV
CSREF Overvoltage Threshold	$V_{OVCSREF} - V_{DAC}$	Relative to nominal $V_{DAC}$ Voltage	150	200	250	mV
CSREF Crowbar Voltage Threshold	$V_{CBCSREF}$	Relative to FBRTN	1.5	1.55	1.6	V
CSREF Reverse Voltage Threshold	$V_{RVCSREF}$	Relative to FBRTN, Latchoff Mode CSREF is falling CSREF is rising	-350	-300 -75	-5.0	mV

- All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
- Guaranteed by design or bench characterization, not production tested.

# ADP3211, ADP3211A

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = PV_{CC} = 5.0\text{ V}$ ,  $FBRTN = GND = PGND = 0\text{ V}$ ,  $H = 5.0\text{ V}$ ,  $L = 0\text{ V}$ ,  $V_{VID} = V_{DAC} = 1.2\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $100^\circ\text{C}$ , unless otherwise noted. (Note 1) Current entering a pin (sunk by the device) has a positive sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
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## VOLTAGE MONITORING and PROTECTION – Power Good

PWRGD Low Voltage	$V_{PWRGD}$	$I_{PWRGD(SINK)} = 4\text{ mA}$		75	200	mV
PWRGD High Leakage Current	$I_{PWRGD}$	$V_{PWRGD} = 5.0\text{ V}$			1.0	$\mu\text{A}$
PWRGD Startup Delay	$T_{SSPWRGD}$	Measured from $\overline{CLKEN}$ neg edge to PWRGD pos edge		8.0		ms
PWRGD Latchoff Delay	$T_{LOFFPWRGD}$	Measured from Out-off-Good-Window event to Latchoff (switching stops)		8.0		ms
PWRGD Propagation Delay (Note 2)	$T_{PDPWRGD}$	Measured from Out-off-Good-Window event to PWRGD neg edge		200		ns
Crowbar Latchoff Delay (Note 2)	$T_{LOFFCB}$	Measured from Crowbar event to Latchoff (switching stops)		200		ns
PWRGD Masking Time	$T_{MSkPWRGD}$	Triggered by any VID change		100		$\mu\text{s}$
CSREF Soft-Stop Resistance		$EN = L$ or Latchoff condition		60		$\Omega$

## CURRENT CONTROL – Current Sense Amplifier (CSAMP)

CSFB, CSREF Common-Mode Range (Note 2)		Voltage range of interest	0		2.0	V
CSFB, CSREF Offset Voltage	$V_{OSCSA}$	CSREF – CSSUM, $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ $T_A = 25^\circ\text{C}$	-1.5 -0.4		+1.5 +0.4	mV
CSFB Bias Current	$I_{BCSFB}$		-50		+50	nA
CSREF Bias Current	$I_{BCSREF}$		-2.0		2.0	$\mu\text{A}$
CSCOMP Voltage Range (Note 2)		Voltage range of interest	0.05		2.0	V
CSCOMP Current	$I_{CSCOMPsource}$ $I_{CSCOMPsink}$	CSCOMP = 2.0 V CSFB forced 200 mV below CSREF CSFB forced 200 mV above CSREF		-650 1.0		$\mu\text{A}$ mA
CSCOMP Slew Rate (Note 2)		$C_{CSCOMP} = 10\text{ pF}$ , CSREF = $V_{DAC}$ , Open loop configuration CSFB forced 200 mV below CSREF CSFB forced 200 mV above CSREF		10 -10		V/ $\mu\text{s}$
Gain Bandwidth (Note 2)	$GBW_{CSA}$	Non-inverting unit gain configuration $R_{FB} = 1\text{ k}\Omega$		20		MHz

## CURRENT MONITORING AND PROTECTION – Current Reference

$I_{REF}$ Voltage	$V_{REF}$	$R_{REF} = 80\text{ k}\Omega$ to set $I_{REF} = 20\text{ }\mu\text{A}$	1.55	1.6	1.65	V
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## CURRENT LIMITER (OCP)

Current Limit (OCP) Threshold	$V_{LIMTH}$	Measured from CSCOMP to CSREF $R_{LIM} = 4.5\text{ k}\Omega$	-115	-90	-70	mV
Current Limit Latchoff Delay		Measured from OCP event to PWRGD de-assertion		8.0		ms

## CURRENT MONITOR

Current Gain Accuracy	$I_{MON}/I_{LIM}$	Measured from $I_{LIM}$ to $I_{MON}$ $I_{LIM} = -20\text{ }\mu\text{A}$ $I_{LIM} = -10\text{ }\mu\text{A}$ $I_{LIM} = -5\text{ }\mu\text{A}$	9.5 9.4 9.0	10 10 10	10.6 10.8 11	
$I_{MON}$ Clamp Voltage	$V_{MAXMON}$	Relative to FBRTN, $I_{LIM} = -30\text{ }\mu\text{A}$ $R_{IMON} = 8\text{ k}\Omega$	1.0		1.15	V

1. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
2. Guaranteed by design or bench characterization, not production tested.

# ADP3211, ADP3211A

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = PV_{CC} = 5.0\text{ V}$ ,  $FBRTN = GND = PGND = 0\text{ V}$ ,  $H = 5.0\text{ V}$ ,  $L = 0\text{ V}$ ,  $V_{VID} = V_{DAC} = 1.2\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $100^\circ\text{C}$ , unless otherwise noted. (Note 1) Current entering a pin (sunk by the device) has a positive sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
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## PULSE WIDTH MODULATOR – Clock Oscillator

$R_T$ Voltage	$V_{RT}$	$R_T = 243\text{ k}\Omega$ , $V_{VID} = 1.2\text{ V}$ See also $V_{RT}(V_{VID})$ formula	1.08	1.2	1.35	V
PWM Clock Frequency Range (Note 2)	$f_{CLK}$	Operation of interest	0.3		3.0	MHz

## RAMP GENERATOR

RAMP Voltage	$V_{RAMP}$	$EN = H$ , $I_{RAMP} = 60\text{ }\mu\text{A}$ $EN = L$	0.9	1.0 $V_{IN}$	1.1	V
RAMP Current Range (Note 2)	$I_{RAMP}$	$EN = H$ $EN = L$ , $RAMP = 19\text{ V}$	1.0 -0.5		100 +0.5	$\mu\text{A}$

## PWM COMPARATOR

PWM Comparator Offset (Note 2)	$V_{OSRPM}$		-3.0		+3.0	mV
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## RPM COMPARATOR

RPM Current	$I_{RPM}$	$V_{VID} = 1.2\text{ V}$ , $R_T = 243\text{ k}\Omega$ See also $I_{RPM}(R_T)$ formula		-6.0		$\mu\text{A}$
RPM Comparator Offset (Note 2)	$V_{OSRPM}$	$V_{COMP} - (1 + V_{RPM})$	-3.0		+3.0	mV

## SWITCH AMPLIFIER

SW Input Resistance	$R_{SW}$	Measured from SW to PGND		1.3		k $\Omega$
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## ZERO CURRENT SWITCHING COMPARATOR

SW ZCS Threshold	$V_{ZCSSW}$	DCM mode, $DPRSLP = 3.3\text{ V}$		-4.0		mV
Masked Off-Time	$t_{OFFMSKD}$	Measured from DRVH neg edge to DRVH pos edge at max frequency of operation		700		ns

## SYSTEM I/O BUFFERS – EN and VID[6:0] INPUTS

Input Voltage	$V_{EN,VID[6:0]}$	Refers to driving signal level Logic low, $I_{sink} = 1\text{ }\mu\text{A}$ Logic high, $I_{source} = -5\text{ }\mu\text{A}$	0.7		0.3	V
Input Current	$I_{EN,VID[6:0]}$	$V_{EN,VID[6:0]} = 0\text{ V}$ $0.2\text{ V} < V_{EN,VID[6:0]} \leq V_{CC}$		10 1.0		nA $\mu\text{A}$
VID Delay Time (Note 2)		Any VID edge to 10% of FB change	200			ns

## GPU INPUT

Input Voltage	$V_{GPU}$	Refers to driving signal level Logic low, $I_{sink} = 1\text{ }\mu\text{A}$ Logic high, $I_{source} = -5\text{ }\mu\text{A}$	4.0		0.3	V
Input Current	$I_{GPU}$	$GPU = L$ or $GPU = H$ (static) $0.8\text{ V} < EN < 1.6\text{ V}$ (during transition)		10 70		nA $\mu\text{A}$

## CLKEN OUTPUT

Output Low Voltage	$V_{CLKEN}$	Logic low, $I_{CLKEN} = 4\text{ mA}$		30	300	mV
Output High, Leakage Current	$I_{CLKEN}$	Logic high, $V_{CLKEN} = V_{CC}$			3.0	$\mu\text{A}$

## SUPPLY

Supply Voltage Range	$V_{CC}$		4.5		5.5	V
Supply Current		$EN = H$ $EN = L$		6.0 60	10 200	mA $\mu\text{A}$
$V_{CC}$ OK Threshold	$V_{CCOK}$	$V_{CC}$ is rising		4.4	4.5	V
$V_{CC}$ UVLO Threshold	$V_{CCUVLO}$	$V_{CC}$ is falling	4.0	4.15		V
$V_{CC}$ Hysteresis (Note 2)				150		mV

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- Guaranteed by design or bench characterization, not production tested.



# ADP3211, ADP3211A

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = PV_{CC} = 5.0\text{ V}$ ,  $FBRTN = GND = PGND = 0\text{ V}$ ,  $H = 5.0\text{ V}$ ,  $L = 0\text{ V}$ ,  $V_{VID} = V_{DAC} = 1.2\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $100^\circ\text{C}$ , unless otherwise noted. (Note 1) Current entering a pin (sunk by the device) has a positive sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
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## HIGH-SIDE MOSFET DRIVER

Pullup Resistance, Sourcing Current Pulldown Resistance, Sinking Current		BST = $PV_{CC}$		2.0 1.0	3.3 2.8	$\Omega$
Transition Times	$t_{r_{DRVH}}$ , $t_{f_{DRVH}}$	BST = $PV_{CC}$ , $C_L = 3\text{ nF}$ , Figure 2		15 13	35 31	ns
Dead Delay Times	$t_{pd_{DRVH}}$	BST = $PV_{CC}$ , Figure 2		10	45	ns
BST Quiescent Current		EN = L (Shutdown) EN = H, No Switching		5.0 200	15	$\mu\text{A}$

## LOW-SIDE MOSFET DRIVER

Pullup Resistance, Sourcing Current Pulldown Resistance, Sinking Current				1.8 0.9	3.0 2.7	$\Omega$
Transition Times	$t_{r_{DRV L}}$ , $t_{f_{DRV L}}$	$C_L = 3\text{ nF}$ , Figure 2		15 14	35 35	ns
Propagation Delay Times	$t_{pd_{DRV L}}$	$C_L = 3\text{ nF}$ , Figure 2		15	30	ns
SW Transition Timeout	$t_{SWTO}$	DRVH = L, SW = 2.5 V	150	250	450	ns
SW Off Threshold	$V_{OFFSW}$			2.2		V
$PV_{CC}$ Quiescent Current		EN = L (Shutdown) EN = H, No Switching		14 200	50	$\mu\text{A}$

## BOOTSTRAP RECTIFIER SWITCH

On-Resistance		EN = L or EN = H and DRV L = H	4	7	11	$\Omega$
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1. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
2. Guaranteed by design or bench characterization, not production tested.
3. Timing is referenced to the 90% and 10% points, unless otherwise noted.

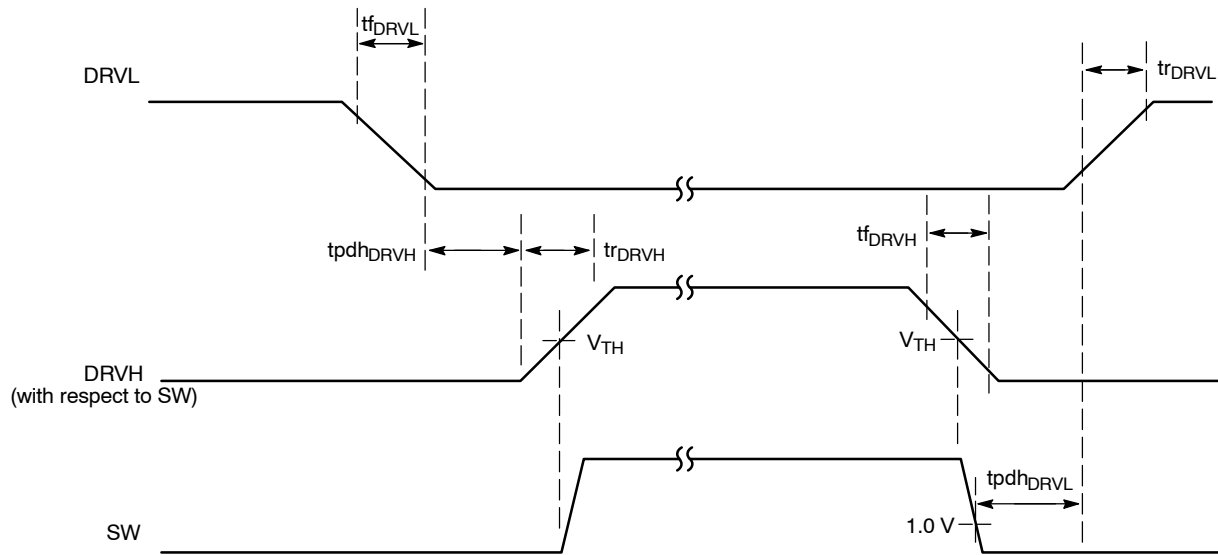


Figure 2. Timing Diagram

# ADP3211, ADP3211A

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{VID} = 1.5\text{ V}$ ,  $T_A = 20^\circ\text{C}$  to  $100^\circ\text{C}$ , unless otherwise noted.

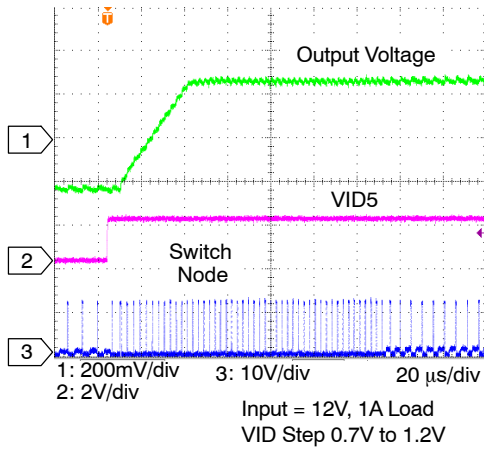


Figure 3. VID Change Soft Transient

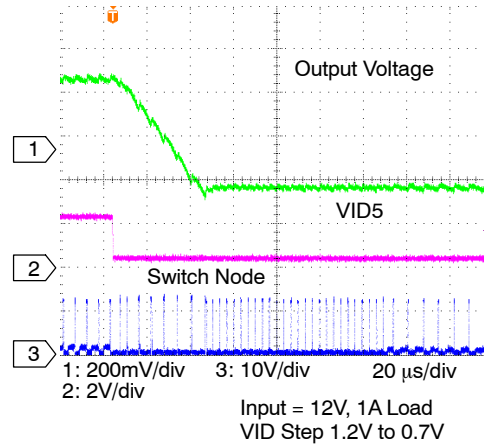


Figure 4. VID Change Soft Transient

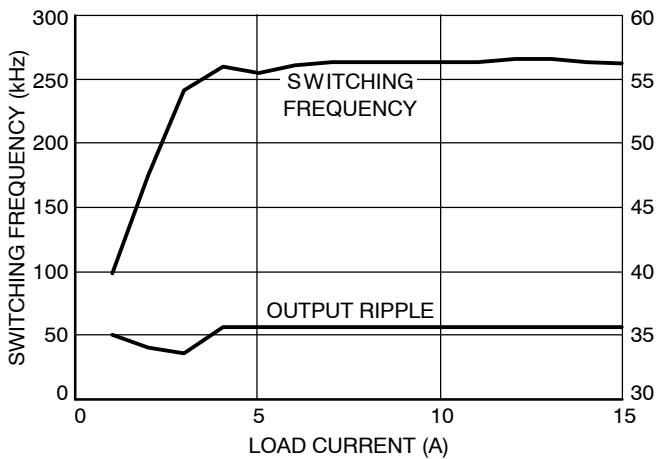


Figure 5. Switching Frequency vs. Load Current in RPM Mode

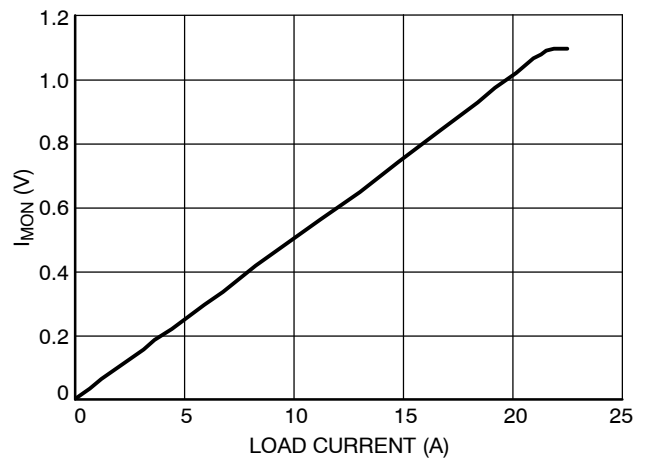


Figure 6.  $I_{MON}$  Voltage vs. Load Current

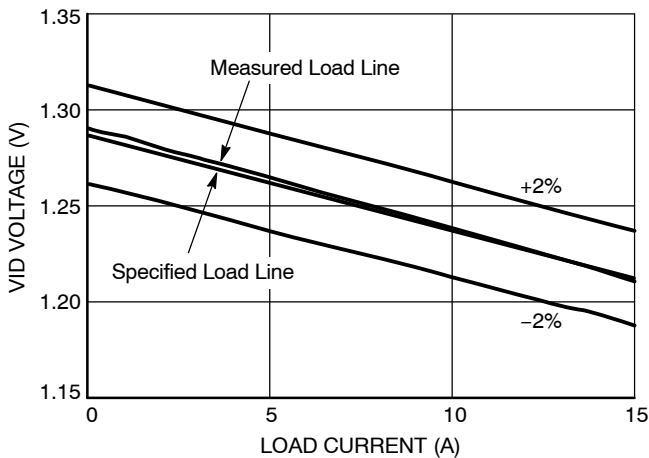


Figure 7. Load Line Accuracy

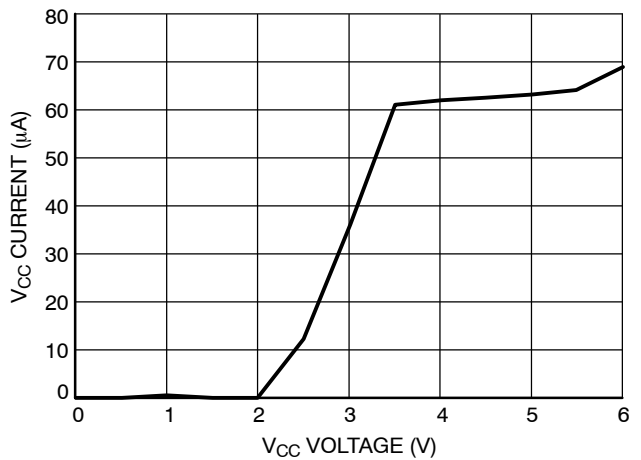


Figure 8.  $V_{CC}$  Current vs.  $V_{CC}$  Voltage with Enable Low

TYPICAL PERFORMANCE CHARACTERISTICS

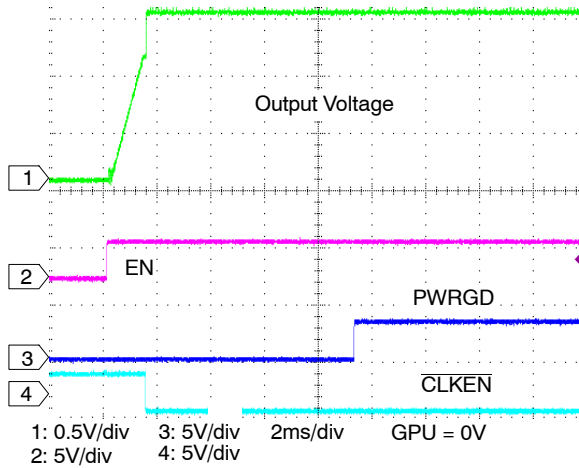


Figure 9. Startup Waveforms CPU Mode

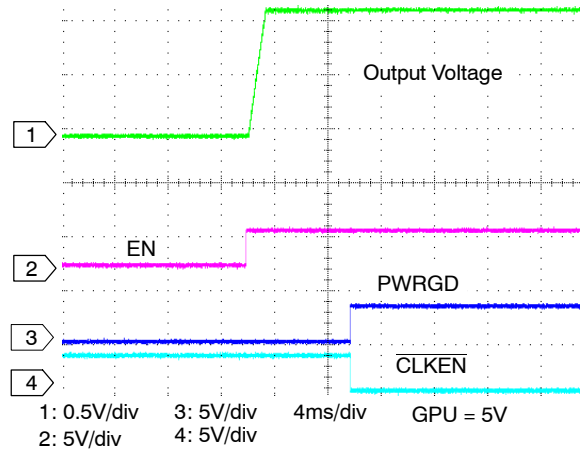


Figure 10. Startup Waveforms GPU Mode

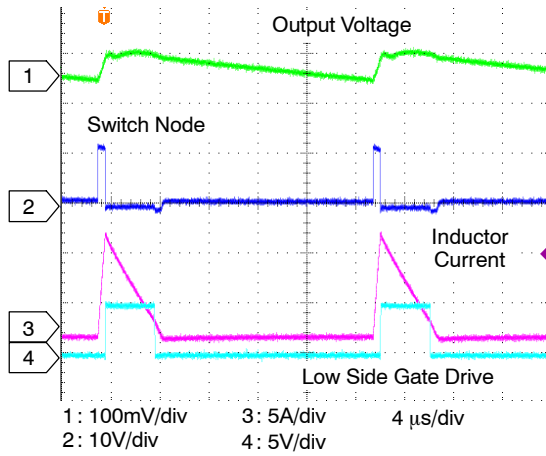


Figure 11. DCM Waveforms, 1 A Load Current

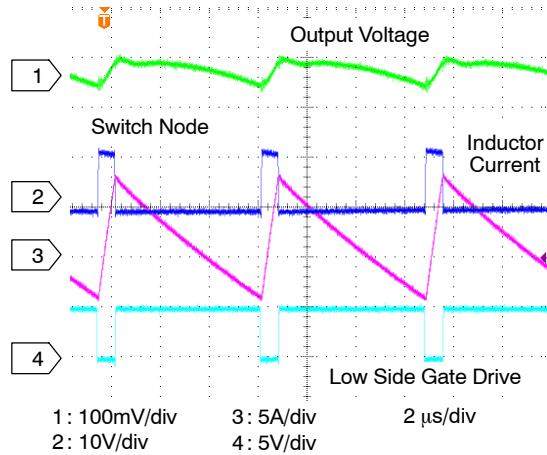


Figure 12. CCM Waveforms, 10 A Load Current

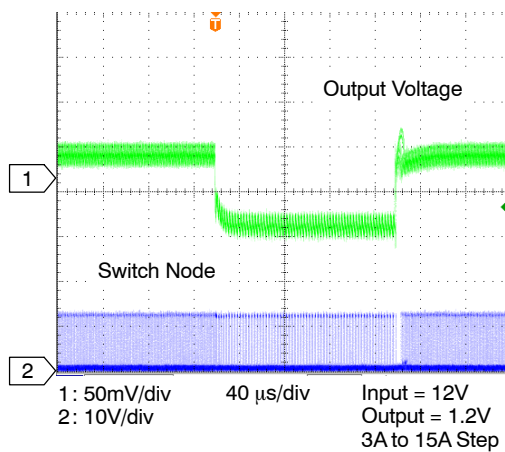


Figure 13. Load Transient

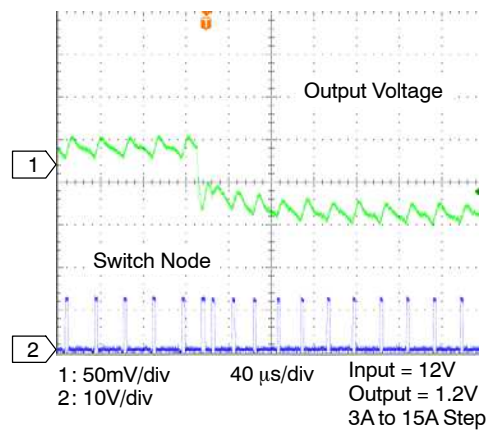


Figure 14. Load Transient

TYPICAL PERFORMANCE CHARACTERISTICS

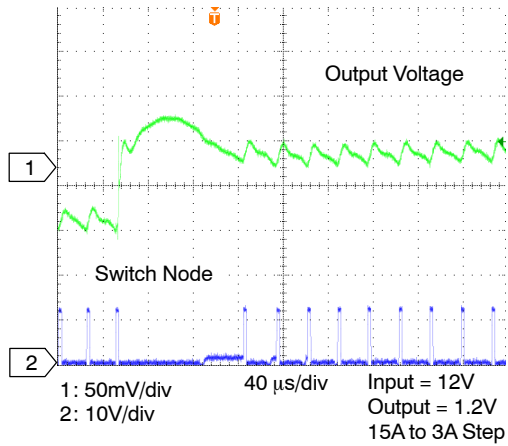


Figure 15. Load Transient

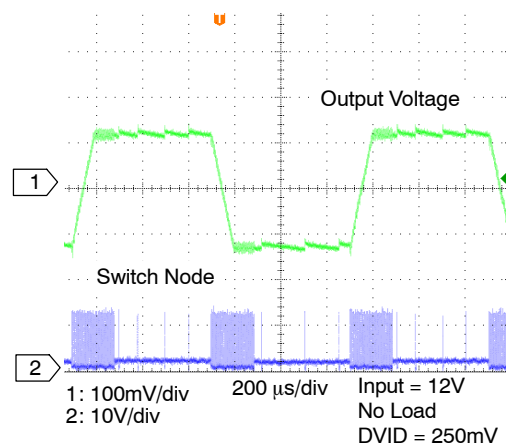


Figure 16. VID on the Fly

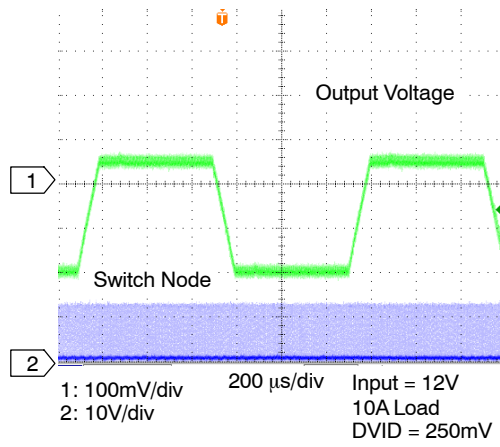


Figure 17. VID on the Fly

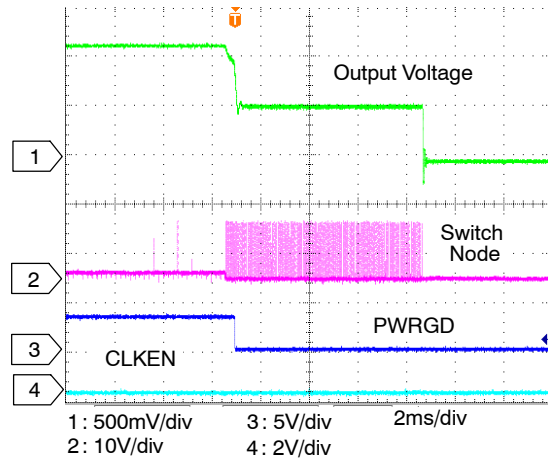


Figure 18. Over Current Protection

## ADP3211, ADP3211A

### Theory of Operation

The ADP3211 is a Ramp Pulse Modulated (RPM) controller for synchronous buck Intel GMCH and CPU core power supply. The internal 7-bit VID DAC conforms to the Intel IMVP-6.5 specifications. The ADP3211 is a stable, high performance architecture that includes

- High speed response at the lowest possible switching frequency and minimal count of output decoupling capacitors
- Minimized thermal switching losses due to lower frequency operation
- High accuracy load line regulation
- High power conversion efficiency with a light load by automatically switching to DCM operation

### Operation Modes

The ADP3211 runs in RPM mode for the purpose of fast transient response and high light load efficiency. During the following transients, the ADP3211 runs in PWM mode:

- Soft-Start
- Soft transient: the period of 110  $\mu$ s following any VID change
- Current overload

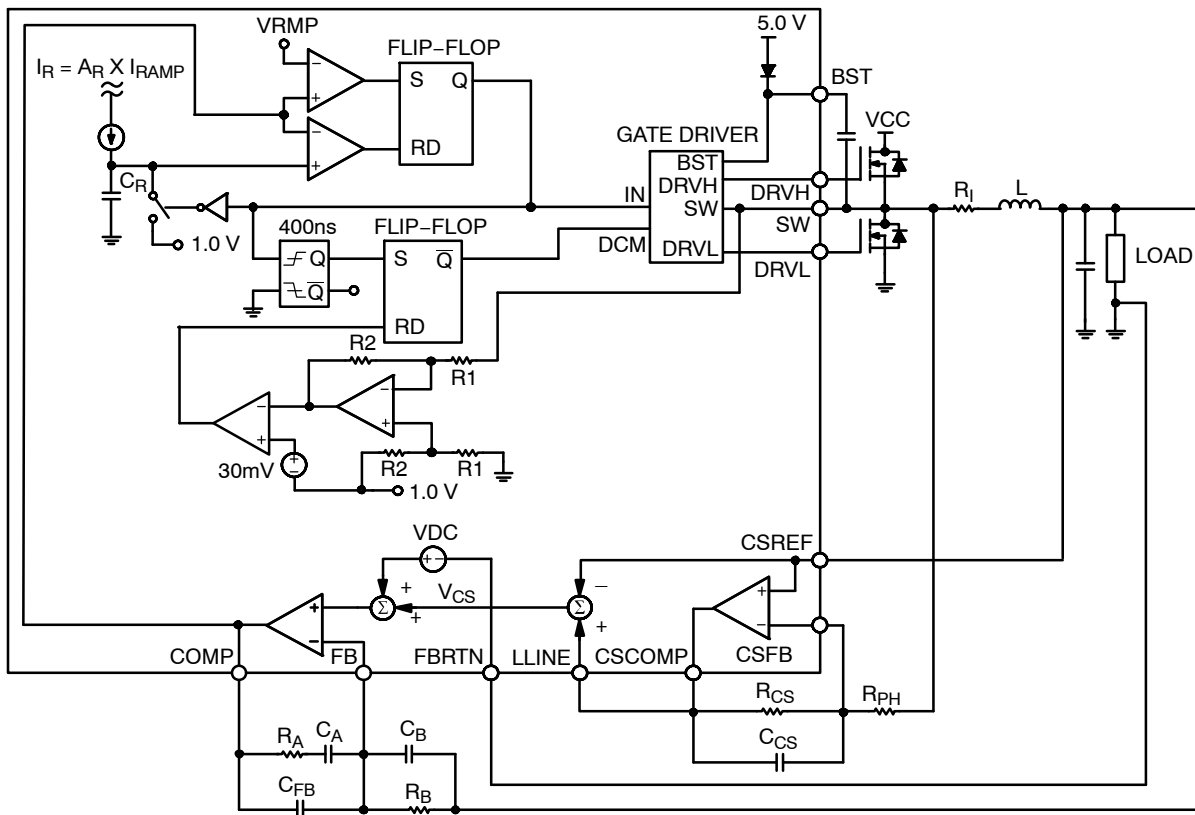


Figure 19. RPM Mode Operation

## ADP3211, ADP3211A

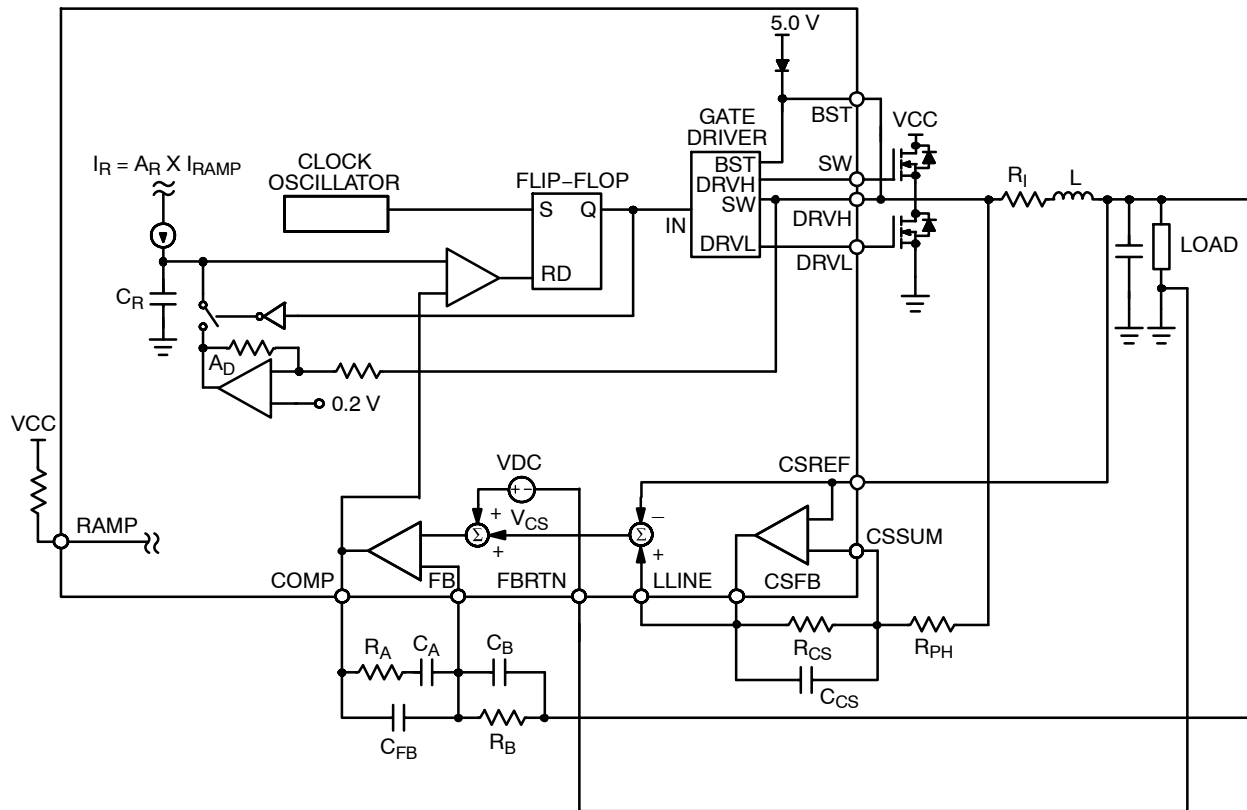


Figure 20. PWM Mode Operation

### Setting Switch Frequency

#### Master Clock Frequency in PWM Mode

When the ADP3211 runs in PWM, the clock frequency is set by an external resistor connected from the RT pin to GND. The frequency varies with the VID voltage: the lower the VID voltage, the lower the clock frequency. The variation of clock frequency with VID voltage maintains constant  $V_{CCGFX}$  ripple and improves power conversion efficiency at lower VID voltages.

#### Switching Frequency in RPM Mode

When the ADP3211 operates in RPM mode, its switching frequency is controlled by the ripple voltage on the COMP pin. Each time the COMP pin voltage exceeds the RPM pin voltage threshold level determined by the VID voltage and the external resistor connected between RPM and ground, an internal ramp signal is started and DRVH is driven high. The slew rate of the internal ramp is programmed by the current entering the RAMP pin. One-third of the RAMP current charges an internal ramp capacitor (5 pF typical) and creates a ramp. When the internal ramp signal intercepts the COMP voltage, the DRVH pin is reset low.

In continuous current mode, the switching frequency of RPM operation is almost constant. While in discontinuous current conduction mode, the switching frequency is reduced as a function of the load current.

### Differential Sensing of Output Voltage

The ADP3211 combines differential sensing with a high accuracy VID DAC, referenced by a precision band gap source and a low offset error amplifier, to meet the rigorous accuracy requirement of the Intel IMVP-6.5 specification. In steady-state mode, the combination of the VID DAC and error amplifier maintain the output voltage for a worst-case scenario within  $\pm 7$  mV of the full operating output voltage and temperature range.

The  $V_{CCGFX}$  output voltage is sensed between the FB and FBRTN pins. FB should be connected through a resistor to the positive regulation point, the  $V_{CC}$  remote sensing pin of the GMCH or CPU. FBRTN should be connected directly to the negative remote sensing point, the  $V_{SS}$  sensing point of the GMCH or CPU. The internal VID DAC and precision voltage reference are referenced to FBRTN and have a typical current of 70  $\mu$ A for guaranteed accurate remote sensing.

### Output Current Sensing

The ADP3211 includes a dedicated current sense amplifier (CSA) to monitor the total output current of the converter for proper voltage positioning vs. load current and for overcurrent detection. Sensing the current delivered to the load is an inherently more accurate method than detecting peak current or sampling the current across

a sense element, such as the low-side MOSFET. The current sense amplifier can be configured several ways, depending on system optimization objectives, and the current information can be obtained by:

- Output inductor ESR sensing without the use of a thermistor for the lowest cost
- Output inductor ESR sensing with the use of a thermistor that tracks inductor temperature to improve accuracy
- Discrete resistor sensing for the highest accuracy

At the positive input of the CSA, the CSREF pin is connected to the output voltage. At the negative input (that is, the CSFB pin of the CSA), signals from the sensing element (in the case of inductor DCR sensing, signals from the switch node side of the output inductors) are connected with a resistor. The feedback resistor between the CSCOMP and CSFB pins sets the gain of the current sense amplifier, and a filter capacitor is placed in parallel with this resistor. The current information is then given as the voltage difference between the CSCOMP and CSREF pins. This signal is used internally as a differential input for the current limit comparator.

An additional resistor divider connected between the CSCOMP and CSREF pins with the midpoint connected to the LLINE pin can be used to set the load line required by the GMCH specification. The current information to set the load line is then given as the voltage difference between the LLINE and CSREF pins. This configuration allows the load line slope to be set independent from the current limit threshold. If the current limit threshold and load line do not have to be set independently, the resistor divider between the CSCOMP and CSREF pins can be omitted and the CSCOMP pin can be connected directly to LLINE. To disable voltage positioning entirely (that is, to set no load line), LLINE should be tied to CSREF.

To provide the best accuracy for current sensing, the CSA has a low offset input voltage and the sensing gain is set by an external resistor ratio.

**Active Impedance Control Mode**

To control the dynamic output voltage droop as a function of the output current, the signal that is proportional to the total output current, converted from the voltage difference between LLINE and CSREF, can be scaled to be equal to the required droop voltage. This droop voltage is calculated by multiplying the droop impedance of the regulator by the output current. This value is used as the control voltage of the PWM regulator. The droop voltage is subtracted from the DAC reference output voltage, and the resulting voltage is used as the voltage positioning set-point. The arrangement results in an enhanced feed-forward response.

**Voltage Control Mode**

A high-gain bandwidth error amplifier is used for the voltage mode control loop. The non-inverting input voltage is set via the 7-bit VID DAC. The VID codes are

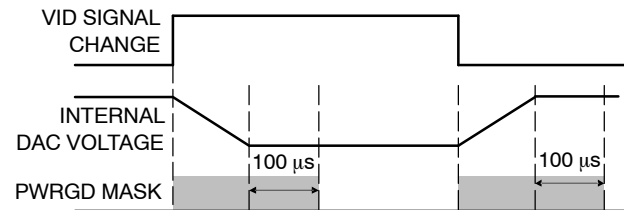
listed in Table NO TAG. The non-inverting input voltage is offset by the droop voltage as a function of current, commonly known as active voltage positioning. The output of the error amplifier is the COMP pin, which sets the termination voltage of the internal PWM ramps.

At the negative input, the FB pin is tied to the output sense location using  $R_{FB}$ , a resistor for sensing and controlling the output voltage at the remote sensing point. The main loop compensation is incorporated in the feedback network connected between the FB and COMP pins.

**Power-Good Monitoring**

The power-good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open-drain output that can be pulled up through an external resistor to a voltage rail, not necessarily the same  $V_{CC}$  voltage rail that is running the controller. A logic high level indicates that the output voltage is within the voltage limits defined by a range around the VID voltage setting. PWRGD goes low when the output voltage is outside of this range.

Following the GMCH and CPU specification, the PWRGD range is defined to be 300 mV less than and 200 mV greater than the actual VID DAC output voltage. To prevent a false alarm, the power-good circuit is masked during any VID change and during soft-start. The duration of the PWRGD mask is set to approximately 130  $\mu$ s by an internal timer. In addition, for a VID change from high to low, there is an additional period of PWRGD masking before the internal DAC voltage drops within 200 mV of the new lower VID DAC output voltage, as shown in Figure 21.



**Figure 21. PWRGD Masking for VID Change**

**Powerup Sequence and Soft-Start**

The power-on ramp-up time of the output voltage is set internally. With GPU pulled to ground, the ADP3211 steps sequentially through each VID code until it reaches the boot voltage. With GPU pulled to 5.0 V, the ADP3211 steps sequentially through each VID code until it reaches the set VID code voltage. The powerup sequence is illustrated in Figure 22 for GPU connected to ground and Figure 23 for GPU connected to 5.0 V.

When GPU is connected to ground, the ADP3211 has a boot voltage of 1.1 V for IMVP-6.5 CPU applications. When GPU is connected to ground, the ADP3211A has a boot voltage of 1.2 V. The boot voltage is the only difference between the ADP3211 and ADP3211A.

## ADP3211, ADP3211A

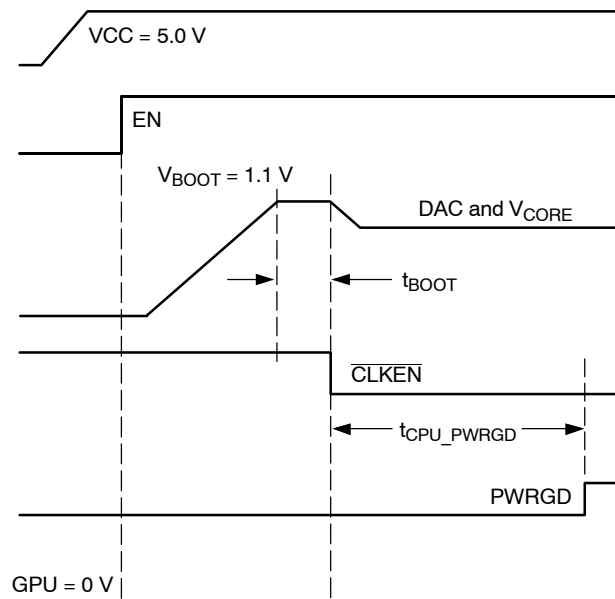


Figure 22. ADP3211 Powerup Sequence for CPU

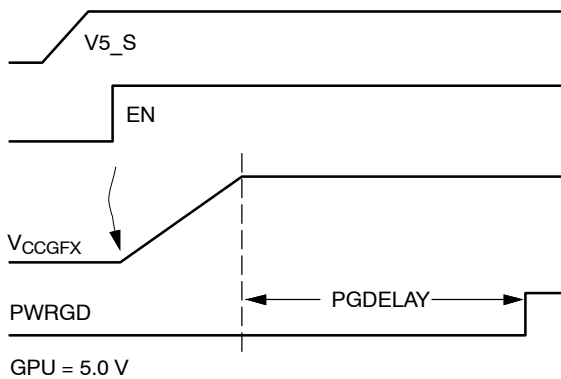


Figure 23. Powerup Sequence for GPU

### VID Change and Soft Transient

With GPU connected to 5.0 V for GPU operation, when a VID input changes, the ADP3211 detects the change but ignores new code for a minimum of 400 ns. This delay is required to prevent the device from reacting to digital signal skew while the 7-bit VID input code is in transition. Additionally, the VID change triggers a PWRGD masking timer to prevent a PWRGD failure. Each VID change resets and re-triggers the internal PWRGD masking timer.

The ADP3211 provides a soft transient function to reduce inrush current during VID transitions. Reducing the inrush current helps decrease the acoustic noise generated by the MLCC input capacitors and inductors.

The soft transient feature is implemented internally. When a new VID code is detected, the ADP3211 steps sequentially through each VID voltage to the final VID voltage.

### Current Limit, Short-Circuit, and Latchoff Protection

The ADP3211 has an adjustable current limit set by the  $R_{CLIM}$  resistor. The ADP3211 compares a programmable current limit set point to the voltage from the output of the current sense amplifier. The level of current limit is set with the resistor from the ILIM pin to CSCOMP. During operation, the voltage on ILIM is equal to the voltage on CSREF. The current through the external resistor connected between  $I_{LIM}$  and CSCOMP is then compared to the internal current limit current  $I_{cl}$ . If the current generated through this resistor into the ILIM pin ( $I_{lim}$ ) exceeds the internal current limit threshold current ( $I_{cl}$ ), the internal current limit amplifier controls the internal COMP voltage to maintain the average output current at the limit.

Normally, the ADP3211 operates in RPM mode. During a current overload, the ADP3211 switches to PWM mode.

With low impedance loads, the ADP3211 operates in a constant current mode to ensure that the external MOSFETs and inductor function properly and to protect the GPU or CPU. With a low constant impedance load, the output voltage decreases to supply only the set current limit. If the output voltage drops below the power-good limit, the PWRGD signal transitions. After the PWRGD single transitions, internal waits 8 ms before latching off the ADP3211.

Figure 24 shows how the ADP3211 reacts to a current overload.



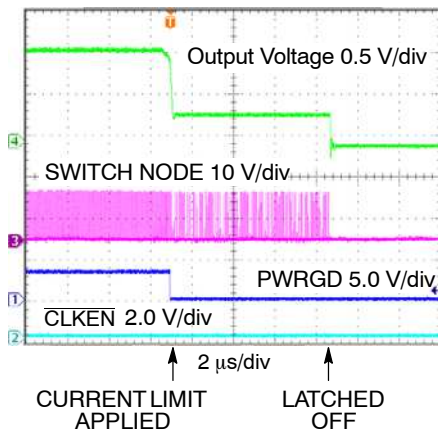


Figure 24. Current Overload

The latchoff function can be reset either by removing and reapplying  $V_{CC}$  or by briefly pulling the EN pin low.

During startup, when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot extend below ground. This secondary current limit clamp controls the minimum internal COMP voltage to the PWM comparators to 1.5 V. This limits the voltage drop across the low-side MOSFETs through the current balance circuitry.

#### Light Load RPM DCM Operation

The ADP3211 operates in RPM mode. With higher loads, the ADP3211 operates in continuous conduction mode (CCM), and the upper and lower MOSFETs run synchronously and in complementary phase. See Figure 25 for the typical waveforms of the ADP3211 running in CCM with a 10 A load current.

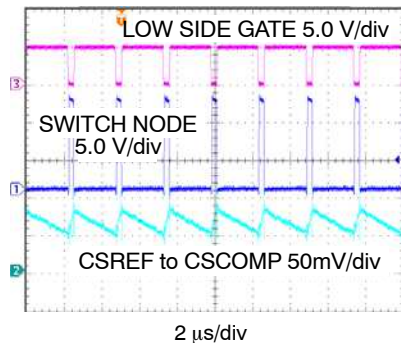


Figure 25. Single-Phase Waveforms in CCM

With lighter loads, the ADP3211 enters discontinuous conduction mode (DCM). Figure 26 shows a typical single-phase buck with one upper FET, one lower FET, an output inductor, an output capacitor, and a load resistor. Figure 27 shows the path of the inductor current with the upper FET on and the lower FET off. In Figure 28 the high-side FET is off and the low-side FET is on. In CCM, if one FET is on, its complementary FET must be off; however, in DCM, both high- and low-side FETs are off and no current flows into the inductor (see Figure 29). Figure 30 shows the inductor current and switch node voltage in DCM.

In DCM with a light load, the ADP3211 monitors the switch node voltage to determine when to turn off the low-side FET. Figure 31 shows a typical waveform in DCM with a 1 A load current. Between  $t_1$  and  $t_2$ , the inductor current ramps down. The current flows through the source drain of the low-side FET and creates a voltage drop across the FET with a slightly negative switch node. As the inductor current ramps down to 0 A, the switch voltage approaches 0 V, as seen just before  $t_2$ . When the switch voltage is approximately -4 mV, the low-side FET is turned off.

Figure 30 shows a small, dampened ringing at  $t_2$ . This is caused by the LC created from capacitance on the switch node, including the CDS of the FETs and the output inductor. This ringing is normal.

The ADP3211 automatically goes into DCM with a light load. Figure 31 shows the typical DCM waveform of the ADP3211 with a 1 A load current. As the load increases, the ADP3211 enters into CCM. In DCM, frequency decreases with load current, and switching frequency is a function of the inductor, load current, input voltage, and output voltage.

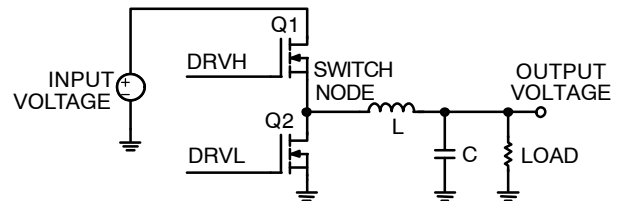


Figure 26. Buck Topology

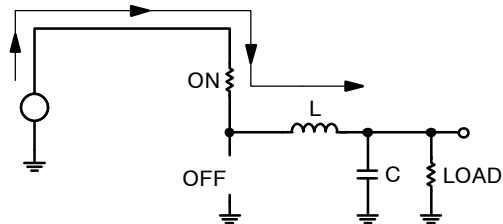


Figure 27. Buck Topology Inductor Current During  $t_0$  and  $t_1$

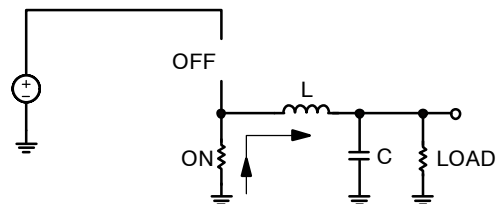


Figure 28. Buck Topology Inductor Current During  $t_1$  and  $t_2$

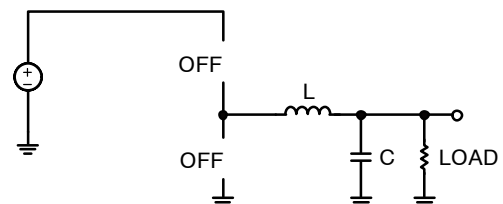


Figure 29. Buck Topology Inductor Current During  $t_2$  and  $t_3$

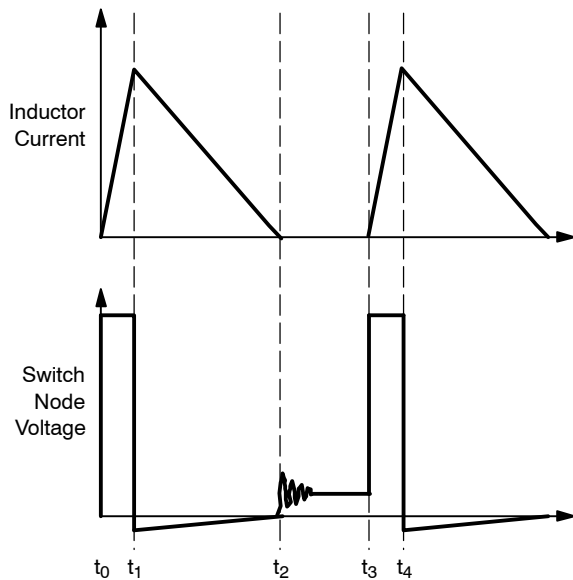


Figure 30. Inductor Current and Switch Node in DCM

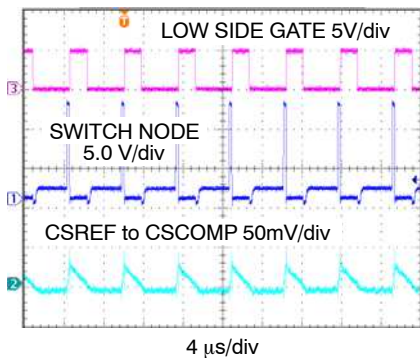


Figure 31. Single-Phase Waveforms in DCM with 1 A Load Current

**Output Crowbar**

To protect the load and output components of the supply, the DRVH output is driven high (turning the low-side MOSFETs on) and DRVL is driven low (turning the high-side MOSFETs off) when the output voltage exceeds the CPU or GMCH OVP threshold.

Turning on the low-side MOSFETs forces the output capacitor to discharge and the current to reverse due to current build up in the inductors. If the output overvoltage is due to a drain-source short of the high-side MOSFET, turning on the low-side MOSFET results in a crowbar across the input voltage rail. The crowbar action blows the fuse of the input rail, breaking the circuit and thus protecting the CPU or GMCH chip-set from destruction.

When the OVP feature is triggered, the ADP3211 is latched off. The latching function can be reset by removing and reapplying  $V_{CC}$  to the ADP3211 or by briefly pulling the EN pin low.

**Reverse Voltage Protection**

Very large reverse current in inductors can cause negative  $V_{CCGFx}$  voltage, which is harmful to the chip-set and other output components. The ADP3211 provides a reverse voltage protection (RVP) function without additional system cost. The  $V_{CCGFx}$  voltage is monitored through the CSREF pin. When the CSREF pin voltage drops to less than  $-300$  mV, the ADP3211 triggers the RVP function by setting both DRVH and DRVL low, thus turning off all MOSFETs. The reverse inductor currents can be quickly reset to 0 by discharging the built-up energy in the inductor into the input dc voltage source via the forward-biased body diode of the high-side MOSFETs. The RVP function is terminated when the CSREF pin voltage returns to greater than  $-100$  mV.

Sometimes the crowbar feature inadvertently results in negative  $V_{CCGFx}$  voltage because turning on the low-side MOSFETs results in a very large reverse inductor current. To prevent damage to the chip-set caused from negative voltage, the ADP3211 maintains its RVP monitoring function even after OVP latching. During OVP latching, if the CSREF pin voltage drops to less than  $-300$  mV, the low-side MOSFETs is turned off by setting DRVL low. DRVL will be set high again when the CSREF voltage recovers to greater than  $-100$  mV.

Figure 32 shows the reverse voltage protection function of the ADP3211. The CSREF pin is disconnected from the output voltage and pulled negative. As the CSREF pin drops to less than  $-300$  mV, the low-side and high-side FETs turn off.

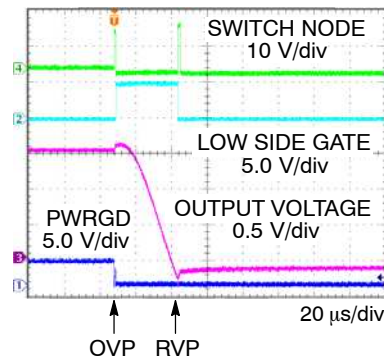


Figure 32. ADP3211 RVP Function

**Output Enable and UVLO**

For the ADP3211 to begin switching, the  $V_{CC}$  supply voltage to the controller must be greater than the  $V_{CCOK}$  threshold and the EN pin must be driven high. If the  $V_{CC}$  voltage is less than the  $V_{CCUVLO}$  threshold or the EN pin is logic low, the ADP3211 shuts off. In shutdown mode, the controller holds DRVH and DRVL low and drives PWRGD to low.

The user must adhere to proper power-supply sequencing during startup and shutdown of the ADP3211. All input pins must be at ground prior to removing or applying  $V_{CC}$ , and all output pins should be left in high impedance state while  $V_{CC}$  is off.

## ADP3211, ADP3211A

### Overlay Protection Circuit

The overlap protection circuit prevents both main power switches, the high side MOSFET Q1 and the low side MOSFET Q2, from being on at the same time. This is done to prevent shoot-through currents from flowing through both power switches and the associated losses that can occur during their on-off transitions. The overlap protection circuit accomplishes this by adaptively controlling the delay from Q1's turn-off to Q2's turn-on, and the delay from Q2's turn-off to Q1's turn-on.

To prevent the overlap of the gate drives during Q1's turn-off and Q2's turn-on, the overlap circuit monitors the voltage at the SW pin and DRVH pin. When the internal PWM signal goes low, Q1 begins to turn off. The overlap protection circuit waits for the voltage at the SW and DRVH pins to both fall below 2.2 V. Once both of these conditions are met, Q2 begins to turn on. Using this method, the overlap protection circuit ensures that Q1 is off before Q2 turns on, regardless of variations in temperature,

supply voltage, gate charge, and drive current. There is, however, a timeout circuit that overrides the waiting period for the SW and DRVH pins to reach 2.2 V. After the timeout period has expired, DRVL is asserted high regardless of the SW and DRVH voltages. The timeout period is approximately 250 ns. In the opposite case, when the internal PWM signal goes high, Q2 begins to turn off after a propagation delay. The overlap protection circuit waits for the voltage at DRVL to fall below 2.2 V, after which DRVH is asserted high and Q1 turns on.

### Output Current Monitor

The ADP3211 includes an output current monitor function. The I<sub>MON</sub> pin outputs an accurate current that is directly proportional to the output current. This current is then run through a parallel RC connected from the I<sub>MON</sub> pin to the FBRTN pin to generate an accurately scaled and filtered voltage. The maximum voltage on I<sub>MON</sub> is internally clamped by the ADP3211 at 1.15 V.

**Table 1. VID Code Table**

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500
0	0	1	0	1	0	1	1.2375
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125

# ADP3211, ADP3211A

**Table 1. VID Code Table**

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000
1	0	1	0	0	0	1	0.4875

# ADP3211, ADP3211A

**Table 1. VID Code Table**

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625
1	1	1	0	1	0	0	0.0500
1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125
1	1	1	1	0	0	0	0.0000
1	1	1	1	0	0	1	0.0000
1	1	1	1	0	1	0	0.0000
1	1	1	1	0	1	1	0.0000
1	1	1	1	1	0	0	0.0000
1	1	1	1	1	0	1	0.0000
1	1	1	1	1	1	0	0.0000
1	1	1	1	1	1	1	0.0000
1	1	1	1	1	1	1	0.0000

# ADP3211, ADP3211A

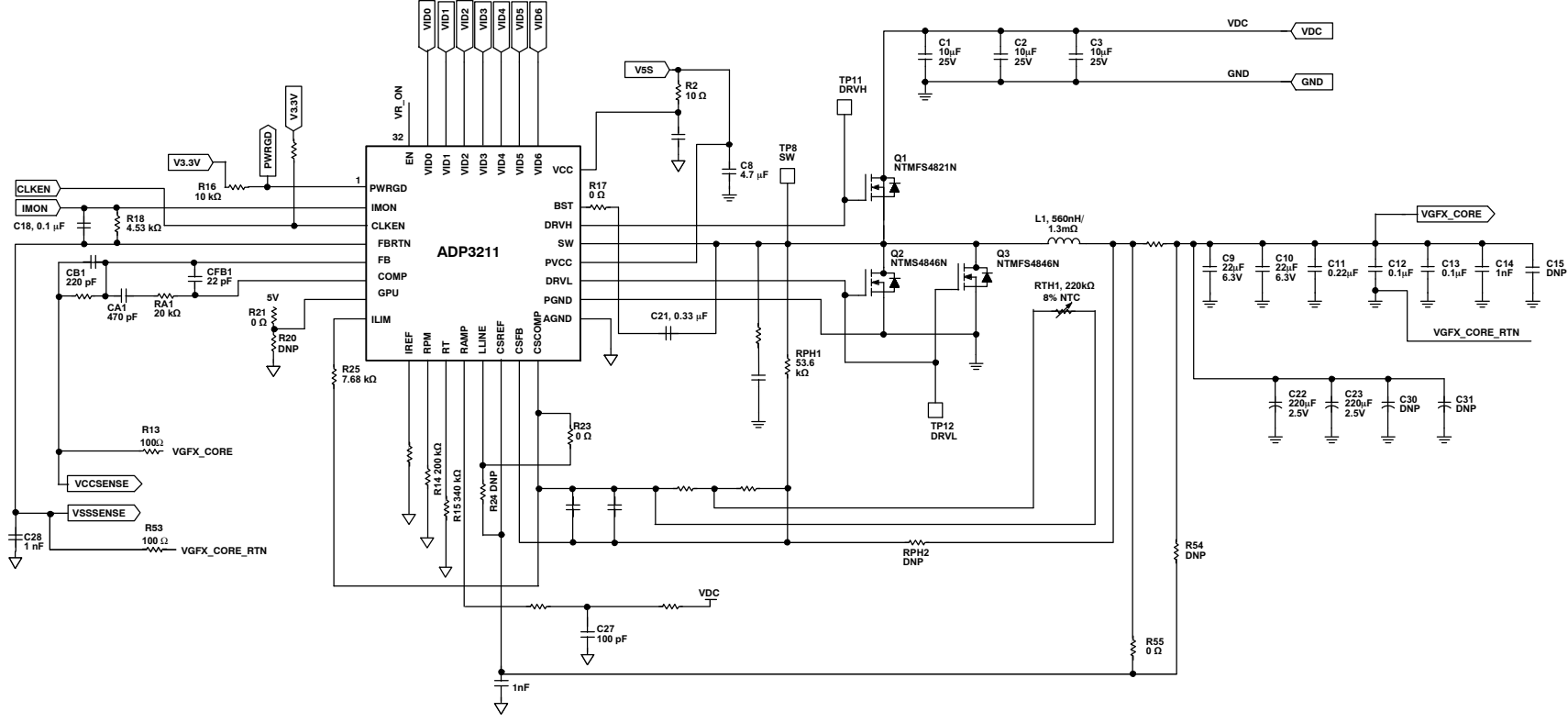


Figure 33. Typical Application Circuit

### Application Information

The ADP3211 application circuit should be fine-tuned in the final design. The equations in the Application Information section are used as a starting point for a new design.

The design parameters for a typical IMVP-6.5-compliant GPU core VR application are as follows:

- Maximum input voltage ( $V_{INMAX}$ ) = 19 V
- Minimum input voltage ( $V_{INMIN}$ ) = 8.0 V
- Output voltage by VID setting ( $V_{VID}$ ) = 1.1 V
- Maximum output current ( $I_O$ ) = 10 A
- Droop resistance ( $R_O$ ) = 8 m $\Omega$
- Nominal output voltage at 10 A load ( $V_{OFL}$ ) = 1.02 V
- Static output voltage drop from no load to full load ( $\Delta V$ ) =  $V_{ONL} - V_{OFL} = 1.1 \text{ V} - 1.02 \text{ V} = 80 \text{ mV}$
- Maximum output current step ( $\Delta I_O$ ) = 8 A
- Switching frequency ( $f_{SW}$ ) = 400 kHz
- Duty cycle at maximum input voltage ( $D_{MAX}$ ) = 0.14
- Duty cycle at minimum input voltage ( $D_{MIN}$ ) = 0.054

### Setting the Clock Frequency for PWM

The ADP3211 operates in fixed frequency PWM mode during startup, for 100  $\mu$ s after a VID change, and in current limit. In PWM operation, the ADP3211 uses a fixed-frequency control architecture. The frequency is set by an external timing resistor ( $R_T$ ). The clock frequency determines the switching frequency, which relates directly to the switching losses and the sizes of the inductors and input and output capacitors. For example, a clock frequency of 400 kHz sets the switching frequency to 400 kHz. This selection represents the trade-off between the switching losses and the minimum sizes of the output filter components. To achieve a 400 kHz oscillator frequency at a VID voltage of 1.1 V,  $R_T$  must be 274 k $\Omega$ . Alternatively, the value for  $R_T$  can be calculated by using the following equation:

$$R_T = \frac{V_{VID} + 1.0 \text{ V}}{2 \times f_{SW} \times 9 \text{ pF}} - 16 \text{ k}\Omega \quad (\text{eq. 1})$$

where:

9 pF and 16 k $\Omega$  are internal IC component values.

$V_{VID}$  is the VID voltage in volts.

$f_{SW}$  is the switching frequency in hertz.

For good initial accuracy and frequency stability, it is recommended to use a 1% resistor.

### Ramp Resistor Selection

The ramp resistor ( $R_R$ ) is used for setting the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. Use this equation to determine a starting value:

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R}$$

$$R_R = \frac{0.5 \times 560 \text{ nH}}{3 \times 5 \times 5.2 \text{ m}\Omega \times 5 \text{ pF}} = 718 \text{ k}\Omega \quad (\text{eq. 2})$$

where:

$A_R$  is the internal ramp amplifier gain.

$A_D$  is the current balancing amplifier gain.

$R_{DS}$  is the total low-side MOSFET on-resistance,

$C_R$  is the internal ramp capacitor value.

### Setting the Switching Frequency for RPM Operation

During the RPM operation, the ADP3211 runs in pseudo-constant frequency if the load current is high enough for continuous current mode. While in DCM, the switching frequency is reduced with the load current in a linear manner. To save power with light loads, lower switching frequency is usually preferred during RPM operation. However, the  $V_{CCGFX}$  ripple specification of IMVP-6.5 sets a limitation for the lowest switching frequency. Therefore, depending on the inductor and output capacitors, the switching frequency in RPM can be equal to, greater than, or less than its counterpart in PWM.

A resistor from RPM to GND sets the pseudo constant frequency as following:

$$R_{RPM} = \frac{2 \times R_T}{V_{VID} + 1.0 \text{ V}} \times \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} - 0.5 \text{ k}\Omega \quad (\text{eq. 3})$$

where:

$A_R$  is the internal ramp amplifier gain.

$C_R$  is the internal ramp capacitor value.

$R_R$  is an external resistor on the RAMPADJ pin to set the internal ramp magnitude.

Because  $R_R = 718 \text{ k}\Omega$ , the following resistance sets up 400 kHz switching frequency in RPM operation.

$$R_{RPM} = \frac{2 \times 274 \text{ k}\Omega}{1.1 \text{ V} + 1.0 \text{ V}} \times \frac{0.5 \times (1 - 0.054) \times 1.1 \text{ V}}{718 \text{ k}\Omega \times 5 \text{ pF} \times 400 \text{ kHz}} - 500 \Omega = 93.1 \text{ k}\Omega \quad (\text{eq. 4})$$

### Inductor Selection

The choice of inductance determines the ripple current of the inductor. Less inductance results in more ripple current, which increases the output ripple voltage and the conduction losses in the MOSFETs. However, this allows the use of smaller-size inductors, and for a specified peak-to-peak transient deviation, it allows less total output capacitance. Conversely, a higher inductance results in lower ripple current and reduced conduction losses, but it requires larger-size inductors and more output capacitance for the same peak-to-peak transient deviation. For a buck converter, the practical value for peak-to-peak inductor ripple current is less than 50% of the maximum dc current of that inductor. Equation 5 shows the relationship between the inductance, oscillator frequency, and peak-to-peak ripple current. Equation 6 can be used to determine the minimum inductance based on a given output ripple voltage.

$$I_R = \frac{V_{VID} \times (1 - D_{MIN})}{f_{SW} \times L} \quad (\text{eq. 5})$$

$$L \geq \frac{V_{VID} \times R_O \times (1 - D_{MIN})}{f_{SW} \times V_{RIPPLE}} \quad (\text{eq. 6})$$

In this example,  $R_O$  is assumed to be the ESR of the output capacitance, which results in an optimal transient response. Solving Equation 6 for a 16 mV peak-to-peak output ripple voltage yields:

$$L \geq \frac{1.1 \text{ V} \times 8 \text{ m}\Omega \times (1 - 0.054)}{400 \text{ kHz} \times 16 \text{ mV}} = 1.4 \text{ }\mu\text{H} \quad (\text{eq. 7})$$

If the resultant ripple voltage is less than the initially selected value, the inductor can be changed to a smaller value until the ripple value is met. This iteration allows optimal transient response and minimum output decoupling. In this example, the iteration showed that a 560 nH inductor was sufficient to achieve a good ripple.

The smallest possible inductor should be used to minimize the number of output capacitors. Choosing a 560 nH inductor is a good choice for a starting point, and it provides a calculated ripple current of 6.6 A. The inductor should not saturate at the peak current of 18.3 A, and it should be able to handle the sum of the power dissipation caused by the winding's average current (10 A) plus the ac core loss.

Another important factor in the inductor design is the DCR, which is used for measuring the inductor current. Too large of a DCR causes excessive power losses, whereas too small of a value leads to increased measurement error. For this example, an inductor with a DCR of 1.3 m $\Omega$  is used.

### Selecting a Standard Inductor

After the inductance and DCR are known, select a standard inductor that best meets the overall design goals. It is also important to specify the inductance and DCR tolerance to maintain the accuracy of the system. Using 10% tolerance for the inductance and 7% for the DCR at room temperature are reasonable values that most manufacturers can meet.

### Power Inductor Manufacturers

The following companies provide surface-mount power inductors optimized for high power applications upon request.

Vishay Dale Electronics, Inc.

(605) 665-9301

Panasonic

(714) 373-7334

Sumida Electric Company

(847) 545-6700

NEC Tokin Corporation

(510) 324-4110

### Output Droop Resistance

The design requires that the regulator output voltage measured at the chip-set pins decreases when the output current increases. The specified voltage drop corresponds to the droop resistance ( $R_O$ ).

The output current is measured by low-pass filtering the voltage across the inductor or current sense resistor. The filter is implemented by the CS amplifier that is configured with  $R_{PH}$ ,  $R_{CS}$ , and  $C_{CS}$ . The output resistance of the regulator is set by the following equations:

$$R_O = \frac{R_{CS}}{R_{PH}} \times R_{SENSE} \quad (\text{eq. 8})$$

$$C_{CS} = \frac{L}{R_{SENSE} \times R_{CS}} \quad (\text{eq. 9})$$

where  $R_{SENSE}$  is the DCR of the output inductors.

Either  $R_{CS}$  or  $R_{PH}$  can be chosen for added flexibility. Due to the current drive ability of the CSCOMP pin, the  $R_{CS}$  resistance should be greater than 100 k $\Omega$ . For example, initially select  $R_{CS}$  to be equal to 200 k $\Omega$ , and then use Equation 9 to solve for  $C_{CS}$ :

$$C_{CS} = \frac{560 \text{ nH}}{1.3 \text{ m}\Omega \times 200 \text{ k}\Omega} = 2.2 \text{ nF} \quad (\text{eq. 10})$$

If  $C_{CS}$  is not a standard capacitance,  $R_{CS}$  can be tuned. In this case, the required  $C_{CS}$  is a standard value and no tuning is required. For best accuracy,  $C_{CS}$  should be a 5% NPO capacitor.

Next, solve for  $R_{PH}$  by rearranging Equation 8 as follows:

$$R_{PH} \geq \frac{1.3 \text{ m}\Omega}{8 \text{ m}\Omega} \times 200 \text{ k}\Omega = 32.5 \text{ k}\Omega \quad (\text{eq. 11})$$

The standard 1% resistor for  $R_{PH}$  is 32.4 k $\Omega$ .

### Inductor DCR Temperature Correction

If the DCR of the inductor is used as a sense element and copper wire is the source of the DCR, the temperature changes associated with the inductor's winding must be compensated for. Fortunately, copper has a well-known temperature coefficient (TC) of 0.39%/°C.

If  $R_{CS}$  is designed to have an opposite but equal percentage of change in resistance, it cancels the temperature variation of the inductor's DCR. Due to the nonlinear nature of NTC thermistors, series resistors  $R_{CS1}$  and  $R_{CS2}$  (see Figure 34) are needed to linearize the NTC and produce the desired temperature coefficient tracking.



## ADP3211, ADP3211A

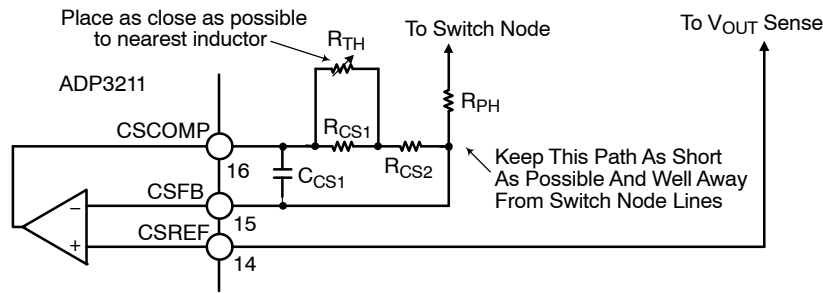


Figure 34. Temperature-Compensation Circuit Values

The following procedure and expressions yield values for  $R_{CS1}$ ,  $R_{CS2}$ , and  $R_{TH}$  (the thermistor value at 25°C) for a given  $R_{CS}$  value.

1. Select an NTC to be used based on its type and value. Because the value needed is not yet determined, start with a thermistor with a value close to  $R_{CS}$  and an NTC with an initial tolerance of better than 5%.
2. Find the relative resistance value of the NTC at two temperatures. The appropriate temperatures will depend on the type of NTC, but 50°C and 90°C have been shown to work well for most types of NTCs. The resistance values are called A ( $A$  is  $R_{TH}(50^\circ\text{C})/R_{TH}(25^\circ\text{C})$ ) and B ( $B$  is  $R_{TH}(90^\circ\text{C})/R_{TH}(25^\circ\text{C})$ ). Note that the relative value of the NTC is always 1 at 25°C.
3. Find the relative value of  $R_{CS}$  required for each of the two temperatures. The relative value of  $R_{CS}$  is based on the percentage of change needed, which is initially assumed to be 0.39%/°C in this example. The relative values are called  $r_1$  ( $r_1$  is  $1/(1 + TC \times (T_1 - 25))$ ) and  $r_2$  ( $r_2$  is  $1/(1 + TC \times (T_2 - 25))$ ), where  $TC$  is 0.0039,  $T_1$  is 50°C, and  $T_2$  is 90°C.
4. Compute the relative values for  $r_{CS1}$ ,  $r_{CS2}$ , and  $r_{TH}$  by using the following equations:

$$r_{CS2} = \frac{(A - B) \times r_1 \times r_2 - A \times (1 - B) \times r_2 + B \times (1 - A) \times r_1}{A \times (1 - B) \times r_1 - B \times (1 - A) \times r_2 - (A - B)}$$

$$r_{CS1} = \frac{(1 - A)}{\frac{1}{1 - r_{CS2}} - \frac{A}{r_1 - r_{CS2}}}$$

$$r_{TH} = \frac{1}{\frac{1}{1 - r_{CS2}} - \frac{1}{r_{CS1}}} \quad (\text{eq. 12})$$

5. Calculate  $R_{TH} = r_{TH} \times R_{CS}$ , and then select a thermistor of the closest value available. In addition, compute a scaling factor  $k$  based on the ratio of the actual thermistor value used relative to the computed one:

$$k = \frac{R_{TH(\text{ACTUAL})}}{R_{TH(\text{CALCULATED})}} \quad (\text{eq. 13})$$

6. Calculate values for  $R_{CS1}$  and  $R_{CS2}$  by using the following equations:

$$R_{CS1} = R_{CS} \times k \times r_{CS1} \quad (\text{eq. 14})$$

$$R_{CS2} = R_{CS} \times ((1 - k) + (k \times r_{CS2}))$$

For example, if a thermistor value of 100 k $\Omega$  is selected in Step 1, an available 0603-size thermistor with a value close to  $R_{CS}$  is the Vishay NTHS0603N04 NTC thermistor, which has resistance values of  $A = 0.3359$  and  $B = 0.0771$ . Using the equations in Step 4,  $r_{CS1}$  is 0.359,  $r_{CS2}$  is 0.729, and  $r_{TH}$  is 1.094. Solving for  $r_{TH}$  yields 219 k $\Omega$ , so a thermistor of 220 k $\Omega$  would be a reasonable selection, making  $k$  equal to 1.005. Finally,  $R_{CS1}$  and  $R_{CS2}$  are found to be 72.2 k $\Omega$  and 146 k $\Omega$ . Choosing the closest 1% resistor values yields a choice of 71.5 k $\Omega$  and 147 k $\Omega$ .

### C<sub>out</sub> Selection

The required output decoupling for processors and platforms is typically recommended by Intel. For systems containing both bulk and ceramic capacitors, however, the following guidelines can be a helpful supplement.

Select the number of ceramics and determine the total ceramic capacitance ( $C_Z$ ). This is based on the number and type of capacitors used. Keep in mind that the best location to place ceramic capacitors is inside the socket; however, the physical limit is twenty 0805-size pieces inside the socket. Additional ceramic capacitors can be placed along the outer edge of the socket. A combined ceramic capacitor value of 40  $\mu\text{F}$  to 50  $\mu\text{F}$  is recommended and is usually composed of multiple 10  $\mu\text{F}$  or 22  $\mu\text{F}$  capacitors.

Ensure that the total amount of bulk capacitance ( $C_X$ ) is within its limits. The upper limit is dependent on the VID OTF output voltage stepping (voltage step,  $V_V$ , in time,  $t_V$ , with error of  $V_{ERR}$ ); the lower limit is based on meeting the critical capacitance for load release at a given maximum load step,  $\Delta I_O$ . The current version of the IMVP-6.5 specification allows a maximum  $V_{CCGFX}$  overshoot ( $V_{OSMAX}$ ) of 10 mV more than the VID voltage for a step-off load current.

$$C_{X(MIN)} \geq \left[ \frac{L \times \Delta I_O}{\left( R_O + \frac{V_{OSMAX}}{\Delta I_O} \right) \times V_{VID}} - C_Z \right] \quad (\text{eq. 15})$$

$$C_{X(MAX)} \leq \frac{L}{k^2 \times R_o^2} \times \frac{V_V}{V_{VID}} \times \left[ \sqrt{1 + \left( t_v \frac{V_{VID}}{V_V} \times \frac{k \times R_o}{L} \right)^2} - 1 \right] - C_Z$$

$$\text{where } k = -1n \left( \frac{V_{ERR}}{V_V} \right) \quad (\text{eq. 16})$$

To meet the conditions of these expressions and the transient response, the ESR of the bulk capacitor bank ( $R_X$ ) should be less than two times the droop resistance,  $R_O$ . If the  $C_{X(MIN)}$  is greater than  $C_{X(MAX)}$ , the system does not meet the VID OTF specifications and may require less inductance. In addition, the switching frequency may have to be increased to maintain the output ripple.

For example, if two pieces of 22  $\mu\text{F}$ , 0805–size MLC capacitors ( $C_Z = 44 \mu\text{F}$ ) are used during a VID voltage change, the  $V_{CCGFX}$  change is 220 mV in 22  $\mu\text{s}$  with a setting error of 10 mV. If  $k = 3.1$ , solving for the bulk capacitance yields:

$$C_{X(MIN)} \geq \left[ \frac{560 \text{ nH} \times 8 \text{ A}}{\left( 5.1 \text{ m}\Omega + \frac{10 \text{ mV}}{8 \text{ A}} \right) \times 1.174 \text{ V}} - 44 \mu\text{F} \right] = 256 \mu\text{F}$$

$$C_{X(MAX)} \leq \frac{560 \text{ nH} \times 220 \text{ mV}}{3.1^2 \times (5.1 \text{ m}\Omega)^2 \times 1.174 \text{ V}} \times \left[ \sqrt{1 + \left( \frac{22 \mu\text{s} \times 1.174 \text{ V} \times 3.1 \times 5.1 \text{ m}\Omega}{220 \text{ mV} \times 560 \text{ nH}} \right)^2} - 1 \right] - 44 \mu\text{F}$$

$$= 992 \mu\text{F} \quad (\text{eq. 17})$$

Using two 220  $\mu\text{F}$  Panasonic SP capacitors with a typical ESR of 7 m $\Omega$  each yields  $C_X = 440 \mu\text{F}$  and  $R_X = 3.5 \text{ m}\Omega$ .

Ensure that the ESL of the bulk capacitors ( $L_X$ ) is low enough to limit the high frequency ringing during a load change. This is tested using:

$$\begin{aligned} L_X &\leq C_Z \times R_O^2 \times Q^2 \\ L_X &\leq 44 \mu\text{F} \times (5.1 \text{ m}\Omega)^2 \times 2 = 2.3 \text{ nH} \end{aligned} \quad (\text{eq. 18})$$

where:

$Q$  is limited to the square root of 2 to ensure a critically damped system.

$L_X$  is about 450 pH for the two SP capacitors, which is low enough to avoid ringing during a load change. If the  $L_X$  of the chosen bulk capacitor bank is too large, the number of ceramic capacitors may need to be increased to prevent excessive ringing.

For this multi–mode control technique, an all ceramic capacitor design can be used if the conditions of Equations 15, 16, and 18 are satisfied.

### Power MOSFETs

For typical 15 A applications, the N–channel power MOSFETs are selected for one high–side switch and two low–side switch. The main selection parameters for the power MOSFETs are  $V_{GS(TH)}$ ,  $Q_G$ ,  $C_{ISS}$ ,  $C_{RSS}$ , and  $R_{DS(ON)}$ . Because the voltage of the gate driver is 5.0 V, logic–level threshold MOSFETs must be used.

The maximum output current,  $I_O$ , determines the  $R_{DS(ON)}$  requirement for the low–side (synchronous) MOSFETs. With conduction losses being dominant, the following expression shows the total power that is dissipated in each synchronous MOSFET in terms of the ripple current per phase ( $I_R$ ) and the average total output current ( $I_O$ ):

$$P_{SF} = (1 - D) \times \left[ \left( \frac{I_O}{n_{SF}} \right)^2 + \frac{1}{12} \times \left( \frac{I_R}{n_{SF}} \right)^2 \right] \times R_{DS(SF)} \quad (\text{eq. 19})$$

where:

$D$  is the duty cycle and is approximately the output voltage divided by the input voltage.

$I_R$  is the inductor peak–to–peak ripple current and is approximately:

$$I_R = \frac{(1 - D) \times V_{OUT}}{L \times f_{SW}} \quad (\text{eq. 20})$$

Knowing the maximum output current and the maximum allowed power dissipation, the user can calculate the required  $R_{DS(ON)}$  for the MOSFET. For an 8–lead SOIC or 8–lead SOIC–compatible MOSFET, the junction to ambient (PCB) thermal impedance is 50°C/W. In the worst case, the PCB temperature is 70°C to 80°C during heavy load operation of the notebook, and a safe limit for  $P_{SF}$  is about 0.8 W to 1.0 W at 120°C junction temperature. Therefore, for this example (15 A maximum), the  $R_{DS(SF)}$  per MOSFET is less than 18.8 m $\Omega$  for the low–side MOSFET. This  $R_{DS(SF)}$  is also at a junction temperature of