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ADP4000

Programmable Multi-Phase Synchronous Buck Converter with I²C Interface

The ADP4000 is an integrated power control IC with an I²C interface. The ADP4000 can be programmed for 1-, 2-, 3-, 4-, 5- or 6-phase operation, allowing for the construction of up to six complementary buck switching stages. The ADP4000 supports $\overline{\text{PSI}}$, which is a power state indicator and can be used to reduce number of operating phases at light loads. The ADP4000 includes an I²C interface, which can be used to program system set points such as voltage offset, load line, phase balance and output voltage. Key system performance data such as CPU current, CPU voltage, and power and fault conditions can also be read back over the I²C interface from the ADP4000.

Features

- I²C Interface
- Supports Both VR11 and VR11.1 Specifications
- Digitally Programmable 0.375 V to 1.6 V Output
- Additional 200 mV Offset Programmable (Max 1.8 V Output)
- Selectable 1-, 2-, 3-, 4-, 5-, or 6-Phase Operation
- Fast-Enhanced PWM FlexMode™
- TRDET to Improve Load Release
- Active Current Balancing Between All Output Phases
- Supports On−The−Fly (OTF) VID Code Changes
- Supports $\overline{\text{PSI}}$ – Power Saving Mode
- This is a Pb−Free Device

Typical Applications

- Servers
- Desktop PC's
- POLs (Memory)

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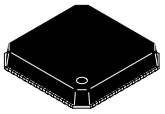
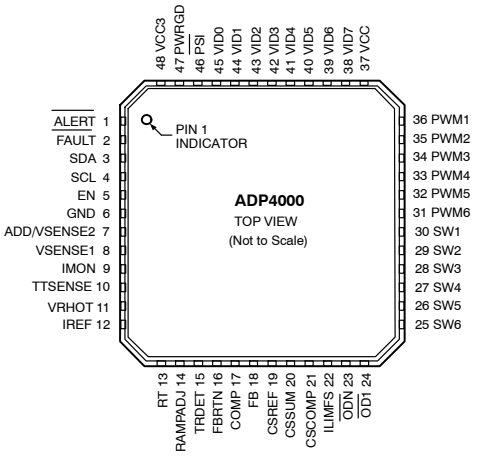
MARKING DIAGRAM



LFCSP48
CASE 932AD

xx	= Device Code
#	= Pb−Free Package
YYWW	= Date Code
XXX	= Assembly Lot
CCC	= Country of Origin

PIN ASSIGNMENT



ORDERING INFORMATION

Device*	Package	Shipping†
ADP4000JCPZ−REEL	LFCSP48	2500/Tape & Reel
ADP4000JCPZ−RL7	LFCSP48	750/Tape & Reel

*The "Z' suffix indicates Pb−Free package.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

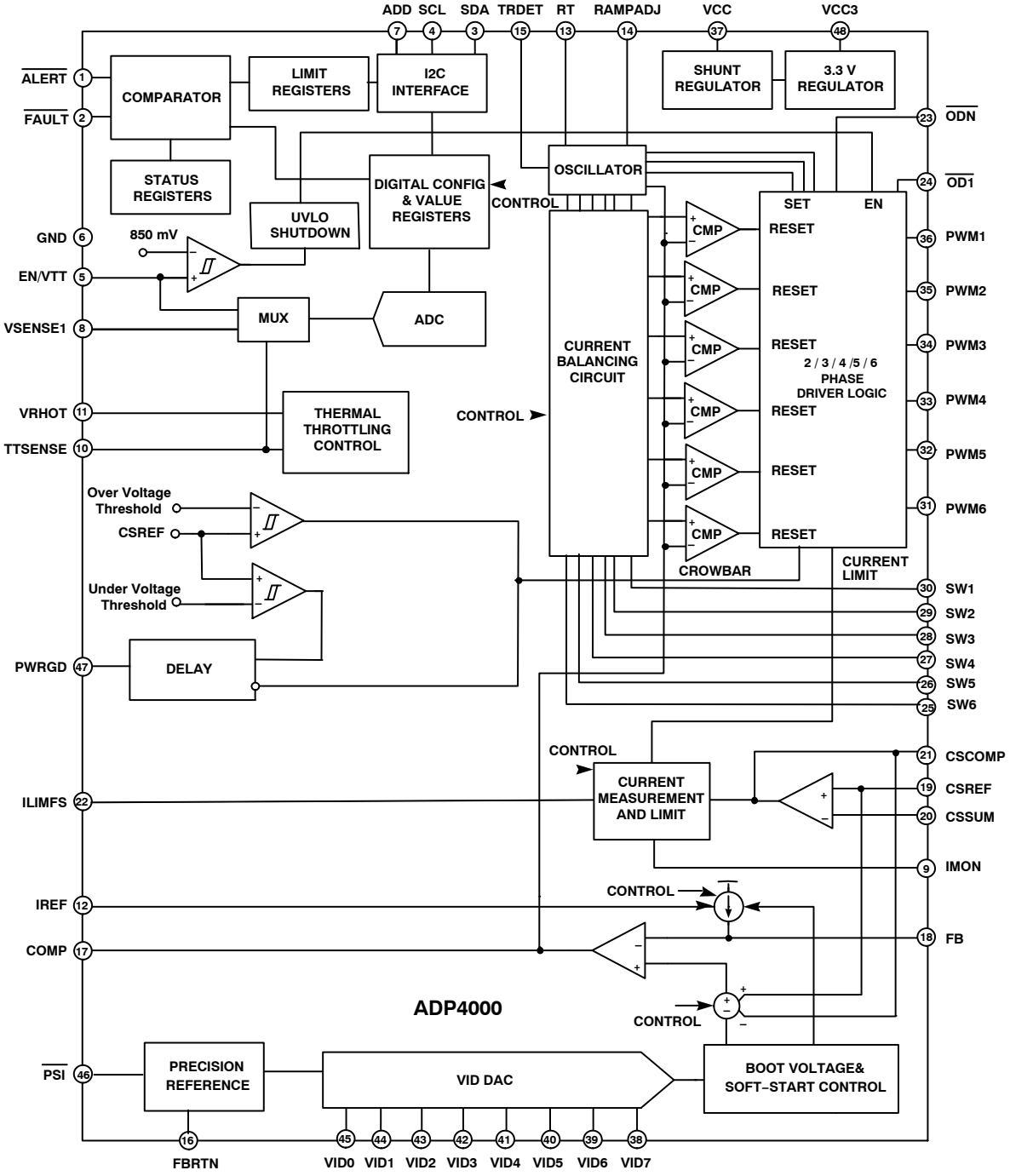


Figure 1. Block Diagram

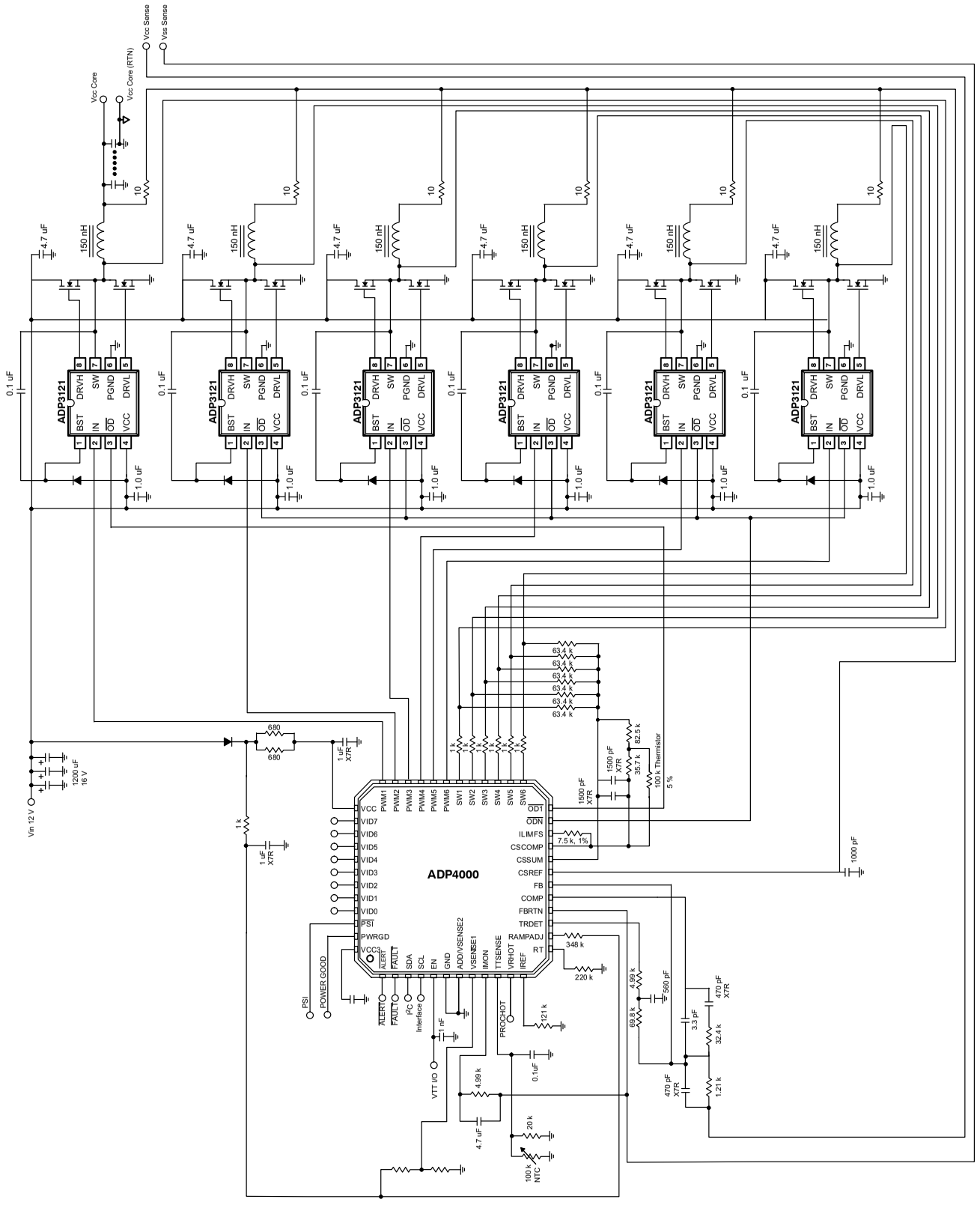


Figure 2. Application Schematic

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range (Note 1)	V_{IN}	−0.3 to 6	V
FBRTN	V_{FBRTN}	−0.3 to + 0.3	V
PWM2 to PWM6, Rampadj		−0.3 to V_{IN} + 0.3	V
SW1 to SW6		−5 to +25	V
SW1 to SW6 (<200 ns|)		−10 to +25	V
All other Inputs and Outputs		−0.3 to V_{IN} + 0.3	V
Storage Temperature Range	TSTG	−65 to 150	°C
Operating Ambient Temperature Range		0 to 85	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2	kV
ESD Capability, Machine Model (Note 2)	ESD_{MM}	100	V
Moisture Sensitivity Level	MSL	3	–
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to Electrical Characteristics and Application Information for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
3. For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Characteristics, LFCSP, 7 mm * 7 mm (Note 1) Thermal Resistance, Junction−to−Air (Note 4) Thermal Resistance, Junction−to−Lead 2 (Note 4)	 $R_{\theta JA}$ $R_{\Psi JL}$	 24 10	°C/W

4. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

OPERATING RANGES (Note 1)

Characteristic	Symbol	Min	Max	Unit
Output Voltage (Adjustable Version Only) (Note 5)	V_{OUT}	0.375	1.8	V
Ambient Temperature	T_A	0	85	°C

5. Maximum limit for $V_{OUT} = V_{OUT(NOM)} - 10\%$.

PIN ASSIGNMENT

Pin No.	Pin Name	Description
1	$\overline{\text{ALERT}}$	$\overline{\text{ALERT}}$ Output. Open drain output that asserts low when the VR exceeds a programmable limit.
2	$\overline{\text{FAULT}}$	$\overline{\text{FAULT}}$ Output. Open drain output that asserts low when a fault has occurred. This fault can be due to VR or current limit, crowbar, or undervoltage. The trip points are loaded into registers.
3	SDA	Digital Input Output. I^2C serial data bidirectional pin. Requires pullup.
4	SCL	Digital Input. I^2C serial bus clock open drain input. Requires pullup.
5	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low.
6	GND	Ground. All internal biasing and the logic output signals of the device are referenced to this ground.
7	ADD/ VSENSE2	I^2C Address Input. Connect a resistor to ground to select one of 8 addresses. This input is reconfigured after startup as an analog voltage monitor, VSENSE2.
8	VSENSE1	Analog Input. Measures an input voltage between 0 and 2.0 V and reports this back over the I^2C interface.
9	IMON	Total Current Output Pin.
10	TTSENSE	VR Temperature Sense Input. An NTC thermistor between this pin and GND is used to remotely sense the temperature at the desired thermal monitoring point.
11	VRHOT	VR HOT Output. Open drain output that signals when the temperature at the monitoring point connected to TTSENSE exceeds the VRHOT temperature threshold.
12	IREF	Current Reference Input. An external resistor from this pin to ground sets the reference current for IFB, IILIMFS, and ITH(X).
13	RT	Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device.
14	RAMPADJ	PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp.
15	TRDET	Transient Detect. This output is asserted low whenever a load release is detected
16	FBRTN	Feedback Return. VID DAC and error amplifier reference for remote sensing of the output voltage.
17	COMP	Error Amplifier Output and Compensation Point.
18	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage. An external resistor between this pin and the output voltage sets the no load offset point.
19	CSREF	Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier and the Power−Good and crowbar functions. This pin should be connected to the common point of the output inductors.
20	CSSUM	Current Sense Summing Node. External resistors from each switch node to this pin sum the average inductor currents together to measure the total output current.
21	CSCOMP	Current Sense Compensation Point. A resistor and capacitor from this pin to CSSUM determines the gain of the current sense amplifier and the positioning loop response time.
22	ILIMFS	Current Sense and Limit Scaling Pin. An external resistor from this pin to CSCOMP sets the internal current sensing signal for current limit and IMON. This value can be over−written using I^2C interface.
23	$\overline{\text{ODN}}$	Output Disable Logic Output for $\overline{\text{PSI}}$ operation. This pin is actively pulled low when $\overline{\text{PSI}}$ is low, otherwise it functions in the same way as $\overline{\text{OD1}}$.
24	$\overline{\text{OD1}}$	Output Disable Logic Output. This pin is actively pulled low when the EN input is low or when V_{CC} is below its UVLO threshold to signal to the Driver IC that the driver high−side and low−side outputs should go low.
25 to 30	SW6 to SW1	Current Balance Inputs. Inputs for measuring the current level in each phase. The SW pins of unused phases should be left open.
31 to 36	PWM6 to PWM1	Logic−Level PWM Outputs. Each output is connected to the input of an external MOSFET driver such as the ADP3121. Connecting PWM6 to V_{CC} disables PWM6, connecting PWM5 to V_{CC} disables PWM5 and PWM6, etc. This means the ADP4000 can be setup to operate as a 1− 2−, 3−, 4−, 5−, or 6−phase controller.
37	VCC	Supply Voltage for the Device. A 340 Ω resistor should be placed between the 12 V system supply and the V_{CC} pin. The internal shunt regulator maintains V_{CC} = 5.0 V.
38 to 45	VID7 to VID0	Voltage Identification DAC Inputs. These eight pins are pulled down to GND, providing a logic zero if left open. When in normal operation mode, the DAC output programs the FB regulation voltage from 0.375 V to 1.6 V.
46	$\overline{\text{PSI}}$	Power State Indicator. Pulling this pin low places the controller in lower power state operation.
47	PWRGD	Power−Good Output. Open−drain output that signals when the output voltage is outside of the proper operating range.
48	VCC3	3.3 V Power Supply Output. A capacitor from this pin to ground provided decoupling for the interval 3.3 V LDO.

ELECTRICAL CHARACTERISTICS

V_{IN} = (5.0 V) FBRTN − GND, for typical values T_A = 25°C, for min/max values T_A = 0°C to 85°C; unless otherwise noted. (Notes 1 and 2)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Reference Current						
Reference Bias Voltage		V_{IREF}	1.75	1.8	1.85	V
Reference Bias Current	R_{IREF} = 121 kΩ	I_{IREF}		15		μA
Error Amplifier						
Output Voltage Range		V_{COMP}	0		4.4	V
Accuracy	Relative to nominal DAC output, referenced to FBRTN (see Figure 2) In startup	V_{FB} $V_{FB(BOOT)}$	−7 1.093	 1.1	+7 1.107	mV V
Load Line Positioning Accuracy			−77	−80	−83	mV
Load Line Range			−350		0	mV
Load Line Attenuation			0		100	%
Differential Non−linearity			−1.0		+1.0	LSB
Input Bias Current		I_{FB}	14.2	16	17.7	μA
Offset Accuracy	VR Offset Register = 111111, VID = 1.0 V VR Offset Register = 011111, VID = 1.0 V			−193.75 193.75		mV
FBRTN Current		I_{FBRTN}		100	200	μA
Output Current	FB forced to V_{OUT} −3%	I_{COMP}		500		μA
Gain Bandwidth Product	COMP = FB	$GBW_{(ERR)}$		20		MHz
Slew Rate	COMP = FB			25		V/μs
BOOT Voltage Hold Time	Internal Timer	t_{BOOT}		2.0		ms
VID Inputs						
Input Low Voltage	VID(X)	$V_{IL(VID)}$			0.3	V
Input High Voltage	VID(X)	$V_{IH(VID)}$	0.8			V
Input Current		$I_{IN(VID)}$		−5.0		μA
VID Transition Delay Time	VID code change to FB change		200			ns
No CPU Detection Turn−Off Delay Time	VID code change to PWM going low		5.0			μs
Oscillator						
Frequency Range		f_{OSC}	0.25		9.0	MHz
Frequency Variation	T_A = 25°C, R_T = 270 kΩ, 6−phase T_A = 25°C, R_T = 130 kΩ, 6−phase T_A = 25°C, R_T = 68 kΩ, 6−phase	f_{PHASE}	225	245 500 850	265	kHz
Output Voltage	RT = 500 kΩ to GND	V_{RT}	1.93	2.03	2.13	V
RAMPADJ Output Voltage	RAMPADJ − FB, V_{FB} = 1.0 V, IRAMPADJ = −150 μA	$V_{RAMPADJ}$	−50		+50	mV
RAMPADJ Input Current Range		$I_{RAMPADJ}$	5.0		60	μA
Current Sense Amplifier						
Offset Voltage	CSSUM − CSREF (see Figure 4)	$V_{OS(CSA)}$	−1.0	0	+1.0	mV
Input Bias Current, CSREF	CSREF = 1.0 V	$I_{BIAS(CSREF)}$	−20		+20	μA
Input Bias Current, CSSUM	CSREF = 1.0 V	$I_{BIAS(CSSUM)}$	−10		+10	nA
Gain Bandwidth Product	CSSUM = CSCOMP	$GBW_{(CSA)}$		10		MHz
Current Sense Amplifier						
Slew Rate	C_{CSCOMP} = 10 pF			10		V/μs
Input Common−Mode Range	CSSUM and CSREF		0		3.0	V
Output Voltage Range			0.05		3.0	V
Output Current		I_{CSCOMP}		500		μA

1. Refer to Absolute Maximum Ratings and Application Information for Safe Operating Area.
2. Guaranteed by design, not production tested.

ELECTRICAL CHARACTERISTICS

V_{IN} = (5.0 V) FBRTN − GND, for typical values T_A = 25°C, for min/max values T_A = 0°C to 85°C; unless otherwise noted. (Notes 1 and 2)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
$\overline{PSI}$						
Input Low Voltage					0.3	V
Input High Voltage			0.8			V
Input Current				−5		μA
Assertion Timing	Fsw = 300kHz			3.3		μs
Deassertion Timing	Fsw = 300kHz				825	ns
TRDET						
Output Low Voltage	I_{OUT} = −6 mA	V_{OL}		150	300	mV
IMON						
Clamp Voltage			1.0		1.15	V
Accuracy	10 x (CSREF − CSCOMP)/R_{ILIM}		−3.0		3.0	%
Output Current					800	μA
Offset			−5.5		5.5	mV
Current Limit Comparator						
I_{LIM} Bias Current	CSREF − CSCOMP)/R_{ILIM}, (CSREF − CSCOMP) = 150 mV, R_{ILIM} = 7.5 kΩ	I_{LIM}		22		μA
Current Limit Threshold Current	4/3 x I_{IREF}	I_{CL}		22		μA
Current Balance Amplifier						
Common−Mode Range		$V_{SW(X)CM}$	−600		+200	mV
Input Resistance	SW(X) = 0 V	$R_{SW(X)}$	12	18	21	kΩ
Input Current	SW(X) = 0 V	$I_{SW(X)}$	8.0	12	18	μA
Input Current Matching	SW(X) = 0 V	$\Delta I_{SW(X)}$	−6.0		+6.0	%
Phase Balance Adjustment Range Low	Phase Bal Registers = 00000			−25		%
Phase Balance Adjustment Range High	Phase Bal Registers = 11111			+25		%
Delay Timer						
Internal Timer	Delay Time Register = 011			2.0		ms
Timer Range Low	Delay Time Register = 000			0.5		ms
Timer Range High	Delay Time Register = 111			4.0		ms
Soft−Start						
Internal Timer	Soft−Start Slope Register = 010			0.5		V/ms
Timer Range Low	Soft−Start Slope Register = 000			0.1		V/ms
Timer Range High	Soft−Start Slope Register = 111			1.5		V/ms
Enable Input						
Input Low Voltage		$V_{IL(EN)}$			0.3	V
Input High Voltage		$V_{IH(EN)}$	0.8			V
Input Current		$I_{IN(EN)}$		−1.0		μA
Delay Time	EN > 0.8 V, Internal Delay	$t_{DELAY(EN)}$		2.0		ms
$\overline{ODN}$ and $\overline{OD1}$ Outputs						
Output Low Voltage	$I_{OD(SINK)}$ = −400 μA	$V_{OL(\overline{ODN/1})}$		160	500	mV
Output High Voltage	$I_{OD(SOURCE)}$ = 400 μA	$V_{OL(\overline{ODN/1})}$	4.0	5.0		V
$\overline{ODN}$ / $\overline{OD1}$ Pulldown Resistor				60		kΩ

1. Refer to Absolute Maximum Ratings and Application Information for Safe Operating Area.
2. Guaranteed by design, not production tested.

ELECTRICAL CHARACTERISTICS

V_{IN} = (5.0 V) FBRTN − GND, for typical values T_A = 25°C, for min/max values T_A = 0°C to 85°C; unless otherwise noted. (Notes 1 and 2)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Power−Good Comparator						
Undervoltage Threshold	Relative to Nominal DAC Output	$V_{PWRGD(UV)}$	−600	−500	−400	mV
Undervoltage Adjustment Range Low	PWRGD_LO Register = 000			−500		mV
Undervoltage Adjustment Range High	PWRGD_LO Register = 111			−150		mV
Overvoltage Threshold	Relative to DAC Output, PWRGD_Hi = 00	$V_{PWRGD(OV)}$	200	300	400	mV
Overvoltage Adjustment Range Low	PWRGD_Hi Register = 11			150		mV
Overvoltage Adjustment Range High	PWRGD_Hi Register = 00			300		mV
Output Low Voltage	$I_{PWRGD(SINK)}$ = −4 mA	$V_{OL(PWRGD)}$		150	300	mV
Power Good Delay Time						
During Soft−Start	Internal Timer			2.0		ms
VID Code Changing			100	250		μs
VID Code Static				200		ns
Crowbar Trip Point	Relative to DAC Output, PWRGD_Hi = 00	$V_{CROWBAR}$	200	300	400	mV
Crowbar Adjustment Range	PWRGD_Hi Register		150		300	mV
Crowbar Reset Point	Relative to FBRTN		250	300	350	mV
Crowbar Delay Time	Overvoltage to PWM going low	$t_{CROWBAR}$				
VID Code Changing			100	250		μs
VID Code Static				400		ns
PWM Outputs						
Output Low Voltage	$I_{PWM(SINK)}$ = −400 μA	$V_{OL(PWM)}$		160	500	mV
Output High Voltage	$I_{PWM(SOURCE)}$ = 400 μA	$V_{OH(PWM)}$	4.0	5.0		V
I²C Interface						
Logic High Input Voltage		$V_{IH(SDA,SCL)}$	2.1			V
Logic Low Input Voltage		$V_{IH(SDA,SCL)}$			0.8	V
Hysteresis				500		mV
SDA Output Low Voltage	I_{SDA} = −6 mA	V_{OL}			0.4	V
Input Current		V_{IH}; I_{IL}	−1		1.0	μA
Input Capacitance		$C_{SCL, SDA}$		5.0		pF
Clock Frequency		f_{SCL}			400	kHz
SCL Falling Edge to SDA Valid Time					1.0	μs
$\overline{\text{ALERT}}$, $\overline{\text{FAULT}}$ Outputs						
Output Low Voltage	I_{OUT} = −6 mA	V_{OL}			0.4	V
Output High Leakage Current	V_{OH} = 5.0 V	V_{OH}			1.0	μA
TTSENSE Inputs						
TTSENSE Voltage Range	Internally Limited		0		3.0	V
Source Current	R_{IREF} = 121 kΩ	I_{TH}	−110	−125	−140	μA
VRHOT Output Low Voltage	$I_{VRHOT(SINK)}$ = −4mA			150	300	mV
Input Voltage Conversion Range			0		2.0	V
ADC Resolution	LSB Weighting			2.0		mV
Analog / Digital Converter						
ADC Input Voltage Range			0		2.0	V
ADC Resolution				1.95		mV
Total Unadjusted Error (TUE)				1.0		%
Differential Non−linearity (DNL)	8 Bits			1.0		LSB

1. Refer to Absolute Maximum Ratings and Application Information for Safe Operating Area.
2. Guaranteed by design, not production tested.

ELECTRICAL CHARACTERISTICS

V_{IN} = (5.0 V) FBRTN − GND, for typical values T_A = 25°C, for min/max values T_A = 0°C to 85°C; unless otherwise noted. (Notes 1 and 2)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Analog / Digital Converter *cont.*						
Conversion Time, Voltage Channel	Averaging Enabled (32 averages)			80		ms
Round Robin Cycle Time				TBD		ms
ADD Input						
ADD Output Current	I_{ADD} = 2/3*I_{IREF}	I_{ADD}		10		μA
Address 000 Threshold					0.1	V
Address 001 Threshold			0.15		0.225	V
Address 010 Threshold			0.3		0.45	V
Address 011 Threshold			0.5		0.675	V
Address 100 Threshold			0.75		0.9	V
Address 101 Threshold			1.0		1.25	V
Address 110 Threshold			1.35		1.7	V
Address 111 Threshold			1.8			V
Supply						
V_{CC}	V_{CC}		4.7	5.25	5.75	V
DC Supply Current (see Figure 2)	V_{SYSTEM} = 13.2 V, R_{SHUNT} = 340 Ω	I_{VCC}		20	25	mA
UVLO Turn−On Current				6.5	11	mA
UVLO Threshold Voltage	V_{CC} Rising	V_{UVLO}	9.5			V
UVLO Turn−Off Voltage	V_{CC} Falling			4.1		V
VCC3 Output Voltage	I_{VCC3} = 1 mA	VCC3	3.0	3.3	3.6	V

1. Refer to Absolute Maximum Ratings and Application Information for Safe Operating Area.
2. Guaranteed by design, not production tested.

TYPICAL CHARACTERISTICS

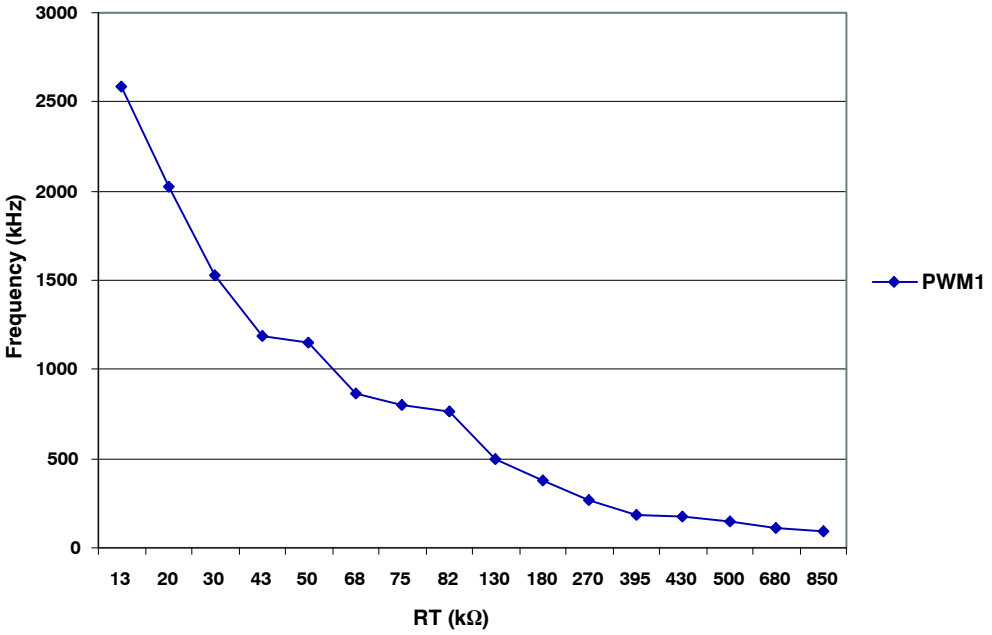


Figure 3. ADP4000 RT vs Frequency

TEST CIRCUITS

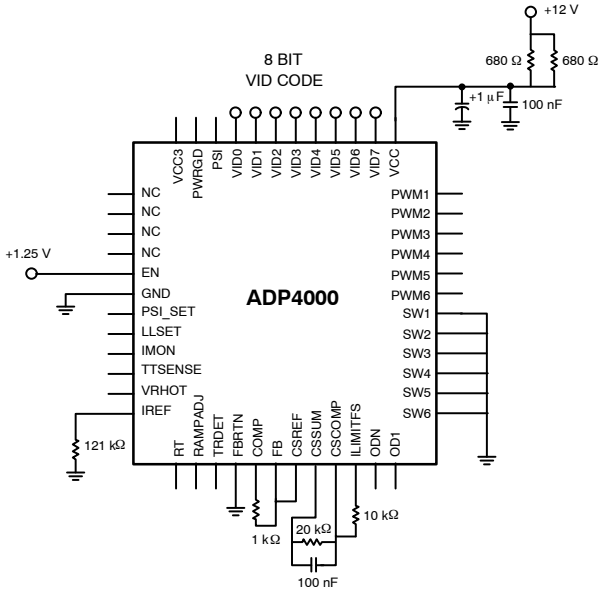


Figure 4. Closed-Loop Output Voltage Accuracy

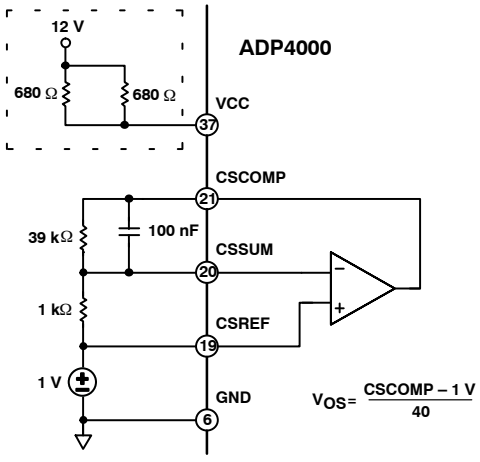


Figure 5. Current Sense Amplifier VOS

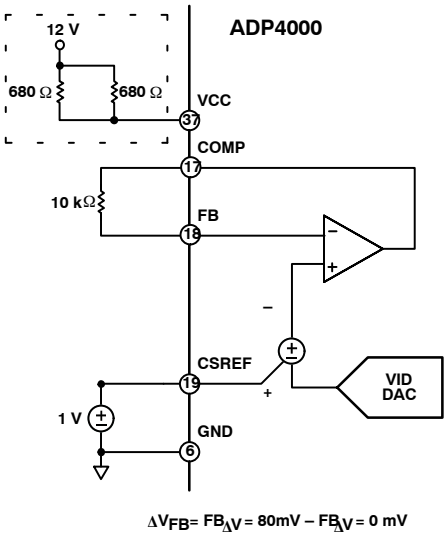


Figure 6. Positioning Voltage

Description

The ADP4000 is a 6−Phase VR11.1 regulator with an I^{2}C Interface Typical application circuits is shown in Figure 2.

Startup Sequence

The ADP4000 follows the VR11 startup sequence shown in Figure 7. After both the EN and UVLO conditions are met, a programmable internal timer goes through one delay cycle TD1. This delay cycle is programmed using Delay Command, default delay = 2 ms, see Table 1 for programmable values). The first six clock cycles of TD2 are blanked from the PWM outputs and used for phase detection as explained in the following section. Then the programmable internal soft−start ramp is enabled (TD2) and the output comes up to the boot voltage of 1.1 V. The boot hold time is also set by Delay Command. This second delay cycle is called TD3. During TD3 the processor VID pins settle to the required VID code. When TD3 is over, the ADP4000 reads the VID inputs and soft−starts either up or down to the final VID voltage (TD4). After TD4 has been completed and the PWRGD masking time (equal to VID on the fly masking) is finished, a third cycle of the internal timer sets the PWRGD blanking (TD5).

The internal delay and soft−start times are programmable using the serial interface and the Delay Command and the Soft−Start Commands.

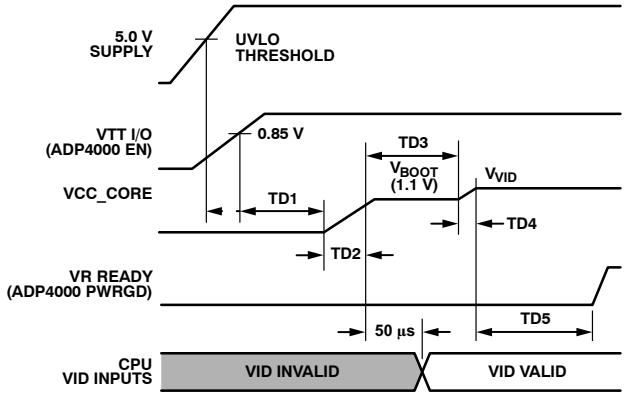


Figure 7. System Startup Sequence for VR11

Internal Delay Timer

An internal timer sets the delay times for the startup sequence, TD1, TD3 and TD5. The default time is 2msec, which can be changed using the I^{2}C interface. This timer is used for multiple delay timings (TD1, TD3 and TD5) during the startup sequence. Also, it is used for timing the current limit latchoff as explained in the Current Limit section. The current limit timer is set to 4 times the delay timer.

Table 1. Delay Codes

Code	Delay (msec)
000	0.5
001	1
010	1.5
011	2 = default
100	2.5
101	3
110	3.5
111	4

The delay timer is programmed using Bits <2:0> of the Ton Delay command (0xD4). The delay can be programmed between 0.5 msec and 4 msec. Table 1 provides the programmable delay times.

Soft−Start

The soft−start slope for the output voltage is set by an internal timer. The default value is 0.5 V/msec, which can be programmed through the I^{2}C interface. After TD1 and the phase detection cycle have been completed, the SS time (TD2 in Figure 7) starts. The SS circuit uses the internal VID DAC to increase the output voltage in 6.25 mV steps up to the 1.1 V boot voltage.

Once the SS circuit has reached the boot voltage, the boot voltage delay time (TD3) is started. The end of the boot voltage delay time signals the beginning of the second soft−start time (TD4). The SS voltage changes from the boot voltage to the programmed VID DAC voltage (either higher or lower) using 6.25 mV steps.

The soft−start slew rate is programmed using Bits <2:0> of the Ton_Rise (0xD5) command code. Table 2 provides the soft−start values.

Table 2. Slew Rate Codes

Code	Slew Rate (V/msec)
000	0.1
001	0.3
010	0.5 = default
011	0.7
100	0.9
101	1.1
110	1.3
111	1.5

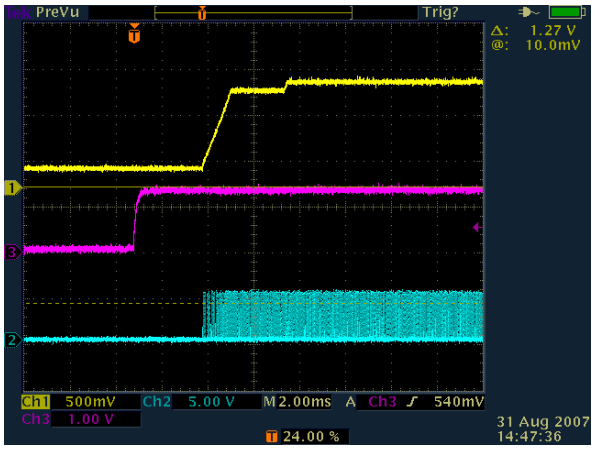


Figure 8. System Startup Sequence for VR11

Figure 8 shows typical startup waveforms for the ADP4000.

Figure 8. Typical Startup Waveforms
Channel 1: CSREF (yellow)
Channel 2: PWM1 (blue)
Channel 3 : Enable (pink)

Phase Detection

During startup, the number of operational phases and their phase relationship is determined by the internal circuitry that monitors the PWM outputs. Normally, the ADP4000 operates as a 6−phase PWM controller.

To operate as a 5−Phase Controller connect PWM6 to V_{CC}.

To operate as a 4−Phase Controller connect PWM5 and PWM6 to V_{CC}.

To operate as a 3−Phase Controller connect PWM4, PWM5 and PWM6 to V_{CC}.

To operate as a 2−Phase Controller connect PWM3, PWM4, PWM5 and PWM6 to V_{CC}.

To operate as a single−phase controller connect PMW2, PWM3, PWM4, PWM5 and PWM6 to V_{CC}.

Prior to soft−start, while EN is high the PWM6, PWM5, PWM4 PWM3 and PWM2 pins sink approximately 100 μA each. An internal comparator checks each pin's voltage vs. a threshold of 3.0 V. If the pin is tied to V_{CC}, it is above the threshold. Otherwise, an internal current sink pulls the pin to GND, which is below the threshold. PWM1 is low during the phase detection interval that occurs during the first six clock cycles of TD2. After this time, if the remaining PWM outputs are not pulled to V_{CC}, the 100 μA current sink is removed, and they function as normal PWM outputs. If they are pulled to V_{CC}, the 100 μA current source is removed, and the outputs are put into a high impedance state.

The PWM outputs are logic-level devices intended for driving fast response external gate drivers such as the ADP3121. Because each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one output can be on at the same time to allow overlapping phases.

Master Clock Frequency

The clock frequency of the ADP4000 is set with an external resistor connected from the RT pin to ground. The frequency follows the graph in Figure 3. To determine the frequency per phase, the clock is divided by the number of phases in use. If all phases are in use, divide by 6. If 4 phases are in use then divide by 4.

$$R_T = \frac{1}{n \times f_{SW} \times Cr} - R_{TO} \qquad \text{(eq. 1)}$$

where CT = 2.2 pF and RTO = 21 k

Output Voltage Differential Sensing

The ADP4000 combines differential sensing with a high accuracy VID DAC and reference, and a low offset error amplifier. This maintains a worst-case specification of ±7 mV differential sensing error over its full operating output voltage and temperature range. The output voltage is sensed between the FB pin and FBRTN pin. FB is connected through a resistor, R_B, to the regulation point, usually the remote sense pin of the microprocessor. FBRTN is connected directly to the remote sense ground point. The internal VID DAC and precision reference are referenced to FBRTN, which has a minimal current of 100 μA to allow accurate remote sensing. The internal error amplifier compares the output of the DAC to the FB pin to regulate the output voltage.

Output Current Sensing

The ADP4000 provides a dedicated current−sense amplifier (CSA) to monitor the total output current for proper voltage positioning vs. load current, for the IMON output and for current-limit detection. Sensing the load current at the output gives the total real time current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element such as the low-side MOSFET. This amplifier can be configured several ways, depending on the objectives of the system, as follows:

- Output inductor DCR sensing without a thermistor for lowest cost.
- Output inductor DCR sensing with a thermistor for improved accuracy with tracking of inductor temperature.
- Sense resistors for highest accuracy measurements.

The positive input of the CSA is connected to the CSREF pin, which is connected to the average output voltage. The inputs to the amplifier are summed together through resistors from the sensing element, such as the switch node side of the output inductors, to the inverting input CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the feedback resistor. This difference signal is used internally to offset the VID DAC for voltage positioning. This difference signal can be adjusted between 50% and 150% of the external value

using the I^{2}C Loadline Calibration (0xDE) and Loadline Set (0xDF) commands.

The difference between CSREF and CSCOMP is used as a differential input for the current-limit comparator.

To provide the best accuracy for sensing current, the CSA is designed to have a low offset input voltage. Also, the sensing gain is determined by external resistors to make it extremely accurate.

The CPU current can also be monitored over the I^{2}C interface. The current limit and the load line can be adjusted from the circuit component values over the I^{2}C interface.

Current Limit Setpoint

The current limit threshold on the ADP4000 is programmed by a resistor between the ILIMFS pin and the CSCOMP pin. The ILIMFS current, I_{ILIMFS}, is compared with an internal current reference of 22 μA. If I_{ILIMFS} exceeds 22 μA then the output current has exceeded the limit and the current limit protection is tripped.

Where $V_{ILIMFS} = V_{CSREF}$

$$I_{ILIMFS} = \frac{V_{ILIMFS} - V_{CSCOMP}}{R_{ILIMFS}} \quad \text{(eq. 2)}$$

$$V_{CSREF} - V_{CSCOMP} = \frac{R_{CS}}{R_{PH}} \times R_L \times I_{LOAD} \quad \text{(eq. 3)}$$

Where R_L = DCR of the Inductor.

Assuming that

$$\frac{R_{CS}}{R_{PH}} \times R_L = 1\ m\Omega \quad \text{(eq. 4)}$$

i.e. the external circuit is set up for a 1mΩ Loadline then the R_{ILIMFS} is calculated as follows

$$I_{ILIMFS} = \frac{1\ m\Omega \times I_{LOAD}}{R_{ILIMITFS}} \quad \text{(eq. 5)}$$

Assuming we want a current limit of 150A that means that I_{LIMFS} must equal 22 μA at that load.

$$20\ \mu A = \frac{1\ m\Omega \times 150\ AD}{R_{ILIMITFS}} = 6.8\ k\Omega \quad \text{(eq. 6)}$$

Solving this equation for $R_{LIMITFS}$ we get 6.8 kΩ. The closest 1% resistor value is 6.8 kΩ.

The current limit threshold can be modified from the resistor programmed value by using the I^{2}C interface using Bits <4:0> of the Current Limit Threshold command (0xE2). The limit is programmable between 50% of the external limit and 146.7% of the external limit. The resolution is 3.3%. Table 3 gives some examples codes.

Table 3. Current Limit

Code	Current Limit (% of external limit)
0 0000	50%
0 0001	53.3%
1 0000	100% = default
1 0001	103.3%
1 1110	143.3%
1 1111	146.7%

Current Limit, Short−Circuit and Latchoff protection

If the current limit is reached and TD5 has completed the controller will start to latchoff. If there is a current limit during startup, the ADP4000 will go through TD1 to TD5, and then start the latchoff. Because the controller continues to cycle the phases during the latchoff, if the short is removed before the timer is complete, the controller can return to normal operation.

The latchoff function can be reset by either removing and reapplying the supply voltage to the ADP4000, or by toggling the EN pin low for a short time.

During startup when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot go below ground. This secondary current limit limits the internal COMP voltage to the PWM comparators to 1.5 V. This limits the voltage drop across the low-side MOSFETs through the current balance circuitry. Typical over-current latchoff waveforms are shown in Figure 9.

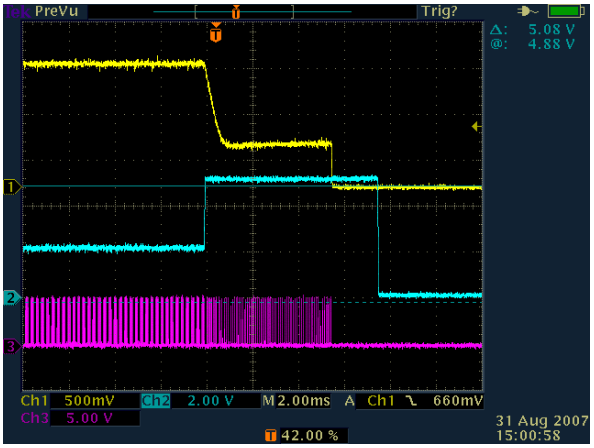


Figure 9. Overcurrent Latchoff Waveforms Channel 1: CSREF, Channel 2: COMP, Channel 3: PWM1

An inherent per phase current limit protects individual phases if one or more phases stops functioning because of a faulty component. This limit is based on the maximum normal mode COMP voltage.

Output Current Monitor

I_{MON} is an analog output from the ADP4000 representing the total current being delivered to the load. It outputs an accurate current that is directly proportional to the current set by the ILIMFS resistor.

$$I_{IMON} = 10 \times I_{ILIMFS} \quad \text{(eq. 7)}$$

The current is then run through a parallel RC connected from the I_{MON} pin to the FBRTN pin to generate an accurately scaled and filtered voltage as per the VR11.1 specification. The size of the resistor is used to set the I_{MON} scaling.

The scaling is set such that I_{MON} = 900mV at the TDC current of the processor. This means that the R_{IMON} resistor should be chosen as follows.

From the Current Limit Setpoint paragraph we know the following:

$$I_{ILIMFS} = \frac{1\ m\Omega \times I_{LOAD}}{R_{ILIMFS}} \quad \text{(eq. 8)}$$

$$I_{IMON} = 10 \times \frac{1\ m\Omega \times I_{LOAD}}{R_{ILIMFS}} \quad \text{(eq. 9)}$$

For a 150 A current limit R_{LIMFS} = 7.5 kΩ. Assuming the TDC = 135 A then V_{MON} should equal 900 mV when I_{LOAD} = 135 A.

When I_{LOAD} = 135A, I_{MON} equals

$$I_{IMON} = 10 \times \frac{1\ m\Omega \times 135\ A}{6.81\ k\Omega} = 198\ \mu A \quad \text{(eq. 10)}$$

$$V_{IMON} = 900\ mV = 198\ \mu A \times R_{MON} \quad \text{(eq. 11)}$$

This gives a value of 4.54 kΩ for R_{MON}.

If the TDC and OCP limit for the processor have to be changed then it may be necessary to change the ILIMITFS resistor only. This is because the ILIMITFS resistor sets up both the current limit and also the current out of the I_{MON} pin, as explained earlier.

The I_{MON} pin also includes an active clamp to limit the I_{MON} voltage to 1.15 V MAX while maintaining accuracy at 900 mV full scale.

Active Impedance Control Mode

For controlling the dynamic output voltage droop as a function of output current, the CSA gain and load line programming can be scaled to be equal to the droop impedance of the regulator times the output current. This droop voltage is then used to set the input control voltage to the system. The droop voltage is subtracted from the DAC reference input voltage directly to tell the error amplifier where the output voltage should be. This allows enhanced feed-forward response.

Load Line Setting

The Loadline is programmable over the I^2C interface on the ADP4000. It is programmed using the Loadline Calibration (0xDE) and Loadline Set (0xDF) commands. The loadline can be adjusted between 0% and 100% of the external R_{CSA}. In this example R_{CSA} = 1 mΩ. R_O needs to 0.8 mΩ. Therefore programming the Loadline Calibration + Loadline Set Register to give a combined percentage of 80% will set the R_O to 0.8 mΩ.

Table 4. Loadline Commands

Code	Loadline (as a percentage of R_{CSA})
0 0000	0%
0 0001	3.3%
1 0000	50% = default
1 0001	53.3%
1 1110	96.7%
1 1111	100%

Current Control Mode and Thermal Balance

The ADP4000 has individual inputs (SW1 to SW6) for each phase that are used for monitoring the current of each phase. This information is combined with an internal ramp to create a current balancing feedback system that has been optimized for initial current balance accuracy and dynamic thermal balancing during operation. This current balance information is independent of the average output current information used for positioning as described in the section.

The magnitude of the internal ramp can be set to optimize the transient response of the system. It also monitors the supply voltage for feed-forward control for changes in the supply. A resistor connected from the power input voltage to the RAMPADJ pin determines the slope of the internal PWM ramp.

The balance between the phases can be programmed using the I^2C Phase Bal SW(x) commands (0xE3 to 0xE8). This allows each phase to be adjusted if there is a difference in temperature due to layout and airflow considerations. The phase balance can be adjusted from a default gain of 5 (Bits 4:0 = 10000). The minimum gain programmable is 3.75 (Bits 4:0 = 00000) and the max gain is 6.25 (Bits 4:0 = 11111).

Voltage Control Mode

A high gain, high bandwidth, voltage mode error amplifier is used for the voltage mode control loop. The control input voltage to the positive input is set via the VID logic according to the voltages listed in VID Code Table. The VID code is set using the VID Input pins or it can be programmed over the I^2C interface using the V_{OUT}_Command. By default, the ADP4000 outputs a voltage corresponding to the VID Inputs. To output a voltage following the V_{OUT}_Command the user first needs to program the required VID Code. Then the VID_EN Bits need to be enabled. The following is the sequence:

1. Program the required VID Code to the V_{OUT}_Command code (0x21)
2. Set the VID_EN bit (Bit 3) in the VR Config 1 A (0xD2) and on the VR Config 1B (0xD3).

This voltage is also offset by the droop voltage for active positioning of the output voltage as a function of current,

commonly known as active voltage positioning. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (FB) is tied to the output sense location with Resistor R_B and is used for sensing and controlling the output voltage at this point. A current source (equal to I_{FB}) from the FB pin flowing through R_B is used for setting the no load offset voltage from the VID voltage. The no load voltage is negative with respect to the VID DAC for Intel CPU's.

The value of R_B can be found using the following equation:

$$R_B = \frac{V_{VID} - V_{ONL}}{I_{IFB}} \quad \text{(eq. 12)}$$

An offset voltage can be added to the control voltage over the serial interface. This is done using Bits <5:0> of the V_{OUT}_TRIM (0xDB) and V_{OUT}_CAL (0xDC) Commands. The max offset that can be applied is ±193.75 mV (even if the sum of the offsets > 193.75mV). The LSB size is 6.25 mV. A positive offset is applied when Bit 5 = 0. A negative offset is applied when Bit 5 = 1.

Table 5. Offset Codes

VOUT_ TRIM CODE	TRIM OFFSET VOLTAGE	VOUT_ CAL CODE	CAL OFFSET VOLTAGE	TOTAL OFFSET VOLTAGE
00 1000	50 mV	00 0010	12.5 mV	62.5 mV
10 0001	-6.25 mV	10 1110	-87.5 mV	-93.75 mV
00 1111	93.75 mV	10 0001	-6.25 mV	87.5 mV

RAMPADJ Input Current

The resistor connected to the Rampadj pin sets the internal PWM ramp. The value for this resistor is chosen to provide the combination of thermal balance, stability and transient response.

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R} \quad \text{(eq. 13)}$$

Where

A_R is the internal ramp amplifier gain (= 0.5)

A_D is the current balancing amplifier gain (= 5)

R_{DS} is the total low side MOSFET on resistance

C_R is the internal ramp capacitor value (= 5pF).

The internal ramp voltage can be calculated as follows:

$$V_R = \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} \quad \text{(eq. 14)}$$

The size of the internal ramp can be made larger or smaller. If it is made larger, stability and noise rejection improves but the transient performance decreases. If the ramp is made smaller then the transient response improves however noise rejection and stability degrades.

COMP Pin Ramp

There is a ramp signal on the COMP signal, which is due to the droop voltage and the output voltage ramps. This ramp adds to the internal ramp to produce the following ramp signal at the PWM input.

$$V_{RT} = \frac{V_R}{\left(1 - \frac{2 \times (1 - n \times D)}{n \times f_{SW} \times C_X \times R_O}\right)} \quad \text{(eq. 15)}$$

Where Cx = bulk capacitance

R_O = Droop

n = number of phases

f_{SW} = switching frequency per phase

D = duty cycle

V_R = Internal Ramp Voltage (calculated in Rampadj section of this data sheet)

This ramp voltage should be set to at least 0.5 V for noise immunity reasons. If it is less than 0.5 V then decrease the ramp resistor.

Dynamic VID

The ADP4000 has the ability to respond to dynamically changing VID inputs while the controller is running. This allows the output voltage to change while the supply is running and supplying current to the load. This is commonly referred to as Dynamic VID (DVID). A DVID can occur under either light or heavy load conditions. The processor signals the controller by changing the VID inputs (or by programming a new V_{OUT}_Command) in a single or multiple steps from the start code to the finish code. This change can be positive or negative.

When a VID bit changes state, the ADP4000 detects the change and ignores the DAC inputs for a minimum of 200 ns. This time prevents a false code due to logic skew while the VID inputs are changing. Additionally, the first VID change initiates the PWRGD and CROWBAR blanking functions for a minimum of 100 μs to prevent a false PWRGD or CROWBAR event. Each VID change resets the internal timer.

If a VID off code is detected the ADP4000 will wait for 5 μsec to ensure that the code is correct before initiating a shutdown of the controller.

The ADP4000 also uses the TON_Transition command code (0xD6) to limit the DVID slew rates. These can be encountered when the system does a large single VID step for power state changes, thus the DVID slew rate needs to be limited to prevent large inrush currents.

The transition slew rate is programmed using Bits <2:0> of the Ton_Transition (0xD6) command code. Table 6 provides the soft−start values.

Table 6. Transition Rate Codes

Code	Transition Rate (V/msec)
000	1
001	3 = default
010	5
011	7
100	9
101	11
110	13
111	15

Enhanced Transients Mode

The ADP4000 incorporates enhanced transient response for both load step up and load release. For load step up it senses the output of the error amp to determine if a load step up has occurred and then sequences on the appropriate number of phases to ramp up the output current.

For load release, it also senses the output of the error amp and uses the load release information to trigger the TRDET pin, which is then used to adjust the error amp feedback for optimal positioning. This is especially important during high frequency load steps.

Additional information is used during load transients to ensure proper sequencing and balancing of phases during high frequency load steps as well as minimizing the stress on components such as the input filter and MOSFET's.

TRDET and Phase Shuffling

The ADP4000 senses the error amp output and triggers the TRDET pin when a load release takes place. The TRDET circuit, as shown in Figure 2, adjusts the feedback for optimal positioning especially during high frequency load steps. TRDET is also used to trigger phase shuffling. If repeated transients take place at the switching frequency then its possible for one phase to carry most of the currrent. To prevent this from happening the ADP4000 will shuffle the phases whenever a load release happens, i.e. it will randomize the phase sequence.

Reference Current

The IREF pin is used to set an internal current reference. This reference current sets I_{FB} and $I_{TTSENSE}$. A resistor to ground programs the current based on the 1.8 V output.

$$I_{REF} = \frac{1.8\ V}{R_{IREF}} \qquad \text{(eq. 16)}$$

Typically, R_{IREF} is set to 121 kΩ to program I_{REF} = 15 μA. The following currents are then equal to

$$I_{FB} = \frac{16}{15} \times I_{REF} = 16\ \mu A$$
$$I_{TTSENSE} = -8\ (IREF) = -120\ \mu A \qquad \text{(eq. 17)}$$

Power Good Monitoring

The power good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open-drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage is within the nominal limits specified in the specifications above based on the VID voltage setting. PWRGD goes low if the output voltage is outside of this specified range, if the VID DAC inputs are in no CPU mode, or whenever the EN pin is pulled low. PWRGD is blanked during a DVID event for a period of 100 μs to prevent false signals during the time the output is changing.

The PWRGD circuitry also incorporates an initial turn-on delay time (TD5). Prior to the SS voltage reaching the programmed VID DAC voltage and the PWRGD masking time finishing, the PWRGD pin is held low. Once the SS circuit reaches the programmed DAC voltage, the internal timer operates.

The default range for the PWRGD comparator is +300 mV and −500 mV. However these values can be adjusted over the I^2C. The high limit is programmed using Bits <1:0> of Command Code 0xE0 and the low limit is programmed using Bits <2:0> of Command code 0xE1. The following is a table of the programmable values.

Table 7. PWRGD High Limits

Code	PWRGD High Limits
00	+300mV (default)
01	+250 mV
10	+200 mV
11	+150 mV

Table 8. PWRGD Low Limits

Code	PWRGD Low Limits
000	-500mV (default)
001	-450 mV
010	-400 mV
011	-350 mV
100	-300 mV
101	-250 mV
110	-200 mV
111	-150 mV

Power State Indicator

The $\overline{PSI}$ pin is an input used to determine the operating state of the load. If this input is pulled low, the load is in a low power state and the controller asserts the $\overline{ODN}$ pin low, which can be used to disable phases and maintain better efficiency at lighter loads.

The sequencing into and out of low power operation is maintained to minimize output deviations as well as providing full power load transients immediately after exiting a low power state.

The user can program how many phases are enabled when $\overline{PSI}$ is asserted. By default only phase 1 is enabled. The number of phases enabled can be changed over the I^2C interface. However extreme care should be taken to ensure that $\overline{OD1}$ is connected to all phases enabled during $\overline{PSI}$. The number of phases enabled during $\overline{PSI}$ is programmed using Bits 7 and 6 of the MFR Config Command (0xD1)

Table 9. # Phases Enabled During $\overline{PSI}$

# of Phases Running Normally	Code	# of Phases Running During $\overline{PSI}$	Phases Running
6	00	1	1
	01	2	1 and 4
	10	3	1, 3 and 5
	11	1	1
5	00	1	1
	01	2	1 and 4
	10	1	1
	11	1	1
4	00	1	1
	01	2	1 and 3
	10	1	1
	11	1	1
3	00	1	1
	01	1	1
	10	1	1
	11	1	1
2	00	1	1
	01	1	1
	10	1	1
	11	1	1
1	00	1	1
	01	1	1
	10	1	1
	11	1	1

The actual phases enabled depend upon how many phases are enabled for normal operation. For example if 4 phases are enabled normally and 2 during $\overline{PSI}$, then Phase 1 and Phase 3 will be enabled during $\overline{PSI}$.

Output Crowbar

As part of the protection for the load and output components of the supply, the PWM outputs are driven low (turning on the low-side MOSFETs) when the output voltage exceeds the upper crowbar threshold. This crowbar action stops once the output voltage falls below the release threshold of approximately 300 mV.

The value for the crowbar limit follows the programmable PWRGD high limit.

Turning on the low-side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output overvoltage is due to a short in the high−side MOSFET, this action current-limits the input supply or blows its fuse, protecting the microprocessor from being destroyed.

Output Enable and UVLO

For the ADP4000 to begin switching, the input supply current to the controller must be higher than the UVLO threshold and the EN pin must be higher than its 0.8 V threshold. This initiates a system startup sequence. If either UVLO or EN is less than their respective thresholds, the ADP4000 is disabled. This holds the PWM outputs at ground and forces PWRGD, $\overline{ODN}$ and $\overline{OD1}$ signals low.

In the application circuit (see Figure 2), the $\overline{OD1}$ pin should be connected to the $\overline{OD}$ inputs of the external drivers for the phases that are always on. The $\overline{ODN}$ pin should be connected to the $\overline{OD}$ inputs of the external drivers on the phases that are shut down during low power operation. Grounding the driver $\overline{OD}$ inputs disables the drivers such that both DRVH and DRVL are grounded. This feature is important in preventing the discharge of the output capacitors when the controller is shut off. If the driver outputs are not disabled, a negative voltage can be generated during output due to the high current discharge of the output capacitors through the inductors.

Thermal Monitoring

The ADP4000 includes a thermal monitoring channel using a thermistor. Temperature trip points can be set for $\overline{ALERT}$ and $\overline{FAULT}$ levels through the I^2C interface. Also, the temperature values can be read back over the I^2C interface.

The VR thermal monitoring circuits require an NTC thermistor to be placed from TTSENSE to GND. For best accuracy, the thermistors can be linearized using resistors. A fixed current of 8 times IREF (normally giving 120 μA) is sourced out of the TTSENSE pin into the thermistor. When the TTSENSE temperature exceeds the OT Fault Limit (0x51), VRHOT is asserted.

The temperature value is reported back in the Read_Temperature1 command. The ADP4000 measures the voltage on the TTSENSE pin and calculates the temperature using the following formula:

Read_Temperature_1 = (TTSENSE Voltage)*TTSENSE Gain + TTSENSE Offset.

The TTSENSE Gain and Offset factors depend upon the combination of thermistor and linearizing register used in the circuit and can be programmed by the user using commands TTSENSE Gain (addr = 0xF7) and TTSENSE Offset (addr = 0xF8). The default values in the ADP4000 are for a 100 k Thermistor and a 20 k Linearizing resistor. If the user would like to measure the voltage directly then the TTSENSE Gain should be programmed to 1 and the Offset should be programmed to 0.

Voltage Monitoring

The ADP4000 can monitor up to three voltages. It can monitor the voltage on the EN pin and reports this back in a register. It can also monitor the voltage on the VSENSE1 and the VSENSE2 pins and report these back in registers over I^2C. The ADC range for the voltage measurements is

0 V to 2.0 V. Voltages greater than 2.0 V can monitored using a resistor divider network. Voltage measurements are 10 bits wide.

Vsense1 is intended to measure the input voltage and report this back in the READ_VIN command. However the input voltage is typically 12 V and the ADC range is only 0 V to 2.0 V. Therefore an external resistor divided is needed, the ADP4000 assumes that an 8−1 resistor divider is used, the ADP4000 measures the voltage on the pin and multiples by 8 and places the result in the Read V_{in} register. The circuit in Figure 2 uses a 6.8 K and a 1.0 k resistor to divide the input voltage by 8.

Shunt Resistor

The ADP4000 uses a shunt to generate 5.0 V from the 12 V supply range. A trade-off can be made between the power dissipated in the shunt resistor and the UVLO threshold. Figure 10 shows the typical resistor value needed to realize certain UVLO voltages. It also gives the maximum power dissipated in the shunt resistor for these UVLO voltages.

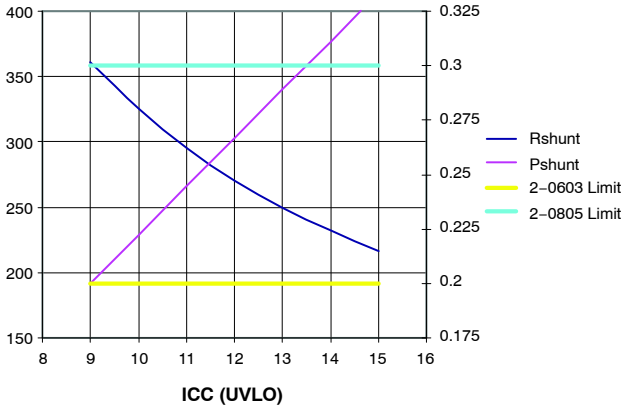


Figure 10. Typical Shunt Resistor Value and Power Dissipation for Different UVLO Voltage

The maximum power dissipated is calculated using the Equation 18.

$$P_{MAX} = \frac{\left(V_{IN(MAX)} - V_{CC(MIN)}\right)^2}{R_{SHUNT}} \qquad \text{(eq. 18)}$$

where:

$V_{IN(MAX)}$ is the maximum voltage from the 12 V input supply (if the 12 V input supply is 12 V ±5%, $V_{IN(MAX)}$ = 12.6 V; if the 12 V input supply is 12 V ±10%, $V_{IN(MAX)}$ = 13.2 V). $V_{CC(MIN)}$ is the minimum V_{CC} voltage of the ADP4000. This is specified as 4.75 V.

R_{SHUNT} is the shunt resistor value.

The CECC standard specification for power rating in surface-mount resistors is: 0603 = 0.1 W, 0805 = 0.125 W, 1206 = 0.25 W.

I²C Interface

Control of the ADP4000 is carried out using the I²C Interface.

The ADP4000 is connected to this bus as a slave device, under the control of a master controller.

To setup the I²C Address the ADP4000 sources a 10 μA current from the ADD pin through an external resistor. The voltage is then measured by the ADC and user to set the I²C address. The table below gives the thresholds for each possible I²C address.

Table 10. Setting Up the I²C Address

Address (8 Bits)	High Threshold	Low Threshold
0xC0	0.1	–
0xC2	0.225	0.15
0xC4	0.45	0.3
0xC6	0.675	0.5
0xC8	0.9	0.75
0xCA	1.25	1.0
0xCC	1.7	1.35
0xCE	–	1.8

Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low−to−high transition when the clock is high might be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

1. When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the tenth clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse; this is known as No Acknowledge. The master takes the data line low during the low period before the tenth clock pulse, and then high during the tenth clock pulse to assert a stop condition.
   Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.
   In the ADP4000, write operations contain one, two or three bytes, and read operations contain one or two bytes. The command code or register address

determines the number of bytes to be read or written, See the register map for more information.

To write data to one of the device data registers or read data from it, the address pointer register must be set so that the correct data register is addressed (i.e. command code), and then data can be written to that register or read from it. The first byte of a read or write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register.

This write byte operation is shown in Figure 12. The device address is sent over the bus, and then R/$\overline{W}$ is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

2. The read byte operation is shown in Figure 13. First the command code needs to be written to the ADP4000 so that the required data is sent back. This is done by performing a write to the ADP4000 as before, but only the data byte containing the register address is sent, because no data is written to the register. A repeated start is then issued and a read operation is then performed consisting of the serial bus address; R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register.
3. It is not possible to read or write a data byte from a data register without first writing to the address pointer register, even if the address pointer register is already at the correct value.
4. In addition to supporting the send byte, the ADP4000 also supports the read byte, write byte, read word and write word protocols.

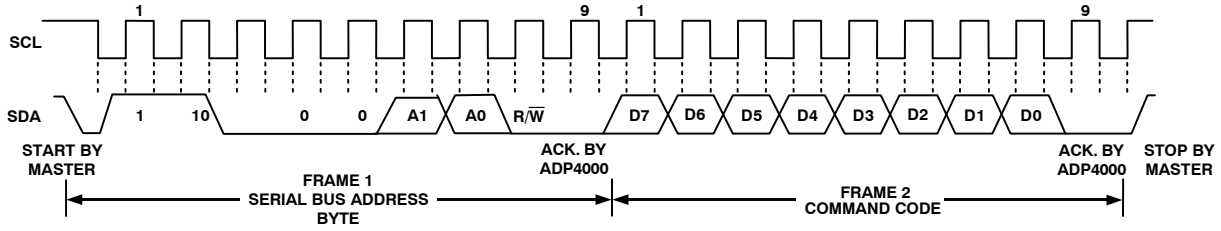


Figure 11. Send Byte

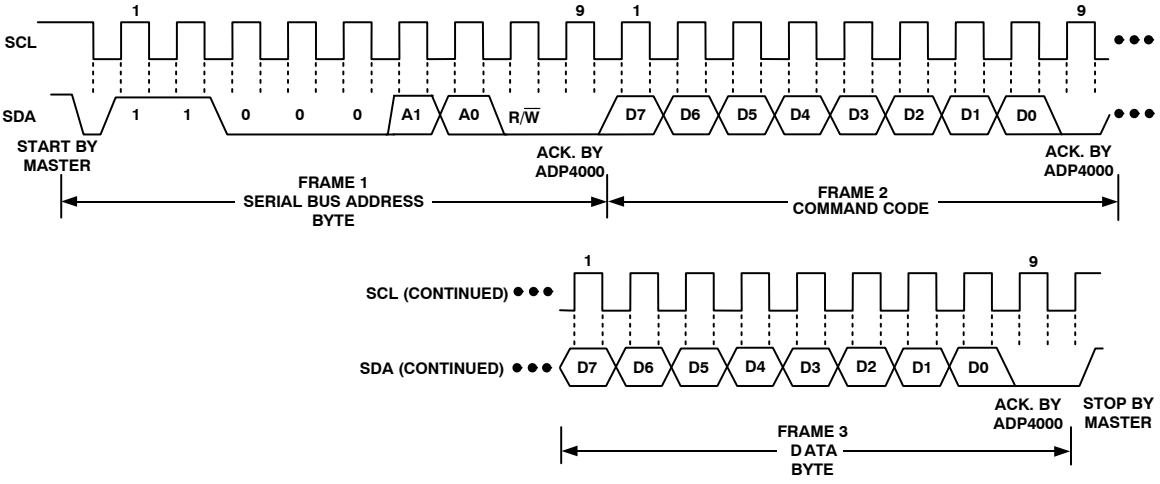


Figure 12. Write Byte

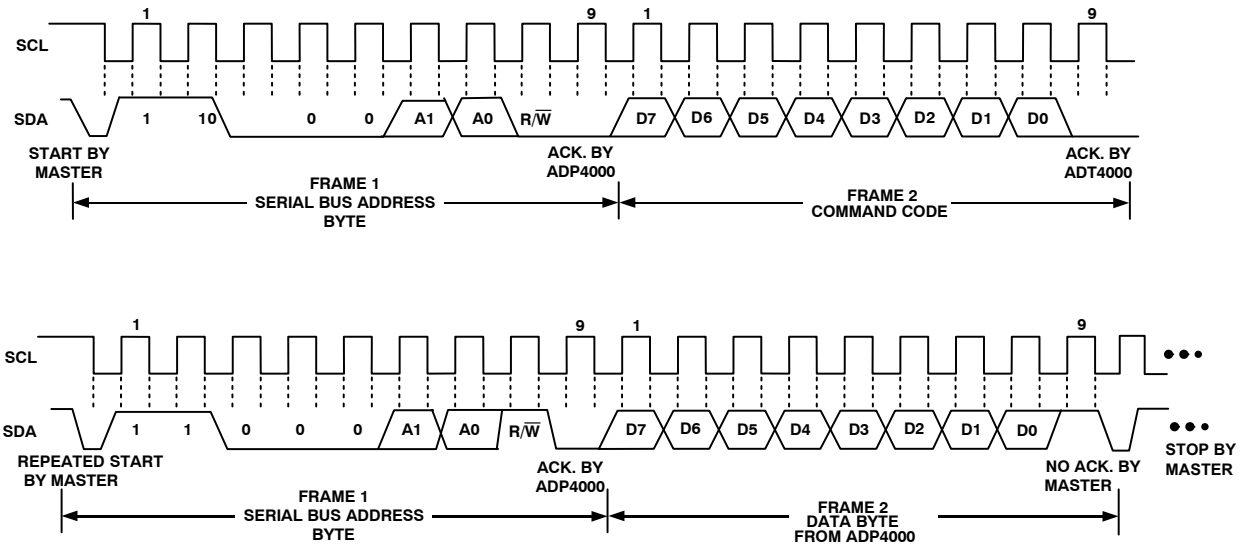


Figure 13. Read Byte

Write Operations

The following abbreviations are used in the diagrams:

S−START
P−STOP
R−READ
W−WRITE
A−ACKNOWLEDGE
$\overline{A}$−NO ACKNOWLEDGE

The ADP4000 uses the following I^2C write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA and the transaction ends.

For the ADP4000, the send byte protocol is used to clear Faults. This operation is shown in Figure 14.

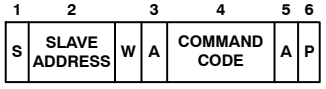


Figure 14. Send Byte Command

If the master is required to read data from the register immediately after setting up the address, it can assert a repeat start condition immediately after the final ACK and carry out a single byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master asserts a stop condition on SDA and the transaction ends.

The byte write operation is shown in Figure 15.

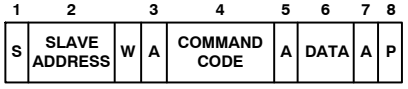


Figure 15. Single Byte Write to a Register

Write Word

In this operation, the master device sends a command byte and two data bytes to the slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends the first data byte.
7. The slave asserts ACK on SDA.
8. The master sends the second data byte.
9. The slave asserts ACK on SDA.

10. The master asserts a stop condition on SDA and the transaction ends.

The word write operation is shown in Figure 16.

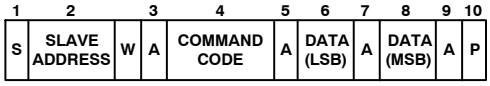


Figure 16. Single Word Write to a Register

Block Write

In this operation, the master device sends a command byte and a byte count followed by the stated number of data bytes to the slave device as follows:

1. The master device asserts a START condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends the byte count N.
7. The slave asserts ACK on SDA.
8. The master sends the first data byte.
9. The slave asserts ACK on SDA.
10. The master sends the second data byte.
11. The slave asserts ACK on SDA.
12. The master sends the remainder of the data byes.
13. The slave asserts an ACK on SDA after each data byte.
14. After the last data byte the master asserts a STOP condition on SDA.

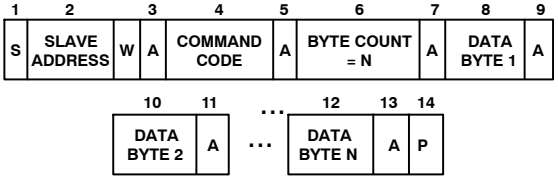


Figure 17. Block Write to a Register

Read Operations

The ADP4000 uses the following I^2C read protocols.

Read Byte

In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserted ACK on SDA.
6. The master sends a repeated start condition on SDA.
7. The master sends the 7 bit slave address followed by the read bit (high).
8. The slave asserts ACK on SDA.
9. The slave sends the Data Byte.
10. The master asserts NO ACK on SDA.
11. The master asserts a stop condition on SDA and the transaction ends.

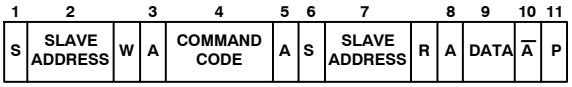


Figure 18. Single Read from a Register

Read Word

In this operation, the master device receives two data bytes from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserted ACK on SDA.
6. The master sends a repeated start condition on SDA.
7. The master sends the 7 bit slave address followed by the read bit (high).
8. The slave asserts ACK on SDA.
9. The slave sends the first Data Byte (low Data Byte).
10. The master asserts ACK on SDA.
11. The slave sends the second Data Byte (high Data Byte).
12. The masters asserts a No ACK on SDA.
13. The master asserts a stop condition on SDA and the transaction ends.

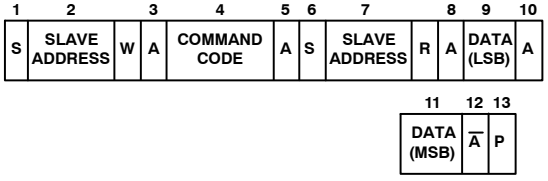


Figure 19. Word Read from a Command Code

Block Read

In this operation, the master device sends a command byte, the slave sends a byte count followed by the stated number of data bytes to the master device as follows:

1. The master device asserts a START condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a REPEATED START condition on SDA.
5. The master sends the 7-bit slave address followed by the read bit (high).
6. The slave asserts ACK on SDA
7. The slave sends the byte count N.

8. The master asserts ACK on SDA.
9. The slave sends the first data byte
10. The master asserts ACK on SDA.
11. The slave sends the remainder of the data byes, the master asserts an ACK on SDA after each data byte.
12. After the last data byte the master asserts a No ACK on SDA.
13. The master asserts a STOP condition on SDA.

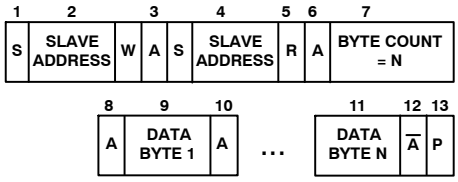


Figure 20. Block Write to a Command Coder

Bus Timeout

The ADP4000 includes an I^{2}C timeout feature. If there is no I^{2}C activity for 35 ms, the ADP4000 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the I^{2}C expecting data. The timeout feature can be disabled.

Configuration Register 1 (0xTBD)

Bit 3 BUS_TO_EN = 1; bus timeout enabled.

Bit 3 TODIS = 0; I^{2}C timeout disabled (default).

Virus Protection

To prevent rogue programs or viruses from accessing critical ADP4000 register settings, the lock bit can be set. Setting Bit 0 of the Lock/Reset sets the lock bit and locks critical registers. In this mode, certain registers can no longer be written to until the ADP4000 is powered down and powered up again. For more information on which registers are locked see the register map.

ON_OFF_Config Command

The I^{2}C interface has an ON_OFF_Config which allows the user to configure when the ADP4000 should start and stop switching. There two control inputs, the EN input (specified as per VR11.1) and the Operation Command. The user can program the ADP4000 to respond to or ignore each of the control inputs. The default configuration is the EN pin is acted on, and the Operation Command is ignored. The EN pin is active high by default but can be programmed to be active low over I^{2}C. The details of the individual bits can be found in the description for Command Code 0x02 (ON_OFF_Config) in Table 11.

Operation Command

The operation command, when enabled in the ON_OFF_Config command, can be used to start and stop the ADP4000 switching. The options available described in the Operation Command (0x01) in Table 11. There are two options for turning off, soft off and immediate off. There are three options for turning on. The first is ON, where the output voltage is soft started towards the Boot Voltage and then to the VID Voltage (same startup sequence as toggling EN). The other two options are margin high and margin low. When these options are selected the output voltage will settle on the VOUT_MARGIN_HIGH VID Code (0x25) or the VOUT_MARGIN_LOW VID Code (0x26).

Limits, $\overline{\text{ALERT}}$s, and $\overline{\text{FAULT}}$s

The ADP4000 monitors a number of voltage rails, temperatures, current etc. For each of the measured values there are $\overline{\text{ALERT}}$ and $\overline{\text{FAULT}}$ limits. When an $\overline{\text{ALERT}}$ or $\overline{\text{FAULT}}$ limit is exceeded then the $\overline{\text{ALERT}}$ or $\overline{\text{FAULT}}$ pin is asserted low and will remain low until the I^{2}C master does a Clear_Faults command and the measured value is back within the programmed limits. Take for example the temperature measurement Read_Temperature1 (0x8D). This value is compared with the OT_WARN_LIMIT (0x51) and the UT_WARN_LIMIT (0x52). If the measured temperature goes above the OT_WARN_LIMIT or under the UT_WARN_LIMIT then the corresponding Status bit is set Status_Temperature Command (0x7D) and an $\overline{\text{ALERT}}$ pin is pulled low. The $\overline{\text{ALERT}}$ pin will remain low until the I^{2}C master does a Clear_Faults command (0x03) and the measured temperature is back within the programmed limits. If the measured temperature exceeds the OT_$\overline{\text{FAULT}}$_LIMIT (0x51) then Bit 7 of the Status_Temperature command gets set and the $\overline{\text{FAULT}}$ pin is asserted low. The intention is that a $\overline{\text{FAULT}}$ condition is worse than an $\overline{\text{ALERT}}$ condition.

Each measured value is compared with appropriate high and low limits and the results of these comparisons are stored in Status Registers. See details of the various status registers in Table 11, commands 0x78, STATUS BYTE to 0x80 STATUS $\overline{\text{ALERT}}$.

The ADP4000 also allows the user to program which measured values can generate an $\overline{\text{ALERT}}$ and a $\overline{\text{FAULT}}$ using the Mask $\overline{\text{ALERT}}$ (0xF9) and Mask $\overline{\text{FAULT}}$ (0xFA) Commands. If the Mask VOUT Bit (Bit 7 is set in the Mask $\overline{\text{ALERT}}$ command) then the measured Vout going outside the programmed limits will set the appropriate Status bit but will not assert $\overline{\text{ALERT}}$ pin low. See command codes 0xF9 and 0xFA in Table 11 for more details.

Linear Mode

Linear Mode is used for reporting back voltage, current and temperatures etc and for programming Limits. The ADP4000 uses Linear Mode. Linear Mode can be decoded as follows:

$$X = Y*2\text{^}N$$

Where X = the value (for example if this is current then it would be Amps, Temperature it would be °C etc). The register readback is 16 Bits, the 5 MSB's are the Exponent (=N) and the 11 LSB's are the mantissa (=Y). Both the

mantissa and exponent are 2's compliment values, if the MSB are 1 then they are negative values.

IOUT_CAL_GAIN and IOUT_CAL_OFFSET

The ADP4000 measures the voltage on the Imon pin and stores that in the READ_IOUT Command (0x8C). However this register should read back Amps. Therefore the IOUT_CAL_GAIN and IOUT_CAL_OFFSET commands need to be programmed to convert the Imon voltage into current in Amps. The following equation is used:

$$\text{READ\_IOUT} = \left(I_{MON}\ \text{Voltage} \times \text{IOUT\_CAL\_GAIN}\right) + \text{IOUT\_CAL\_OFFSET} \quad \text{(eq. 19)}$$

The IOUT_CAL_GAIN defaults to 1 and IOUT_CAL_OFFSET defaults to 0 which means the Imon voltage is stored in the READ_IOUT Command.

VR11 VID CODES for the ADP4000

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
OFF	0	0	0	0	0	0	0	0
OFF	0	0	0	0	0	0	0	1
1.60000	0	0	0	0	0	0	1	0
1.59375	0	0	0	0	0	0	1	1
1.58750	0	0	0	0	0	1	0	0
1.58125	0	0	0	0	0	1	0	1
1.57500	0	0	0	0	0	1	1	0
1.56875	0	0	0	0	0	1	1	1
1.56250	0	0	0	0	1	0	0	0
1.55625	0	0	0	0	1	0	0	1
1.55000	0	0	0	0	1	0	1	0
1.54375	0	0	0	0	1	0	1	1
1.53750	0	0	0	0	1	1	0	0
1.53125	0	0	0	0	1	1	0	1
1.52500	0	0	0	0	1	1	1	0
1.51875	0	0	0	0	1	1	1	1
1.51250	0	0	0	1	0	0	0	0
1.50625	0	0	0	1	0	0	0	1
1.50000	0	0	0	1	0	0	1	0
1.49375	0	0	0	1	0	0	1	1
1.48750	0	0	0	1	0	1	0	0
1.48125	0	0	0	1	0	1	0	1
1.47500	0	0	0	1	0	1	1	0
1.46875	0	0	0	1	0	1	1	1
1.46250	0	0	0	1	1	0	0	0
1.45625	0	0	0	1	1	0	0	1
1.45000	0	0	0	1	1	0	1	0
1.44375	0	0	0	1	1	0	1	1
1.43750	0	0	0	1	1	1	0	0
1.43125	0	0	0	1	1	1	0	1
1.42500	0	0	0	1	1	1	1	0
1.41875	0	0	0	1	1	1	1	1
1.41250	0	0	1	0	0	0	0	0
1.40625	0	0	1	0	0	0	0	1
1.40000	0	0	1	0	0	0	1	0
1.39375	0	0	1	0	0	0	1	1
1.38750	0	0	1	0	0	1	0	0
1.38125	0	0	1	0	0	1	0	1
1.37500	0	0	1	0	0	1	1	0
1.36875	0	0	1	0	0	1	1	1
1.36250	0	0	1	0	1	0	0	0
1.35625	0	0	1	0	1	0	0	1
1.35000	0	0	1	0	1	0	1	0
1.34375	0	0	1	0	1	0	1	1
1.33750	0	0	1	0	1	1	0	0
1.33125	0	0	1	0	1	1	0	1

VR11 VID CODES for the ADP4000

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.32500	0	0	1	0	1	1	1	0
1.31875	0	0	1	0	1	1	1	1
1.31250	0	0	1	1	0	0	0	0
1.30625	0	0	1	1	0	0	0	1
1.30000	0	0	1	1	0	0	1	0
1.29375	0	0	1	1	0	0	1	1
1.28750	0	0	1	1	0	1	0	0
1.28125	0	0	1	1	0	1	0	1
1.27500	0	0	1	1	0	1	1	0
1.26875	0	0	1	1	0	1	1	1
1.26250	0	0	1	1	1	0	0	0
1.25625	0	0	1	1	1	0	0	1
1.25000	0	0	1	1	1	0	1	0
1.24375	0	0	1	1	1	0	1	1
1.23750	0	0	1	1	1	1	0	0
1.23125	0	0	1	1	1	1	0	1
1.22500	0	0	1	1	1	1	1	0
1.21875	0	0	1	1	1	1	1	1
1.21250	0	1	0	0	0	0	0	0
1.20625	0	1	0	0	0	0	0	1
1.20000	0	1	0	0	0	0	1	0
1.19375	0	1	0	0	0	0	1	1
1.18750	0	1	0	0	0	1	0	0
1.18125	0	1	0	0	0	1	0	1
1.17500	0	1	0	0	0	1	1	0
1.16875	0	1	0	0	0	1	1	1
1.16250	0	1	0	0	1	0	0	0
1.15625	0	1	0	0	1	0	0	1
1.15000	0	1	0	0	1	0	1	0
1.14375	0	1	0	0	1	0	1	1
1.13750	0	1	0	0	1	1	0	0
1.13125	0	1	0	0	1	1	0	1
1.12500	0	1	0	0	1	1	1	0
1.11875	0	1	0	0	1	1	1	1
1.11250	0	1	0	1	0	0	0	0
1.10625	0	1	0	1	0	0	0	1
1.10000	0	1	0	1	0	0	1	0
1.09375	0	1	0	1	0	0	1	1
1.08750	0	1	0	1	0	1	0	0
1.08125	0	1	0	1	0	1	0	1
1.07500	0	1	0	1	0	1	1	0
1.06875	0	1	0	1	0	1	1	1
1.06250	0	1	0	1	1	0	0	0
1.05625	0	1	0	1	1	0	0	1
1.05000	0	1	0	1	1	0	1	0
1.04375	0	1	0	1	1	0	1	1