Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# Dual 3 MHz, 600 mA Buck Regulator with 150 mA LDO

# ADP5022

## FEATURES

- **Input voltage range: 2.4 V to 5.5 V**
- **Tiny 16-ball, 2 mm × 2 mm WLCSP package**
- **Overcurrent and thermal protection**
- **Soft start**
- **Factory programmable undervoltage lockout on VDDA**
  - **system supply of either 2.2 V or 3.9 V**
- **Factory programmable default output voltages for all**
  - **3 channels**
- **Buck1 and Buck2 key specifications**
  - **Current mode architecture for excellent transient response**
  - **3 MHz operating frequency**
  - **Uses tiny multilayer inductors and capacitors**
  - **Forced PWM and auto PWM/PSM modes**
  - **Out-of-phase operation for reduced input filtering**
  - **100% duty cycle low dropout mode**
  - **24 µA typical quiescent current per channel, no switching**
- **LDO key specifications**
  - **Stable with 1 µF ceramic output capacitors**
  - **High PSRR**
    - **60 dB up to 10 KHz**
  - **Low output noise**
    - **65 µV rms output noise at VOUT3 = 3.3 V**
  - **Low dropout voltage: 150 mV @ 150 mA load**
  - **11 µA typical ground current at no load**

## APPLICATIONS

- **USB devices**
- **Handheld products**
- **Multivoltage power for processors, ASICS, FPGAs,**
  - **and RF chipsets**

## GENERAL DESCRIPTION

The ADP5022 is a micro power management unit (micro PMU) that combines two high performance buck regulators and a low dropout regulator (LDO) in a tiny 16-ball 2.08 mm × 2.08 mm WLCSP to meet demanding performance and board space requirements.

The high switching frequency of the buck regulators enables tiny multilayer external components and minimizes the board space required. When the MODE pin is set high, the buck regulators operate in forced PWM mode. When the MODE pin is set low, the buck regulators automatically switch operating modes, depending on the load current level. At higher output loads, the buck regulators operate in PWM mode. When the load current falls below a predefined threshold, the regulators operate in power save mode (PSM), improving the light-load efficiency.

The two bucks operate out-of-phase to reduce the input capacitor requirement and noise.

The low quiescent current, low dropout voltage, and wide input voltage range of the ADP5022 LDO extends the battery life of portable devices. The LDO maintains power supply rejection greater than 60 dB for frequencies as high as 10 kHz while operating with a low headroom voltage.

Each regulator in the ADP5022 has a dedicated, independent enable pin. A high voltage level applied to the enable pin activates the respective regulator. The default output voltages are factory programmable and can be set to a wide range of options.

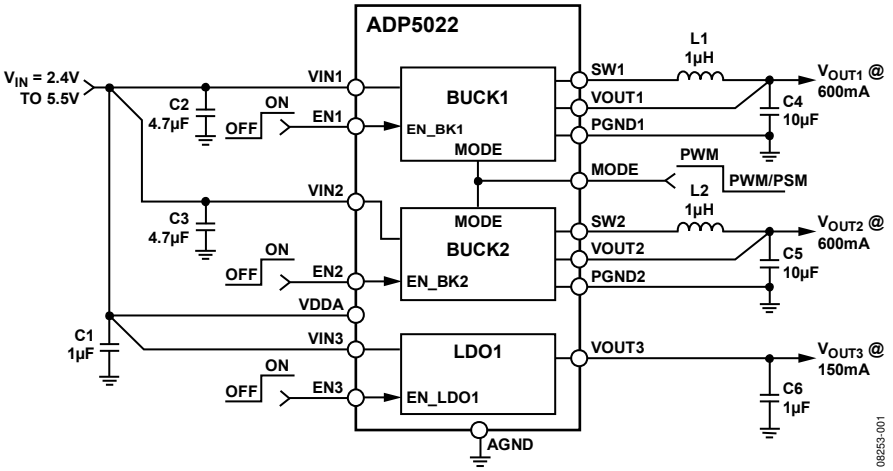


*Figure 1. Typical Applications Circuit*

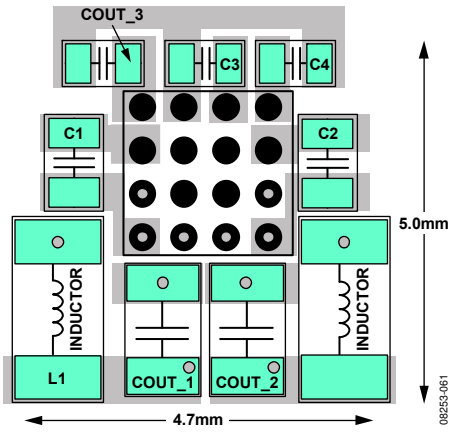


*Figure 2. Typical PCB Layout*

**Rev. C**



**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781.329.4700** **www.analog.com**
**Fax: 781.461.3113** 

# ADP5022* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

## COMPARABLE PARTS

View a parametric search of comparable parts.

## DOCUMENTATION

**Data Sheet**

- ADP5022: Dual 3 MHz, 600 mA Buck Regulator with 150 mA LDO Data Sheet

**User Guides**

- UG-014: Evaluation Board for the ADP5022 Micro PMU

## SOFTWARE AND SYSTEMS REQUIREMENTS

- ADP150 Regulator Fixed Voltage Linux Driver

## TOOLS AND SIMULATIONS

- ADIsimPower™ Voltage Regulator Design Tool

## REFERENCE MATERIALS

**Solutions Bulletins & Brochures**

- Integrated Power Solutions for Altera FPGAs
- Integrated, High Power Solutions for Xilinx FPGAs

## DESIGN RESOURCES

- ADP5022 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all ADP5022 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

Submit feedback for this data sheet.

# TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Revision History ... 2
Specifications ... 3
Buck1 and Buck2 Specifications ... 4
LDO Specifications ... 5
Absolute Maximum Ratings ... 6
Thermal Data ... 6
Thermal Resistance ... 6
ESD Caution ... 6
Pin Configuration and Function Descriptions ... 7
Typical Performance Characteristics ... 8
Theory of Operation ... 16
Power Management Unit ... 16
Buck Section ... 17
LDO Section ... 18
Applications Information ... 19
Buck External Component Selection ... 19
LDO Capacitor Selection ... 20
PCB Layout Guidelines ... 22
Evaluation Board schematics and Artwork ... 23
Suggested Layout ... 23
Outline Dimensions ... 25
Ordering Guide ... 25

## REVISION HISTORY

**10/10—Rev. B to Rev. C**

Changes to Figure 2 ... 1
Changes to Table 9 ... 20

**6/10—Rev. A to Rev. B**

Changes to Ordering Guide ... 25

**11/09—Revision A: Initial Version**

# SPECIFICATIONS

VDDA = VIN1 = VIN2 = 3.6 V, VIN3 = (VOUT3 + 0.5 V) or 2.4 V, whichever is greater, VIN3 ≤ VIN1, $T_J$ = −40°C to +125°C, unless otherwise noted.[1]

**Table 1.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INPUT VOLTAGE RANGE | | | | | | |
| System and Buck Input Supplies Voltage Range | $V_{DDA}$, $V_{IN1}$, and $V_{IN2}$ | Low UVLO level models | 2.4 | | 5.5 | V |
| | | High UVLO level models | 4.5 | | 5.5 | V |
| LDO Input Supply Voltage Range | $V_{IN3}$ | | 2.3 | | 5.5 | V |
| SHUTDOWN CURRENT | | | | | | |
| | $I_{GND-SD}$ | EN1 = EN2 = EN3 = GND | | 0.5 | | µA |
| | | EN1 = EN2 = EN3 = GND<br>$T_J$ = −40°C to +85°C | | | 2 | µA |
| THERMAL SHUTDOWN | | | | | | |
| Thermal Shutdown Threshold | $TSD_{TH}$ | $T_J$ rising | | 150 | | °C |
| Thermal Shutdown Hysteresis | $TSD_{HYS}$ | | | 20 | | °C |
| EN1, EN2, EN3, MODE INPUTS | | | | | | |
| EN1, EN2, EN3, MODE Input Logic High | $V_{IH}$ | VDDA = VIN1 = VIN2 | 1.2 | | | V |
| EN1, EN2, EN3, MODE Input Logic Low | $V_{IL}$ | VDDA = VIN1 = VIN2 | | | 0.4 | V |
| EN1, EN2, EN3, MODE Input Leakage Current | $V_{I-LEAKAGE}$ | Pin at (VDDA = VIN1 = VIN2) or GND | | 0.05 | 1 | µA |
| STANDBY CURRENT | | | | | | |
| All Channels Enabled, No Load | $I_{STBY}$ | | | 80 | | µA |
| All Channels Enabled, No Load, No Buck Switching | $I_{STBY-NOSW}$ | | | 59 | 85 | µA |
| VIN3 UNDERVOLTAGE LOCKOUT | | | | | | |
| Input Voltage Rising | $UVLO_{VIN3RISE}$ | | | | 2.20 | V |
| Input Voltage Falling | $UVLO_{VIN3FALL}$ | | 1.45 | | | V |
| VDDA UNDERVOLTAGE LOCKOUT | | | | | | |
| Input Voltage Rising | $UVLO_{VDDARISE}$ | High UVLO level (factory programmed) | | | 4.15 | V |
| | | Low UVLO level (factory programmed) | | | 2.35 | V |
| Input Voltage Falling | $UVLO_{VDDAFALL}$ | High UVLO level (factory programmed) | 3.40 | | | V |
| | | Low UVLO level (factory programmed) | 2.00 | | | V |

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control.

## BUCK1 AND BUCK2 SPECIFICATIONS

VDDA = VIN1 = VIN2 = 3.6 V, VIN3 = (VOUT3 + 0.5 V) or 2.4 V, whichever is greater, VIN3 ≤ VIN1, $T_J$ = −40°C to +125°C, unless otherwise noted.[1]

**Table 2.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OPERATING SUPPLY CURRENT | | | | | | |
| Buck1 Only | $I_{GND1}$ | $I_{LOAD1}$ = 0 mA, device not switching, EN1 = VDDA, EN2 = EN3 = GND | | 24 | | µA |
| Buck2 Only | $I_{GND2}$ | $I_{LOAD2}$ = 0 mA, device not switching, EN2 = VDDA, EN1 = EN3 = GND | | 32 | | µA |
| Buck1 and Buck2 Only | $I_{GND1-2}$ | $I_{LOAD1}$ = $I_{LOAD1}$ = 0 mA, device not switching, EN1 = EN2 = VDDA, EN3 = GND | | 48 | 64 | µA |
| OUTPUT VOLTAGE ACCURACY | $V_{OUT1}$, $V_{OUT2}$ | PWM mode, VIN1 = VIN2 = 2.4 V to 5.5 V, $I_{LOAD1}$ = $I_{LOAD2}$ = 0 mA − 600 mA | −3 | | +3 | % |
| POWER SAVE MODE TO PWM CURRENT THRESHOLD | $I_{PSM-PWM}$ | | | 105 | | mA |
| PWM TO POWER SAVE MODE CURRENT THRESHOLD | $I_{PWM-PSM}$ | | | 100 | | mA |
| SW CHARACTERISTICS, BUCK1 and BUCK2 | | | | | | |
| PFET On Resistance | $R_{PFET}$ | Typical at VIN1 = VIN2 = 3.6 V | | 165 | 275 | mΩ |
| | | Typical at VIN1 = VIN2 = 5.0 V | | 125 | | mΩ |
| NFET On Resistance | $R_{NFET}$ | Typical at VIN1 = VIN2 = 3.6 V | | 125 | 220 | mΩ |
| | | Typical at VIN1 = VIN2 = 5.0 V | | 100 | | mΩ |
| Current Limit | $I_{LIMIT1}$, $I_{LIMIT2}$ | PFET switch peak current limit | 750 | 950 | 1050 | mA |
| OSCILLATOR FREQUENCY | $F_{SW}$ | | 2.5 | 3.0 | 3.5 | MHz |
| START-UP TIME[2] | | | | | | |
| From Shutdown State | $T_{STARTUP12-SD}$ | | | 250 | | µs |

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control.
[2] Start-up time is defined as the time from a rising edge on EN1/EN2 to VOUT1/VOUT2 reaching 90% of their nominal value.

## LDO SPECIFICATIONS

VDDA = VIN1 = VIN2 = 3.6 V, VIN3 = (VOUT3 + 0.5 V) or 2.3 V, whichever is greater, VIN3 ≤ VIN1, $I_{OUT3}$ = 10 mA; $C_{IN3}$ = $C_{OUT3}$ = 1 µF, $T_J$ = −40°C to +125°C, unless otherwise noted.[1]

**Table 3.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OPERATING SUPPLY CURRENT[2] | $I_{VIN3-GND}$ | | | | | |
| | | $I_{OUT3}$ = 0 µA | | 11 | 21 | µA |
| | | $I_{OUT3}$ = 10 mA | | 16 | 29 | µA |
| | | $I_{OUT3}$ = 150 mA | | 31 | 43 | µA |
| OUTPUT VOLTAGE ACCURACY | $V_{OUT3}$ | | | | | |
| | | 100 µA < $I_{OUT3}$ < 150 mA, VIN3 = (VOUT3 + 0.5 V) to 5.5 V | −2 | | +2 | % |
| REGULATION | | | | | | |
| Line Regulation | $\Delta VOUT3/\Delta V_{IN3}$ | VIN3 = (VOUT3 + 0.5 V) to 5.5 V, $I_{OUT}$ = 1 mA | −0.03 | | +0.03 | %/V |
| Load Regulation[3] | $\Delta VOUT3/\Delta I_{OUT3}$ | $I_{OUT3}$ = 1 mA to 150 mA | | 0.002 | 0.0075 | %/mA |
| DROPOUT VOLTAGE[4] | | | | | | |
| | $V_{DROPOUT}$ | VOUT3 = 3.0 V, $I_{OUT3}$ = 10 mA | | 7 | | mV |
| | | VOUT3 = 3.0 V, $I_{OUT3}$ = 150 mA | | 110 | 150 | mV |
| START-UP TIME[5] | | | | | | |
| From Shutdown State | $T_{STARTUP3-SD}$ | | | 200 | | µs |
| CURRENT-LIMIT THRESHOLD[6] | $I_{LIMIT3}$ | | 160 | 240 | 350 | mA |
| OUTPUT NOISE | $OUT_{NOISE}$ | | | | | |
| | | 10 Hz to 100 kHz, VIN3 = 5 V, VOUT3 = 3.3 V | | 65 | | µV rms |
| | | 10 Hz to 100 kHz, VIN3= 5 V, VOUT3 = 2.4 V | | 52 | | µV rms |
| | | 10 Hz to 100 kHz, VIN3 = 5 V, VOUT3 = 1.2 V | | 40 | | µV rms |
| POWER SUPPLY REJECTION RATIO | PSRR | | | | | |
| | | 10 kHz, VIN3 = 5 V, VOUT3 = 3.3 V | | 60 | | dB |
| | | 10 kHz, VIN3 = 5 V, VOUT3 = 2.3 V | | 66 | | dB |
| | | 10 kHz, VIN3 = 5 V, VOUT3 = 1.2 V | | 70 | | dB |

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control.
[2] LDO operating supply current is the current drawn from VIN3 to AGND when the LDO is enabled. Whenever any regulator channel is enabled, current is drawn from VIN1 to AGND. This current is 8 µA typical and is included in the $I_{GND1}$, $I_{GND2}$, and $I_{GND1-2}$ specifications.
[3] Based on an end-point calculation using 1 mA and 150 mA loads.
[4] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 2.3 V.
[5] Start-up time is defined as the time between the rising edge of EN3 to VOUT3 being at 90% of its nominal value.
[6] Current-limit threshold is defined as the current at which VOUT3 drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V or 2.7 V.

# ABSOLUTE MAXIMUM RATINGS

**Table 4.**

| Parameter | Rating |
|---|---|
| VDDA, VIN1, VIN2, VIN3, VOUT1, VOUT2, VOUT3, EN1, EN2, EN3, MODE to GND | −0.3 V to +6 V |
| Storage Temperature Range | −65°C to +150°C |
| Operating Junction Temperature Range | −40°C to +125°C |
| Soldering Conditions | JEDEC J-STD-020 |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL DATA

Absolute maximum ratings apply individually only, not in combination.

The ADP5022 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature ($T_A$) does not guarantee that the junction temperature ($T_J$) is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated. In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature may exceed the maximum limit as long as the junction temperature is within specification limits. $T_J$ of the device is dependent on $T_A$, the power dissipation ($P_D$) of the device, and the junction-to-ambient thermal resistance ($\theta_{JA}$) of the package. Maximum $T_J$ is calculated from $T_A$ and $P_D$ using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

$\theta_{JA}$ of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of $\theta_{JA}$ may vary, depending on PCB material, layout, and environmental conditions. The specified values of $\theta_{JA}$ are based on a 4-layer, 4" × 3" circuit board. Refer to JEDEC JESD 51-9 for detailed information on the board construction. For additional information, see the AN-617 Application Note, *MicroCSP™ Wafer Level Chip Scale Package*.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered on a circuit board.

**Table 5. Thermal Resistance**

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| 16-Ball, 0.5 mm Pitch WLCSP | 65 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

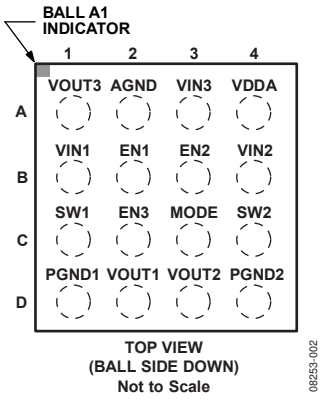


*Figure 3. Pin Configuration*

**Table 6. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| A1 | VOUT3 | LDO Output Voltage and Sensing Input. |
| A2 | AGND | Analog Ground. |
| A3 | VIN3 | LDO Input Supply (VIN3 ≤ VIN1 = VIN2 = VDDA). |
| A4 | VDDA | Supply Input for the Housekeeping Block and UVLO Sensing. |
| B1 | VIN1 | Buck1 Input Supply (VIN1 = VIN2 = VDDA). |
| B2 | EN1 | Buck1 Activation. Set EN1 = high: turn on Buck1. Set EN1 = low: turn off Buck1. |
| B3 | EN2 | Buck2 Activation. Set EN2 = high: turn on Buck2. Set EN2 = low: turn off Buck2. |
| B4 | VIN2 | Buck2 Input Supply (VIN2 = VIN1 = VDDA). |
| C1 | SW1 | Buck1 Switching Node. |
| C2 | EN3 | LDO Activation. Set EN3 = high: turn on LDO. EN3 = low: turn off LDO. |
| C3 | MODE | Buck1/Buck2 Operating Mode: MODE = high: forced PWM operation. MODE = low: auto PWM/PSM operation. |
| C4 | SW2 | Buck2 Switching Node. |
| D1 | PGND1 | Dedicated Power Ground for Buck1. |
| D2 | VOUT1 | Buck1 Output Voltage Sensing Input. |
| D3 | VOUT2 | Buck2 Output Voltage Sensing Input. |
| D4 | PGND2 | Dedicated Power Ground for Buck2. |

# TYPICAL PERFORMANCE CHARACTERISTICS

VIN1 = VIN2 = VIN3 = VDDA = 5.0 V, $T_A$ = 25°C, unless otherwise noted.

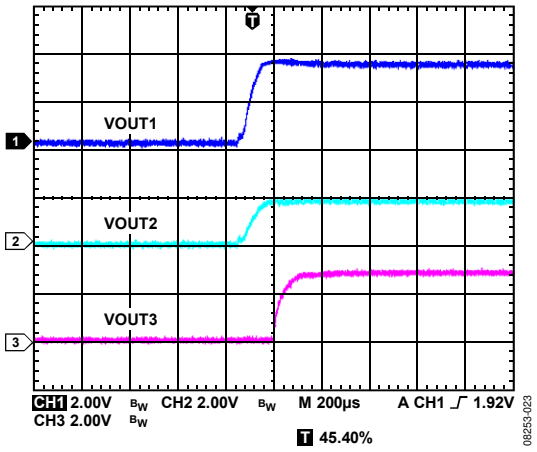


*Figure 4. 3-Channel Start-Up Waveforms, VIN3 Cascaded from VOUT1*

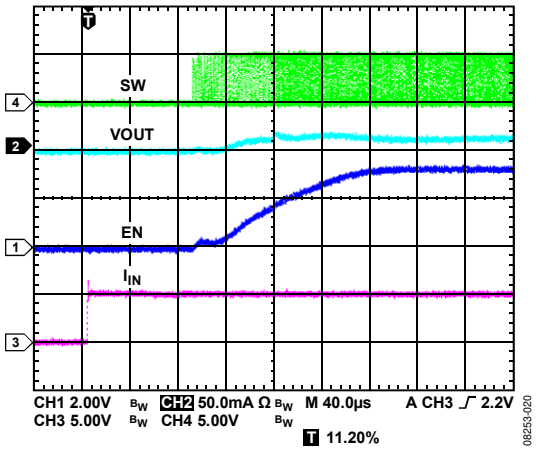


*Figure 7. Buck2 Startup, VOUT2 = 1.8 V, $I_{OUT2}$ = 5 mA*

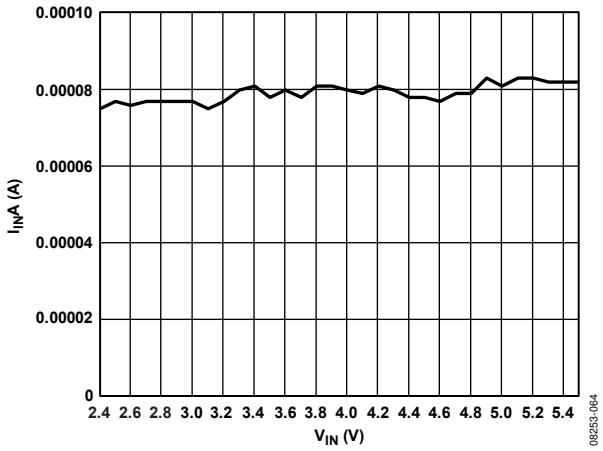


*Figure 5. System Quiescent Current vs. Input Voltage, VOUT1 = 0.8 V, VOUT2 = 2.5 V, VIN3 = VOUT2, VOUT3 = 1.2 V, All Channels Unloaded*

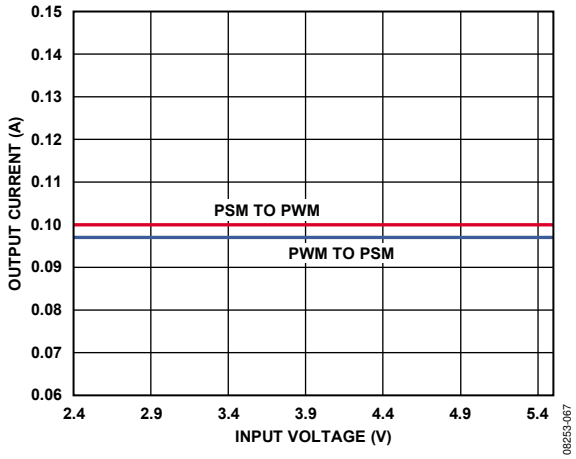


*Figure 8. Buck 2 PSM to PWM Transition, VOUT2 = 1.8 V*

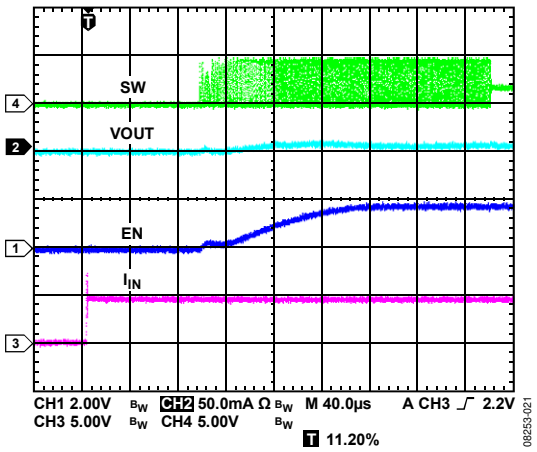


*Figure 6. Buck1 Startup, VOUT1 = 3.3 V, $I_{OUT1}$ = 10 mA*

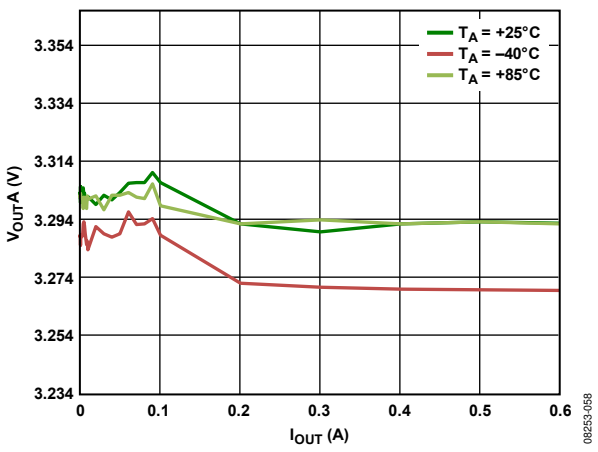


*Figure 9. Buck1 Load Regulation Across Temperature, VOUT1 = 3.3 V, Auto Mode*

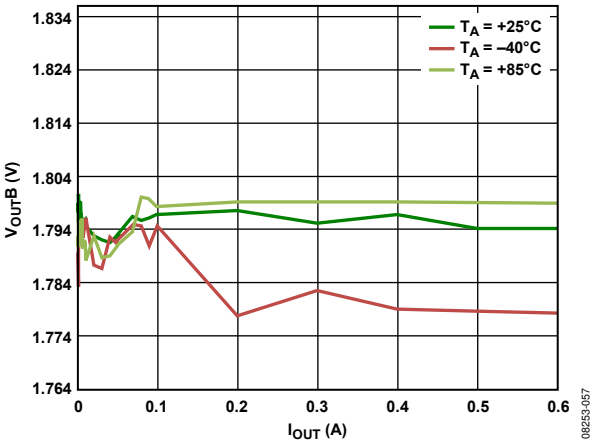


*Figure 10. Buck2 Load Regulation Across Temperature, VOUT2 = 1.8 V, Auto Mode*

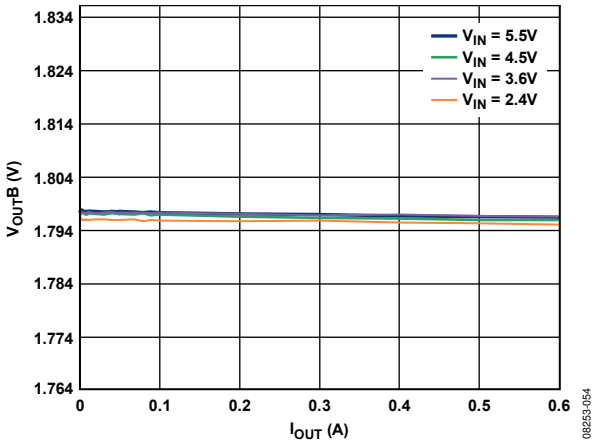


*Figure 11. Buck 2 Load Regulation Across Input Voltage, VOUT1 = 1.8 V, PWM Mode*

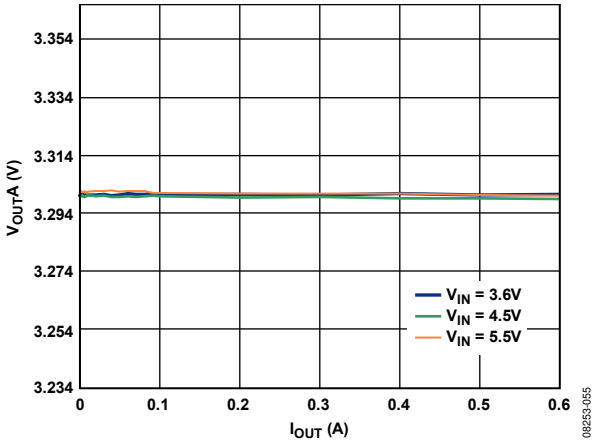


*Figure 12. Buck1 Load Regulation Across Input Voltage, VOUT2 = 3.3 V, PWM Mode*

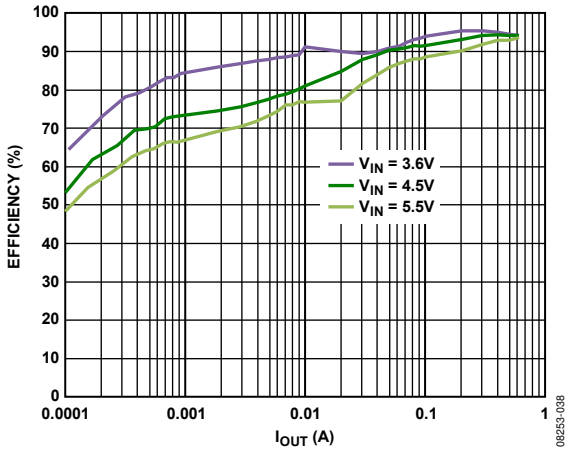


*Figure 13. Buck1 Efficiency vs. Load Current, Across Input Voltage, VOUT1 = 3.3 V, Auto Mode*

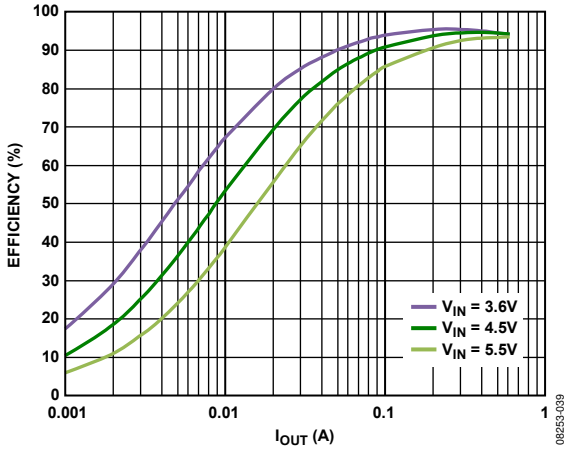


*Figure 14. Buck1 Efficiency vs. Load Current, Across Input Voltage, VOUT1 = 3.3 V, PWM Mode*

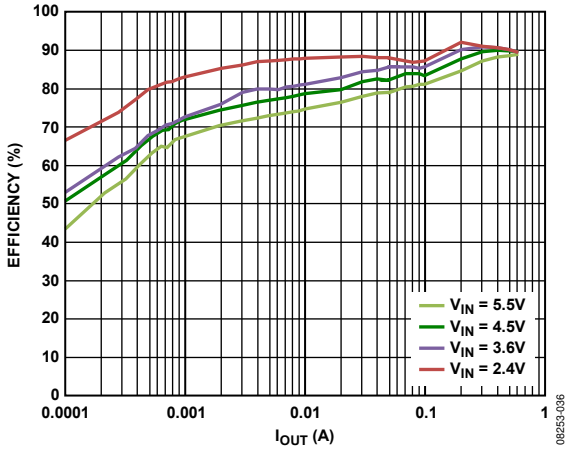


*Figure 15. Buck2 Efficiency vs. Load Current, Across Input Voltage, VOUT2 = 1.8 V, Auto Mode*

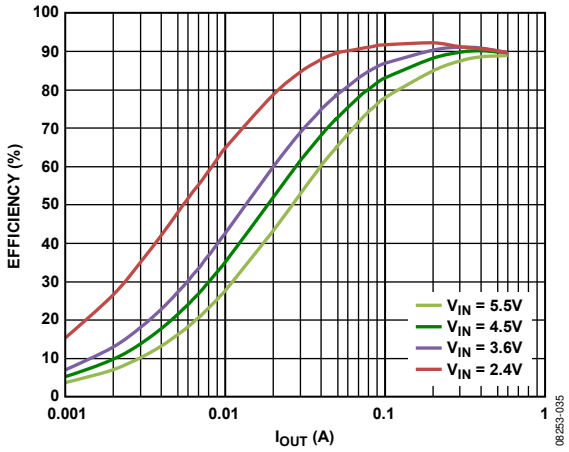


Figure 16. Buck2 Efficiency vs. Load Current, Across Input Voltage, VOUT2 = 1.8 V, PWM Mode

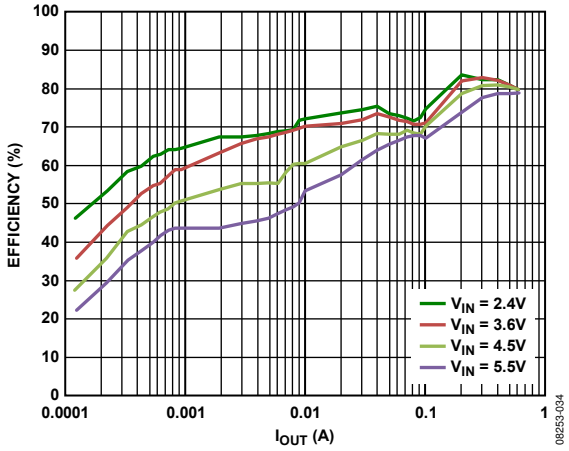


Figure 17. Buck1 Efficiency vs. Load Current, Across Input Voltage, VOUT1 = 0.8 V, Auto Mode

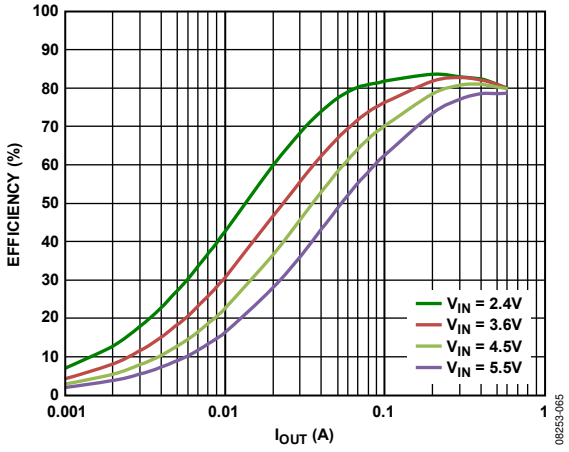


Figure 18. Buck1 Efficiency vs. Load Current, Across Input Voltage, VOUT1 = 0.8 V, PWM Mode

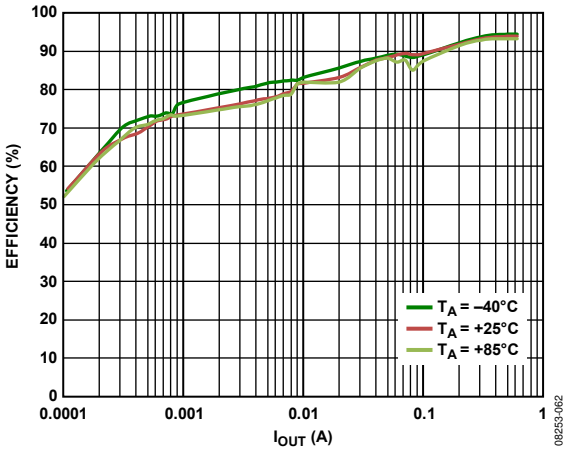


Figure 19. Buck1 Efficiency vs. Load Current, Across Temperature, VOUT1 = 3.3 V, Auto Mode

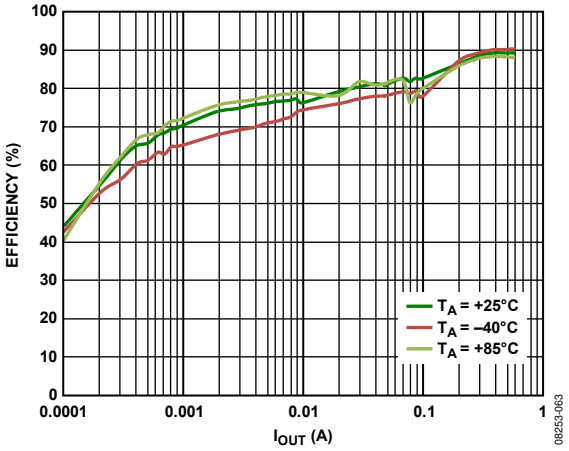


Figure 20. Buck2 Efficiency vs. Load Current, Across Temperature, VOUT2 = 1.8 V, Auto Mode

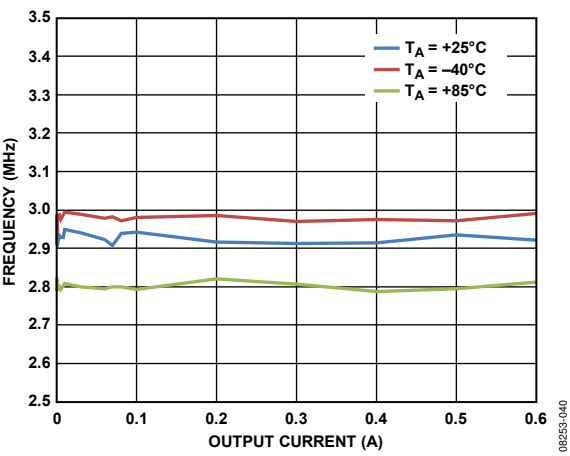


Figure 21. Buck2 Switching Frequency vs. Output Current, Across Temperature, VOUT2 = 1.8 V, PWM Mode

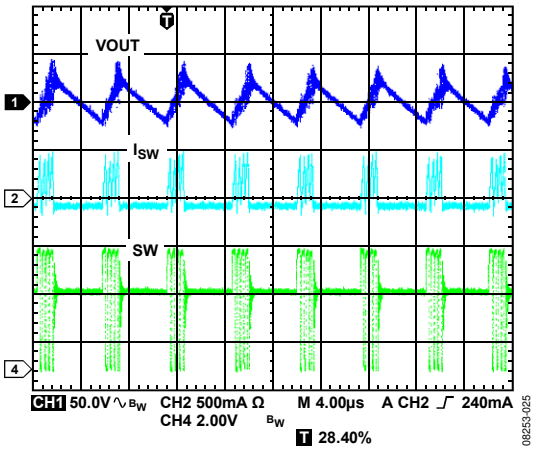


Figure 22. Typical Waveforms, VOUT1 = 3.3 V, $I_{OUT1}$ = 30 mA, Auto Mode

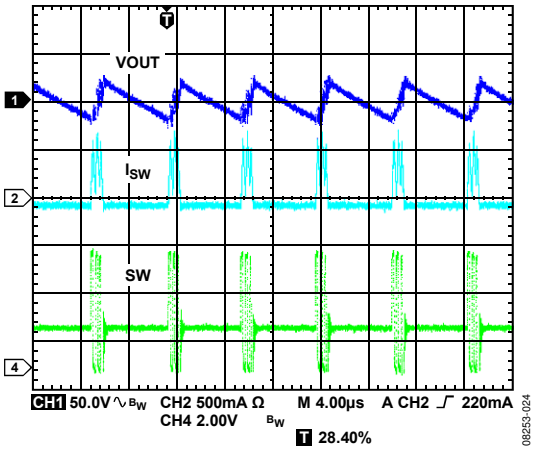


Figure 23. Typical Waveforms, VOUT2 = 1.8 V, $I_{OUT2}$ = 30 mA, Auto Mode

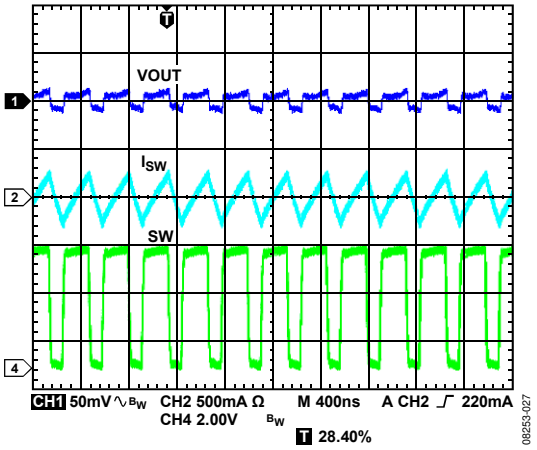


Figure 24. Typical Waveforms, VOUT1 = 3.3 V, $I_{OUT1}$ = 30 mA, PWM Mode

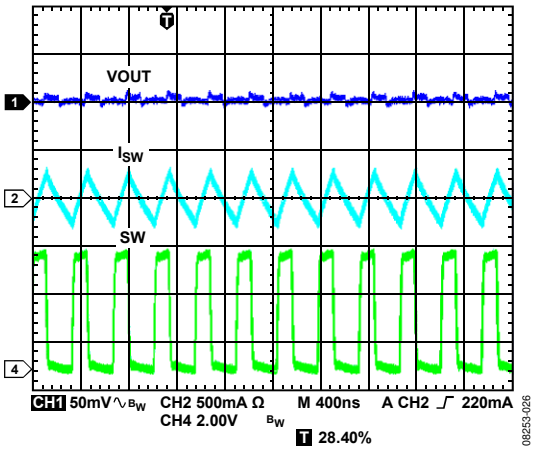


Figure 25. Typical Waveforms, VOUT2 = 1.8 V, $I_{OUT2}$ = 30 mA, PWM Mode

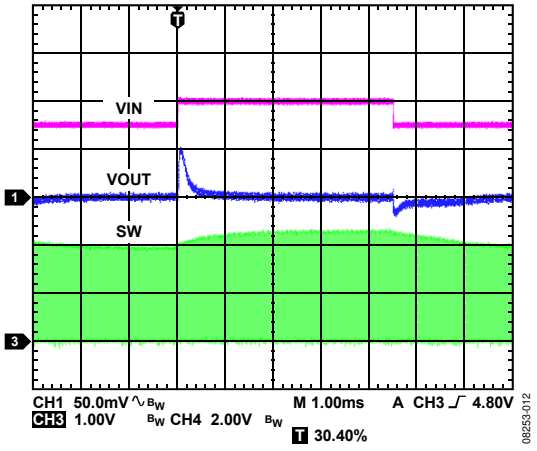


Figure 26. Buck1 Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, VOUT1 = 3.3 V, PWM Mode

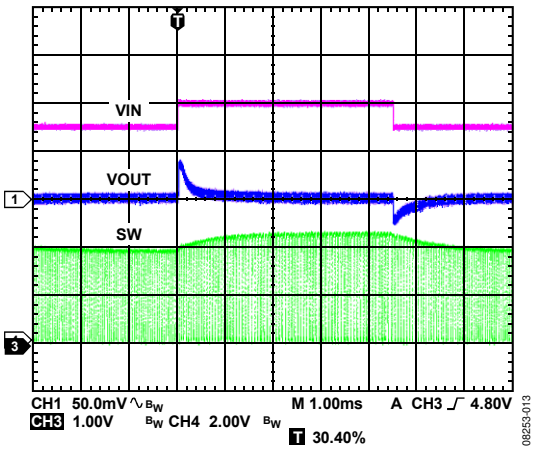


Figure 27. Buck2 Response to Line Transient, $V_{IN}$ = 4.5 V to 5.0 V, VOUT2 = 1.8 V, PWM Mode

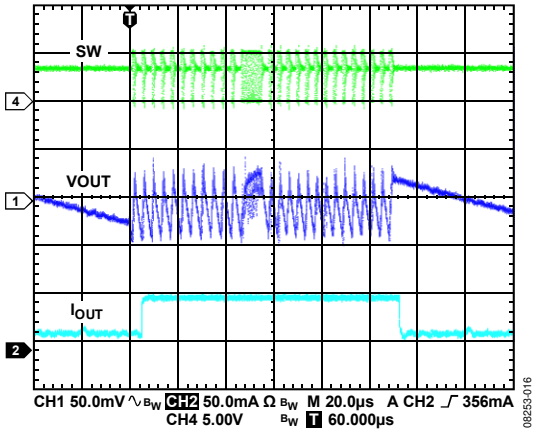


Figure 28. Buck1 Response to Load Transient, $I_{OUT1}$ from 1 mA to 50 mA, VOUT1 = 3.3 V, Auto Mode

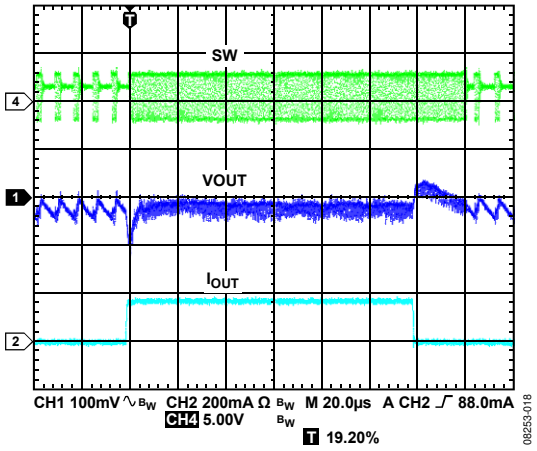


Figure 31. Buck2 Response to Load Transient, $I_{OUT2}$ from 20 mA to 180 mA, VOUT2 = 1.8 V, Auto Mode

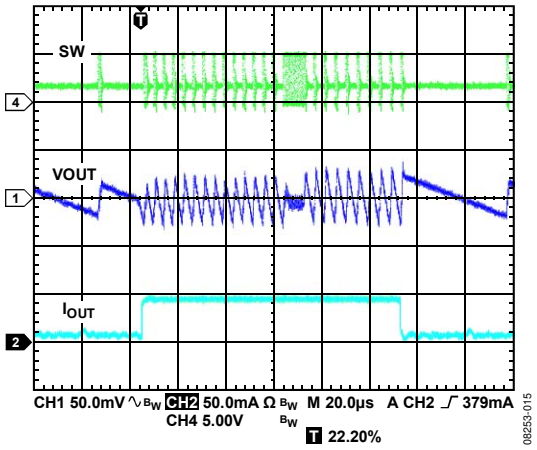


Figure 29. Buck2 Response to Load Transient, $I_{OUT2}$ from 1 mA to 50 mA, VOUT2 = 1.8 V, Auto Mode

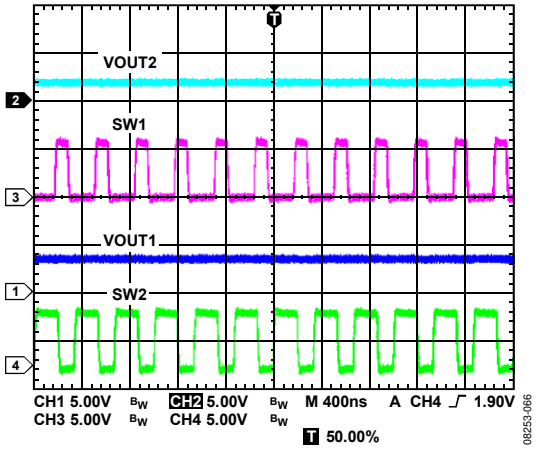


Figure 32. VOUT and SW Waveforms for Buck1 and Buck2 in PWM Mode Showing Out-of-Phase Operation

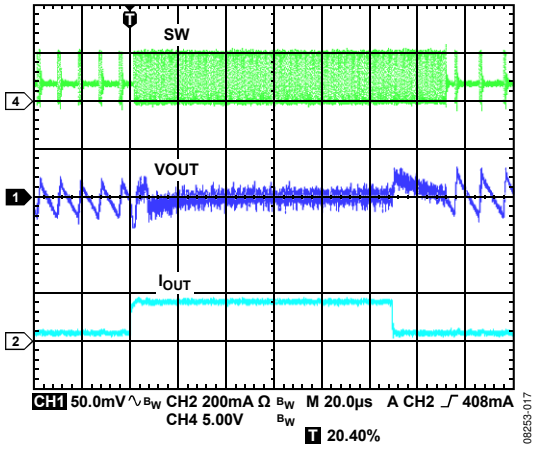


Figure 30. Buck1 Response to Load Transient, $I_{OUT1}$ from 20 mA to 180 mA, VOUT1 = 3.3 V, Auto Mode

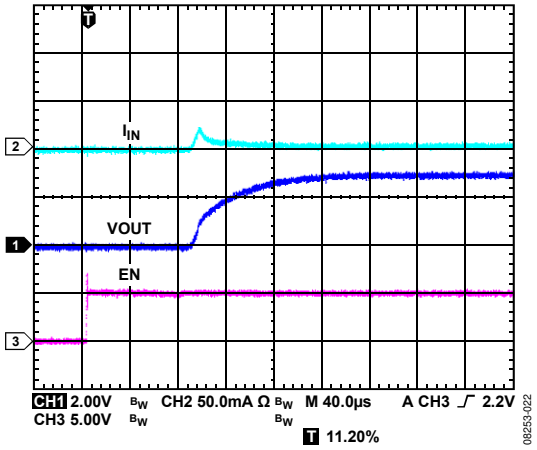


Figure 33. LDO Startup, VOUT3 = 3.0 V, $I_{OUT3}$ = 5 mA

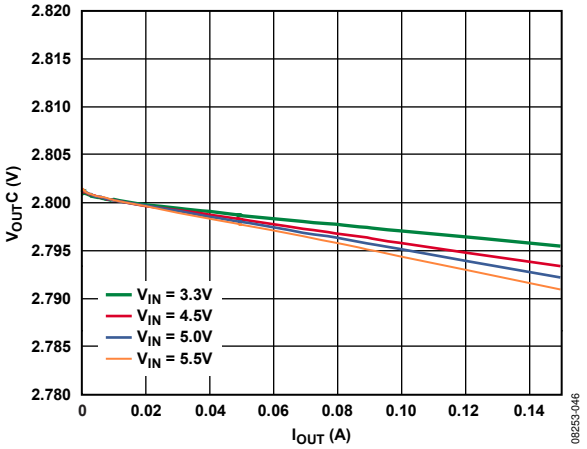


Figure 34. LDO Load Regulation Across Input Voltage, VOUT3 = 2.8 V

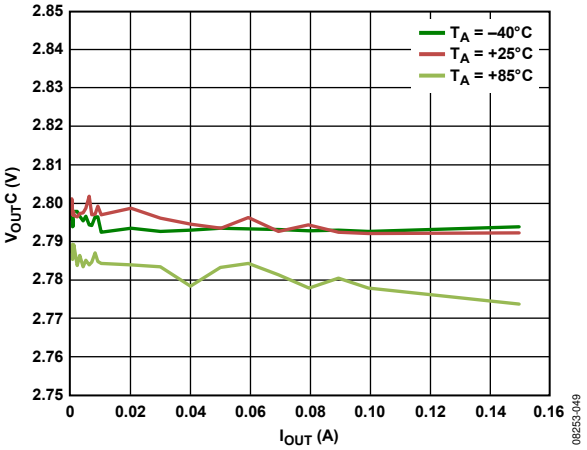


Figure 35. LDO Load Regulation Across Temperature, VIN3 = 3.3 V, VOUT3 = 2.8 V

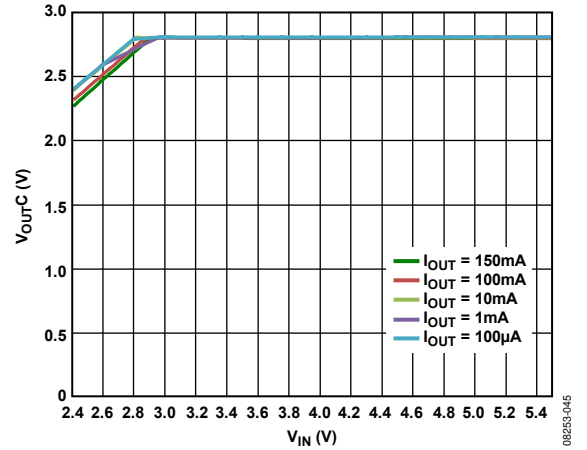


Figure 36. LDO Line Regulation Across Output Load, VOUT3 = 2.8 V

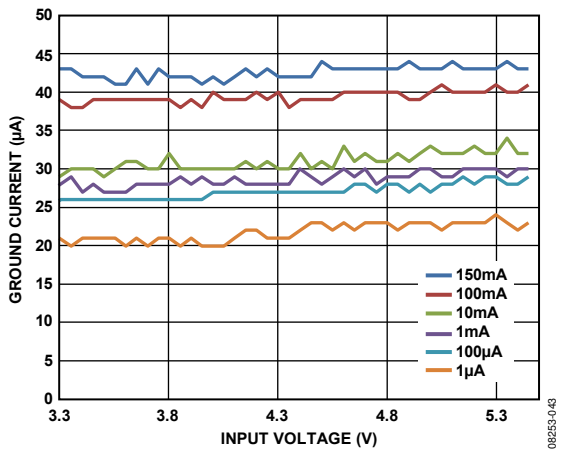


Figure 37. LDO Ground Current vs. Input Voltage, Across Output Load, VOUT3 = 2.8 V

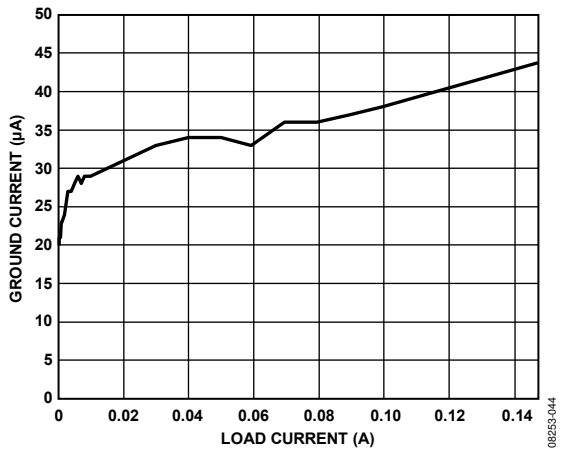


Figure 38. LDO Ground Current vs. Output Load, VIN3 = 3.3 V, VOUT3 = 2.8 V

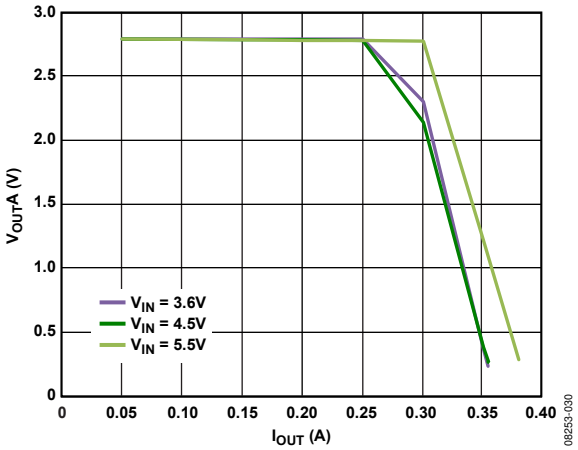


Figure 39. LDO Current Capability Across Input Voltage, VOUT3 = 2.8 V

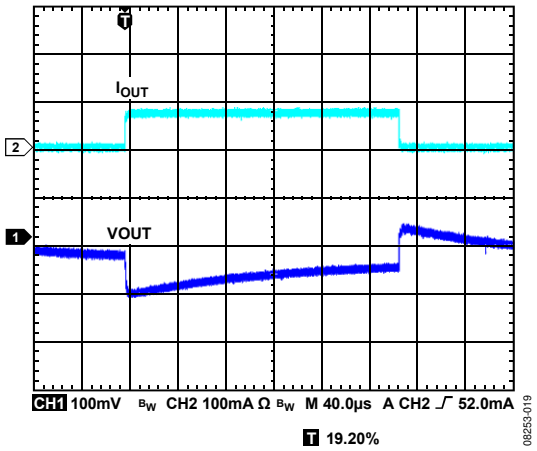


Figure 40. LDO Response to Load Transient, $I_{OUT3}$ from 1 mA to 80 mA, VOUT3 = 2.8 V

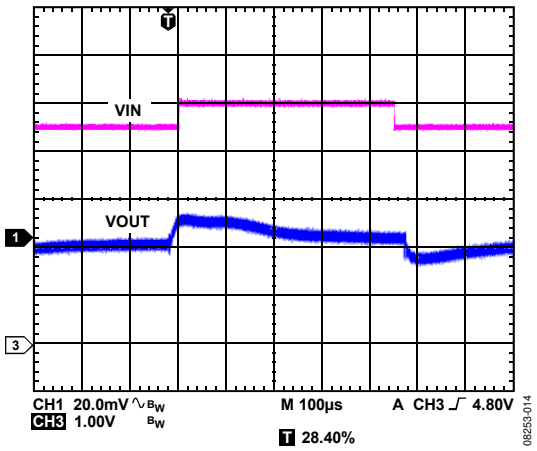


Figure 41. LDO Response to Line Transient, Input Voltage from 4.5 V to 5.5 V, VOUT3 = 2.8 V

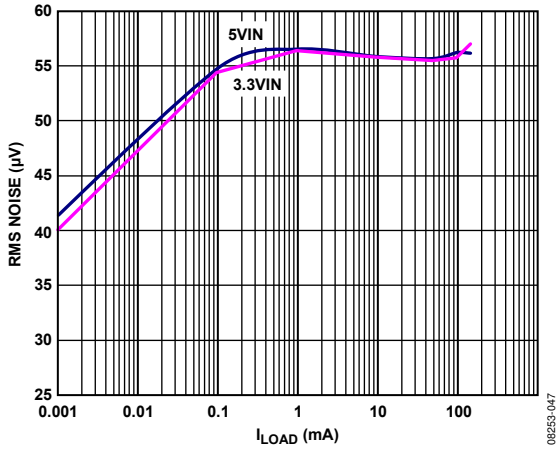


Figure 42. LDO Output Noise vs. Load Current, Across Input Voltage, VOUT3 = 2.8 V

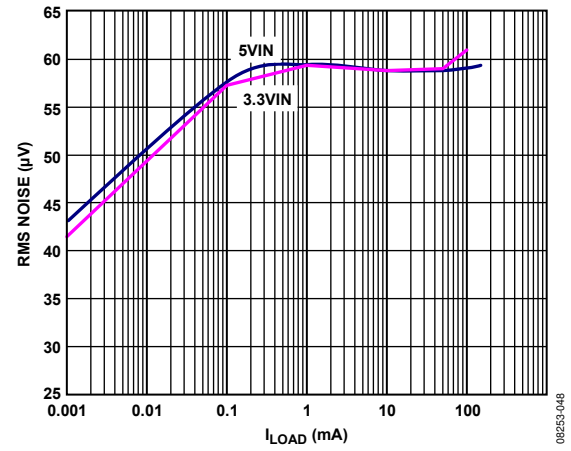


Figure 43. LDO Output Noise vs. Load Current, Across Input Voltage, VOUT3 = 3.0 V

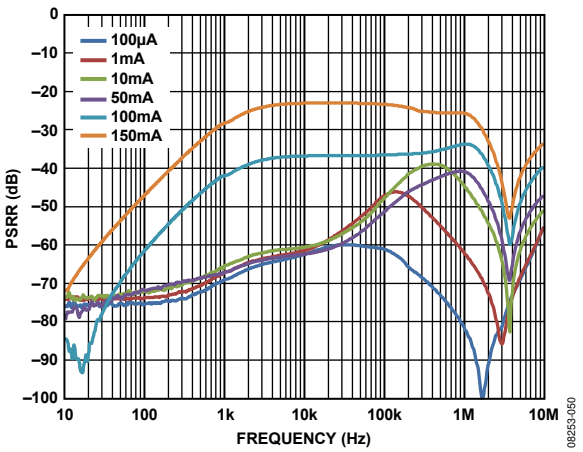


Figure 44. LDO PSRR Across Output Load, VIN3 = 3.3 V, VOUT3 = 2.8 V

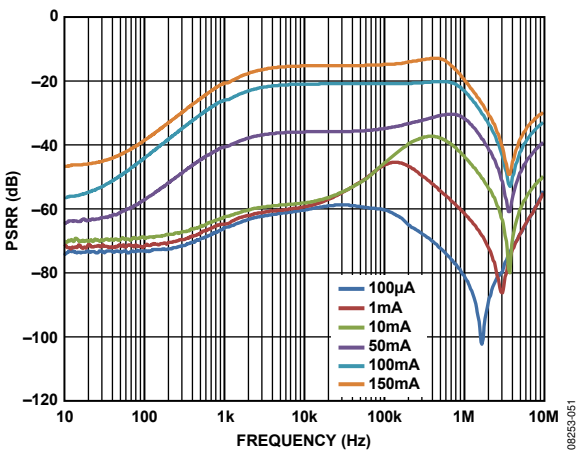


Figure 45. LDO PSRR Across Output Load, VIN3 = 3.3 V, VOUT3 = 3.0 V

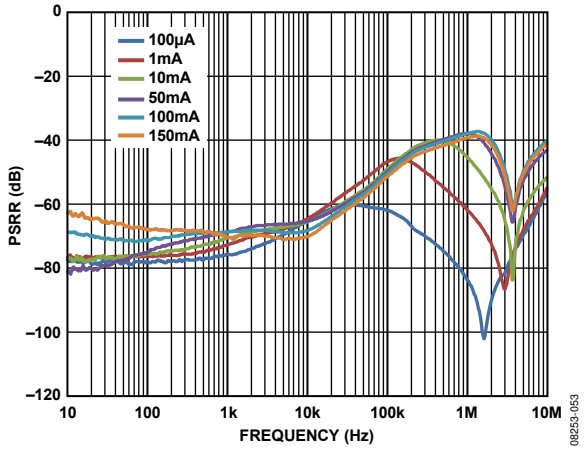


Figure 46. LDO PSRR Across Output Load, VIN3 = 5.0 V, VOUT3 = 2.8 V

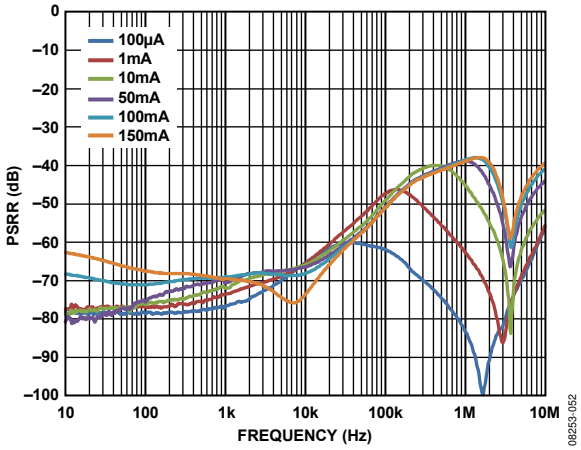


Figure 47. LDO PSRR Across Output Load, VIN3 = 5.0 V, VOUT3 = 3.0 V

# THEORY OF OPERATION

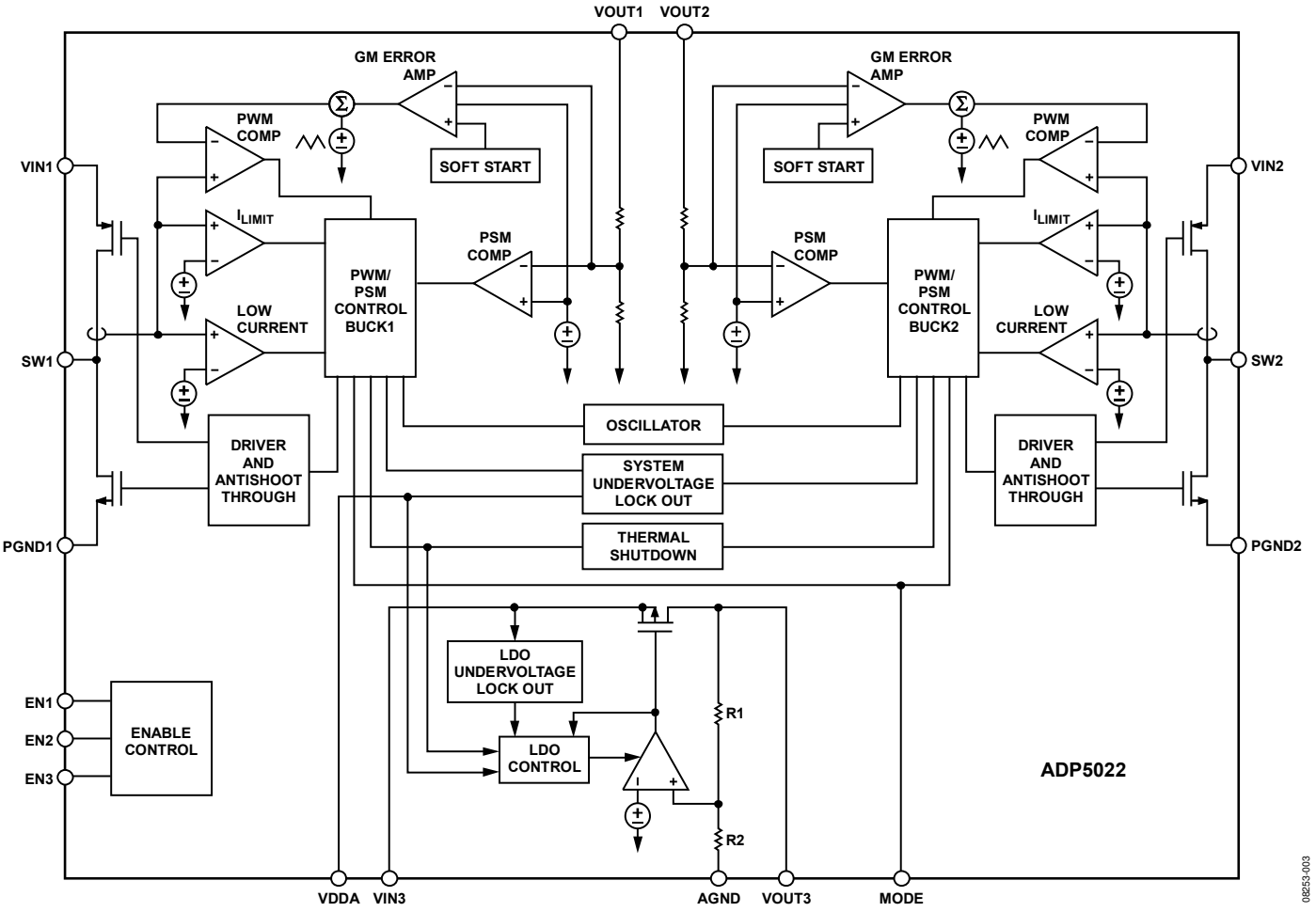


*Figure 48. Functional Block Diagram*

## POWER MANAGEMENT UNIT

The ADP5022 is a micro power management units (micro PMU) combining two step-down (buck) dc-to-dc converters and a single low dropout linear regulator (LDO). The high switching frequency and tiny 16-ball WLCSP package allow for a small power management solution.

To combine these high performance converters and regulators into the micro PMU, there is a system controller allowing them to operate together.

Each regulator has a dedicated enable pin. EN1 controls the activation for Buck1, EN2 controls the activation for Buck2, and EN3 controls the activation of the LDO. Logic high applied to the ENx pin turns on the regulator, and a logic low applied to the ENx pin turns off the regulator. When a regulator is turned on, the output voltage is controlled through a soft start circuit to avoid a large inrush current due to the discharged output capacitors.

The buck regulators can operate in forced PWM mode if the MODE pin is at a logic high level. In forced PWM mode, the switching frequency of the two bucks is always constant and does not change with the load current. If the MODE pin is at a logic low level, the switching regulators operate in an auto PWM/ PSM mode. In this mode, the regulators operate at fixed PWM frequency when the load current is above the power saving current threshold. When the load current falls below the power saving current threshold, the regulator in question enters power saving mode where the switching occurs in bursts. The burst repetition is a function of the current load and the output capacitor value. This operating mode reduces the switching and quiescent current losses. The auto PWM/PSM mode transition is controlled independently for each buck regulator.

The two bucks operate synchronized to each other.

### *Thermal Protection*

In the event that the junction temperature rises above 150°C, the thermal shutdown circuit turns off the converters and the LDO. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 20°C hysteresis is included so that when thermal shutdown occurs, the bucks and LDO do not return to operation until the on-chip temperature drops below 130°C. When coming out of thermal shutdown, soft start is initiated.

### *Undervoltage Lockout*

To protect against battery discharge, undervoltage lockout (UVLO) circuitry is integrated in the system. If the input voltage on VDDA drops below a typical 2.15 V UVLO threshold, all channels shut down. In the buck channels, both the power switch and the synchronous rectifier turn off. When the voltage on VDDA rises above the UVLO threshold, the part is enabled once more.

Alternatively, the user can select device models with a UVLO set at a higher level, suitable for USB applications. For these models, the device hits the turn-off threshold when the input supply drops to 3.65 V typical.

### *Enable/Shutdown*

When all three enable pins are held low, the device is in shutdown mode, and the input current remains below 2 μA.

## BUCK SECTION

The two bucks use a fixed frequency and high speed current mode architecture.

The bucks operate with an input voltage of 2.4 V to 5.5 V.

### *Control Scheme*

The bucks operate with a fixed frequency, current mode PWM control architecture at medium to high loads for high efficiency but shift to a power save mode (PSM) control scheme at light loads to lower the regulation power losses. When operating in fixed frequency PWM mode, the duty cycle of the integrated switches is adjusted and regulates the output voltage. When operating in PSM at light loads, the output voltage is controlled in a hysteretic manner, with higher output voltage ripple. During part of this time, the converter is able to stop switching and enters an idle mode, which improves conversion efficiency.

### *PWM Mode*

In PWM mode, the bucks operate at a fixed frequency of 3 MHz set by an internal oscillator. At the start of each oscillator cycle, the PFET switch is turned on, sending a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current threshold that turns off the PFET switch and turns on the NFET synchronous rectifier. This sends a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle. The buck regulates the output voltage by adjusting the peak inductor current threshold.

### *Power Save Mode (PSM)*

The bucks smoothly transition to PSM operation when the load current decreases below the PSM current threshold. When either of the bucks enter power save mode, an offset is induced in the PWM regulation level, which makes the output voltage rise. When the output voltage reaches a level approximately 1.5% above the PWM regulation level, PWM operation is turned off. At this point, both power switches are off, and the buck enters an idle mode. The output capacitor discharges until the output voltage falls to the PWM regulation voltage, at which point the device drives the inductor to make the output voltage rise again to the upper threshold. This process is repeated while the load current is below the PSM current threshold.

### *PSM Current Threshold*

The PSM current threshold is set to 100 mA. The bucks employ a scheme that enables this current to remain accurately controlled, independent of input and output voltage levels. This scheme also ensures that there is very little hysteresis between the PSM current threshold for entry to and exit from the PSM. The PSM current threshold is optimized for excellent efficiency over all load currents.

### *Oscillator/Phasing of Inductor Switching*

The ADP5022 ensures that both bucks operate at the same switching frequency when both bucks are in PWM mode.

Additionally, the ADP5022 ensures that when both bucks are in PWM mode, they operate out-of-phase, whereby the Buck2 PFET starts conducting exactly half a clock period after the Buck1 PFET starts conducting.

### *Enable/Shutdown*

The bucks start operation with soft start when the EN1 or EN2 pin is toggled from logic low to logic high. Pulling the EN1 or EN2 pin low disables that channel.

### *Short-Circuit Protection*

The bucks include frequency foldback to prevent output current runaway on a hard short. When the voltage at the feedback pin falls below half the target output voltage, indicating the possibility of a hard short at the output, the switching frequency is reduced to half the internal oscillator frequency. The reduction in the switching frequency allows more time for the inductor to discharge, preventing a runaway of output current.

### *Soft Start*

The bucks have an internal soft start function that ramps the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the converter.

### *Current Limit*

Each buck has protection circuitry to limit the amount of positive current flowing through the PFET switch and the amount of negative current flowing through the synchronous rectifier. The positive current limit on the power switch limits the amount of current that can flow from the input to the output. The negative current limit prevents the inductor current from reversing direction and flowing out of the load.

### *100% Duty Operation*

With a drop in input voltage or with an increase in load current, the buck may reach a limit where, even with the PFET switch on 100% of the time, the output voltage drops below the desired output voltage. At this limit, the buck transitions to a mode where the PFET switch stays on 100% of the time. When the input conditions change again and the required duty cycle falls, the buck immediately restarts PWM regulation without allowing overshoot on the output voltage. This is particularly useful in battery-powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. Maintaining regulation is dependent on the input voltage, load current, and output voltage. This can be calculated from the following equation:

$$V_{IN(MIN)} = V_{OUT(MAX)} + I_{LOAD(MAX)} \times (R_{DS(on)MAX} + R_L)$$

where:

$V_{OUT(MAX)}$ is the nominal output voltage plus the maximum tolerance.

$I_{LOAD(MAX)}$ is the maximum load current plus inductor ripple current.

$R_{DS(on)MAX}$ is the maximum P-channel switch $R_{DS(on)}$.

$R_L$ is the DC resistance of the inductor.

## LDO SECTION

The LDO is a low quiescent current, low dropout linear regulator and provides up to 150 mA of output current. Drawing a low 30 µA quiescent current (typical) at full load makes the LDO ideal for battery-operated portable equipment.

The LDO operates with an input voltage of 2.3 V to 5.5 V.

It also provides high power supply rejection ratio (PSRR), low output noise, and excellent line and load transient response with just a small 1 µF ceramic input and output capacitor.

Internally, the LDO consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to flow and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, reducing the current flowing to the output.

### *LDO Undervoltage Lockout*

The ADP5022 integrates an undervoltage lockout function on the VIN3 input voltage, which ensures that the LDO output drive is disabled whenever VIN3 is below a threshold of approximately 2.0 V. Where the ADP5022 is configured to supply VIN3 from either VOUT1 or VOUT2, this ensures that the LDO powers up safely in this cascaded configuration.

# APPLICATIONS INFORMATION

## BUCK EXTERNAL COMPONENT SELECTION

Trade-offs between performance parameters such as efficiency and transient response can be made by varying the choice of external components in the applications circuit, as shown in Figure 1.

### *Inductor*

The high switching frequency of the ADP5022 bucks allows for the selection of small chip inductors. For best performance, use inductor values between 0.7 µH and 3 µH. Suggested inductors are shown in Table 7.

The peak-to-peak inductor current ripple is calculated using the following equation:

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

where:
$f_{SW}$ is the switching frequency.
$L$ is the inductor value.

The minimum dc current rating of the inductor must be greater than the inductor peak current. The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{I_{RIPPLE}}{2}$$

Inductor conduction losses are caused by the flow of current through the inductor, which has an associated internal dc resistance (DCR). Larger sized inductors have smaller DCR, which may decrease inductor conduction losses. Inductor core losses are related to the magnetic permeability of the core material. Because the bucks are high switching frequency dc-to-dc converters, shielded ferrite core material is recommended for its low core losses and low EMI.

**Table 7. Suggested 1.0 µH Inductors**

| Vendor | Model | Dimensions (mm) | $I_{SAT}$ (mA) | DCR (mΩ) |
|---|---|---|---|---|
| Murata | LQM2MPN1R0NG0B | 2.0 × 1.6 × 0.9 | 1400 | 85 |
| Murata | LQM18FN1R0M00B | 1.6 × 0.8 × 0.8 | 150 | 26 |
| Taiyo Yuden | CBMF1608T1R0M | 1.6 × 0.8 × 0.8 | 290 | 90 |
| Coilcraft | EPL2014-102ML | 2.0 × 2.0 × 1.4 | 900 | 59 |
| TDK | GLFR1608T1R0M-LR | 1.6 × 0.8 × 0.8 | 230 | 80 |
| Coilcraft | 0603LS-102 | 1.8 × 1.69 × 1.1 | 400 | 81 |
| Toko | MDT2520-CN | 2.5 × 2.0 × 1.2 | 1350 | 85 |

### Output Capacitor

Higher output capacitor values reduce the output voltage ripple and improve load transient response. When choosing this value, it is also important to account for the loss of capacitance due to output voltage dc bias.

Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

The worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage is calculated using the following equation:

$$C_{EFF} = C_{OUT} \times (1 - TEMPCO) \times (1 - TOL)$$

where:
$C_{EFF}$ is the effective capacitance at the operating voltage.
$TEMPCO$ is the worst-case capacitor temperature coefficient.
$TOL$ is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and $C_{OUT}$ is 9.2481 µF at 1.8 V, as shown in Figure 49.

Substituting these values in the equation yields

$$C_{EFF} = 9.2481\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 7.0747\ \mu F$$

To guarantee the performance of the bucks, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

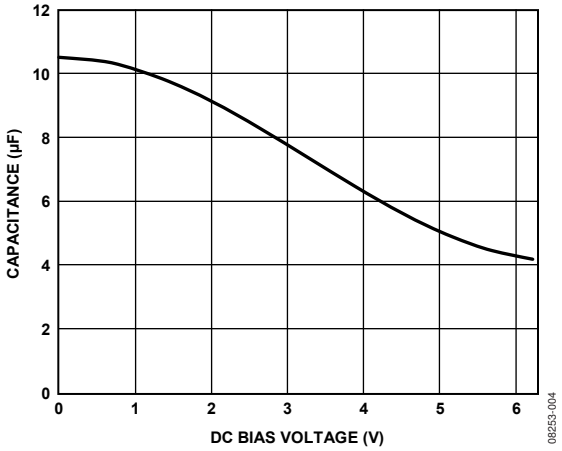


*Figure 49. Typical Capacitor Performance*

The peak-to-peak output voltage ripple for the selected output capacitor and inductor values is calculated using the following equation:

$$V_{RIPPLE} = \frac{V_{IN}}{(2\pi \times f_{SW}) \times 2 \times L \times C_{OUT}} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}}$$

Capacitors with lower equivalent series resistance (ESR) are preferred to guarantee low output voltage ripple, as shown in the following equation:

$$ESR_{COUT} \leq \frac{V_{RIPPLE}}{I_{RIPPLE}}$$

The effective capacitance needed for stability, which includes temperature and dc bias effects, is a minimum of 7 µF and a maximum of 40 µF.

**Table 8. Suggested 10 µF Capacitors**

| Vendor | Type | Model | Case Size | Voltage Rating (V) |
|---|---|---|---|---|
| Murata | X5R | GRM188R60J106 | 0603 | 6.3 |
| Taiyo Yuden | X5R | JMK107BJ475 | 0603 | 6.3 |
| TDK | X5R | C1608JB0J106K | 0603 | 6.3 |
| Panasonic | X5R | ECJ1VB0J106M | 0603 | 6.3 |

The buck regulators require 10 µF output capacitors to guarantee stability and response to rapid load variations and to transition in and out the PWM/PSM modes. In certain applications, where one or both buck regulator powers a processor, the operating state is known because it is controlled by software. In this condition, the processor can drive the MODE pin according to the operating state; consequently, it is possible to reduce the output capacitor from 10 µF to 4.7 µF because the regulator does not expect a large load variation when working in PSM mode, see Figure 50.

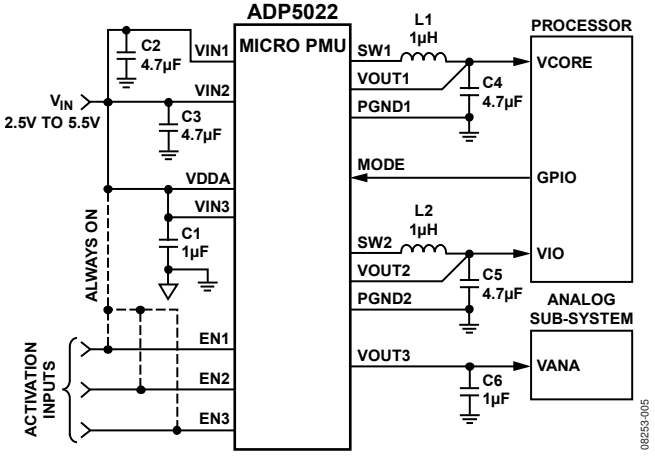


*Figure 50. Processor System Power Management with PSM/PWM Control*

### *Input Capacitor*

Higher value input capacitors help to reduce the input voltage ripple and improve transient response. Maximum input capacitor current is calculated using the following equation:

$$I_{CIN} \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

To minimize supply noise, place the input capacitor as close to the VIN pin of the BUCK as possible. As with the output capacitor, a low ESR capacitor is recommended.

The effective capacitance needed for stability, which includes temperature and dc bias effects, is a minimum of 3 µF and a maximum of 10 µF. A list of suggested capacitors is shown in Table 9.

**Table 9. Suggested 4.7 µF Capacitors**

| Vendor | Type | Model | Case Size | Voltage Rating (V) |
|---|---|---|---|---|
| Murata | X5R | GRM188R60J475ME19D | 0603 | 6.3 |
| Taiyo Yuden | X5R | JMK107BJ475 | 0603 | 6.3 |
| Panasonic | X5R | ECJ-0EB0J475M | 0402 | 6.3 |

## LDO CAPACITOR SELECTION

### *Output Capacitor*

The ADP5022 LDO is designed for operation with small, space-saving ceramic capacitors but functions with most commonly used capacitors as long as care is taken with the ESR value. The ESR of the output capacitor affects stability of the LDO control loop. A minimum of 0.70 µF capacitance with an ESR of 1 Ω or less is recommended to ensure stability of the ADP5022. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP5022 to large changes in load current.

### *Input Bypass Capacitor*

Connecting a 1 µF capacitor from VIN3 to GND reduces the circuit sensitivity to printed circuit board (PCB) layout, especially when long input traces or high source impedance are encountered. If greater than 1 µF of output capacitance is required, increase the input capacitor to match it.

**Table 10. Suggested 1.0 µF Capacitors**

| Vendor | Type | Model | Case Size | Voltage Rating (V) |
|---|---|---|---|---|
| Murata | X5R | GRM155B30J105K | 0402 | 6.3 |
| TDK | X5R | C1005JB0J105KT | 0402 | 6.3 |
| Panasonic | X5R | ECJ0EB0J105K | 0402 | 6.3 |
| Taiyo Yuden | X5R | LMK105BJ105MV-F | 0402 | 10.0 |

### *Input and Output Capacitor Properties*

Use any good quality ceramic capacitors with the ADP5022 as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any LDO because of their poor temperature and dc bias characteristics.

Figure 51 depicts the capacitance vs. voltage bias characteristic of a 0402 1 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

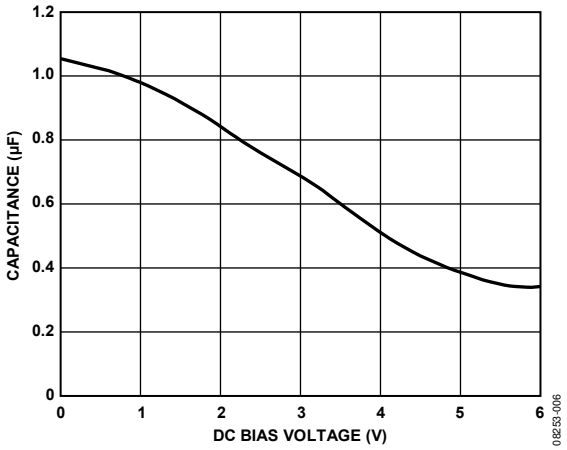


*Figure 51. Capacitance vs. Voltage Characteristic*

Use the following equation to determine the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL)$$

where:
$C_{BIAS}$ is the effective capacitance at the operating voltage.
*TEMPCO* is the worst-case capacitor temperature coefficient.
*TOL* is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10% and $C_{BIAS}$ is 0.94 µF at 1.8 V as shown in Figure 51.

Substituting these values into the following equation.

$$C_{EFF} = 0.94\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP5022, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors are evaluated for each application.

# PCB LAYOUT GUIDELINES

Poor layout can affect ADP5022 performance, causing electromagnetic interference (EMI) and electromagnetic compatibility (EMC) problems, ground bounce, and voltage losses. Poor layout can also affect regulation and stability. A good layout is implemented using the following guidelines:

- Place the inductor, input capacitor, and output capacitor close to the IC using short tracks. These components carry high switching frequencies, and large tracks act as antennas.
- Route the output voltage path away from the inductor and SW node to minimize noise and magnetic interference.
- Maximize the size of ground metal on the component side to help with thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.

# EVALUATION BOARD SCHEMATICS AND ARTWORK

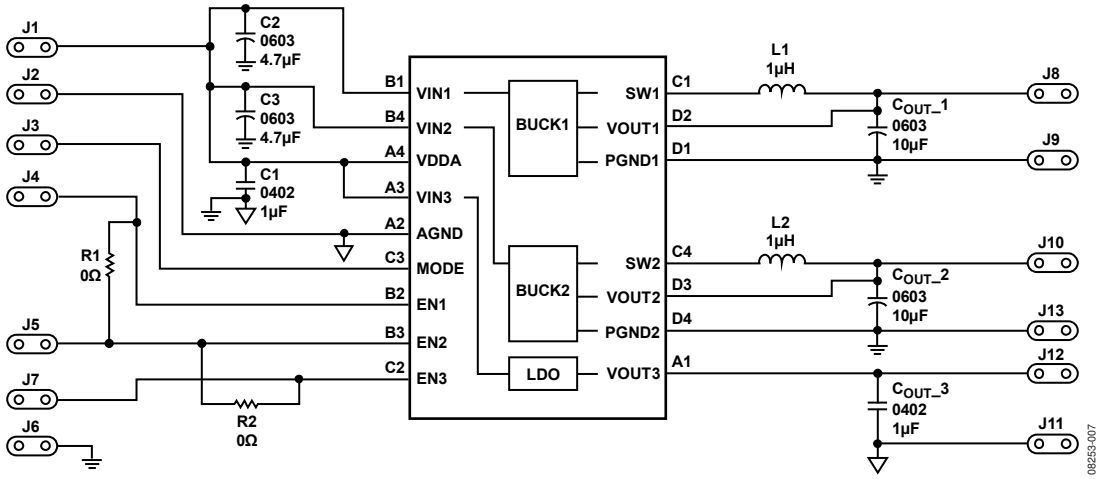


*Figure 52. Evaluation Board Schematic*

## SUGGESTED LAYOUT

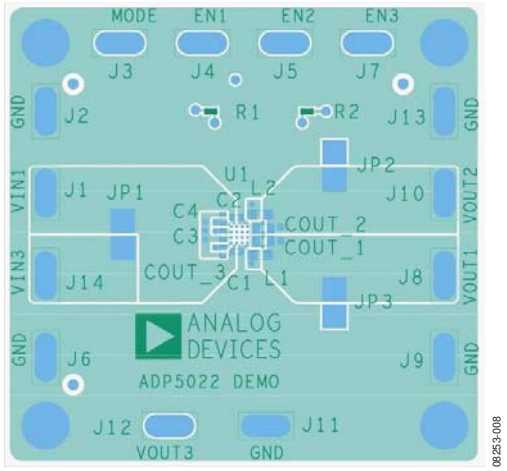


*Figure 53. Top Layer, Recommended Layout*

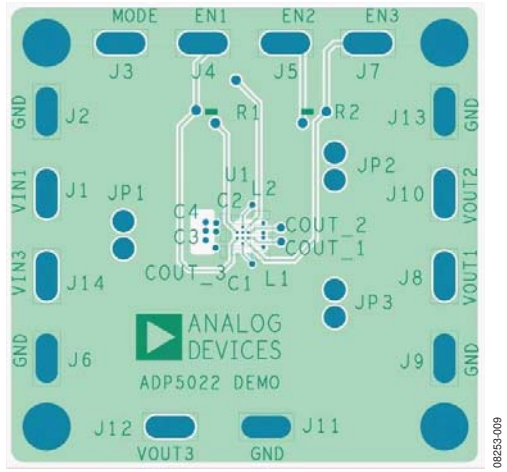


*Figure 54. Second Layer, Recommended Layout*

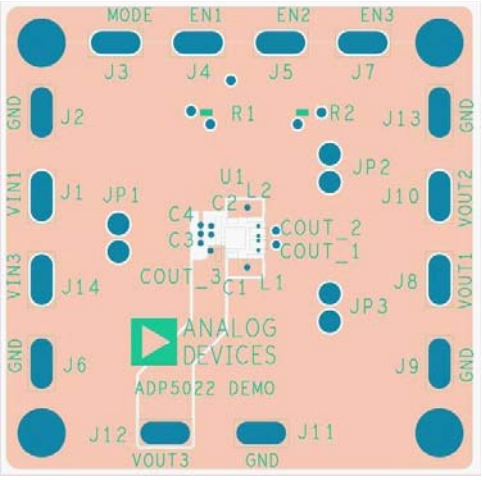


*Figure 55. Third Layer, Recommended Layout*

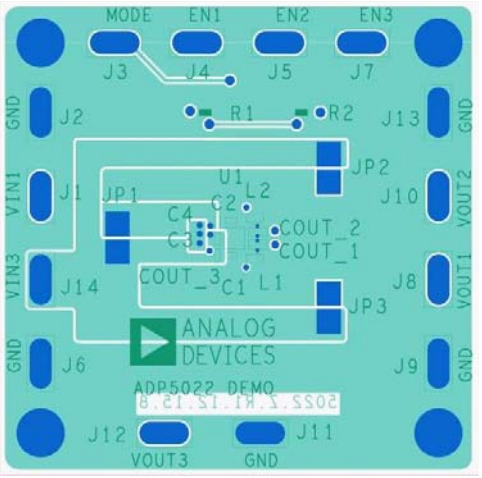


*Figure 56. Bottom Layer, Recommended Layout*