Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Micro PMU with 1.2 A Buck Regulator and Two 300 mA LDOs

Data Sheet

ADP5040

FEATURES

- **Input voltage range: 2.3 V to 5.5 V**
- **One 1.2 A buck regulator**
- **Two 300 mA LDOs**
- **20-lead, 4 mm × 4 mm LFCSP package**
- **Overcurrent and thermal protection**
- **Soft start**
- **Undervoltage lockout**
- **Buck key specifications**
  - **Output voltage range: 0.8 V to 3.8 V**
  - **Current mode topology for excellent transient response**
  - **3 MHz operating frequency**
  - **Peak efficiency up to 96%**
  - **Uses tiny multilayer inductors and capacitors**
  - **Mode pin selects forced PWM or auto PWM/PSM modes**
  - **100% duty cycle low dropout mode**
- **LDOs key specifications**
  - **Output voltage range: 0.8 V to 5.2 V**
  - **Low V_{IN} from 1.7 V to 5.5 V**
  - **Stable with 2.2 µF ceramic output capacitors**
  - **High PSRR**
  - **Low output noise**
  - **Low dropout voltage**
  - **−40°C to +125°C junction temperature range**

GENERAL DESCRIPTION

The ADP5040 combines one high performance buck regulator and two low dropout regulators (LDO) in a small 20-lead LFCSP to meet demanding performance and board space requirements.

The high switching frequency of the buck regulator enables the use of tiny multilayer external components and minimizes board space.

When the MODE pin is set to logic high, the buck regulator operates in forced pulse width modulation (PWM) mode. When the MODE pin is set to logic low, the buck regulator operates in PWM mode when the load is around the nominal value. When the load current falls below a predefined threshold the regulator operates in power save mode (PSM) improving the light-load efficiency. The low quiescent current, low dropout voltage, and wide input voltage range of the ADP5040 LDOs extend the battery life of portable devices. The ADP5040 LDOs maintain a power supply rejection greater than 60 dB for frequencies as high as 10 kHz while operating with a low headroom voltage.

Each regulator in the ADP5040 is activated by a high level on the respective enable pin. The output voltages of the regulators are programmed though external resistor dividers to address a variety of applications.

FUNCTIONAL BLOCK DIAGRAM

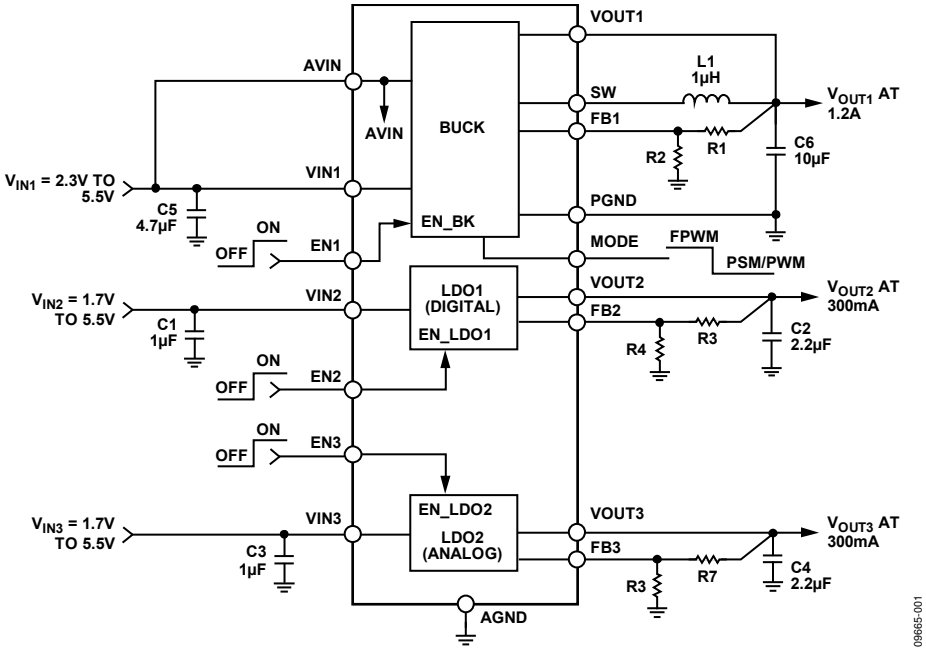

Figure 1.

Rev. B Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

ADP5040* PRODUCT PAGE QUICK LINKS

Last Content Update: 03/09/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADP5040 Evaluation Board

DOCUMENTATION

Data Sheet

- ADP5040: Micro PMU with 1.2A Buck Regulator and Two 300 mA LDOs Data Sheet

TOOLS AND SIMULATIONS

- 5V uPMU BuckDesigner
- ADIsimPower™ Voltage Regulator Design Tool

REFERENCE MATERIALS

Press

- Multi-output Regulators with Supervisory and Watchdog Timers Reduce Component Count, Increase Power Density and Reliability

Solutions Bulletins & Brochures

- Integrated Power Solutions for Altera FPGAs
- Integrated, High Power Solutions for Xilinx FPGAs

Technical Articles

- Isolation Architecture, Circuit, and Component Selection in Power Inverter Applications

DESIGN RESOURCES

- ADP5040 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADP5040 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

3/2017—Rev. A to Rev. B

Changes to Figure 2 and Table 7 ... 8

1/2014—Rev. 0 to Rev. A

Change to Figure 1 ... 1
Change to Figure 106 ... 30
Change to Figure 108 ... 33
Change to Figure 109 ... 34

12/2011—Revision 0: Initial Version

SPECIFICATIONS

GENERAL SPECIFICATIONS

AVIN, VIN1 = 2.3 V to 5.5 V; AVIN, VIN1 ≥VIN2, VIN3; VIN2, VIN3 = 1.7 V to 5.5 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Description	Min	Typ	Max	Unit
AVIN UNDERVOLTAGE LOCKOUT	$UVLO_{AVIN}$					
Input Voltage Rising	$UVLO_{AVINRISE}$					
Option 0					2.275	V
Option 1					3.9	V
Input Voltage Falling	$UVLO_{AVINFALL}$					
Option 0			1.95			V
Option 1			3.1			V
SHUTDOWN CURRENT	I_{GND-SD}	ENx = GND		0.1	2	µA
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			20		°C
START-UP TIME[1]						
BUCK	t_{START1}			250		µs
LDO1, LDO2	t_{START2}	V_{OUT2}, V_{OUT3} = 3.3 V		85		µs
Enx, MODE, INPUTS						
Input Logic High	V_{IH}	2.5 V ≤ AVIN ≤ 5.5 V	1.2			V
Input Logic Low	V_{IL}	2.5 V ≤ AVIN ≤ 5.5 V			0.4	V
Input Leakage Current	$V_{I-LEAKAGE}$	ENx = AVIN or GND		0.05	1	µA

[1] Start-up time is defined as the time from the moment EN1 = EN2 = EN3 transfers from 0 V to V_{AVIN} to the moment VOUT1, VOUT2, and VOUT3 reach 90% of their nominal level. Start-up times are shorter for individual channels if another channel is already enabled. See the Typical Performance Characteristics section for more information.

BUCK SPECIFICATIONS

AVIN, VIN1 = 2.3 V to 5.5 V; V_{OUT1} = 1.8 V; L = 1 µH; C_{IN} = 10 µF; C_{OUT} = 10 µF; T_J= −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.[1]

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Voltage Range	V_{IN1}		2.3		5.5	V
OUTPUT CHARACTERISTICS						
Output Voltage Accuracy	V_{OUT1}	PWM mode, I_{LOAD} = 0 mA to 1200 mA	−3		+3	%
Line Regulation	$(\Delta V_{OUT1}/V_{OUT1})/\Delta V_{IN1}$	PWM mode		−0.05		%/V
Load Regulation	$(\Delta V_{OUT1}/V_{OUT1})/\Delta I_{OUT1}$	I_{LOAD} = mA to 1200 mA, PWM mode		−0.1		%/A
VOLTAGE FEEDBACK	V_{FB1}		0.485	0.5	0.515	V
PWM TO POWER SAVE MODE CURRENT THRESHOLD	I_{PSM_L}			100		mA
INPUT CURRENT CHARACTERISTICS		MODE = ground				
DC Operating Current	I_{NOLOAD}	I_{LOAD} = 0 mA, device not switching, all other channels disabled		21	35	µA
Shutdown Current	I_{SHTD}	EN1 = 0 V, $T_A = T_J$ = −40°C to +125°C		0.2	1.0	µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SW CHARACTERISTICS						
SW On Resistance	R_{PFET}	PFET, AVIN = VIN1 = 3.6 V		180	240	mΩ
		PFET, AVIN = VIN1 = 5 V		140	190	mΩ
	R_{NFET}	NFET, AVIN = VIN1 = 3.6 V		170	235	mΩ
		NFET, AVIN = VIN1 = 5 V		150	210	mΩ
Current Limit	I_{LIMIT}	PFET switch peak current limit	1600	1950	2300	mA
ACTIVE PULL-DOWN		EN1 = 0 V		85		Ω
OSCILLATOR FREQUENCY	F_{OSC}		2.5	3.0	3.5	MHz

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

LDO1, LDO2 SPECIFICATIONS

V_{IN2}, V_{IN3} = (V_{OUT2},V_{OUT3} + 0.5 V) or 1.7 V (whichever is greater) to 5.5 V; AVIN, VIN1 ≥ VIN2, VIN3; C_{IN} = 1 µF, C_{OUT} = 2.2 µF; T_J= −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted. [1]

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN2}, V_{IN3}	T_J = −40°C to +125°C	1.7		5.5	V
OPERATING SUPPLY CURRENT						
Bias Current per LDO[2]	$I_{VIN2BIAS}$/$I_{VIN3BIAS}$	I_{OUT3} = I_{OUT4} = 0 µA		10	30	µA
		I_{OUT2} = I_{OUT3} = 10 mA		60	100	µA
		I_{OUT2} = I_{OUT3} = 300 mA		165	245	µA
Total System Input Current	I_{IN}	Includes all current into AVIN, VIN1, VIN2 and VIN3				
LDO1 or LDO2 Only		I_{OUT2} = I_{OUT3} = 0 µA, all other channels disabled		53		µA
LDO1 and LDO2 Only		I_{OUT2} = I_{OUT3} = 0 µA, buck disabled		74		µA
OUTPUT VOLTAGE ACCURACY	V_{OUT2}, V_{OUT3}	100 µA < I_{OUT2} < 300 mA, 100 µA < I_{OUT3} < 300 mA V_{IN2} = (V_{OUT2} + 0.5 V) to 5.5 V, V_{IN3} = (V_{OUT3} + 0.5 V) to 5.5 V	−3		+3	%
REFERENCE VOLTAGE	V_{FB2}, V_{FB3}		0.485	0.500	0.515	V
REGULATION						
Line Regulation	($\Delta V_{OUT2}/V_{OUT2}$)/ΔV_{IN2} ($\Delta V_{OUT3}/V_{OUT3}$)/ΔV_{IN3}	V_{IN2} = (V_{OUT2} + 0.5 V) to 5.5 V V_{IN3} = (V_{OUT3} + 0.5 V) to 5.5 V I_{OUT2} = I_{OUT3} = 1 mA	−0.03		+0.03	%/V
Load Regulation[3]	($\Delta V_{OUT2}/V_{OUT2}$)/ΔI_{OUT2} ($\Delta V_{OUT3}/V_{OUT3}$)/ΔI_{OUT3}	I_{OUT2} = I_{OUT3} = 1 mA to 300 mA		0.002	0.0075	%/mA
DROPOUT VOLTAGE[4]	$V_{DROPOUT}$					
		V_{OUT2} = V_{OUT3} = 5.0 V, I_{OUT2} = I_{OUT3} = 300 mA		72		mV
		V_{OUT2} = V_{OUT3} = 3.3 V, I_{OUT2} = I_{OUT3} = 300 mA		86	140	mV
		V_{OUT2} = V_{OUT3} = 2.5 V, I_{OUT2} = I_{OUT3} = 300 mA		107		mV
		V_{OUT2} = V_{OUT3} = 1.8 V, I_{OUT2} = I_{OUT3} = 300 mA		180		mV
ACTIVE PULL-DOWN	R_{PDLDO}	EN2/EN3 = 0 V		600		Ω
CURRENT-LIMIT THRESHOLD[5]	I_{LIMIT}	T_J = −40°C to +125°C	335	470		mA
OUTPUT NOISE	$OUT_{LDO2NOISE}$	10 Hz to 100 kHz, V_{IN3} = 5 V, V_{OUT3} = 3.3 V		123		µV rms
		10 Hz to 100 kHz, V_{IN3} = 5 V, V_{OUT3} = 2.8 V		110		µV rms
		10 Hz to 100 kHz, V_{IN3} = 5 V, V_{OUT3} = 1.5 V		59		µV rms
	$OUT_{LDO1NOISE}$	10 Hz to 100 kHz, V_{IN2} = 5 V, V_{OUT2} = 3.3 V		140		µV rms
		10 Hz to 100 kHz, V_{IN2} = 5 V, V_{OUT2} = 2.8 V		129		µV rms
		10 Hz to 100 kHz, V_{IN2} = 5 V, V_{OUT2} = 1.5 V		66		µV rms

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY REJECTION RATIO	PSRR	1 kHz, V_{IN2}, V_{IN3} = 3.3 V, V_{OUT2}, V_{OUT3} = 2.8 V, I_{OUT} = 100 mA		66		dB
		100 kHz, V_{IN2}, V_{IN3} = 3.3 V, V_{OUT2}, V_{OUT3} = 2.8 V, I_{OUT} = 100 mA		57		dB
		1 MHz, V_{IN2}, V_{IN3} = 3.3 V, V_{OUT2}, V_{OUT3} = 2.8 V, I_{OUT} = 100 mA		60		dB

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
[2] This is the input current into V_{IN2} and V_{IN3}, which is not delivered to the output load.
[3] Based on an end-point calculation using 1 mA and 300 mA loads.
[4] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 1.7 V.
[5] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V, or 2.7 V.

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

Table 4.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CAPACITANCE (BUCK)[1]	C_{MIN1}	T_J = −40°C to +125°C	4.7		40	µF
OUTPUT CAPACITANCE (BUCK)[2]	C_{MIN2}	T_J = −40°C to +125°C	7		40	µF
INPUT AND OUTPUT CAPACITANCE[3] (LDO1, LDO2)	C_{MIN34}	T_J = −40°C to +125°C	0.70			µF
CAPACITOR ESR	R_{ESR}	T_J = −40°C to +125°C	0.001		1	Ω

[1] The minimum input capacitance should be greater than 4.7 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended, whereas Y5V and Z5U capacitors are not recommended for use with the buck.
[2] The minimum output capacitance should be greater than 7 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended, whereas Y5V and Z5U capacitors are not recommended for use with the buck.
[3] The minimum input and output capacitance should be greater than 0.70 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended, whereas Y5V and Z5U capacitors are not recommended for use with LDOs.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVIN to AGND	−0.3 V to +6 V
VIN1 to AVIN	−0.3 V to +0.3 V
PGND to AGND	−0.3 V to +0.3 V
VIN2, VIN3, VOUTx, ENx, MODE, FBx, SW to AGND	−0.3 V to (AVIN + 0.3 V)
SW to PGND	−0.3 V to (VIN1 + 0.3 V)
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020
ESD Human Body Model	3000 V
ESD Charged Device Model	1500 V
ESD Machine Model	200 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead, 0.5 mm pitch LFCSP	38	4.2	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

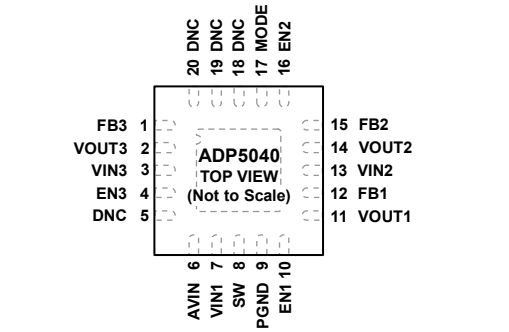

Figure 2. Pin Configuration—View from Top of the Die

Table 7. Preliminary Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FB3	LDO2 Feedback Input.
2	VOUT3	LDO2 Output Voltage.
3	VIN3	LDO2 Input Supply (1.7 V to 5.5 V).
4	EN3	Enable LDO2. EN3 = high: turn on LDO2; EN3 = low: turn off LDO2.
6	AVIN	Housekeeping Input Supply (2.3 V to 5.5 V).
7	VIN1	Buck Input Supply (2.3 V to 5.5 V).
8	SW	Buck Switching Node.
9	PGND	Dedicated Power Ground for Buck Regulator.
10	EN1	Enable Buck. EN1 = high: turn on buck; EN1 = low: turn off buck.
11	VOUT1	Buck Output Sensing Node.
12	FB1	Buck Feedback Input.
13	VIN2	LDO1 Input Supply (1.7 V to 5.5 V).
14	VOUT2	LDO1 Output Voltage.
15	FB2	LDO1 Feedback Input.
16	EN2	Enable LDO1. EN2 = high: turn on LDO1; EN2 = low: turn off LDO1.
17	MODE	Buck Mode. Mode = high: buck regulator operates in fixed PWM mode; mode = low: buck regulator operates in power save mode (PSM) at light load and in constant PWM at higher load.
5, 18, 19, 20	DNC	Do Not Connect. Do not connect this pin.
0	EPAD	Exposed Pad. (AGND = Analog Ground). The exposed pad must be connected to the system ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

VIN1 = VIN2 = VIN3 = AVIN = 5.0 V, T_A = 25°C, unless otherwise noted.

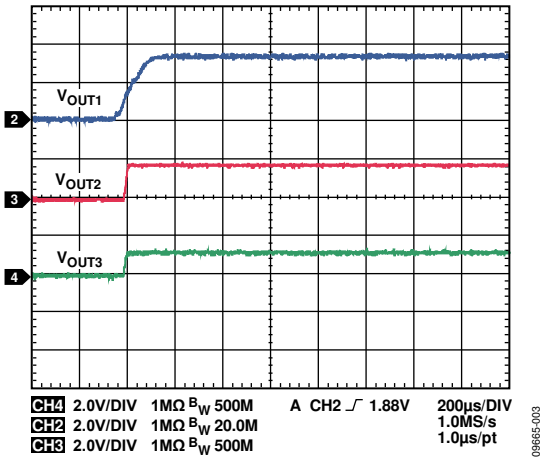

Figure 3. 3-Channel Start-Up Waveforms

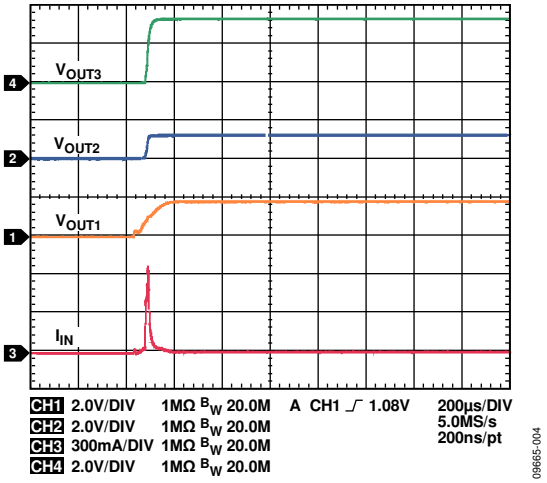

Figure 4. Total Inrush Current, All Channels Started Simultaneously

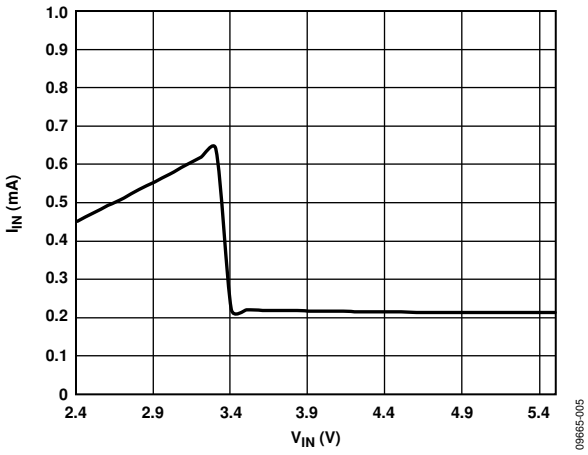

Figure 5. System Quiescent Current (Sum of All the Input Currents) vs. Input Voltage
V_{OUT1} = 1.8 V, V_{OUT2} = V_{OUT3} = 3.3 V (UVLO = 3.3 V)

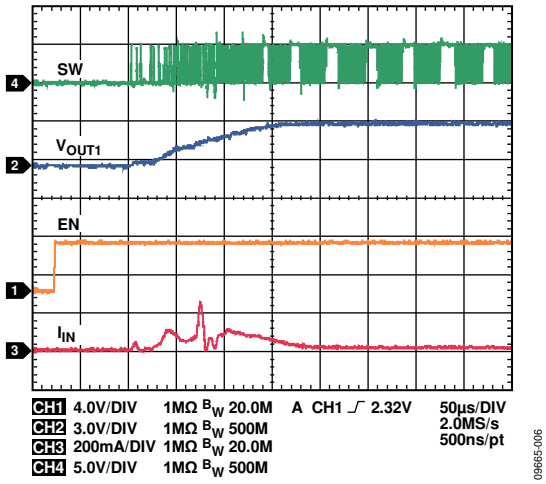

Figure 6. Buck Startup, V_{OUT1} = 3.3 V, I_{OUT2} = 20 mA

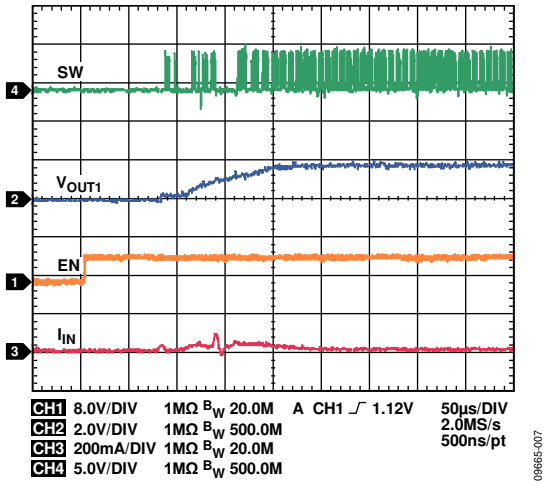

Figure 7. Buck Startup, V_{OUT1} = 1.8 V, I_{OUT} = 20 mA

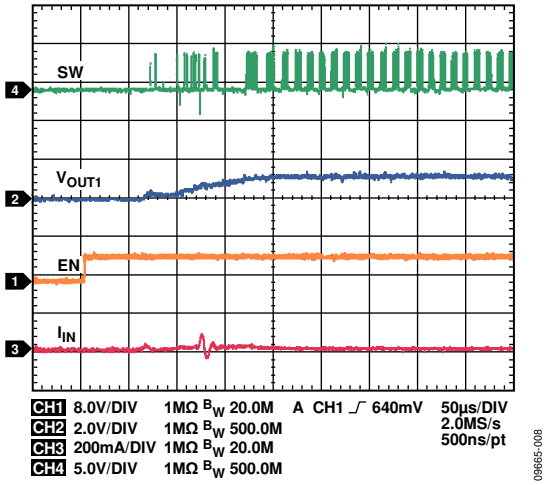

Figure 8. Buck Startup, V_{OUT1} = 1.2 V, I_{OUT} = 20 mA

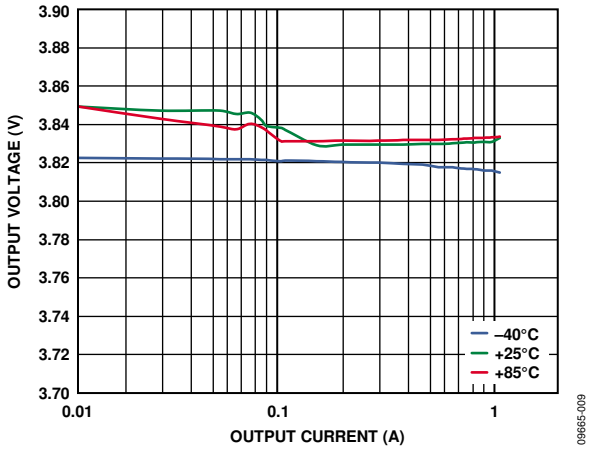

Figure 9. Buck Load Regulation Across Temperature, V_{OUT1} = 3.8 V, Auto Mode

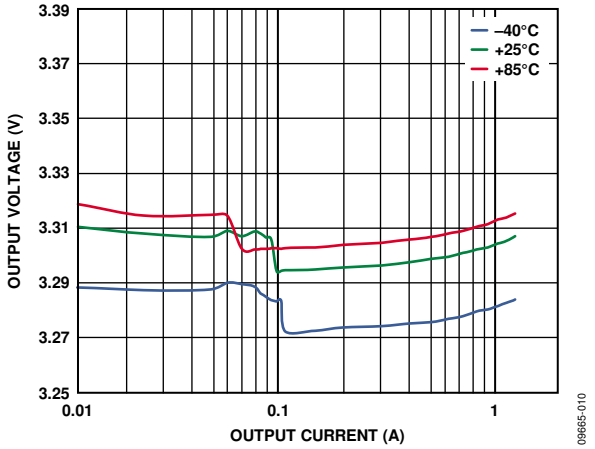

Figure 10. Buck Load Regulation Across Temperature, V_{OUT1} = 3.3 V, Auto Mode

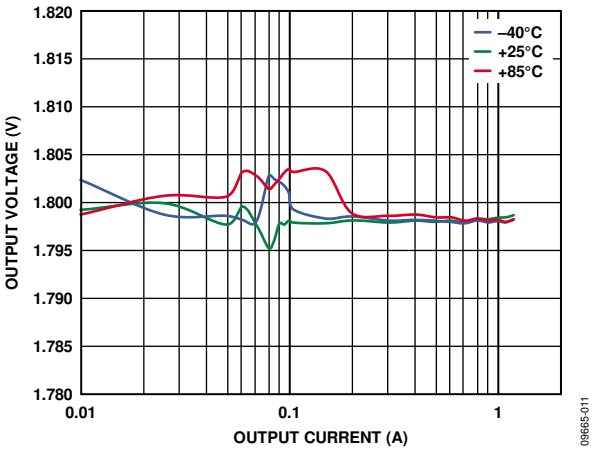

Figure 11. Buck Load Regulation Across Temperature, V_{OUT1} = 1.8 V, Auto Mode

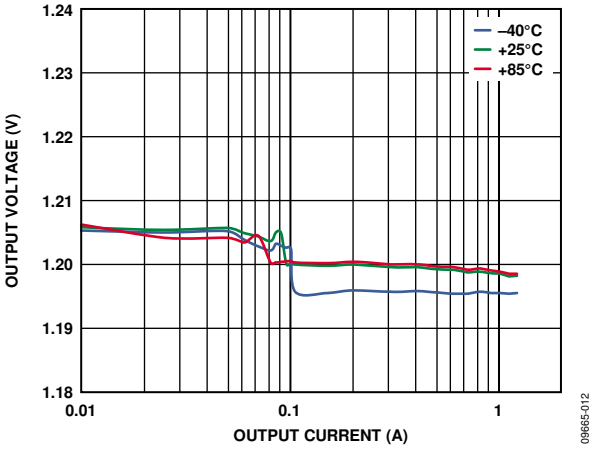

Figure 12. Buck Load Regulation Across Temperature, V_{OUT1} = 1.2 V, Auto Mode

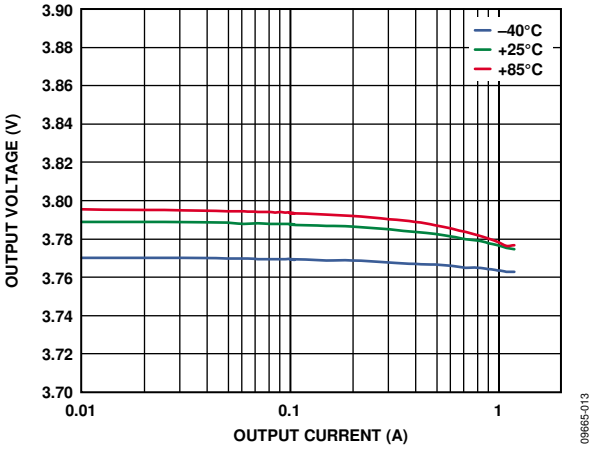

Figure 13. Buck Load Regulation Across Temperature, V_{OUT1} = 3.8 V, PWM Mode

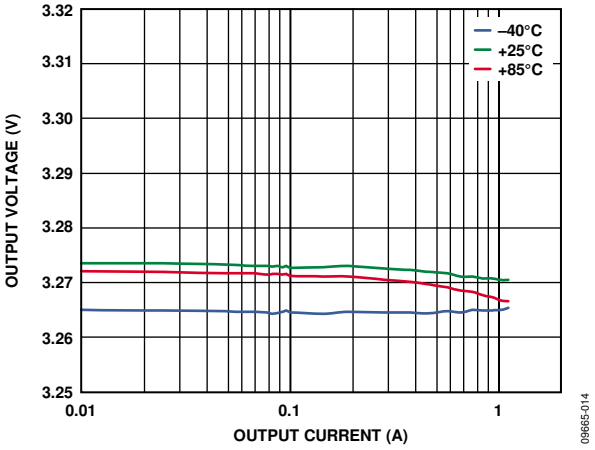

Figure 14. Buck Load Regulation Across Temperature, V_{OUT1} = 3.3 V, PWM Mode

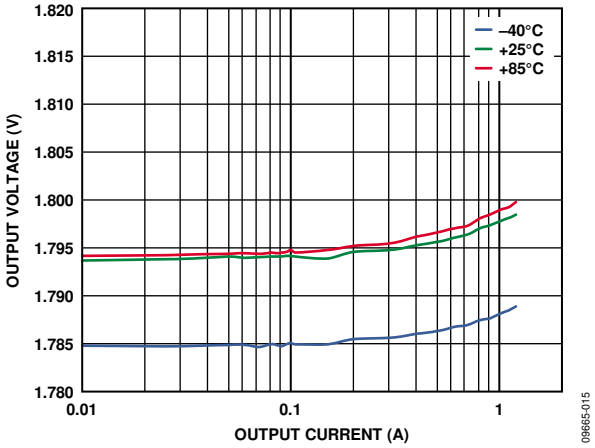

Figure 15. Buck Load Regulation Across Temperature, V_{OUT1} = 1.8 V, PWM Mode

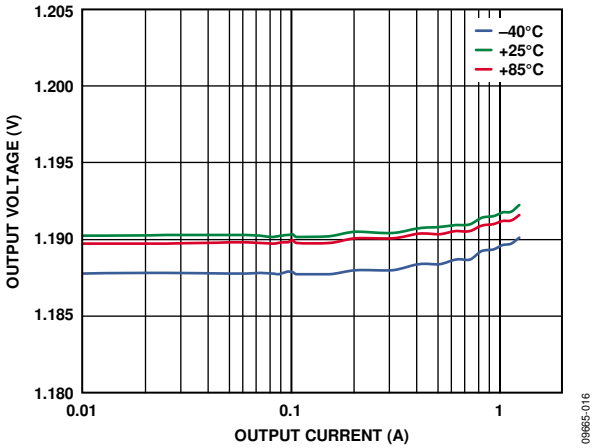

Figure 16. Buck Load Regulation Across Temperature, V_{OUT1} = 1.2 V, PWM Mode

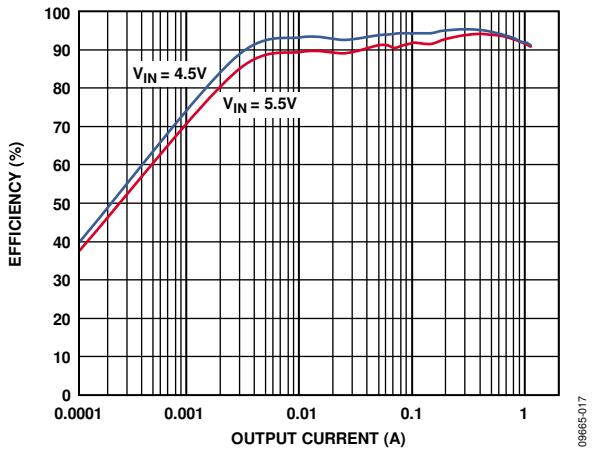

Figure 17. Buck Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 3.8 V, Auto Mode

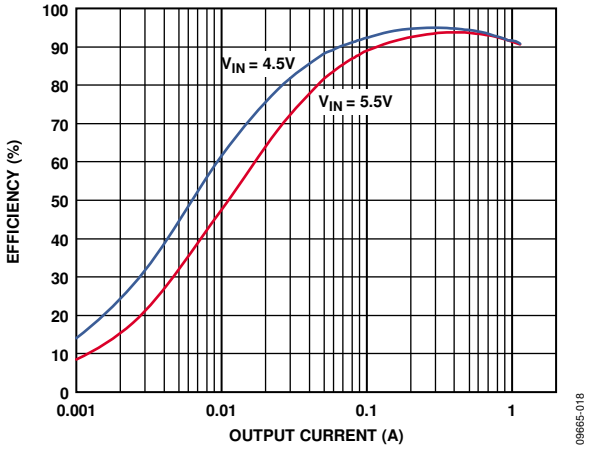

Figure 18. Buck Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 3.8 V, PWM Mode

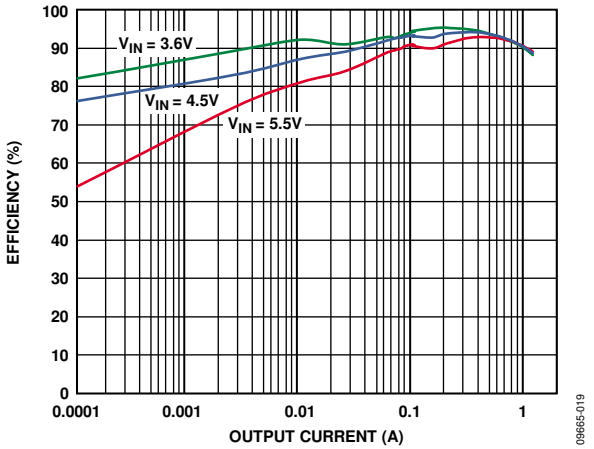

Figure 19. Buck Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 3.3 V, Auto Mode

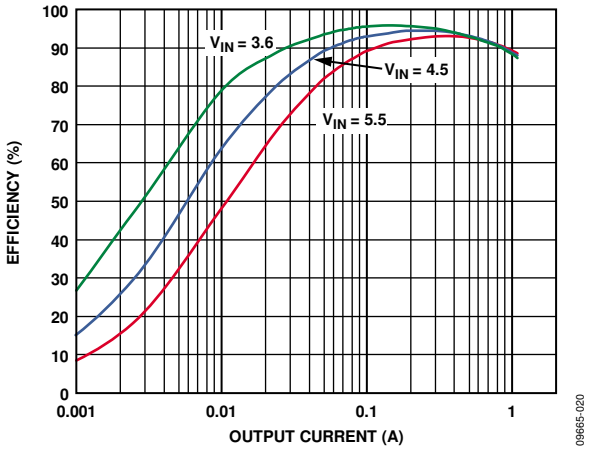

Figure 20. Buck Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 3.3 V, PWM Mode

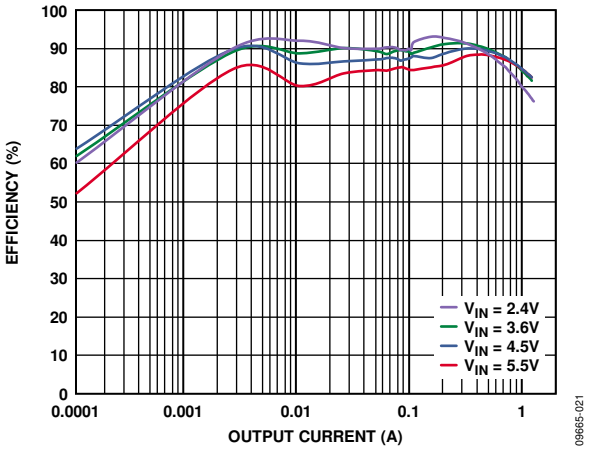

Figure 21. Buck Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 1.8 V, Auto Mode

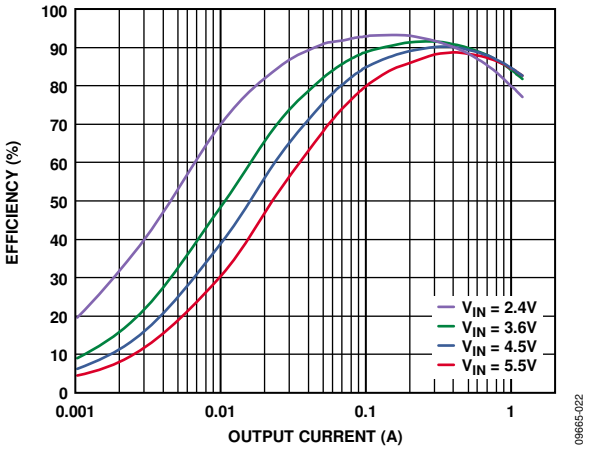

Figure 22. Buck Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 1.8 V, PWM Mode

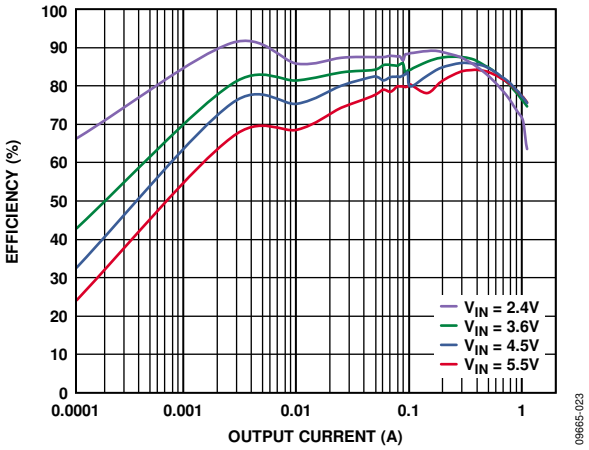

Figure 23. Buck Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 1.2 V, Auto Mode

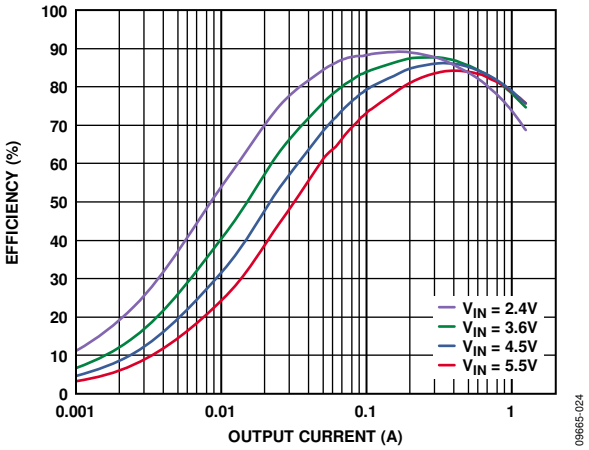

Figure 24. Buck Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 1.2 V, PWM Mode

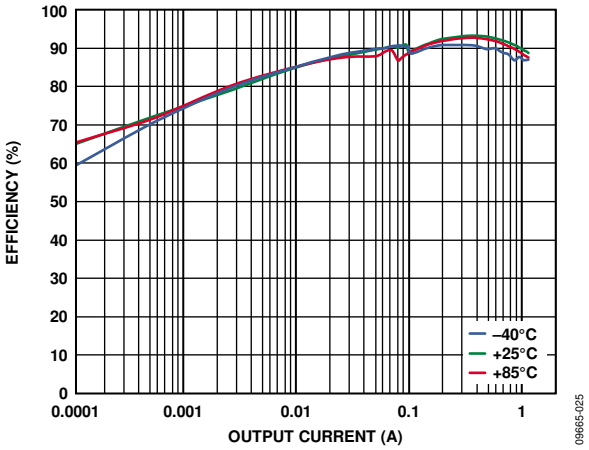

Figure 25. Buck Efficiency vs. Load Current, Across Temperature, V_{IN} = 5.0 V, V_{OUT1} = 3.3 V, Auto Mode

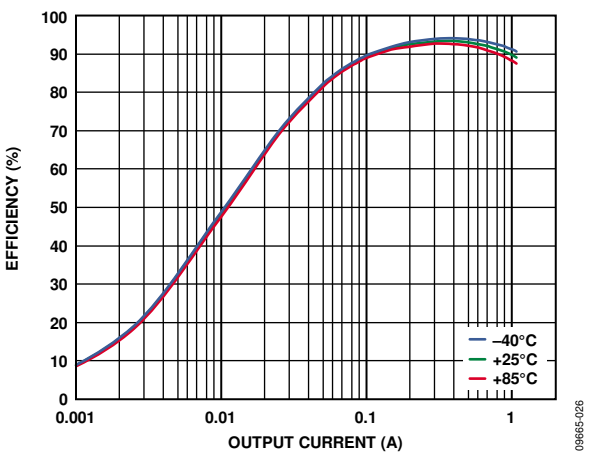

Figure 26. Buck Efficiency vs. Load Current, Across Temperature, V_{IN} = 5.0 V, V_{OUT1} = 3.3 V, PWM Mode

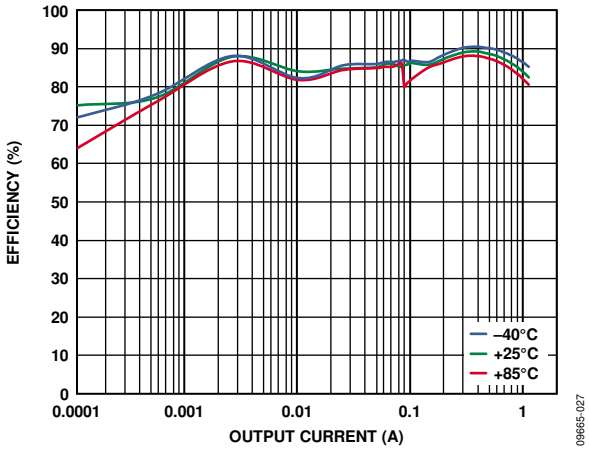

Figure 27. Buck Efficiency vs. Load Current, Across Temperature, V_{IN} = 5.0 V, V_{OUT1} = 1.8 V, Auto Mode

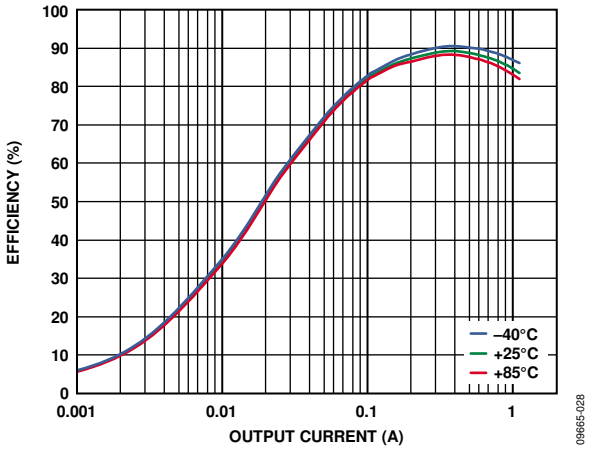

Figure 28. Buck Efficiency vs. Load Current, Across Temperature, V_{IN} = 5.0 V, V_{OUT1} = 1.8 V, PWM Mode

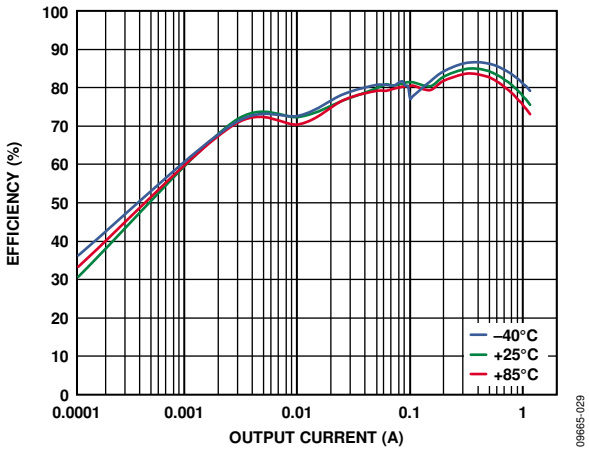

Figure 29. Buck Efficiency vs. Load Current, Across Temperature, V_{IN} = 5.0 V, V_{OUT1} = 1.2 V, Auto Mode

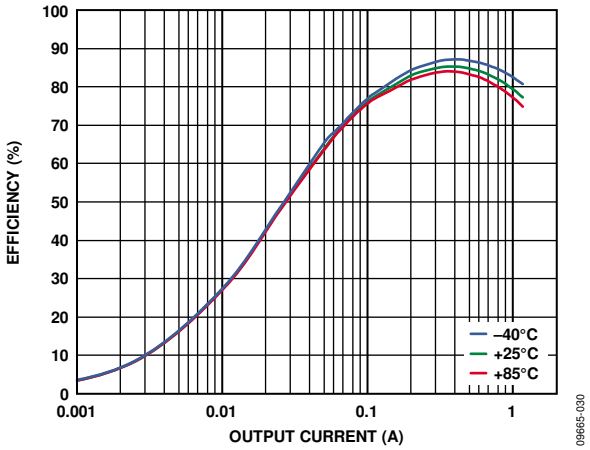

Figure 30. Buck Efficiency vs. Load Current, Across Temperature, V_{IN} = 5.0 V, V_{OUT1} = 1.2 V, PWM Mode

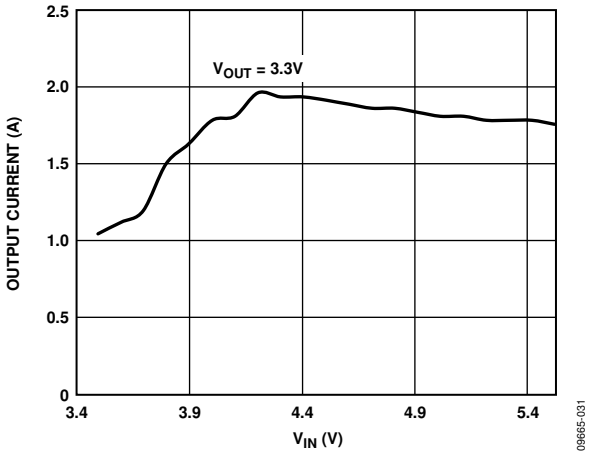

Figure 31. Buck DC Current Capability vs. Input Voltage

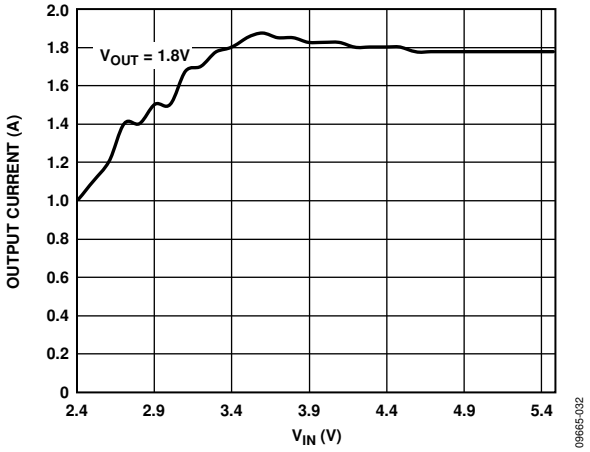

Figure 32. Buck DC Current Capability vs. Input Voltage

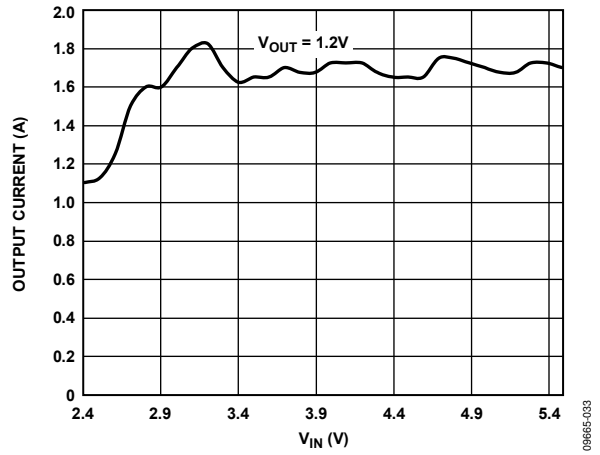

Figure 33. Buck DC Current Capability vs. Input Voltage

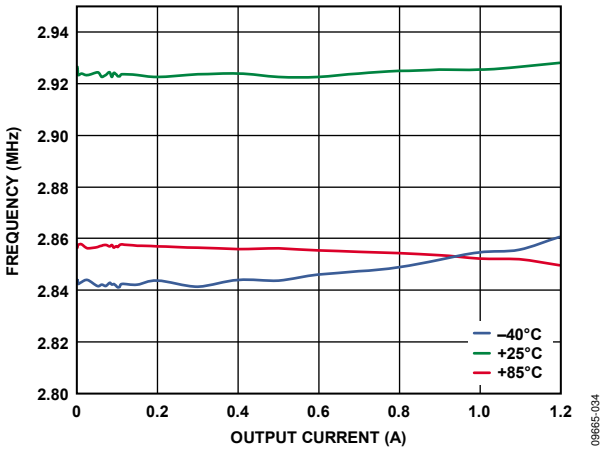

Figure 34. Buck Switching Frequency vs. Output Current, Across Temperature, V_{OUT1} = 1.8 V, PWM Mode

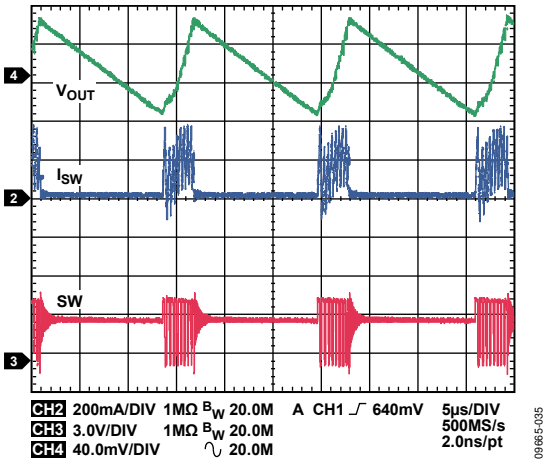

Figure 35. Typical Waveforms, V_{OUT1} = 3.3 V, I_{OUT1} = 30 mA, Auto Mode

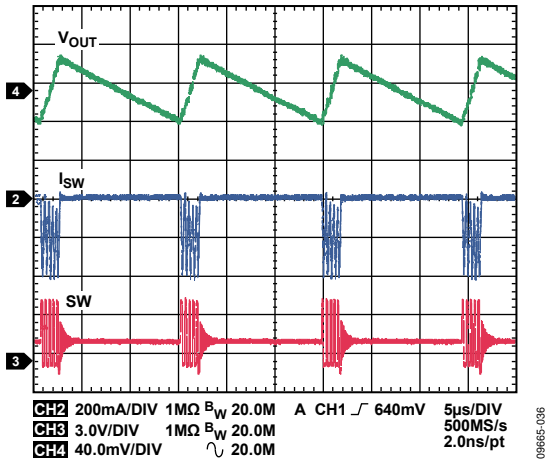

Figure 36. Typical Waveforms, V_{OUT1} = 1.8 V, I_{OUT1} = 30 mA, Auto Mode

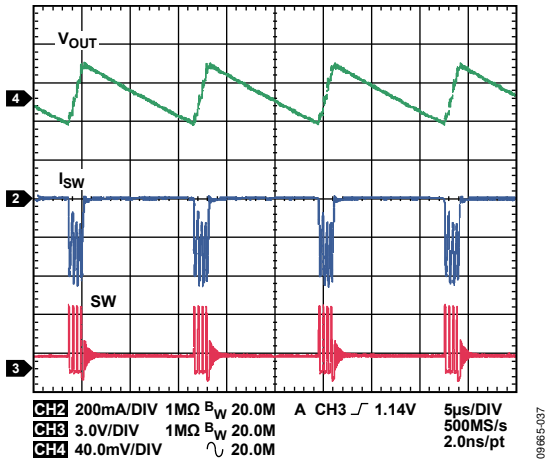

Figure 37. Typical Waveforms, V_{OUT1} = 1.2 V, I_{OUT1} = 30 mA, Auto Mode

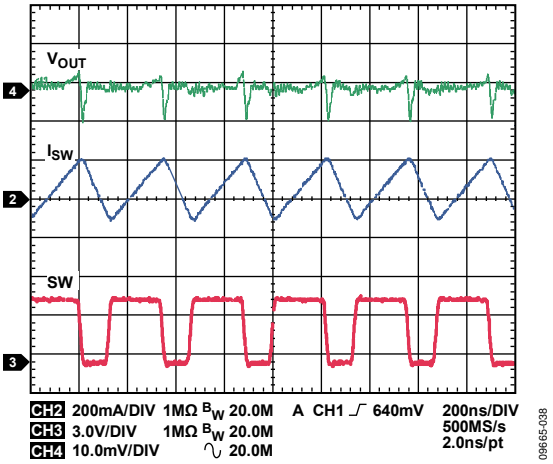

Figure 38. Typical Waveforms, V_{OUT1} = 3.3 V, I_{OUT1} = 30 mA, PWM Mode

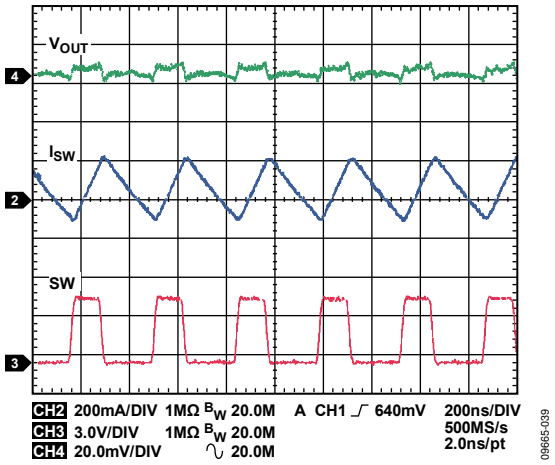

Figure 39. Typical Waveforms, V_{OUT1} = 1.8 V, I_{OUT1} = 30 mA, PWM Mode

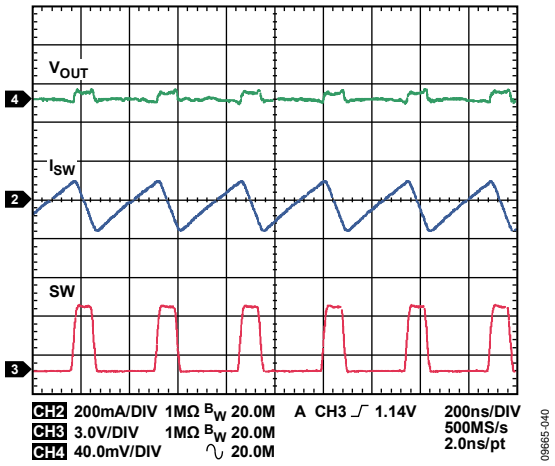

Figure 40. Typical Waveforms, V_{OUT1} = 1.2 V, I_{OUT1} = 30 mA, PWM Mode

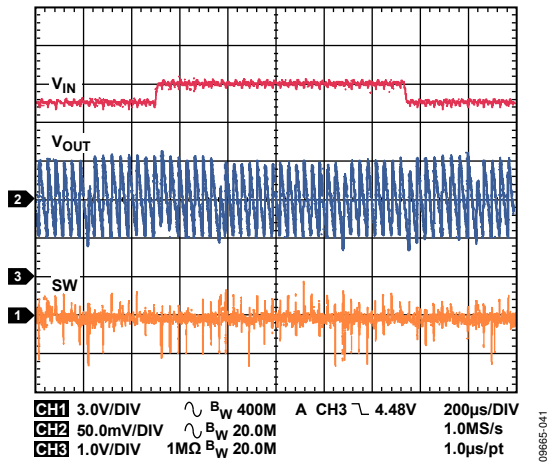

Figure 41. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, V_{OUT1} = 3.3 V, I_{OUT1} = 5 mA, Auto Mode

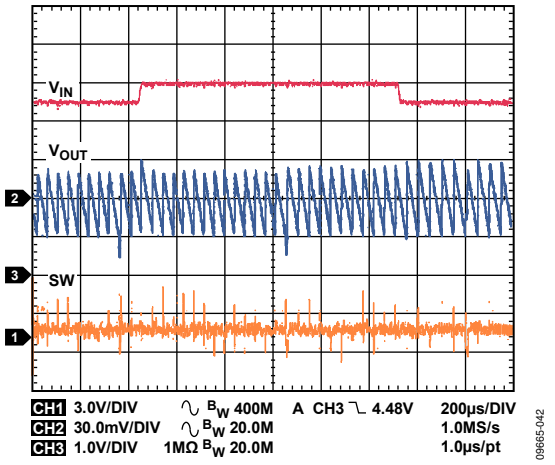

Figure 42. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, V_{OUT1} = 1.8 V, I_{OUT1} = 5 mA, Auto Mode

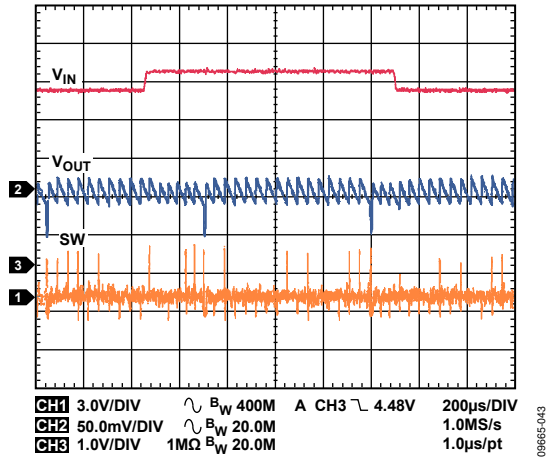

Figure 43. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, V_{OUT1} = 1.2 V, I_{OUT1} = 5 mA, Auto Mode

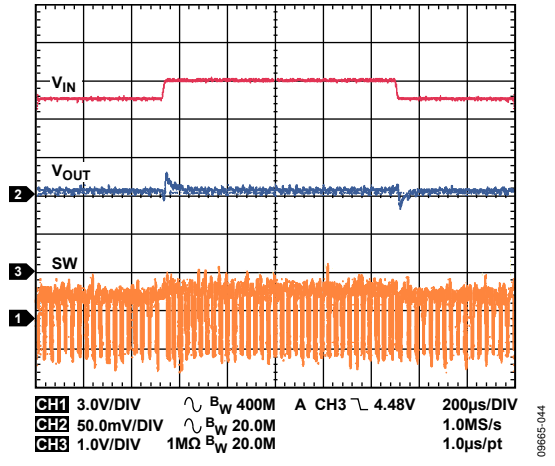

Figure 44. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, V_{OUT1} = 3.3 V, PWM Mode

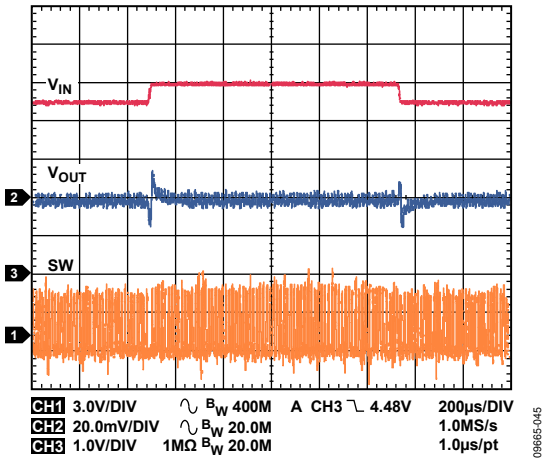

Figure 45. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, V_{OUT1} = 1.8 V, PWM Mode

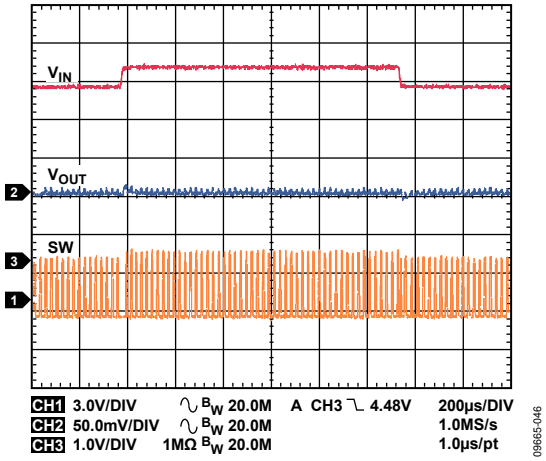

Figure 46. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, V_{OUT1} = 1.2 V, PWM Mode

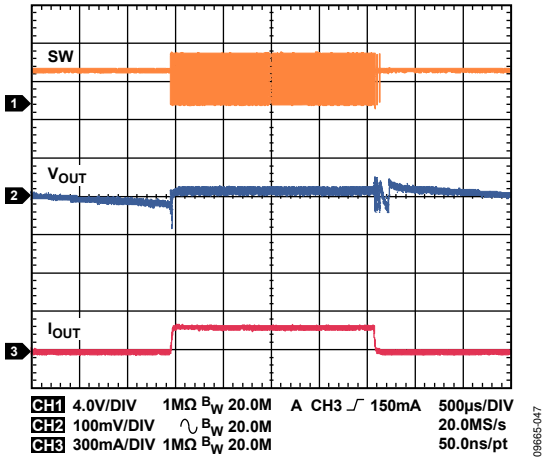

Figure 47. Buck Response to Load Transient, I_{OUT1} = 20 mA to 200 mA, V_{OUT1} = 3.3 V, Auto Mode

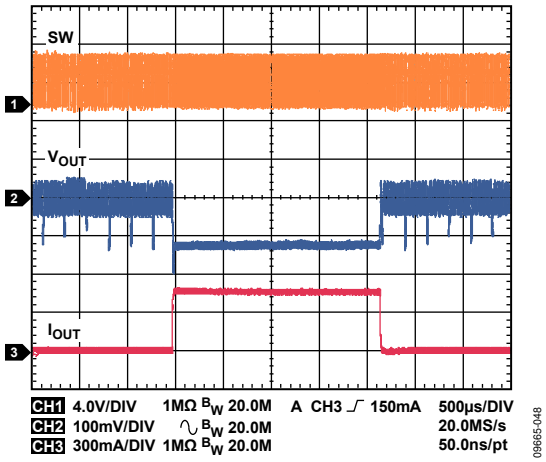

Figure 48. Buck Response to Load Transient, I_{OUT1} = 50 mA to 500 mA, V_{OUT1} = 3.3 V, Auto Mode

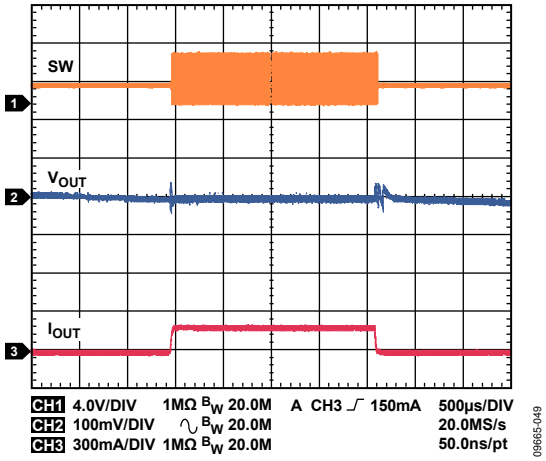

Figure 49. Buck Response to Load Transient, I_{OUT1} = 20 mA to 200 mA, V_{OUT1} = 1.8 V, Auto Mode

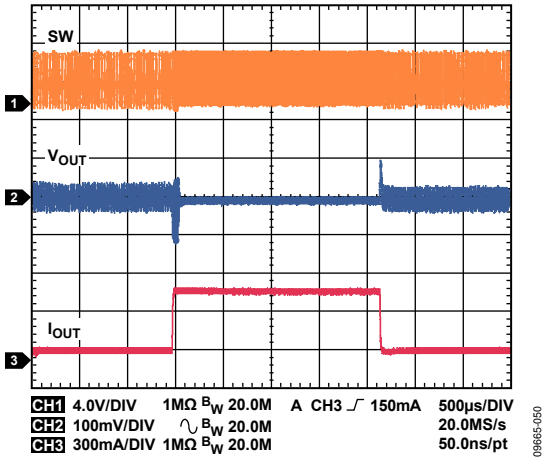

Figure 50. Buck Response to Load Transient, I_{OUT1} = 50 mA to 500 mA, V_{OUT1} = 1.8 V, Auto Mode

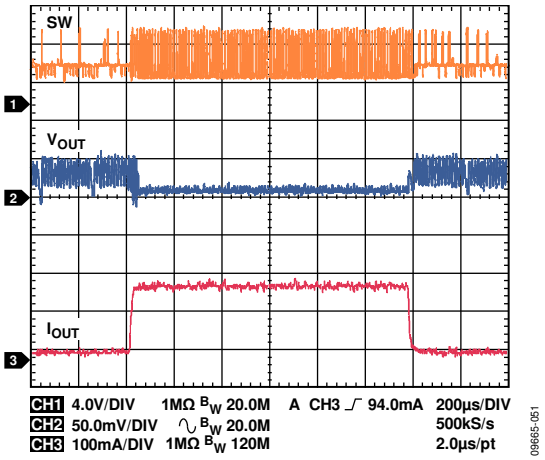

Figure 51. Buck Response to Load Transient, I_{OUT1} = 20 mA to 200 mA, V_{OUT1} = 1.2 V, Auto Mode

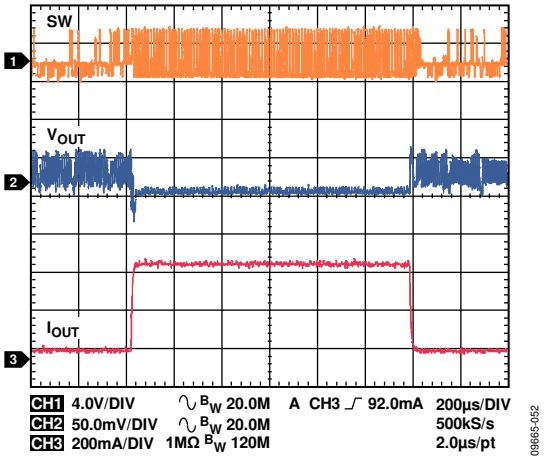

Figure 52. Buck Response to Load Transient, I_{OUT1} = 50 mA to 500 mA, V_{OUT1} = 1.2 V, Auto Mode

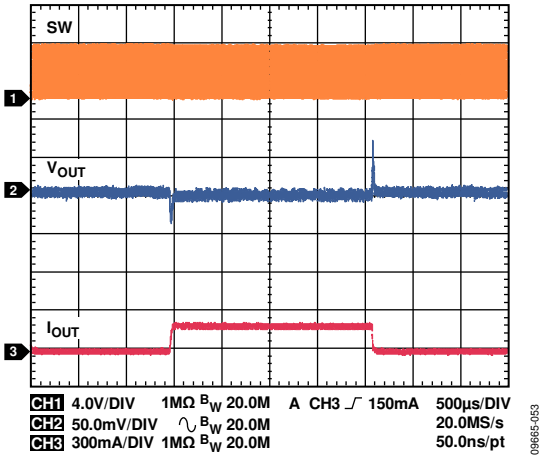

Figure 53. Buck Response to Load Transient, I_{OUT1} = 20 mA to 200 mA, V_{OUT1} = 3.3 V, PWM Mode

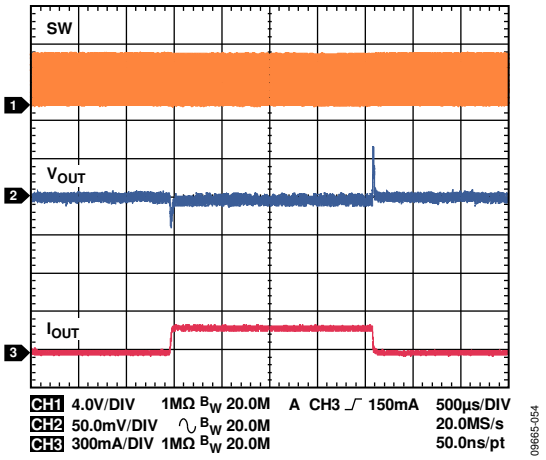

Figure 54. Buck Response to Load Transient, I_{OUT1} = 50 mA to 500 mA, V_{OUT1} = 3.3 V, PWM Mode

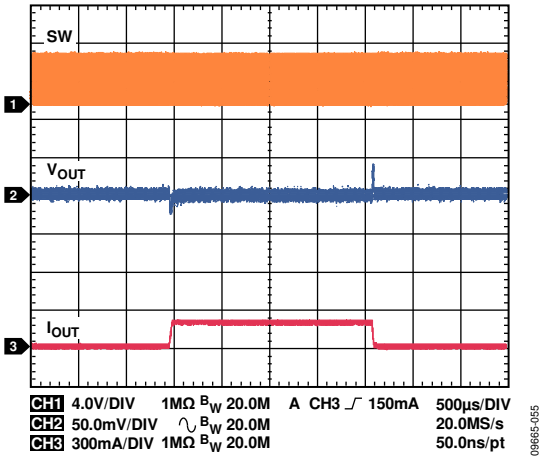

Figure 55. Buck Response to Load Transient, I_{OUT1} = 20 mA to 200 mA, V_{OUT1} = 1.8 V, PWM Mode

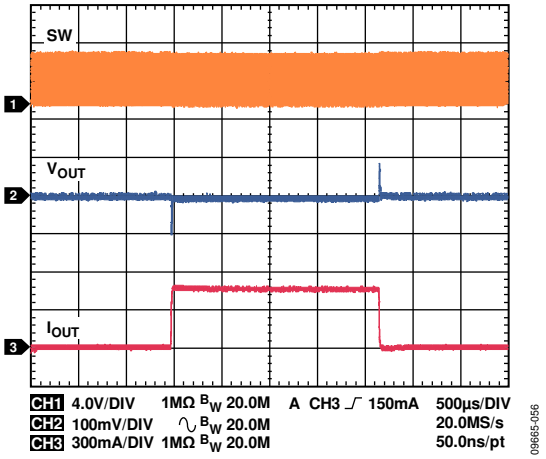

Figure 56. Buck Response to Load Transient, I_{OUT1} = 50 mA to 500 mA, V_{OUT1} = 1.8 V, PWM Mode

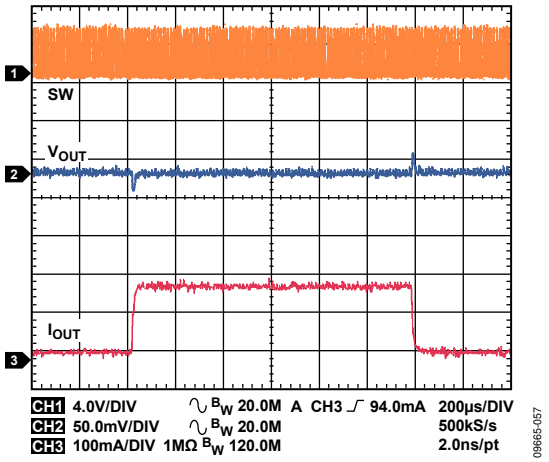

Figure 57. Buck Response to Load Transient, I_{OUT1} = 20 mA to 200 mA, V_{OUT1} = 1.2 V, PWM Mode

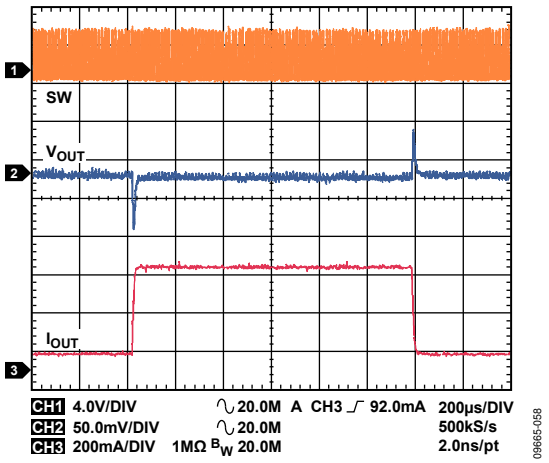

Figure 58. Buck Response to Load Transient, I_{OUT1} = 50 mA to 500 mA, V_{OUT1} = 1.2 V, PWM Mode

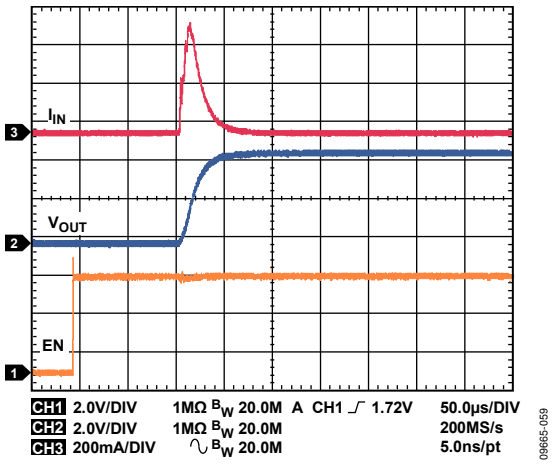

Figure 59. LDO1, LDO2 Startup, V_{OUT} = 4.7 V, I_{OUT} = 5 mA

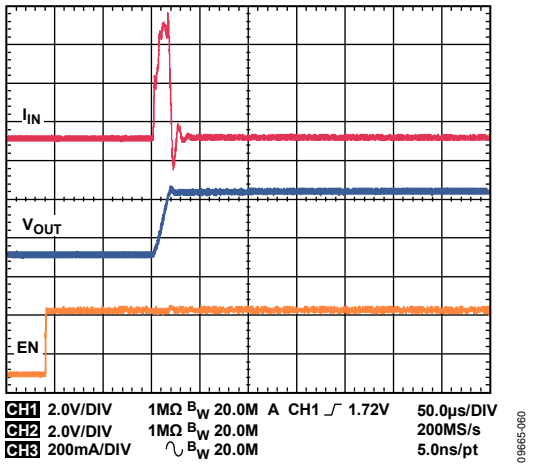

Figure 60. LDO1, LDO2 Startup, V_{OUT} = 3.3 V, I_{OUT} = 5 mA

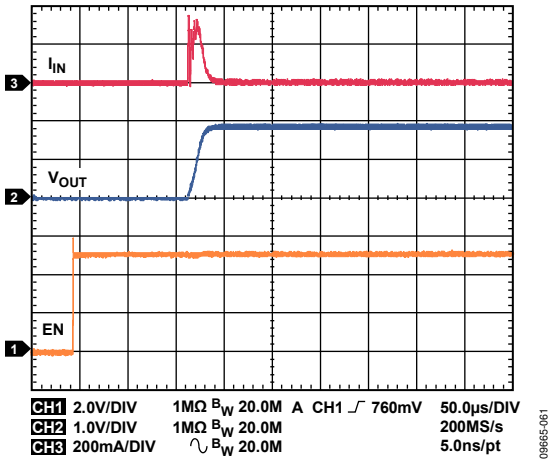

Figure 61. LDO1, LDO2 Startup, V_{OUT} = 1.8 V, I_{OUT} = 5 mA

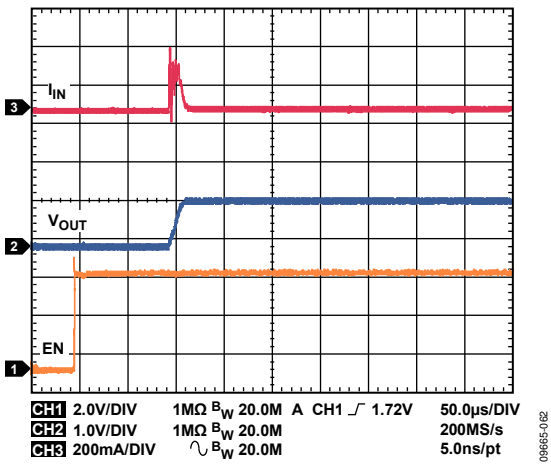

Figure 62. LDO1, LDO2 Startup, V_{OUT} = 1.2 V, I_{OUT} = 5 mA

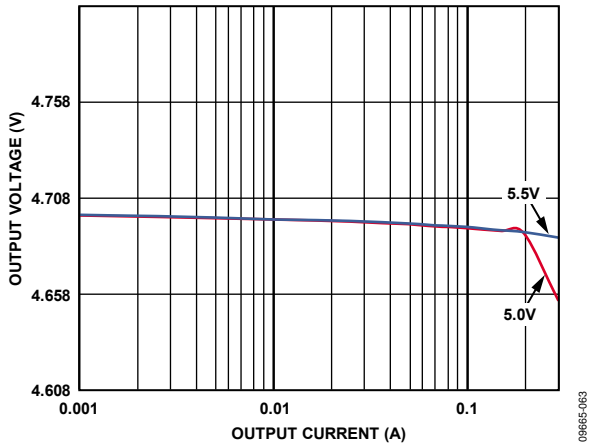

Figure 63. LDO1, LDO2 Load Regulation Across Input Voltage, V_{OUT} = 4.7 V

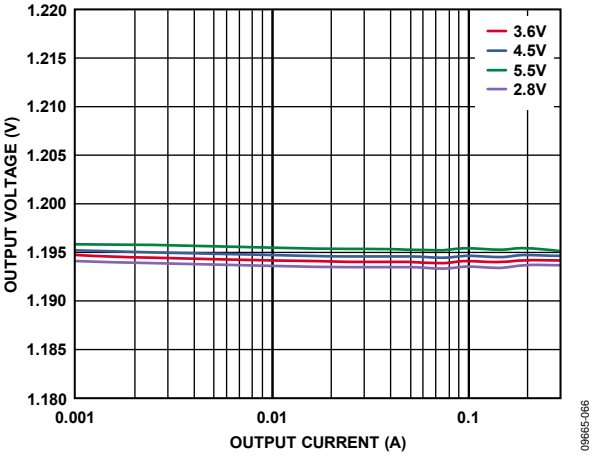

Figure 66. LDO1, LDO2 Load Regulation Across Input Voltage, V_{OUT} = 1.2 V

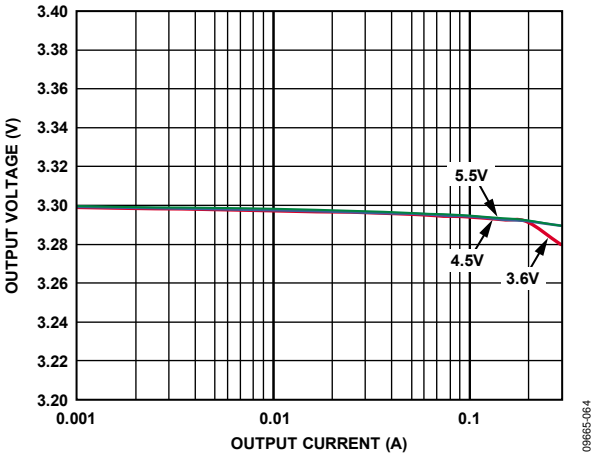

Figure 64. LDO1, LDO2 Load Regulation Across Input Voltage, V_{OUT} = 3.3 V

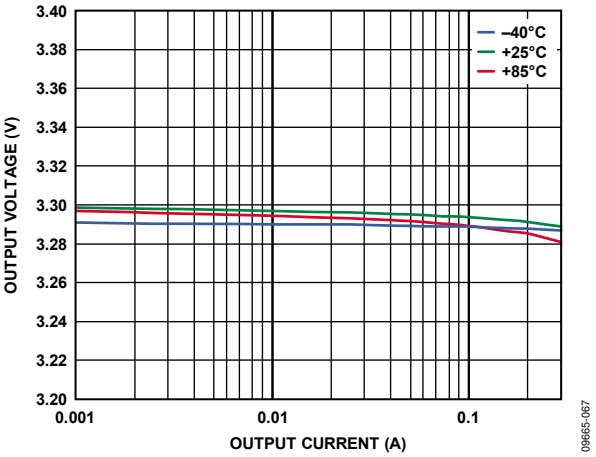

Figure 67. LDO1, LDO2 Load Regulation Across Temperature, V_{IN} = 3.6 V, V_{OUT} = 3.3 V

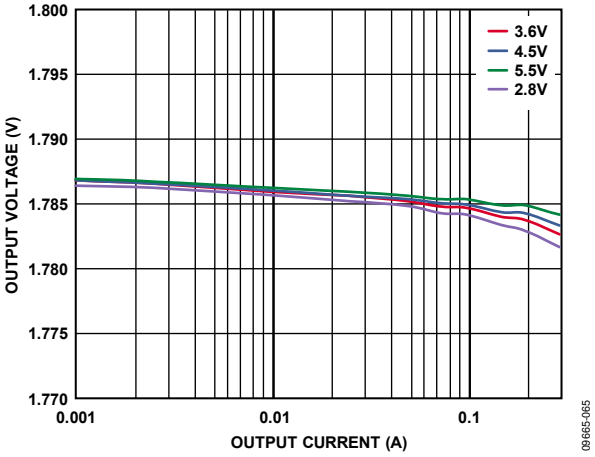

Figure 65. LDO1, LDO2 Load Regulation Across Input Voltage, V_{OUT} = 1.8 V

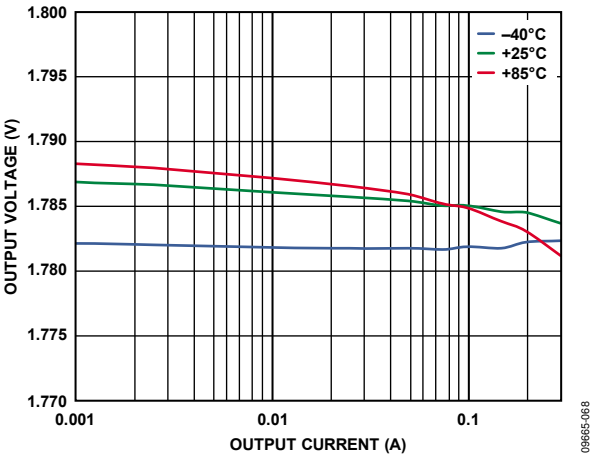

Figure 68. LDO1, LDO2 Load Regulation Across Temperature, V_{IN} = 3.6 V, V_{OUT} = 1.8 V

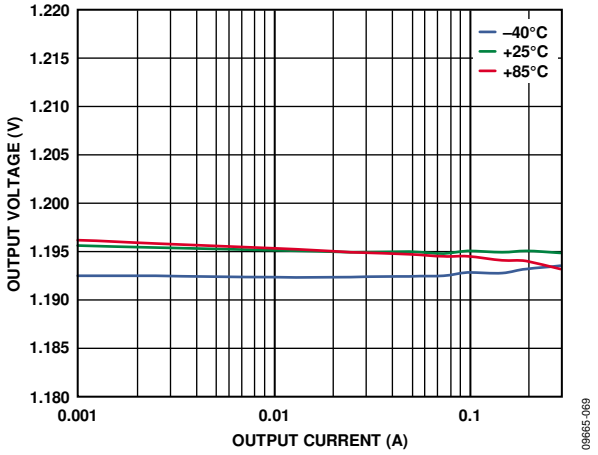

Figure 69. LDO1, LDO2 Load Regulation Across Temperature, V_{IN} = 3.6 V, V_{OUT} = 1.2 V

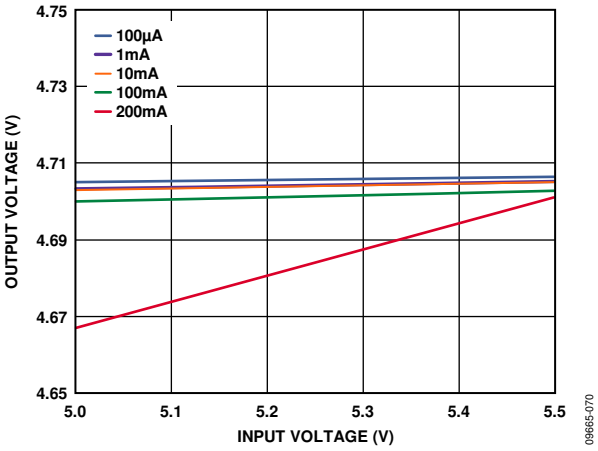

Figure 70. LDO1, LDO2 Line Regulation Across Input Voltage, V_{OUT} = 4.7 V

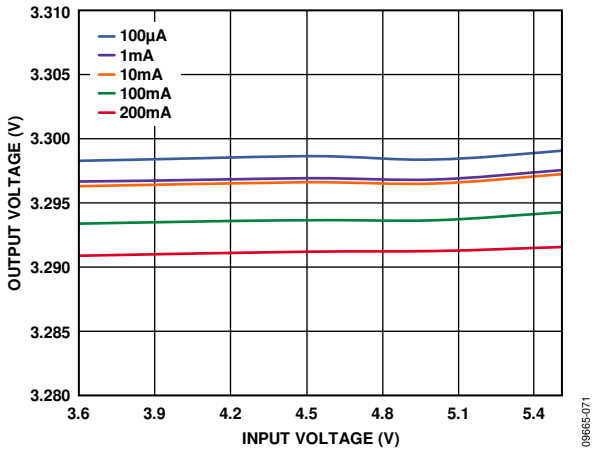

Figure 71. LDO1, LDO2 Line Regulation Across Input Voltage, V_{OUT} = 3.3 V

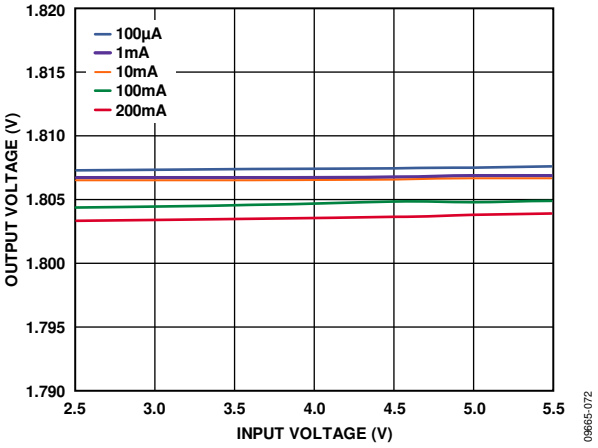

Figure 72. LDO1, LDO2 Line Regulation Across Input Voltage, V_{OUT} = 1.8 V

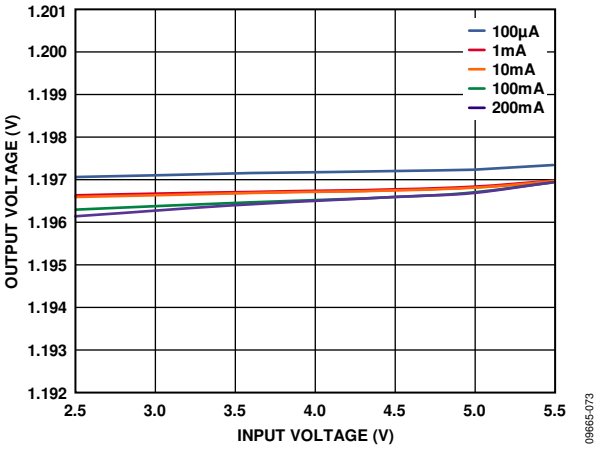

Figure 73. LDO1, LDO2 Line Regulation Across Input Voltage, V_{OUT} = 1.2 V

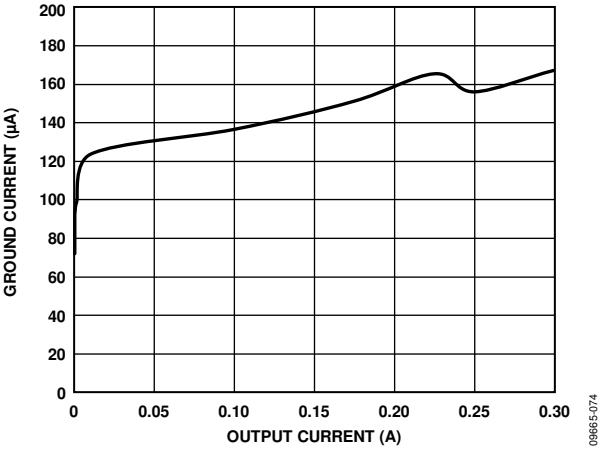

Figure 74. LDO1, LDO2 Ground Current vs. Output Current, V_{OUT} = 3.3 V

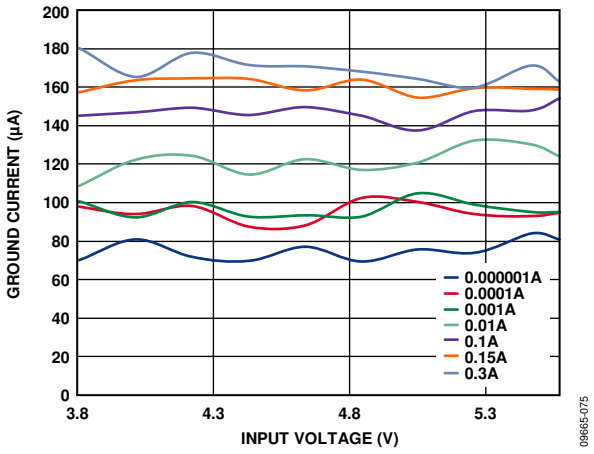

Figure 75. LDO1, LDO2 Ground Current vs. Input Voltage, Across Output Load (A), V_{OUT} = 3.3 V

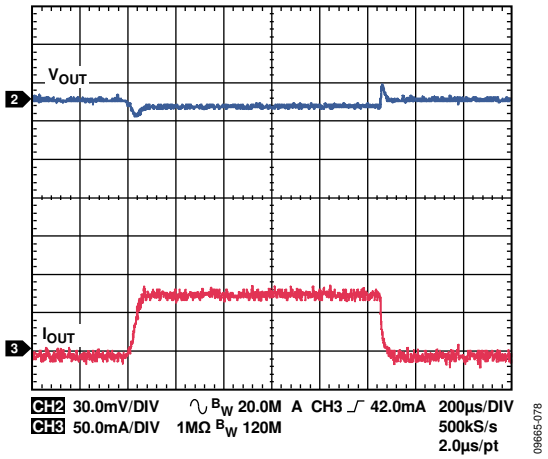

Figure 78. LDO1, LDO2 Response to Load Transient, I_{OUT} from 1 mA to 80 mA, V_{OUT} = 3.3 V

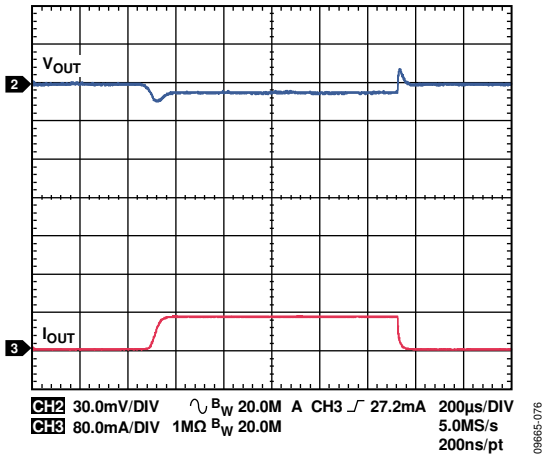

Figure 76. LDO1, LDO2 Response to Load Transient, I_{OUT} from 1 mA to 80 mA, V_{OUT} = 4.7 V

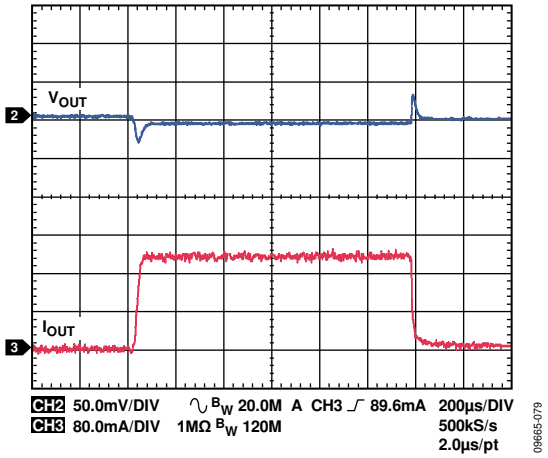

Figure 79. LDO1, LDO2 Response to Load Transient, I_{OUT} from 10 mA to 200 mA, V_{OUT} = 3.3 V

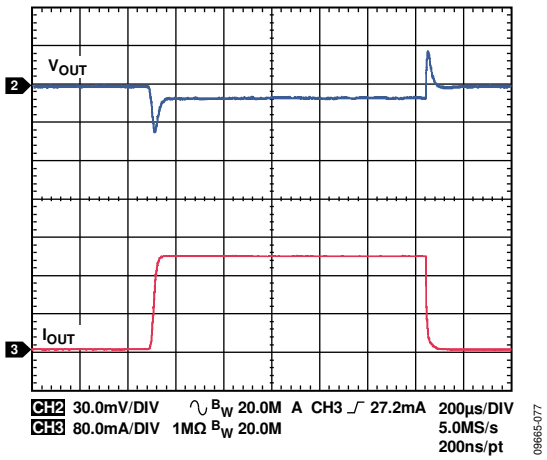

Figure 77. LDO1, LDO2 Response to Load Transient, I_{OUT} from 10 mA to 200 mA, V_{OUT} = 4.7 V

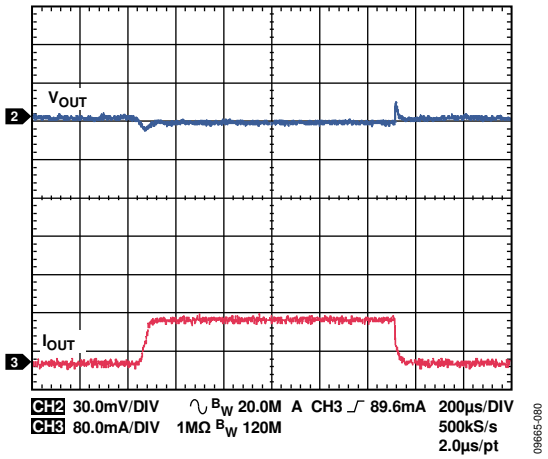

Figure 80. LDO1, LDO2 Response to Load Transient, I_{OUT} from 1 mA to 80 mA, V_{OUT} = 1.8 V

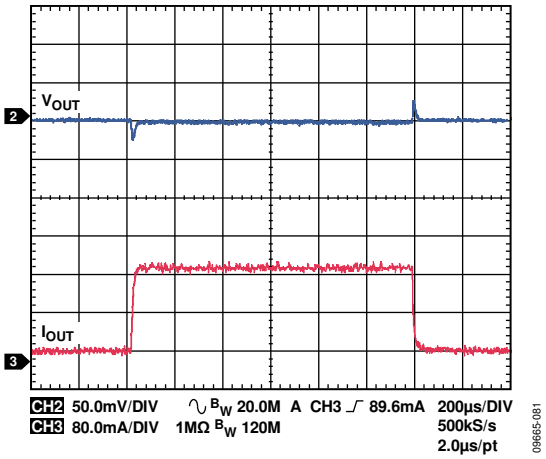

Figure 81. LDO1, LDO2 Response to Load Transient, I_{OUT} from 10 mA to 200 mA, V_{OUT} = 1.8 V

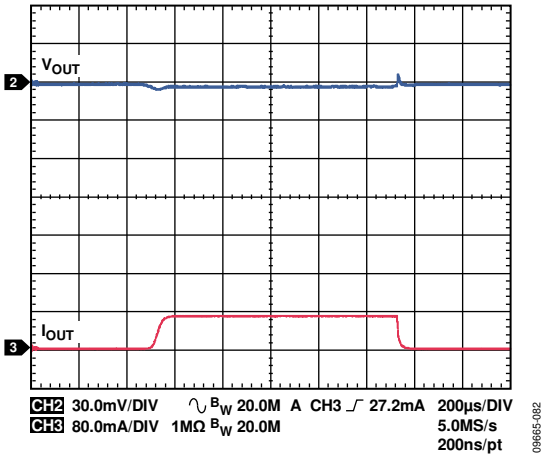

Figure 82. LDO1, LDO2 Response to Load Transient, I_{OUT} from 1 mA to 80 mA, V_{OUT} = 1.2 V

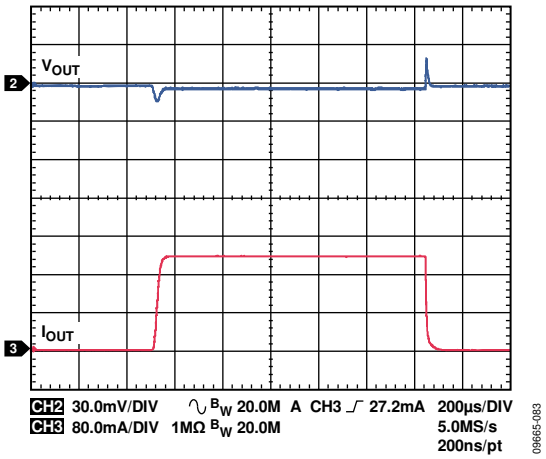

Figure 83. LDO1, LDO2 Response to Load Transient, I_{OUT} from 10 mA to 200 mA, V_{OUT} = 1.2 V

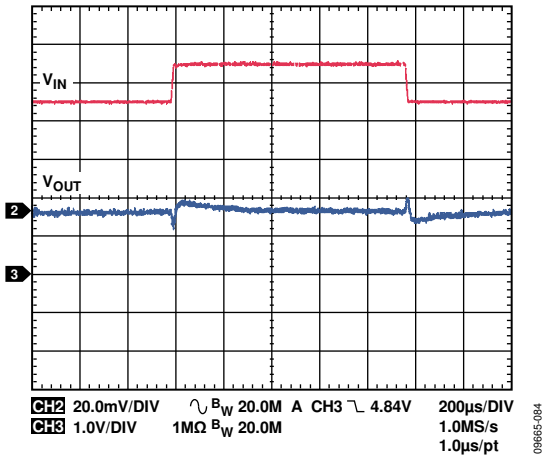

Figure 84. LDO1, LDO2 Response to Line Transient, Input Voltage from 4.5 V to 5.5 V, V_{OUT} = 3.3 V

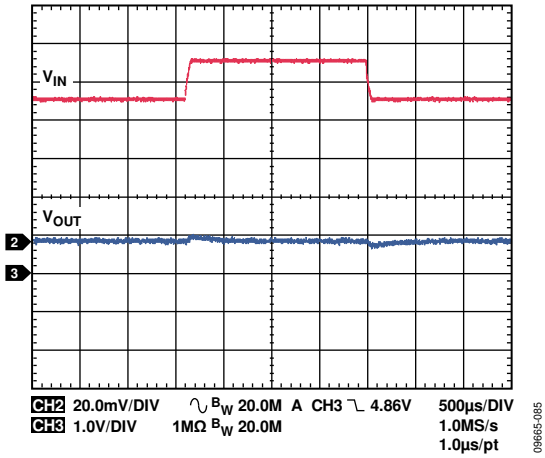

Figure 85. LDO1, LDO2 Response to Line Transient, Input Voltage from 4.5 V to 5.5 V, V_{OUT} = 1.8 V

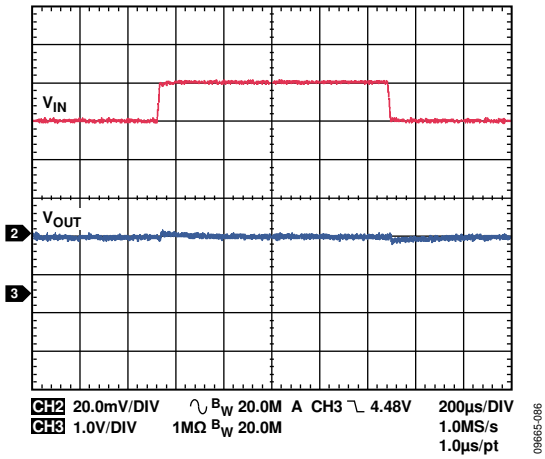

Figure 86. LDO1, LDO2 Response to Line Transient, Input Voltage from 4.5 V to 5.5 V, V_{OUT} = 1.2 V

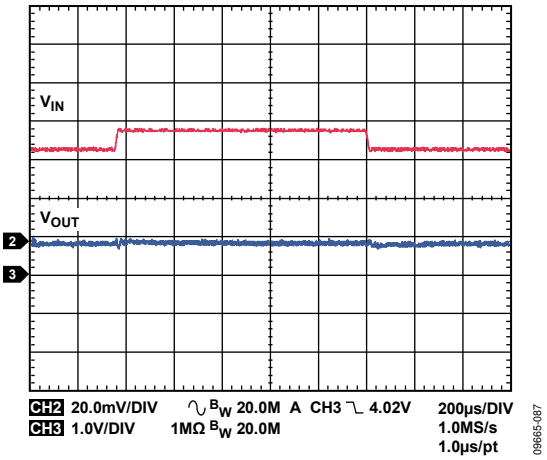

Figure 87. LDO1, LDO2 Response to Line Transient, Input Voltage from 3.3 V to 3.8 V, V_{OUT} = 1.8 V

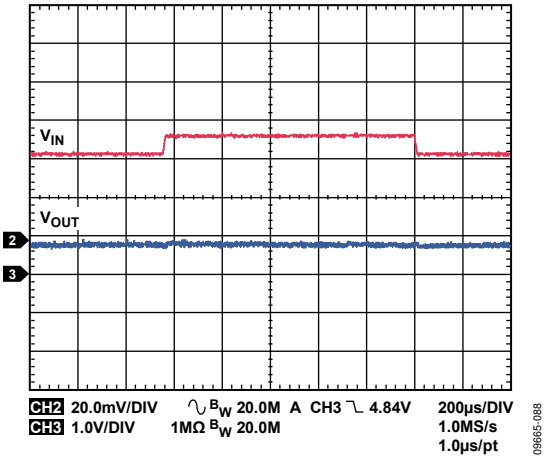

Figure 88. LDO1, LDO2 Response to Line Transient, Input Voltage from 3.3 V to 3.8 V, V_{OUT} = 1.2 V

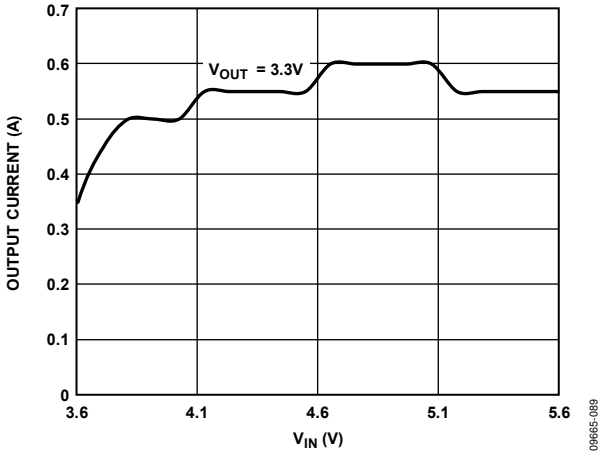

Figure 89. LDO1, LDO2 Output Current Capability vs. Input Voltage

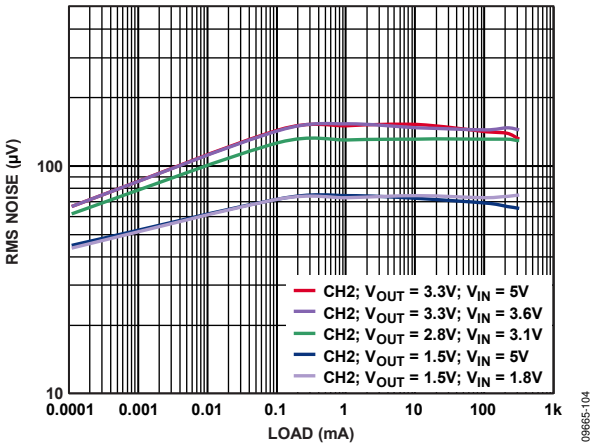

Figure 90. LDO1 Output Noise vs. Load Current, Across Input and Output Voltage

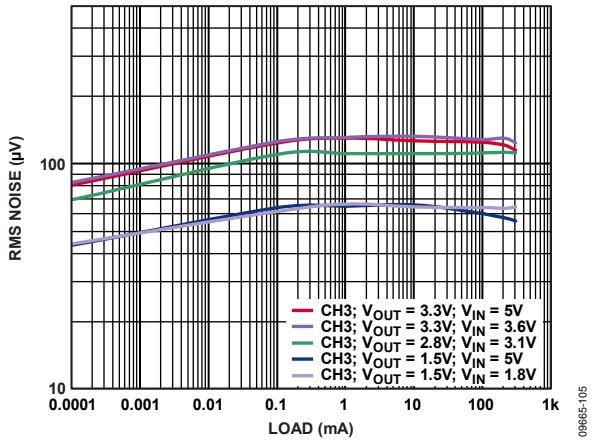

Figure 91. LDO2 Output Noise vs. Load Current, Across Input and Output Voltage

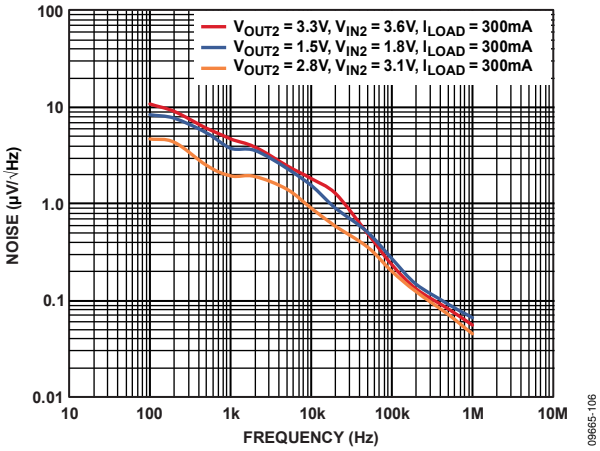

Figure 92. LDO1 Noise Spectrum Across Output Voltage, $V_{IN} = V_{OUT} + 0.3$ V

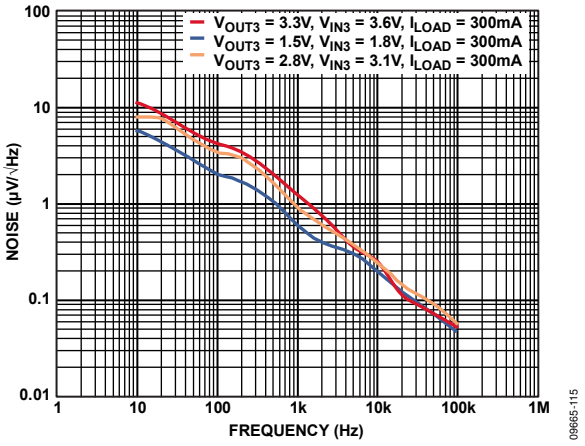

Figure 93. LDO2 Noise Spectrum Across Output Voltage, $V_{IN} = V_{OUT} + 0.3$ V

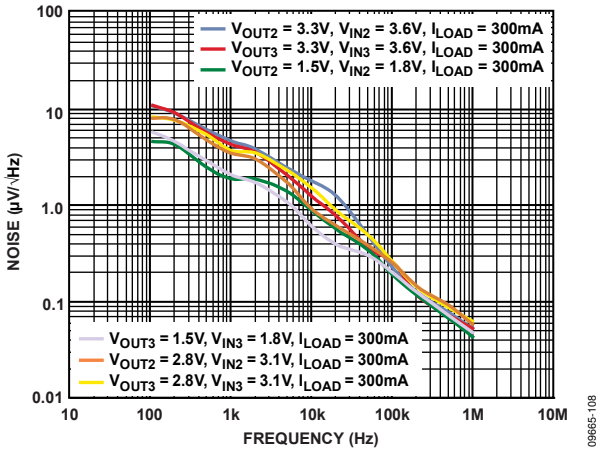

Figure 94. LDO1 vs. LDO2 Noise Spectrum

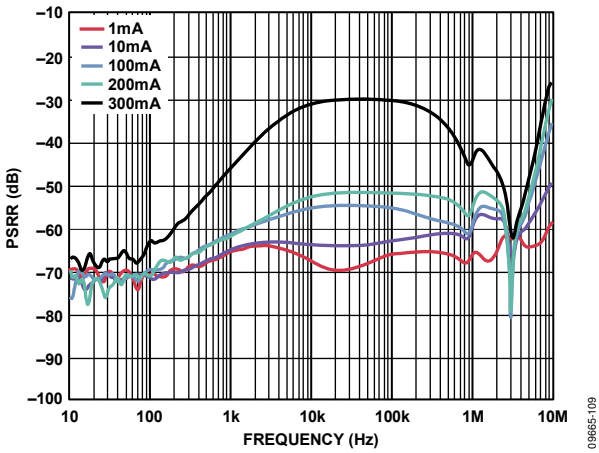

Figure 95. LDO2 PSRR Across Output Load, $V_{IN3} = 3.3$ V, $V_{OUT3} = 2.8$ V

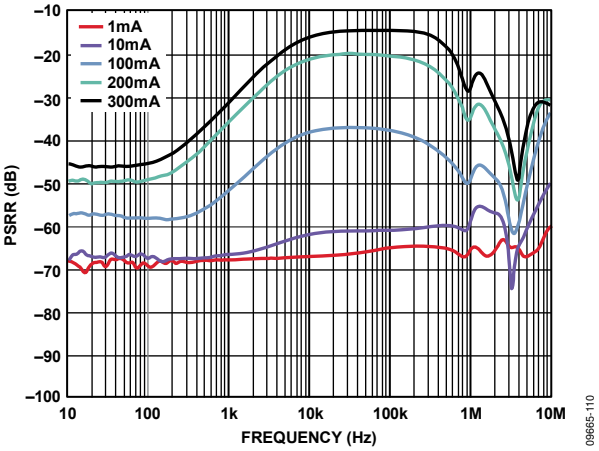

Figure 96. LDO2 PSRR Across Output Load, $V_{IN3} = 3.1$ V, $V_{OUT3} = 2.8$ V

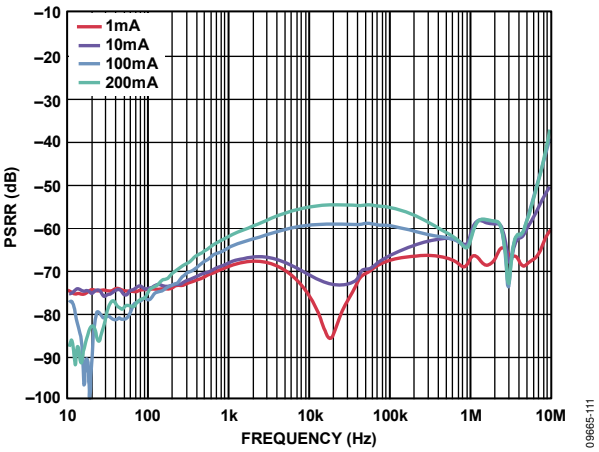

Figure 97. LDO2 PSRR Across Output Load, $V_{IN3} = 5.0$ V, $V_{OUT3} = 3.3$ V

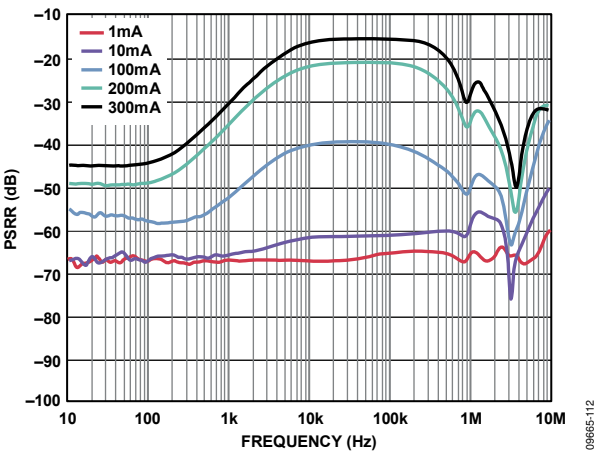

Figure 98. LDO2 PSRR Across Output Load, $V_{IN3} = 3.6$ V, $V_{OUT3} = 3.3$ V

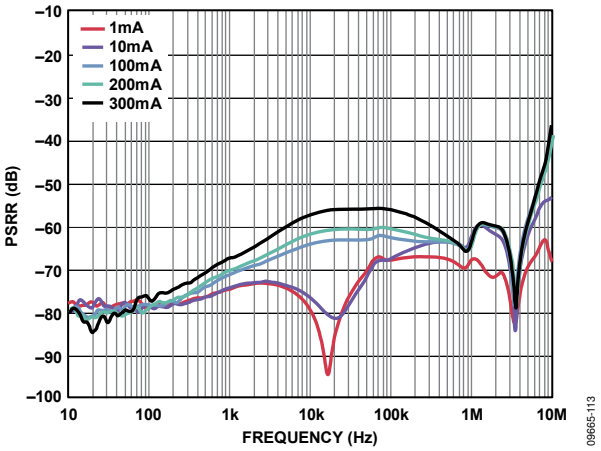

Figure 99. LDO1 PSRR Across Output Load, V_{IN2} = 5.0 V, V_{OUT2} = 1.5 V

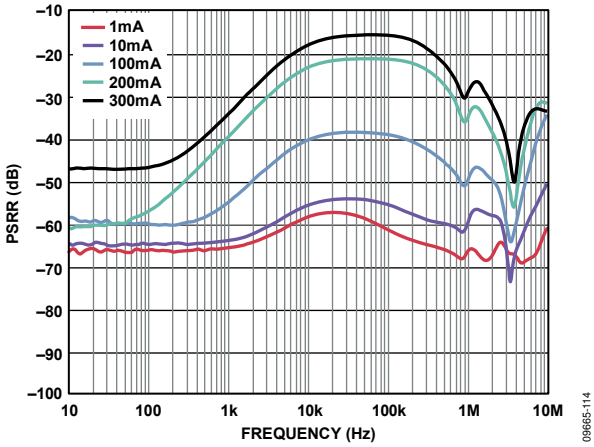

Figure 100. LDO1 PSRR Across Output Load, V_{IN2} = 1.8 V, V_{OUT2} = 1.5 V