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FEATURES

- Input voltage range: 2.3 V to 5.5 V**
- One 1.2 A buck regulator**
- Two 300 mA LDOs**
- 20-lead, 4 mm × 4 mm LFCSP package**
- Overcurrent and thermal protection**
- Soft start**
- Undervoltage lockout**
- Open-drain processor reset with externally adjustable threshold monitoring**
- Guaranteed reset output valid to $V_{AVIN} = 1 V$**
- Manual reset input**
- Watchdog refresh input**
- Buck key specifications**
 - Output voltage range: 0.8 V to 3.8 V**
 - Current mode topology for excellent transient response**
 - 3 MHz operating frequency**
 - Peak efficiency up to 96%**
 - Uses tiny multilayer inductors and capacitors**
 - Mode pin selects forced PWM or auto PWM/PSM mode**
 - 100% duty cycle low dropout mode**
- LDOs key specifications**
 - Output voltage range: 0.8 V to 5.2 V**
 - Low input supply voltage from 1.7 V to 5.5 V**
 - Stable with 2.2 μF ceramic output capacitors**
 - High PSRR**
 - Low output noise**
 - Low dropout voltage**
 - 40°C to +125°C junction temperature range**

GENERAL DESCRIPTION

The [ADP5041](#) combines one high performance buck regulator and two low dropout regulators (LDO) in a small 20-lead LFCSP to meet demanding performance and board space requirements.

The high switching frequency of the buck regulator enables use of tiny multilayer external components and minimizes board space.

When the MODE pin is set to logic high, the buck regulator operates in forced PWM mode. When the MODE pin is set to logic low, the buck regulator operates in PWM mode when the load is around the nominal value. When the load current falls below a predefined threshold, the regulator operates in power save mode (PSM), improving the light load efficiency. The low quiescent current, low dropout voltage, and wide input voltage

FUNCTIONAL BLOCK DIAGRAM

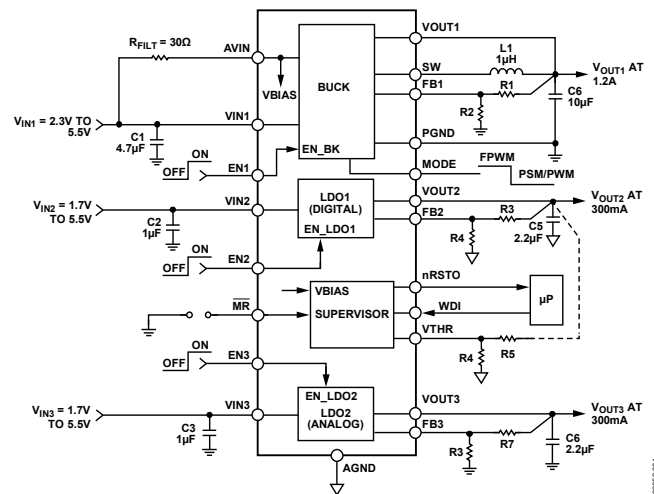


Figure 1.

range of the [ADP5041](#) LDOs extend the battery life of portable devices. The [ADP5041](#) LDOs maintain a power supply rejection greater than 60 dB for frequencies as high as 10 kHz while operating with a low headroom voltage.

Each regulator in the [ADP5041](#) is activated by a high level on the respective enable pin. The output voltages of the regulators and the reset threshold are programmed through external resistor dividers to address a variety of applications. The [ADP5041](#) contains supervisory circuits that monitor power supply voltage levels and code execution integrity in microprocessor-based systems. They also provide power-on reset signals. An on-chip watchdog timer can reset the microprocessor if it fails to strobe within a preset timeout period.

Rev. 0

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ADP5041* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADP5041 Evaluation Board

DOCUMENTATION

Data Sheet

- ADP5041: Micro PMU with 1.2 A Buck, Two 300 mA LDOs Supervisory, Watchdog and Manual Reset Preliminary Data Sheet

TOOLS AND SIMULATIONS

- 5V uPMU BuckDesigner
- ADIsimPower™ Voltage Regulator Design Tool

REFERENCE MATERIALS

Press

- Multi-output Regulators with Supervisory and Watchdog Timers Reduce Component Count, Increase Power Density and Reliability

Solutions Bulletins & Brochures

- Integrated Power Solutions for Altera FPGAs
- Integrated, High Power Solutions for Xilinx FPGAs

DESIGN RESOURCES

- ADP5041 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADP5041 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

Features	1	Buck Section.....	27
Functional Block Diagram	1	LDO Section	28
General Description	1	Supervisory Section	28
Revision History	2	Applications Information	31
Specifications.....	3	Buck External Component Selection.....	31
General Specifications	3	LDO External Component Selection	32
Supervisory Specifications	3	Output Capacitor.....	32
Buck Specifications.....	4	Supervisory Section	33
LDO1, LDO2 Specifications	5	Power Dissipation/Thermal Considerations	34
Input and Output Capacitor, Recommended Specifications..	6	Application Diagram	36
Absolute Maximum Ratings.....	7	PCB Layout Guidelines.....	37
Thermal Resistance	7	Suggested Layout	37
ESD Caution.....	7	Bill of Materials.....	38
Pin Configuration and Function Descriptions.....	8	Factory Programmable Options.....	39
Typical Performance Characteristics	9	Outline Dimensions	40
Theory of Operation	26	Ordering Guide	40
Power Management Unit.....	26		

REVISION HISTORY

12/11—Revision 0: Initial Version

SPECIFICATIONS

GENERAL SPECIFICATIONS

AVIN, VIN1 = 2.3 V to 5.5 V; AVIN, VIN1 ≥ VIN2, VIN3; VIN2, VIN3 = 1.7 V to 5.5 V, T_J = -40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
AVIN UNDERVOLTAGE LOCKOUT	UVLO _{AVIN}					
Input Voltage Rising	UVLO _{AVINRISE}					
Option 0					2.275	V
Option 1					3.9	V
Input Voltage Falling	UVLO _{AVINFALL}					
Option 0			1.95			V
Option 1			3.1			V
SHUTDOWN CURRENT	I _{GND-SD}	ENx = GND		0.1	2	μA
Thermal Shutdown Threshold	TS _{SD}	T _J rising		150		°C
Thermal Shutdown Hysteresis	TS _{SD-HYS}			20		°C
START-UP TIME ¹						
Buck	t _{START1}			250		μs
LDO1, LDO2	t _{START2}	V _{OUT2} , V _{OUT3} = 3.3 V		85		μs
ENx, WDI, MODE, MR INPUTS						
Input Logic High	V _{IH}	2.5 V ≤ AVIN ≤ 5.5 V	1.2			V
Input Logic Low	V _{IL}	2.5 V ≤ AVIN ≤ 5.5 V			0.4	V
Input Leakage Current	V _{I-LEAKAGE}	ENx = AVIN or GND		0.05	1	μA
OPEN-DRAIN OUTPUT						
nRSTO Output Voltage	V _{OL1V}	AVIN ≥ 1.0 V, I _{SINK} = 50 μA			0.3	V
	V _{OL1V2}	AVIN ≥ 1.2 V, I _{SINK} = 100 μA			0.3	V
	V _{OL2V7}	AVIN ≥ 2.7 V, I _{SINK} = 1.2 mA			0.3	V
	V _{OL4V5}	AVIN ≥ 4.5 V, I _{SINK} = 3.2 mA			0.4	V
Open-Drain Reset Output Leakage Current		AVIN = 5.5 V			1	μA

¹ Start-up time is defined as the time from the moment EN1 = EN2 = EN3 transfers from 0 V to VAVIN to the moment VOUT1, VOUT2, and VOUT3 are reaching 90% of their nominal levels. Start-up times are shorter for individual channels if another channel is already enabled. See the Typical Performance Characteristics section for more information.

SUPERVISORY SPECIFICATIONS

AVIN, VIN1 = 2.3 V to 5.5 V; T_J = -40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
Supply Current (Supervisory Circuit Only)		45	55	μA	AVIN = VIN1 = EN1 = EN2 = EN3 = 5.5 V
		43	52	μA	AVIN = VIN1 = EN1 = EN2 = EN3 = 3.6 V
THRESHOLD VOLTAGE	0.495	0.500	0.505	V	
RESET TIMEOUT PERIOD					
Option 0	24	30	36	ms	
Option 1	160	200	240	ms	
V _{CC} TO RESET DELAY (t _{RD})		80		μs	VIN falling at 1 mV/μs

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
WATCHDOG INPUT					
Watchdog Timeout Period					
Option 0	81.6	102	122.4	ms	
Option 1	1.28	1.6	1.92	sec	
WDI Pulse Width	80			ns	$V_{IL} = 0.4\text{ V}, V_{IH} = 1.2\text{ V}$
WDI Input Threshold	0.4		1.2	V	
WDI Input Current (Source)	8	15	20	μA	$V_{WDI} = V_{CC}$, time average
WDI Input Current (Sink)	-30	-25	-15	μA	$V_{WDI} = 0\text{ V}$, time average
MANUAL RESET INPUT					
$\overline{\text{MR}}$ Input Pulse Width	1			μs	
$\overline{\text{MR}}$ Glitch Rejection		220		ns	
$\overline{\text{MR}}$ Pull-Up Resistance	25	52	90	k Ω	
$\overline{\text{MR}}$ to Reset Delay		280		Ns	$V_{CC} = 5\text{ V}$

BUCK SPECIFICATIONS

AVIN, VIN1 = 2.3 V to 5.5 V; V_{OUT1} = 1.8 V; L = 1 μH ; C_{IN} = 10 μF ; C_{OUT} = 10 μF ; T_J = -40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.¹

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Voltage Range	V _{IN1}		2.3		5.5	V
OUTPUT CHARACTERISTICS						
Output Voltage Accuracy	V _{OUT1}	PWM mode, I _{LOAD} = 0 mA to 1200 mA	-3		+3	%
Line Regulation	($\Delta V_{OUT1}/V_{OUT1}$)/ ΔV_{IN1}	PWM mode		-0.05		%/V
Load Regulation	($\Delta V_{OUT1}/V_{OUT1}$)/ ΔI_{OUT1}	I _{LOAD} = 0 mA to 1200 mA, PWM mode		-0.1		%/A
VOLTAGE FEEDBACK	V _{FB1}		0.485	0.5	0.515	V
PWM TO POWER SAVE MODE CURRENT THRESHOLD	I _{PSM_L}			100		mA
INPUT CURRENT CHARACTERISTICS						
DC Operating Current	I _{NOLOAD}	MODE = ground I _{LOAD} = 0 mA, device not switching, all other channels disabled		21	35	μA
Shutdown Current	I _{SHTD}	EN1 = 0 V, T _A = T _J = -40°C to +125°C		0.2	1.0	μA
SW CHARACTERISTICS						
SW On Resistance	R _{PFET}	PFET, AVIN = VIN1 = 3.6 V		180	240	m Ω
	R _{NFET}	PFET, AVIN = VIN1 = 5 V		140	190	m Ω
		NFET, AVIN = VIN1 = 3.6 V		170	235	m Ω
		NFET, AVIN = VIN1 = 5 V		150	210	m Ω
Current Limit	I _{LIMIT}	PFET switch peak current limit	1600	1950	2300	mA
ACTIVE PULL-DOWN		EN1 = 0 V		85		Ω
OSCILLATOR FREQUENCY	f _{OSC}		2.5	3.0	3.5	MHz

¹ All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

LDO1, LDO2 SPECIFICATIONS

$V_{IN2}, V_{IN3} = (V_{OUT2}, V_{OUT3} + 0.5 \text{ V})$ or 1.7 V (whichever is greater) to 5.5 V; $AVIN, VIN1 \geq VIN2, VIN3$; $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 2.2 \mu\text{F}$; $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$ for minimum/maximum specifications and $T_A = 25^\circ\text{C}$ for typical specifications, unless otherwise noted.¹

Table 4.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN2}, V_{IN3}	$T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$	1.7		5.5	V
OPERATING SUPPLY CURRENT						
Bias Current per LDO ²	$I_{VIN2BIAS}/I_{VIN3BIAS}$	$I_{OUT2} = I_{OUT3} = 0 \mu\text{A}$ $I_{OUT2} = I_{OUT3} = 10 \text{ mA}$ $I_{OUT2} = I_{OUT3} = 300 \text{ mA}$		10 60 165	30 100 245	μA μA μA
Total System Input Current	I_{IN}	Includes all current into $AVIN, VIN1, VIN2,$ and $VIN3$				
LDO1 or LDO2 Only		$I_{OUT2} = I_{OUT3} = 0 \mu\text{A}$, all other channels disabled		53		μA
LDO1 and LDO2 Only		$I_{OUT2} = I_{OUT3} = 0 \mu\text{A}$, buck disabled		74		μA
OUTPUT VOLTAGE ACCURACY	V_{OUT2}, V_{OUT3}	$100 \mu\text{A} < I_{OUT2} < 300 \text{ mA}$, $100 \mu\text{A} < I_{OUT3} < 300 \text{ mA}$ $VIN2 = (V_{OUT2} + 0.5 \text{ V})$ to 5.5 V $VIN3 = (V_{OUT3} + 0.5 \text{ V})$ to 5.5 V	-3		+3	%
REFERENCE VOLTAGE	V_{FB2}, V_{FB3}		0.485	0.500	0.515	V
REGULATION						
Line Regulation	$(\Delta V_{OUT2}/V_{OUT2})/\Delta V_{IN2}$ $(\Delta V_{OUT3}/V_{OUT3})/\Delta V_{IN3}$	$VIN2 = (V_{OUT2} + 0.5 \text{ V})$ to 5.5 V $VIN3 = (V_{OUT3} + 0.5 \text{ V})$ to 5.5 V $I_{OUT2} = I_{OUT3} = 1 \text{ mA}$	-0.03		+0.03	%/V
Load Regulation ³	$(\Delta V_{OUT2}/V_{OUT2})/\Delta I_{OUT2}$ $(\Delta V_{OUT3}/V_{OUT3})/\Delta I_{OUT3}$	$I_{OUT2} = I_{OUT3} = 1 \text{ mA}$ to 300 mA		0.002	0.0075	%/mA
DROPOUT VOLTAGE ⁴	$V_{DROPOUT}$	$V_{OUT2} = V_{OUT3} = 5.0 \text{ V}$, $I_{OUT2} = I_{OUT3} = 300 \text{ mA}$ $V_{OUT2} = V_{OUT3} = 3.3 \text{ V}$, $I_{OUT2} = I_{OUT3} = 300 \text{ mA}$ $V_{OUT2} = V_{OUT3} = 2.5 \text{ V}$, $I_{OUT2} = I_{OUT3} = 300 \text{ mA}$ $V_{OUT2} = V_{OUT3} = 1.8 \text{ V}$, $I_{OUT2} = I_{OUT3} = 300 \text{ mA}$		72 86 107 180	140	mV mV mV mV
ACTIVE PULL-DOWN	R_{PDLDO}	$EN2/EN3 = 0 \text{ V}$		600		Ω
CURRENT-LIMIT THRESHOLD ⁵	I_{LIMIT}	$T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$	335	470		mA
OUTPUT NOISE	$OUT_{LDO2NOISE}$ $OUT_{LDO1NOISE}$	10 Hz to 100 kHz, $V_{IN3} = 5 \text{ V}$, $V_{OUT3} = 3.3 \text{ V}$ 10 Hz to 100 kHz, $V_{IN3} = 5 \text{ V}$, $V_{OUT3} = 2.8 \text{ V}$ 10 Hz to 100 kHz, $V_{IN3} = 5 \text{ V}$, $V_{OUT3} = 1.5 \text{ V}$ 10 Hz to 100 kHz, $V_{IN2} = 5 \text{ V}$, $V_{OUT2} = 3.3 \text{ V}$ 10 Hz to 100 kHz, $V_{IN2} = 5 \text{ V}$, $V_{OUT2} = 2.8 \text{ V}$ 10 Hz to 100 kHz, $V_{IN2} = 5 \text{ V}$, $V_{OUT2} = 1.5 \text{ V}$		123 110 59 140 129 66		$\mu\text{V rms}$ $\mu\text{V rms}$ $\mu\text{V rms}$ $\mu\text{V rms}$ $\mu\text{V rms}$ $\mu\text{V rms}$
POWER SUPPLY REJECTION RATIO	PSRR	1 kHz, $V_{IN2}, V_{IN3} = 3.3 \text{ V}$, $V_{OUT2}, V_{OUT3} = 2.8 \text{ V}$, $I_{OUT} = 100 \text{ mA}$ 100 kHz, $V_{IN2}, V_{IN3} = 3.3 \text{ V}$, $V_{OUT2}, V_{OUT3} = 2.8 \text{ V}$, $I_{OUT} = 100 \text{ mA}$ 1 MHz, $V_{IN2}, V_{IN3} = 3.3 \text{ V}$, $V_{OUT2}, V_{OUT3} = 2.8 \text{ V}$, $I_{OUT} = 100 \text{ mA}$		66 57 60		dB dB dB

¹ All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

² This is the input current into $VIN2$ and $VIN3$ that is not delivered to the output load.

³ Based on an end-point calculation using 1 mA and 300 mA loads.

⁴ Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only to output voltages above 1.7 V.

⁵ Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V, or 2.7 V.

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CAPACITANCE (BUCK) ¹	C _{MIN1}	T _J = -40°C to +125°C	4.7		40	μF
OUTPUT CAPACITANCE (BUCK) ²	C _{MIN2}	T _J = -40°C to +125°C	7		40	μF
INPUT AND OUTPUT CAPACITANCE ³ (LDO1, LDO2)	C _{MIN34}	T _J = -40°C to +125°C	0.70			μF
CAPACITOR ESR	R _{ESR}	T _J = -40°C to +125°C	0.001		1	Ω

¹ The minimum input capacitance should be greater than 4.7 μF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended, whereas Y5V and Z5U capacitors are not recommended for use with the buck.

² The minimum output capacitance should be greater than 7 μF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended, whereas Y5V and Z5U capacitors are not recommended for use with the buck.

³ The minimum input and output capacitance should be greater than 0.70 μF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended, whereas Y5V and Z5U capacitors are not recommended for use with LDOs.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVIN to AGND	-0.3 V to +6 V
VIN1 to AVIN	-0.3 V to +0.3 V
PGND to AGND	-0.3 V to +0.3 V
VIN2, VIN3, VOUTx, ENx, MODE, MR, WDI, nRSTO, FBx, VTHR, SW to AGND	-0.3 V to (AVIN + 0.3 V)
SW to PGND	-0.3 V to (VIN1 + 0.3 V)
Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature Range	-40°C to +125°C
Soldering Conditions	JEDEC J-STD-020
ESD Human Body Model	3000 V
ESD Charged Device Model	1500 V
ESD Machine Model	200 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead, 0.5 mm pitch LFCSP	38	4.2	°C/W

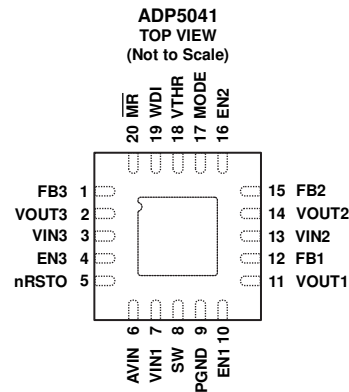
ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD MUST BE CONNECTED TO SYSTEM GROUND PLANE.

09852-002

Figure 2. Pin Configuration—View from Top of the Die

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FB3	LDO2 Feedback Input.
2	VOUT3	LDO2 Output Voltage.
3	VIN3	LDO2 Input Supply (1.7 V to 5.5 V).
4	EN3	Enable LDO2. EN3 = high: turn on LDO2; EN3 = low: turn off LDO2.
5	nRSTO	Open-Drain Reset Output, Active Low.
6	AVIN	Housekeeping and Supervisory Input Supply (2.3 V to 5.5 V).
7	VIN1	Buck Input Supply (2.3 V to 5.5 V).
8	SW	Buck Switching Node.
9	PGND	Dedicated Power Ground for Buck Regulator.
10	EN1	Enable Buck. EN1 = high: turn on buck; EN1 = low: turn off buck.
11	VOUT1	Buck Output Sensing Node.
12	FB1	Buck Feedback Input.
13	VIN2	LDO1 Input Supply (1.7 V to 5.5 V).
14	VOUT2	LDO1 Output Voltage.
15	FB2	LDO1 Feedback Input.
16	EN2	Enable LDO1. EN2 = high: turn on LDO1; EN2 = low: turn off LDO1.
17	MODE	Buck Mode. MODE = high; buck regulator operates in fixed PWM mode; MODE = low; buck regulator operates in power saving mode (PSM) at light load and in constant PWM at higher load.
18	VTHR	Reset Threshold Programming.
19	WDI	Watchdog Refresh Input from Processor. If WDI is in high-Z, watchdog is disabled.
20	$\overline{\text{MR}}$	Manual Reset Input, Active Low.
0	EPAD	Exposed Pad (Analog Ground). The exposed pad must be connected to the system ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

VIN1 = VIN2 = VIN3 = AVIN = 5.0 V, TA = 25°C, unless otherwise noted.

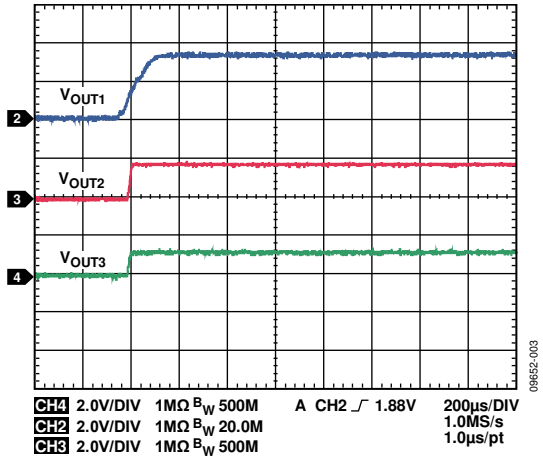


Figure 3. 3-Channel Start-Up Waveforms

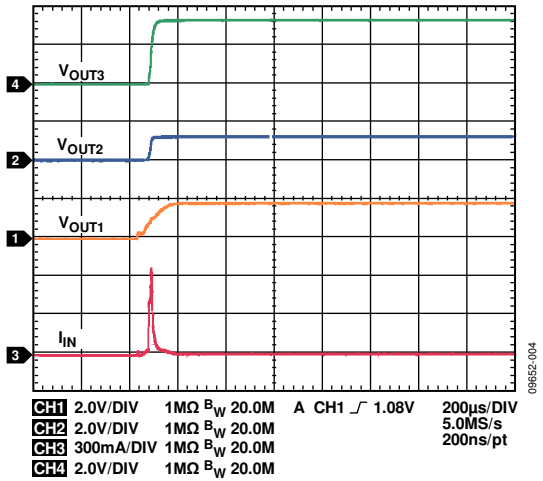


Figure 4. Total Inrush Current, All Channels Started Simultaneously

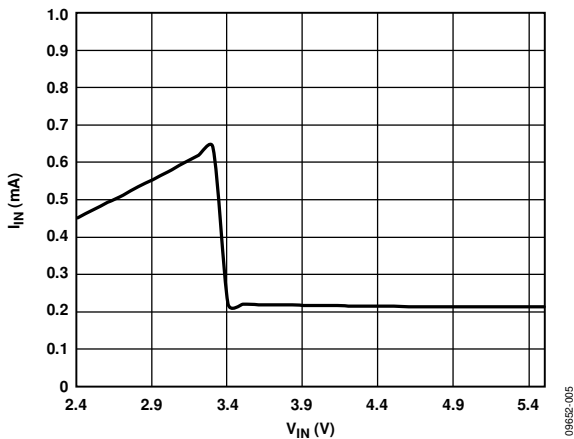


Figure 5. System Quiescent Current (Sum of All the Input Currents) vs. Input Voltage
 VOUT1 = 1.8 V, VOUT2 = VOUT3 = 3.3 V, (UVLO = 3.3 V)

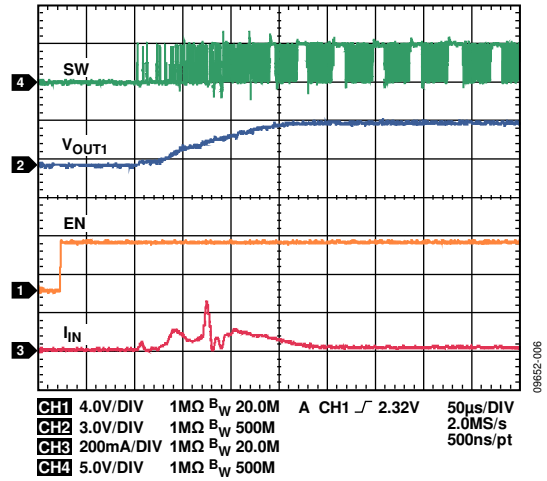


Figure 6. Buck Startup, VOUT1 = 3.3 V, IOUT2 = 20 mA

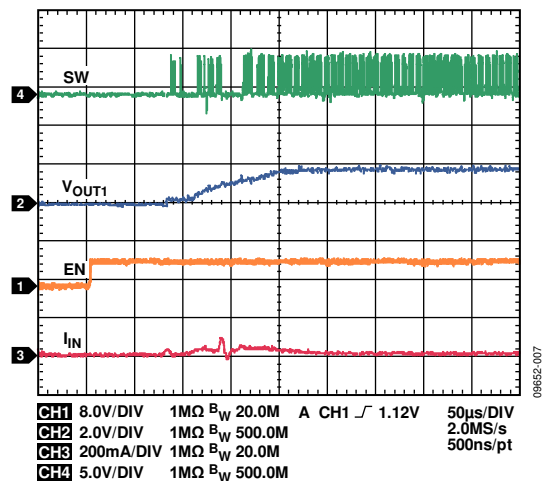


Figure 7. Buck Startup, VOUT1 = 1.8 V, IOUT = 20 mA

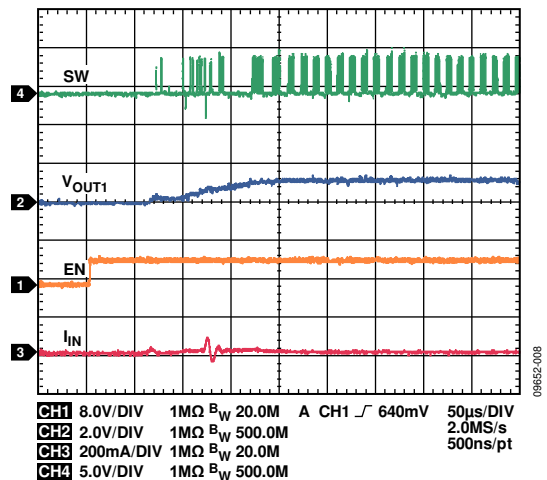


Figure 8. Buck Startup, VOUT1 = 1.2 V, IOUT = 20 mA

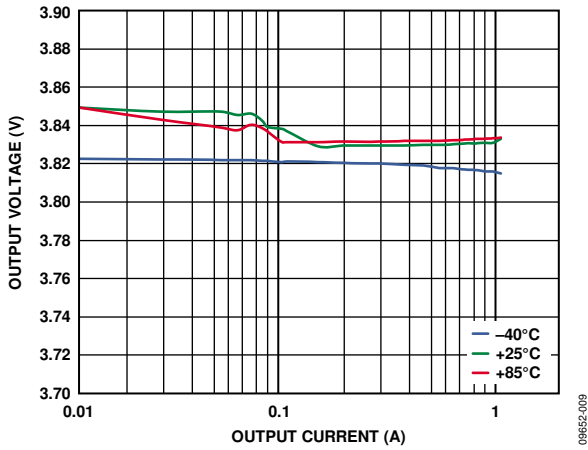


Figure 9. Buck Load Regulation Across Temperature, $V_{OUT1} = 3.8\text{ V}$, Auto Mode

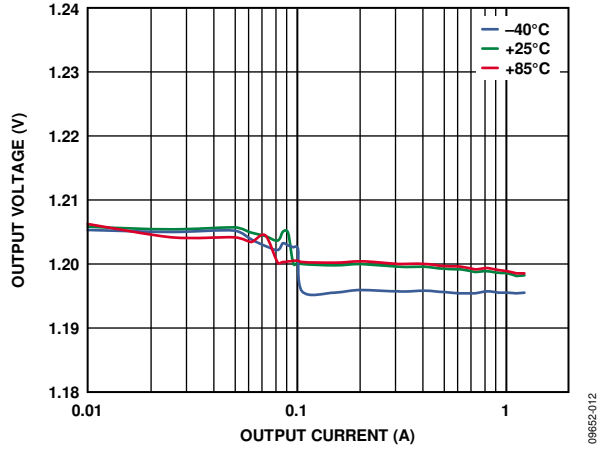


Figure 12. Buck Load Regulation Across Temperature, $V_{OUT1} = 1.2\text{ V}$, Auto Mode

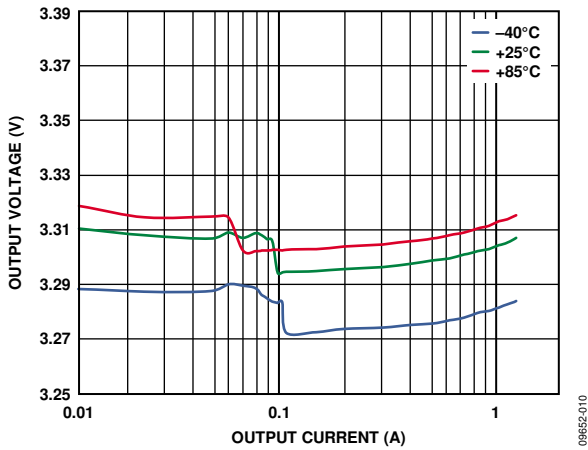


Figure 10. Buck Load Regulation Across Temperature, $V_{OUT1} = 3.3\text{ V}$, Auto Mode

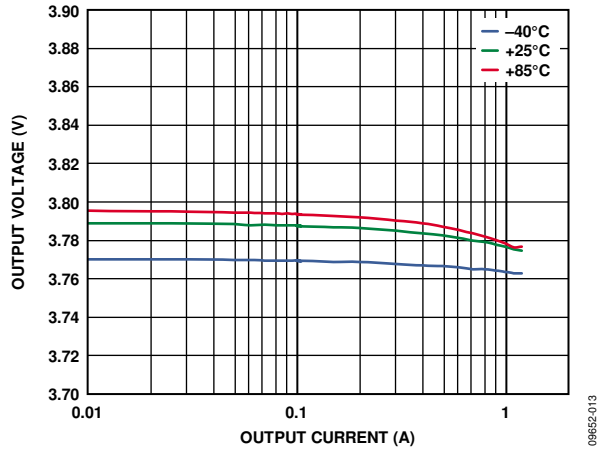


Figure 13. Buck Load Regulation Across Temperature, $V_{OUT1} = 3.8\text{ V}$, PWM Mode

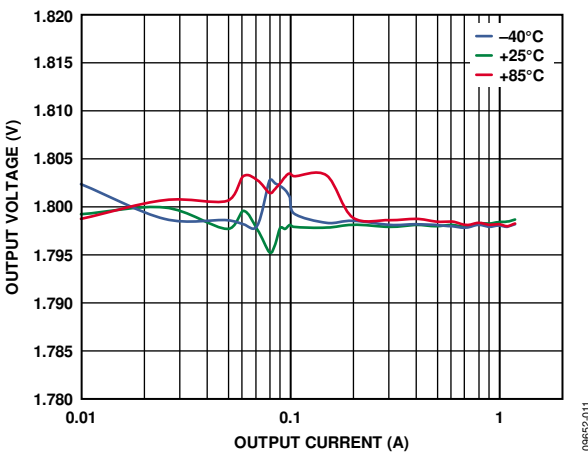


Figure 11. Buck Load Regulation Across Temperature, $V_{OUT1} = 1.8\text{ V}$, Auto Mode

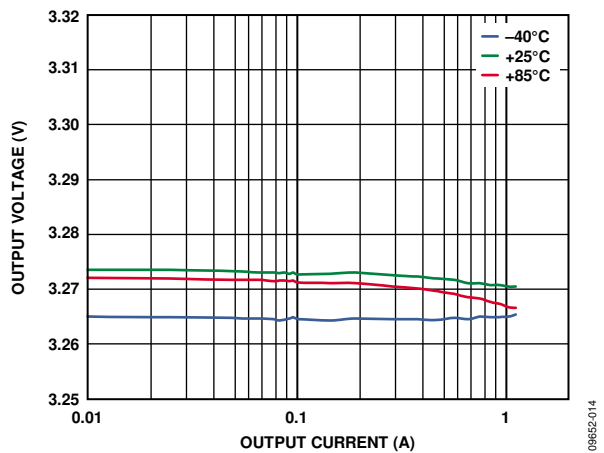


Figure 14. Buck Load Regulation Across Temperature, $V_{OUT1} = 3.3\text{ V}$, PWM Mode

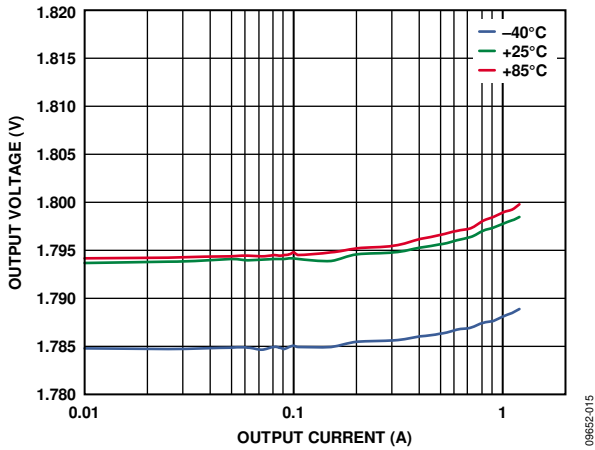


Figure 15. Buck Load Regulation Across Temperature, $V_{OUT1} = 1.8\text{ V}$, PWM Mode

09652-015

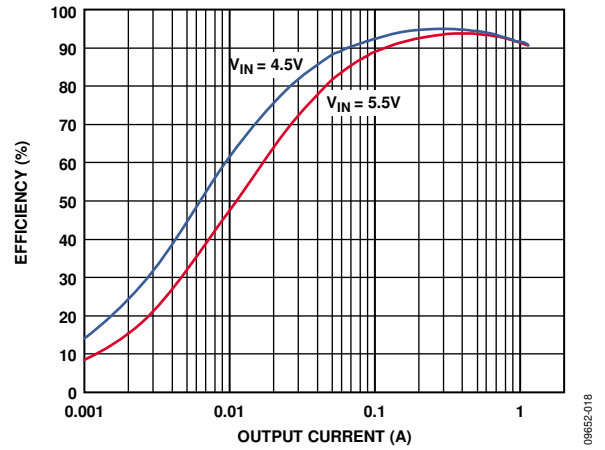


Figure 18. Buck Efficiency vs. Load Current, Across Input Voltage, $V_{OUT1} = 3.8\text{ V}$, PWM Mode

09652-018

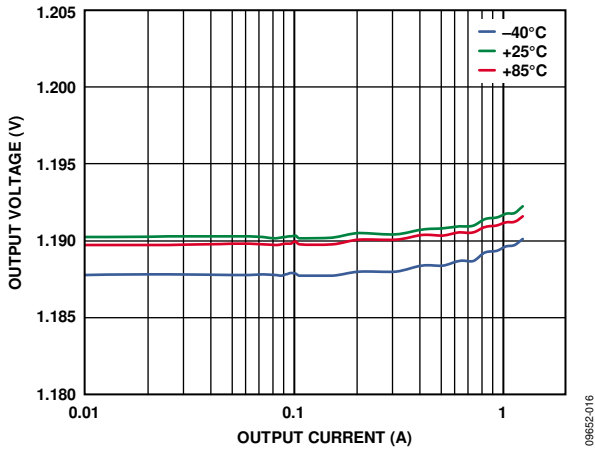


Figure 16. Buck Load Regulation Across Temperature, $V_{OUT1} = 1.2\text{ V}$, PWM Mode

09652-016

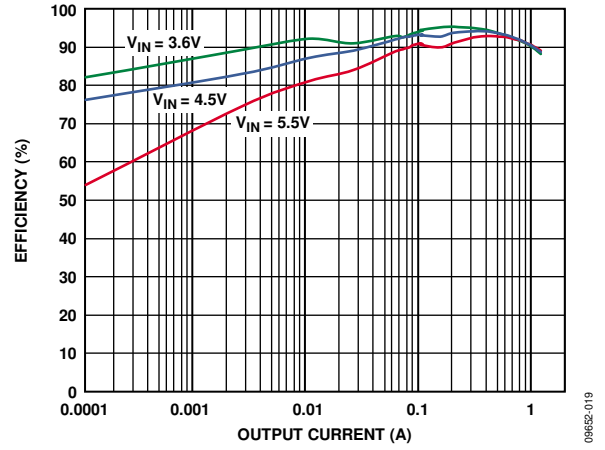


Figure 19. Buck Efficiency vs. Load Current, Across Input Voltage, $V_{OUT1} = 3.3\text{ V}$, Auto Mode

09652-019

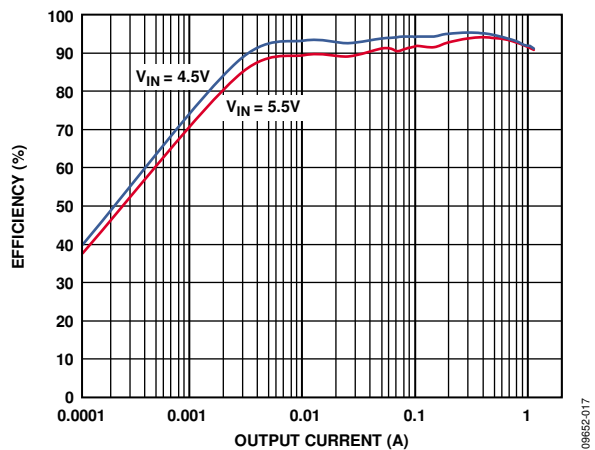


Figure 17. Buck Efficiency vs. Load Current, Across Input Voltage, $V_{OUT1} = 3.8\text{ V}$, Auto Mode

09652-017

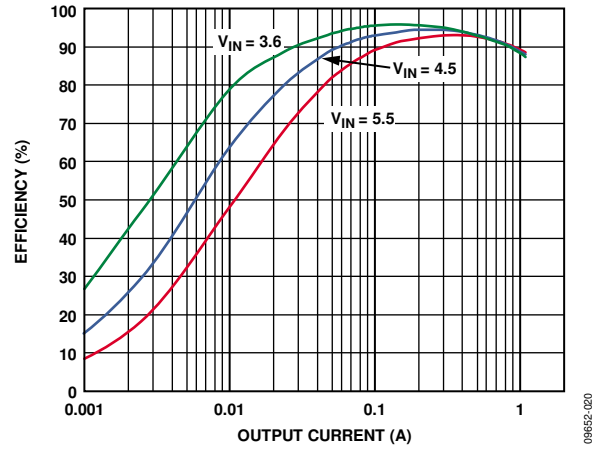


Figure 20. Buck Efficiency vs. Load Current, Across Input Voltage, $V_{OUT1} = 3.3\text{ V}$, PWM Mode

09652-020

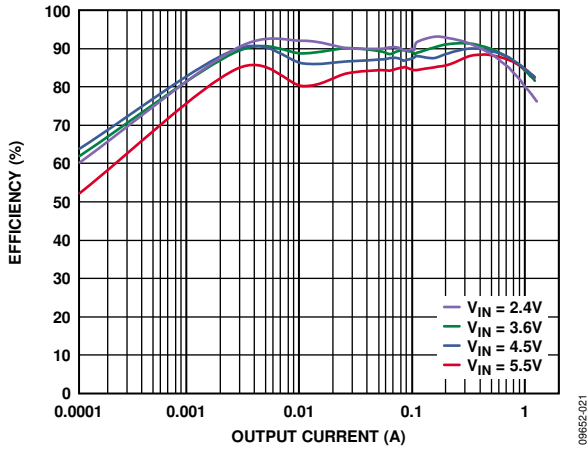


Figure 21. Buck Efficiency vs. Load Current, Across Input Voltage, $V_{OUT1} = 1.8\text{ V}$, Auto Mode

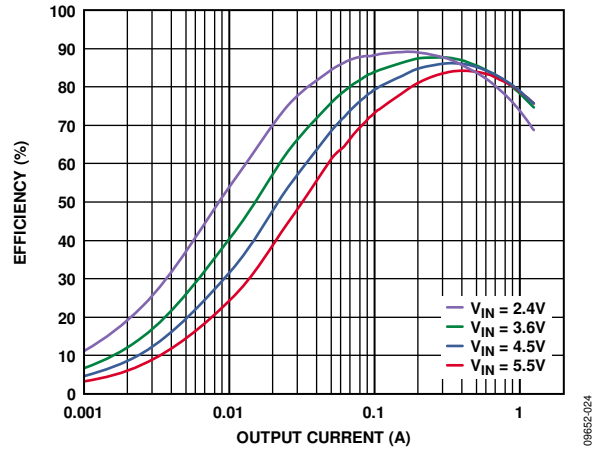


Figure 24. Buck Efficiency vs. Load Current, Across Input Voltage, $V_{OUT1} = 1.2\text{ V}$, PWM Mode

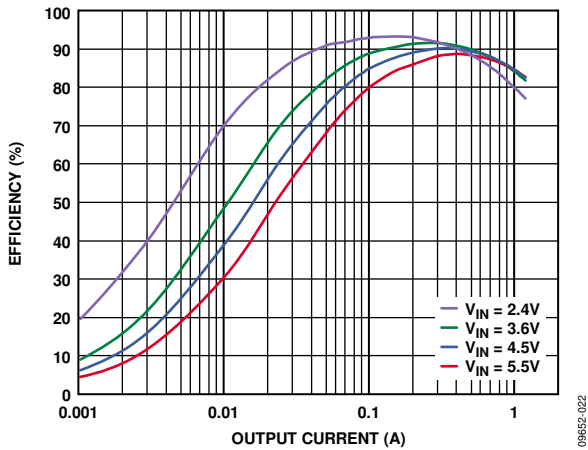


Figure 22. Buck Efficiency vs. Load Current, Across Input Voltage, $V_{OUT1} = 1.8\text{ V}$, PWM Mode

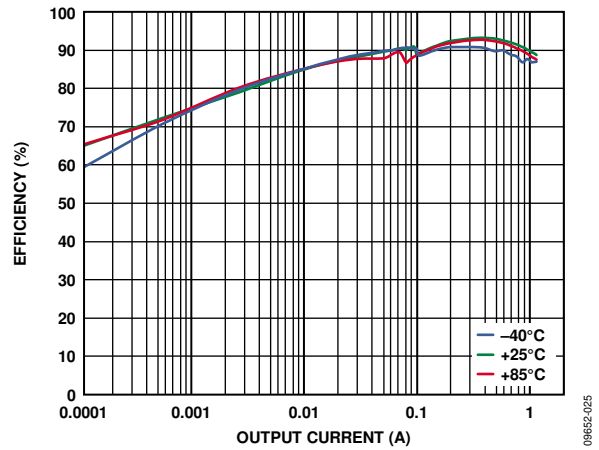


Figure 25. Buck Efficiency vs. Load Current, Across Temperature, $V_{IN} = 5.0\text{ V}$, $V_{OUT1} = 3.3\text{ V}$, Auto Mode

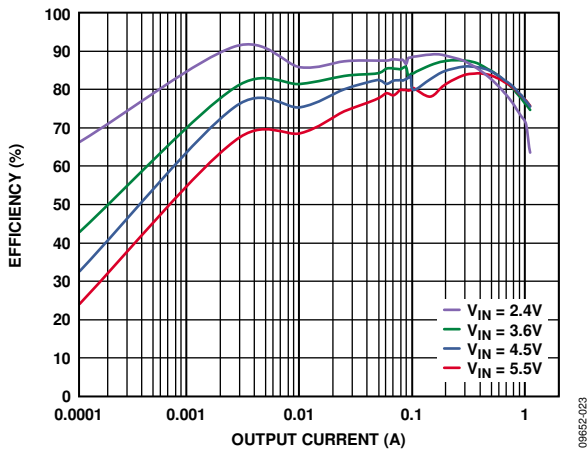


Figure 23. Buck Efficiency vs. Load Current, Across Input Voltage, $V_{OUT1} = 1.2\text{ V}$, Auto Mode

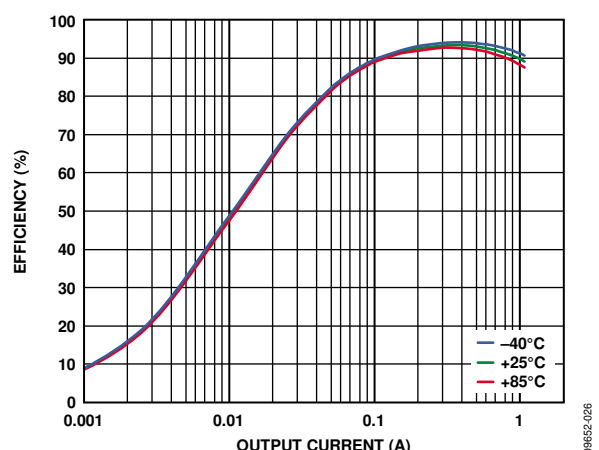


Figure 26. Buck Efficiency vs. Load Current, Across Temperature, $V_{IN} = 5.0\text{ V}$, $V_{OUT1} = 3.3\text{ V}$, PWM Mode

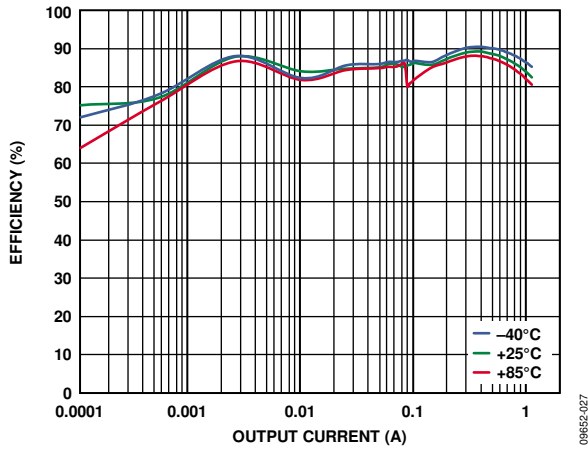


Figure 27. Buck Efficiency vs. Load Current, Across Temperature, $V_{IN} = 5.0\text{ V}$, $V_{OUT1} = 1.8\text{ V}$, Auto Mode

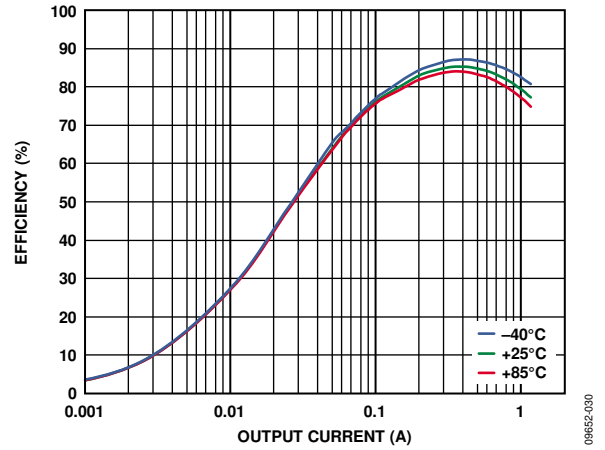


Figure 30. Buck Efficiency vs. Load Current, Across Temperature, $V_{IN} = 5.0\text{ V}$, $V_{OUT1} = 1.2\text{ V}$, PWM Mode

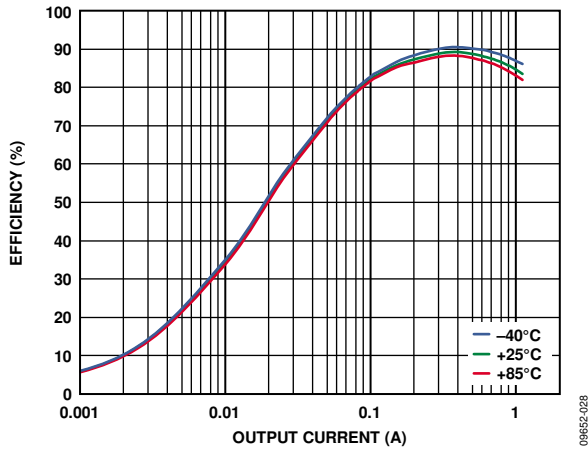


Figure 28. Buck Efficiency vs. Load Current, Across Temperature, $V_{IN} = 5.0\text{ V}$, $V_{OUT1} = 1.8\text{ V}$, PWM Mode

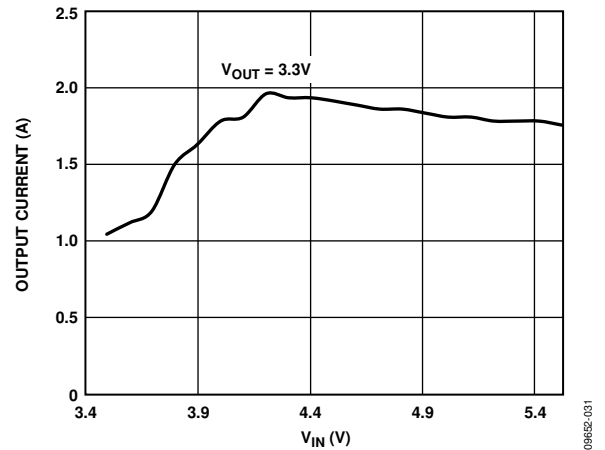


Figure 31. Buck DC Current Capability vs. Input Voltage

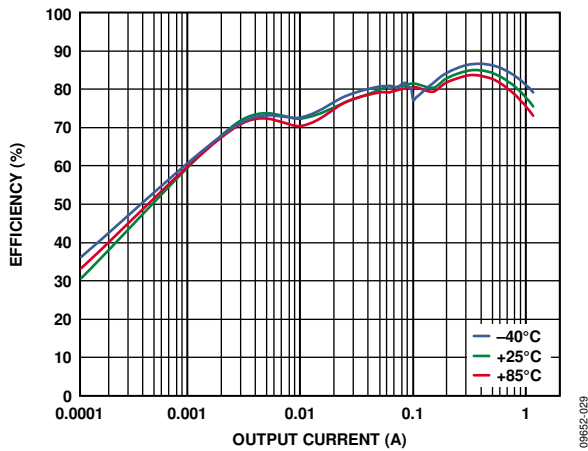


Figure 29. Buck Efficiency vs. Load Current, Across Temperature, $V_{IN} = 5.0\text{ V}$, $V_{OUT1} = 1.2\text{ V}$, Auto Mode

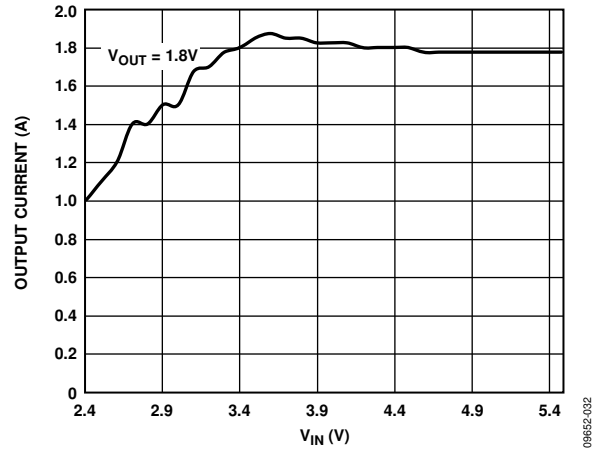


Figure 32. Buck DC Current Capability vs. Input Voltage

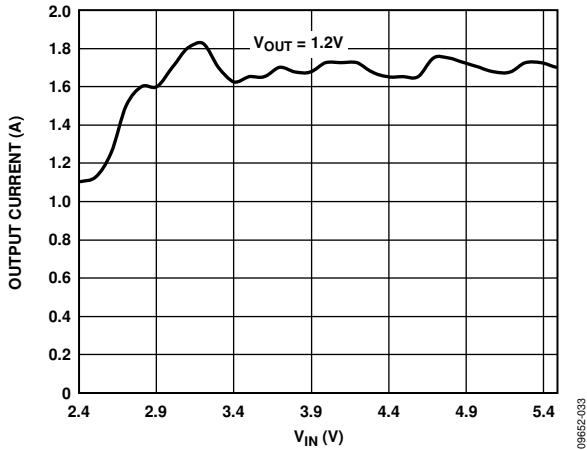


Figure 33. Buck DC Current Capability vs. Input Voltage

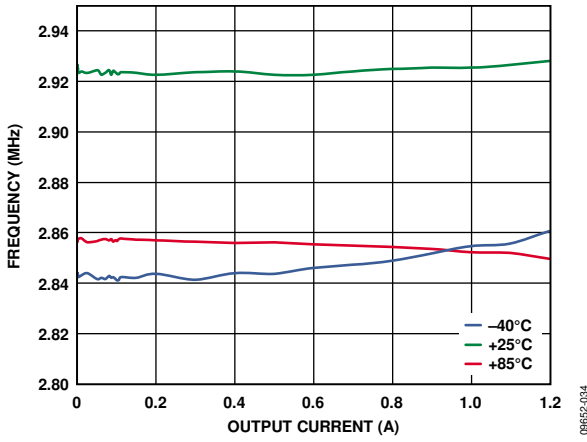


Figure 34. Buck Switching Frequency vs. Output Current, Across Temperature, $V_{OUT1} = 1.8V$, PWM Mode

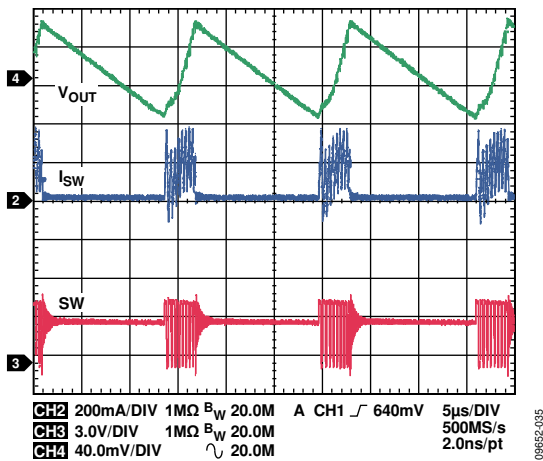


Figure 35. Typical Waveforms, $V_{OUT1} = 3.3V$, $I_{OUT1} = 30mA$, Auto Mode

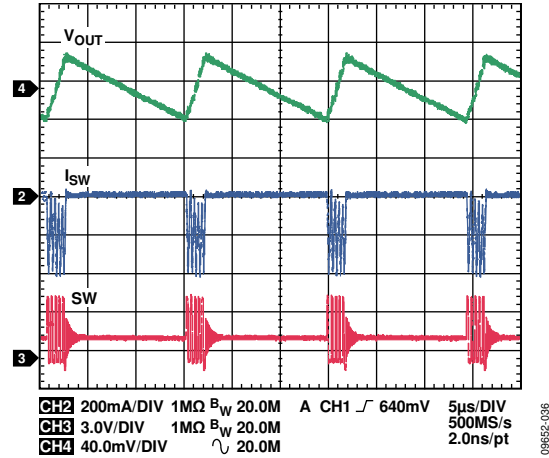


Figure 36. Typical Waveforms, $V_{OUT1} = 1.8V$, $I_{OUT1} = 30mA$, Auto Mode

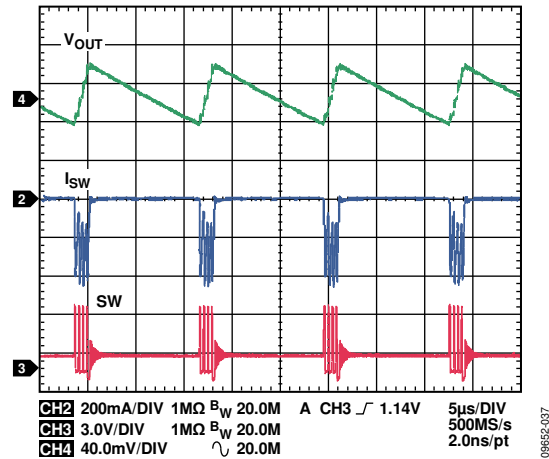


Figure 37. Typical Waveforms, $V_{OUT1} = 1.2V$, $I_{OUT1} = 30mA$, Auto Mode

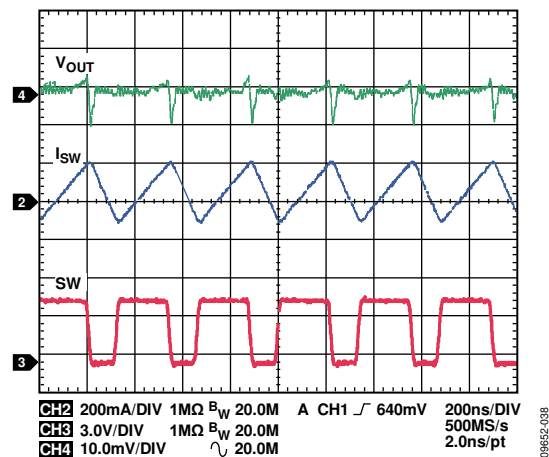


Figure 38. Typical Waveforms, $V_{OUT1} = 3.3V$, $I_{OUT1} = 30mA$, PWM Mode

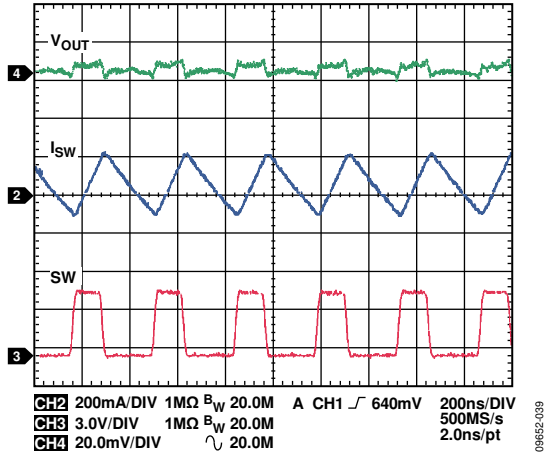


Figure 39. Typical Waveforms, $V_{OUT1} = 1.8\text{ V}$, $I_{OUT1} = 30\text{ mA}$, PWM Mode

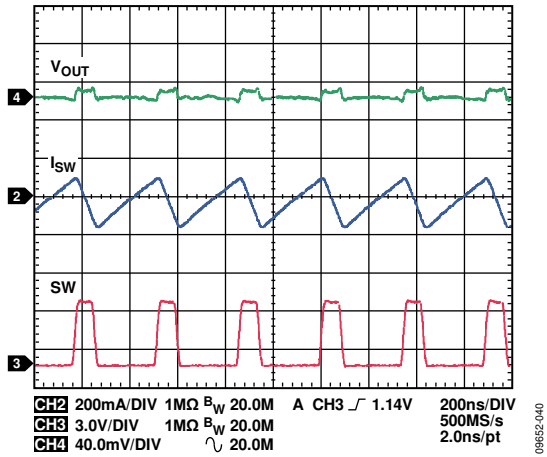


Figure 40. Typical Waveforms, $V_{OUT1} = 1.2\text{ V}$, $I_{OUT1} = 30\text{ mA}$, PWM Mode

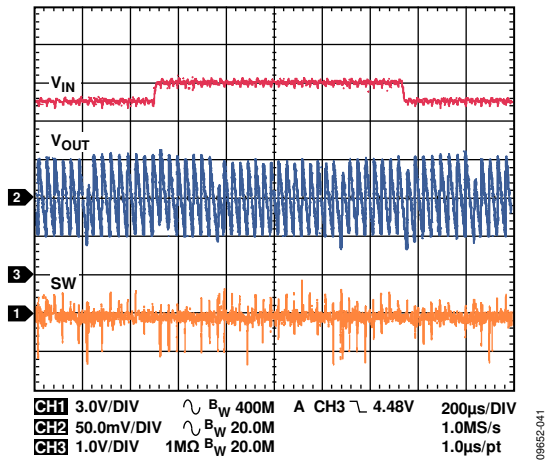


Figure 41. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, $V_{OUT1} = 3.3\text{ V}$, $I_{OUT1} = 5\text{ mA}$, Auto Mode

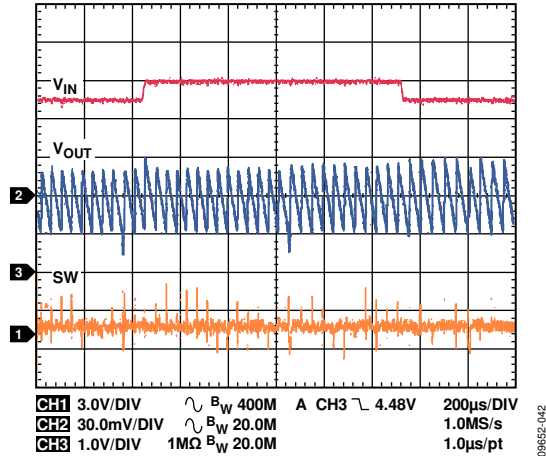


Figure 42. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, $V_{OUT1} = 1.8\text{ V}$, $I_{OUT1} = 5\text{ mA}$, Auto Mode

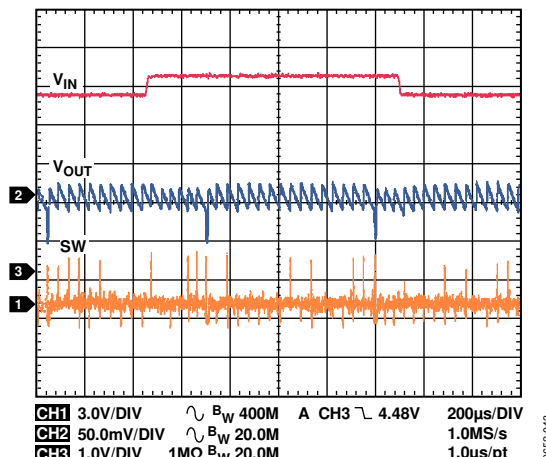


Figure 43. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, $V_{OUT1} = 1.2\text{ V}$, $I_{OUT1} = 5\text{ mA}$, Auto Mode

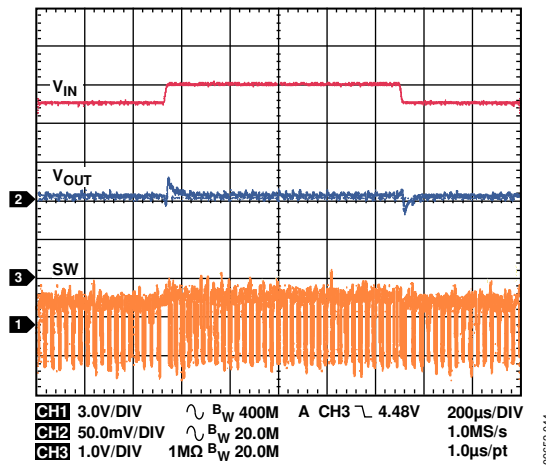


Figure 44. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, $V_{OUT1} = 3.3\text{ V}$, PWM Mode

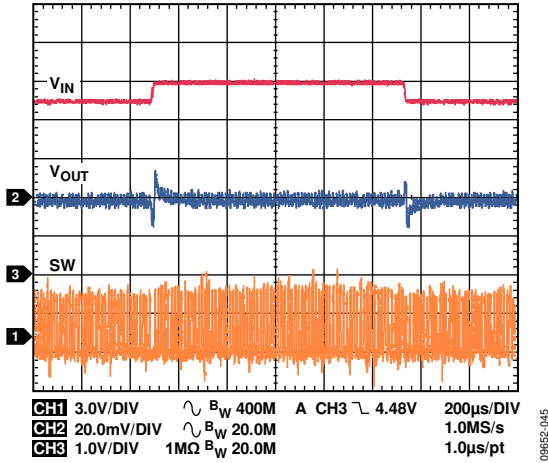


Figure 45. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, $V_{OUT1} = 1.8$ V, PWM Mode

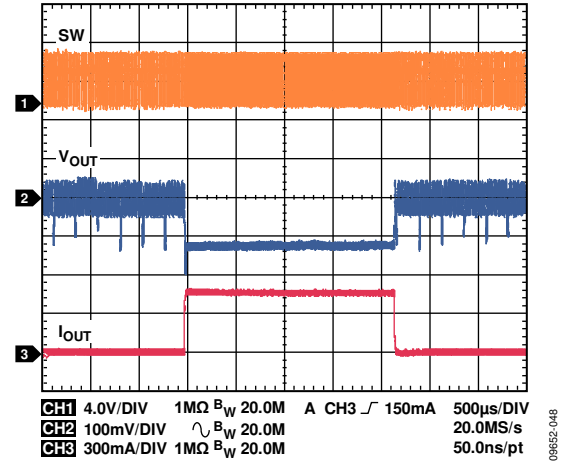


Figure 48. Buck Response to Load Transient, $I_{OUT1} = 50$ mA to 500 mA, $V_{OUT1} = 3.3$ V, Auto Mode

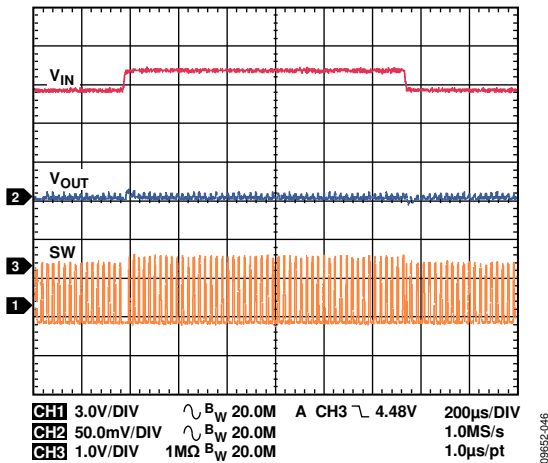


Figure 46. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, $V_{OUT1} = 1.2$ V, PWM Mode

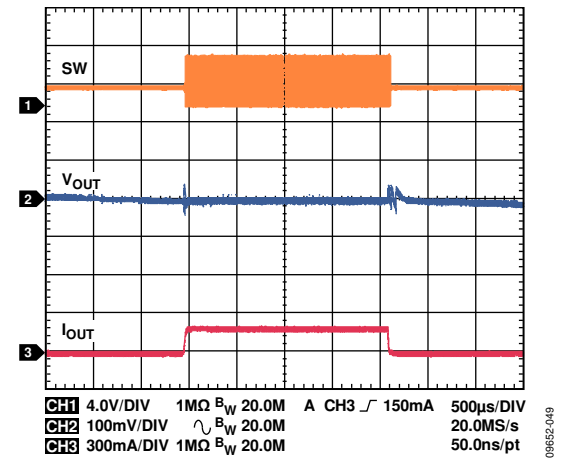


Figure 49. Buck Response to Load Transient, $I_{OUT1} = 20$ mA to 200 mA, $V_{OUT1} = 1.8$ V, Auto Mode

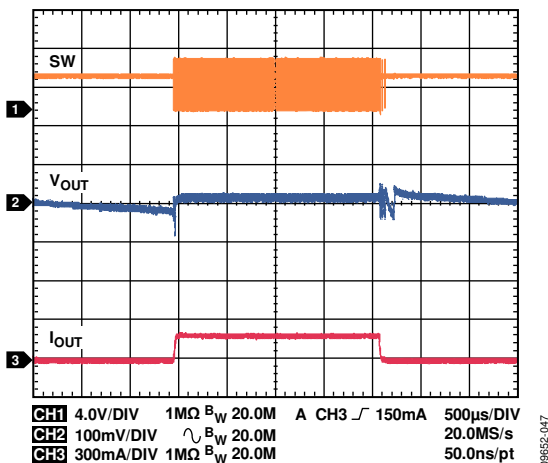


Figure 47. Buck Response to Load Transient, $I_{OUT1} = 20$ mA to 200 mA, $V_{OUT1} = 3.3$ V, Auto Mode

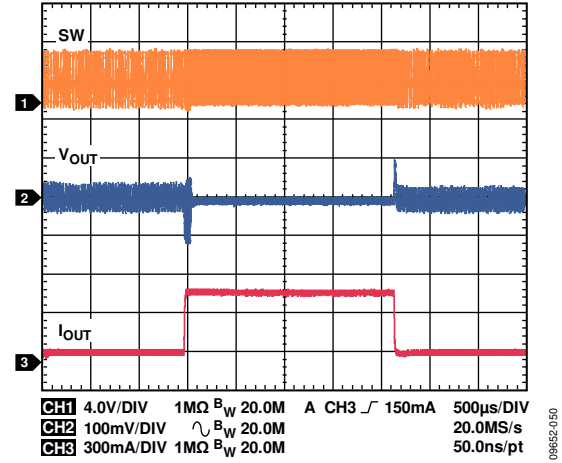


Figure 50. Buck Response to Load Transient, $I_{OUT1} = 50$ mA to 500 mA, $V_{OUT1} = 1.8$ V, Auto Mode

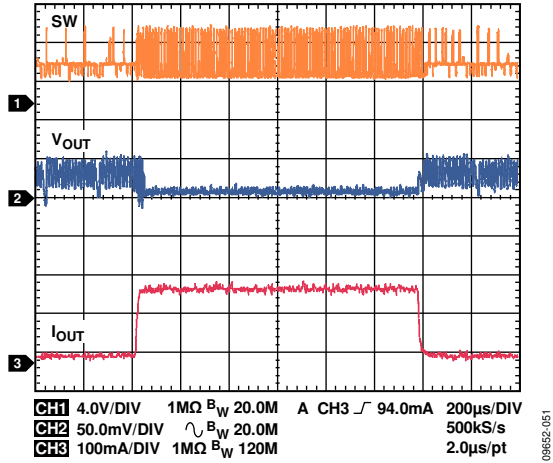


Figure 51. Buck Response to Load Transient, $I_{OUT1} = 20\text{ mA}$ to 200 mA , $V_{OUT1} = 1.2\text{ V}$, Auto Mode

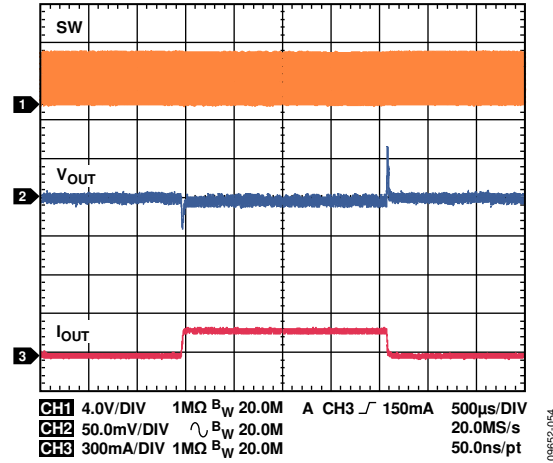


Figure 54. Buck Response to Load Transient, $I_{OUT1} = 50\text{ mA}$ to 500 mA , $V_{OUT1} = 3.3\text{ V}$, PWM Mode

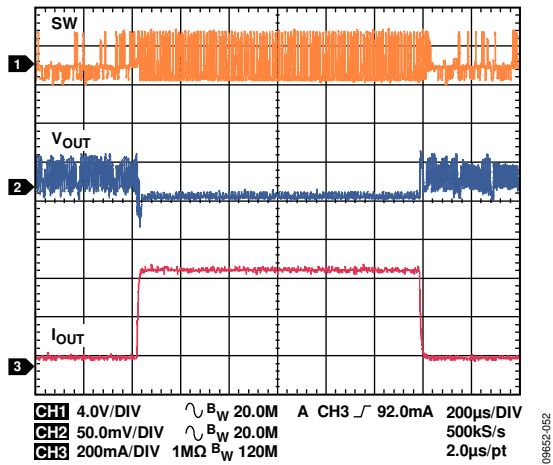


Figure 52. Buck Response to Load Transient, $I_{OUT1} = 50\text{ mA}$ to 500 mA , $V_{OUT1} = 1.2\text{ V}$, Auto Mode

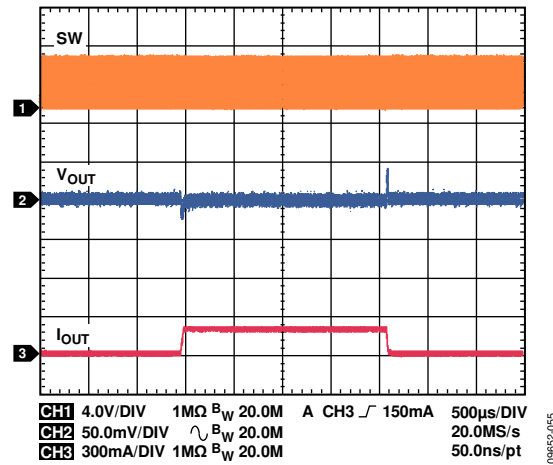


Figure 55. Buck Response to Load Transient, $I_{OUT1} = 20\text{ mA}$ to 200 mA , $V_{OUT1} = 1.8\text{ V}$, PWM Mode

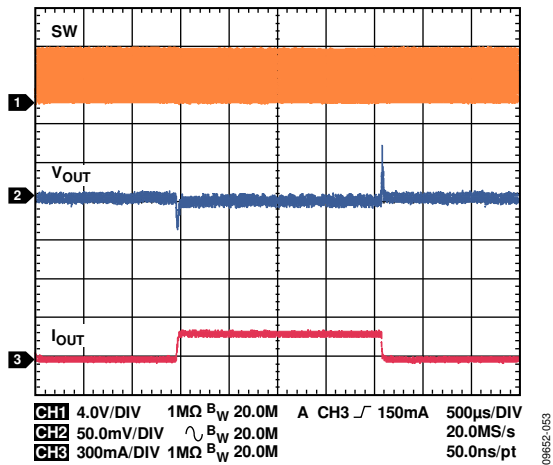


Figure 53. Buck Response to Load Transient, $I_{OUT1} = 20\text{ mA}$ to 200 mA , $V_{OUT1} = 3.3\text{ V}$, PWM Mode

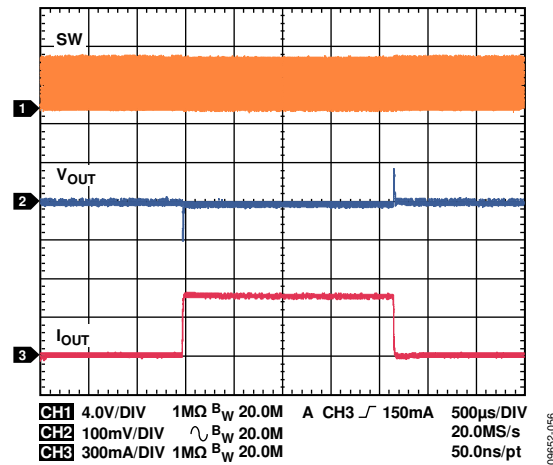


Figure 56. Buck Response to Load Transient, $I_{OUT1} = 50\text{ mA}$ to 500 mA , $V_{OUT1} = 1.8\text{ V}$, PWM Mode

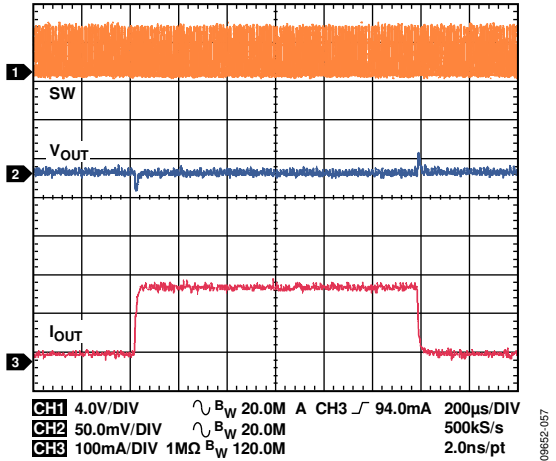


Figure 57. Buck Response to Load Transient, $I_{OUT1} = 20\text{ mA}$ to 200 mA , $V_{OUT1} = 1.2\text{ V}$, PWM Mode

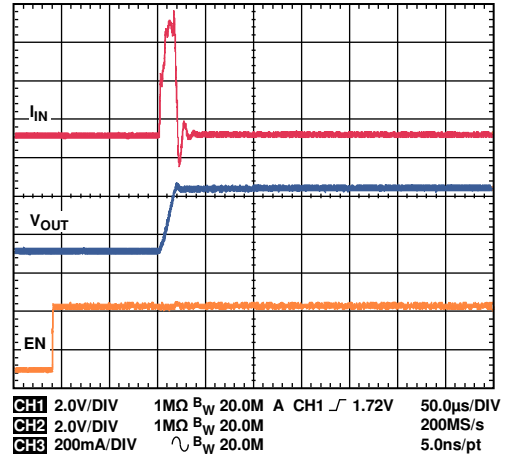


Figure 60. LDO1, LDO2 Startup, $V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 5\text{ mA}$

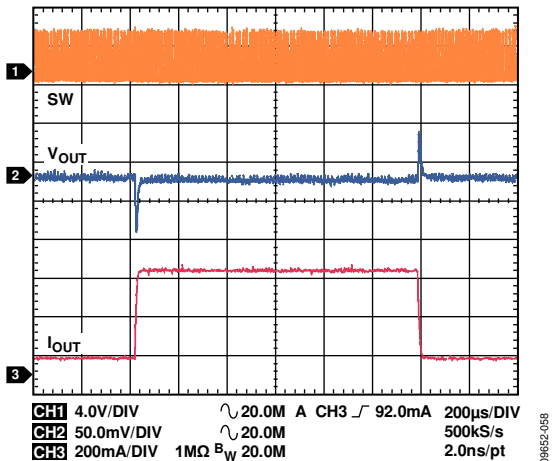


Figure 58. Buck Response to Load Transient, $I_{OUT1} = 50\text{ mA}$ to 500 mA , $V_{OUT1} = 1.2\text{ V}$, PWM Mode

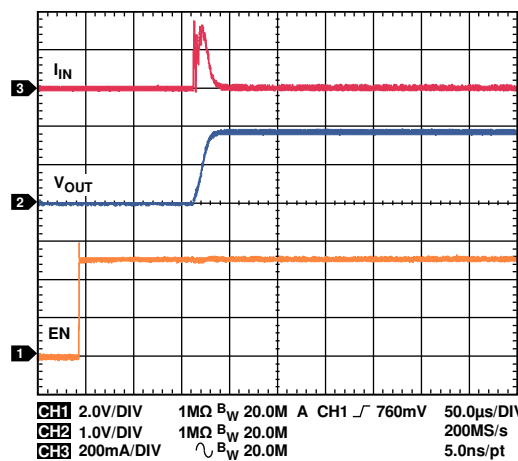


Figure 61. LDO1, LDO2 Startup, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 5\text{ mA}$

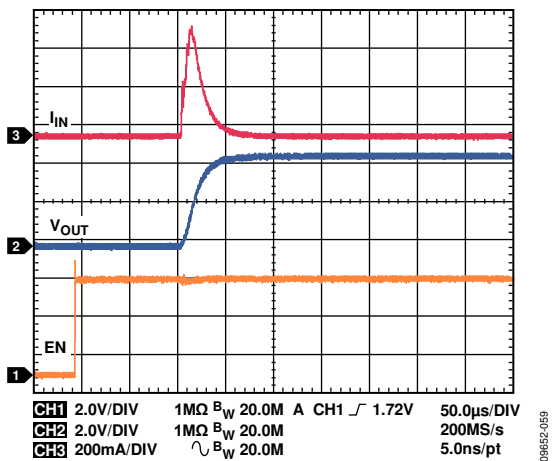


Figure 59. LDO1, LDO2 Startup, $V_{OUT} = 4.7\text{ V}$, $I_{OUT} = 5\text{ mA}$

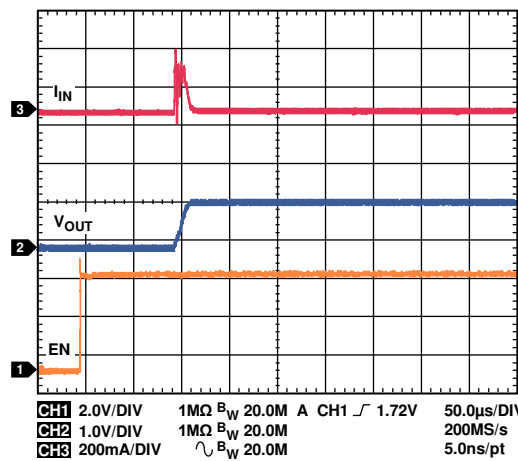


Figure 62. LDO1, LDO2 Startup, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 5\text{ mA}$

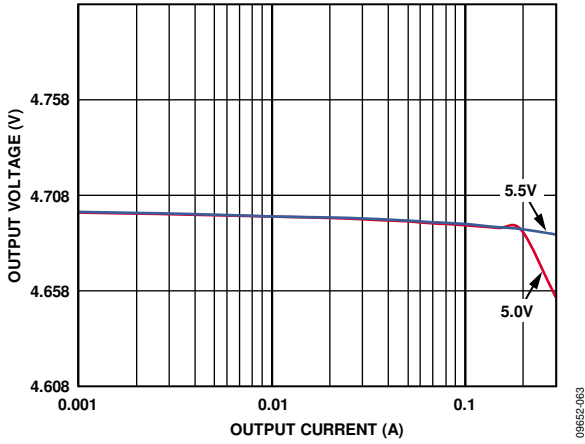


Figure 63. LDO1, LDO2 Load Regulation Across Input Voltage, $V_{OUT} = 4.7\text{ V}$

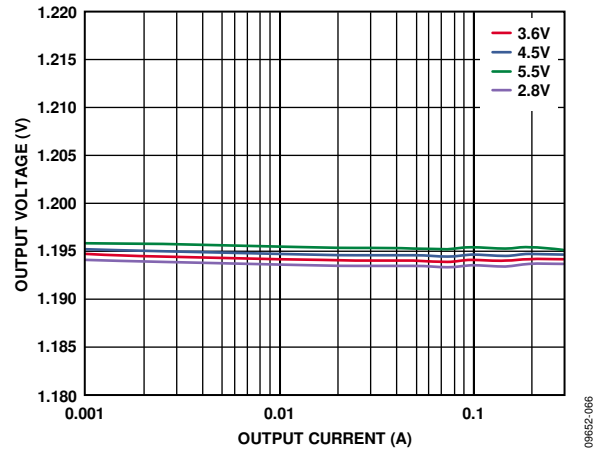


Figure 66. LDO1, LDO2 Load Regulation Across Input Voltage, $V_{OUT} = 1.2\text{ V}$

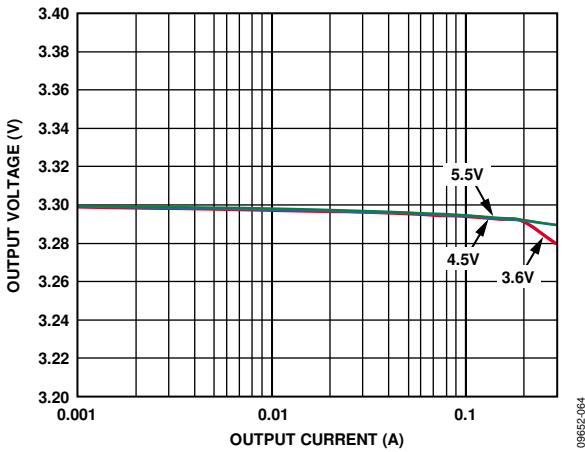


Figure 64. LDO1, LDO2 Load Regulation Across Input Voltage, $V_{OUT} = 3.3\text{ V}$

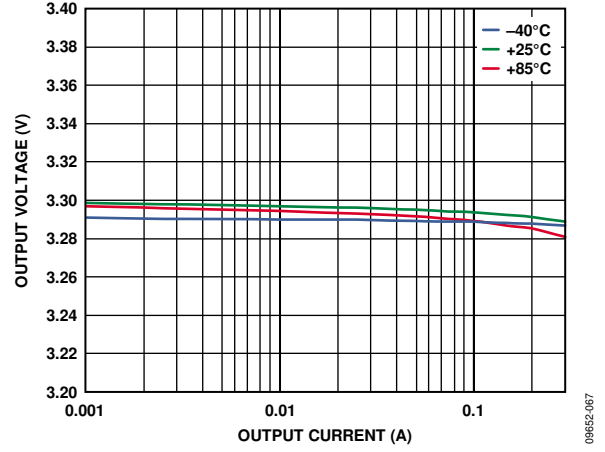


Figure 67. LDO1, LDO2 Load Regulation Across Temperature, $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 3.3\text{ V}$

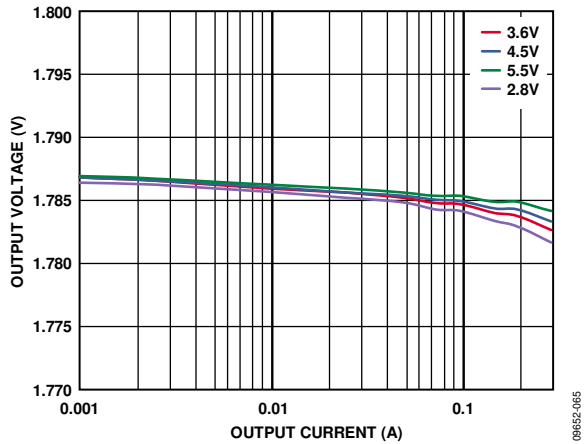


Figure 65. LDO1, LDO2 Load Regulation Across Input Voltage, $V_{OUT} = 1.8\text{ V}$

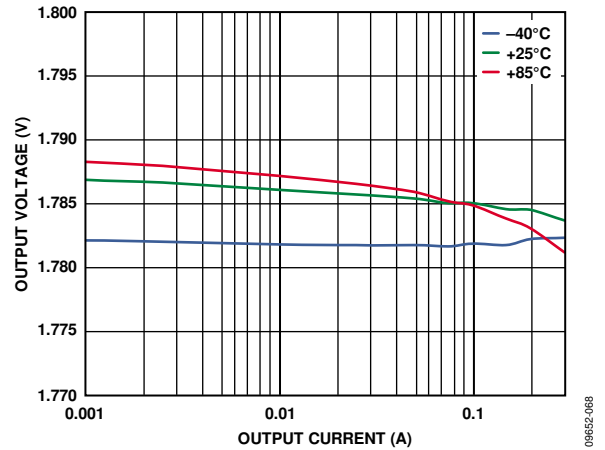


Figure 68. LDO1, LDO2 Load Regulation Across Temperature, $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 1.8\text{ V}$

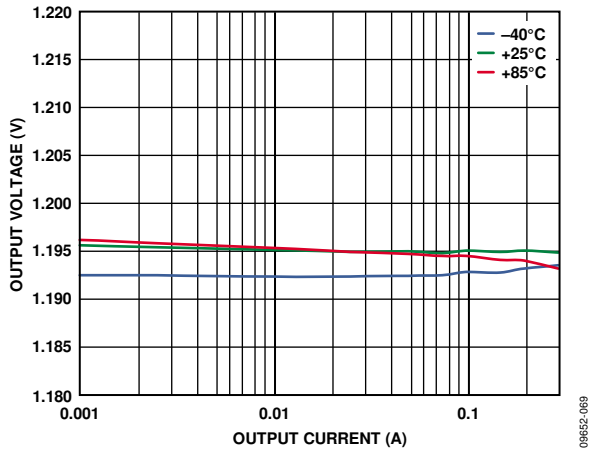


Figure 69. LDO1, LDO2 Load Regulation Across Temperature, $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 1.2\text{ V}$

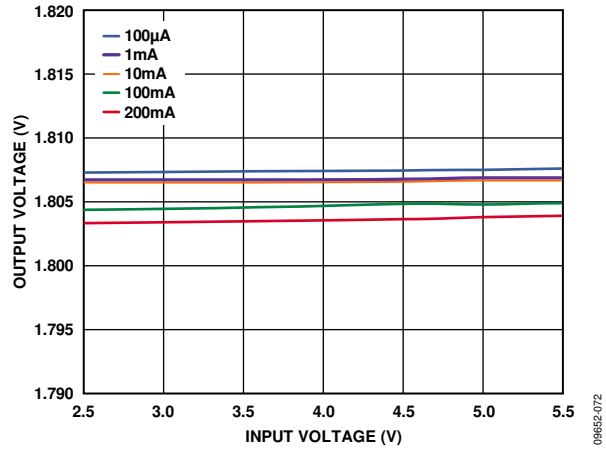


Figure 72. LDO1, LDO2 Line Regulation Across Input Voltage, $V_{OUT} = 1.8\text{ V}$

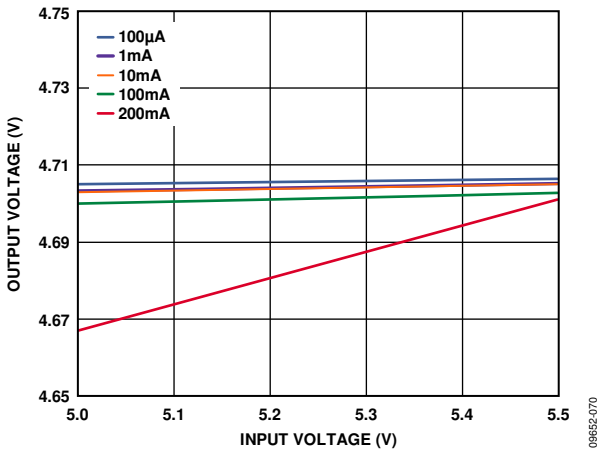


Figure 70. LDO1, LDO2 Line Regulation Across Input Voltage, $V_{OUT} = 4.7\text{ V}$

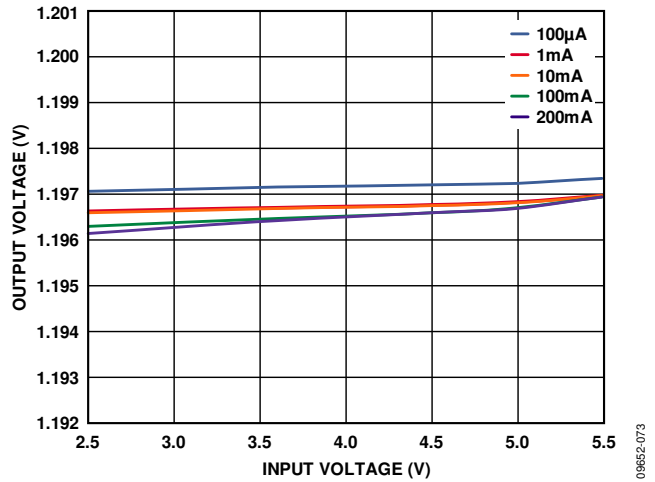


Figure 73. LDO1, LDO2 Line Regulation Across Input Voltage, $V_{OUT} = 1.2\text{ V}$

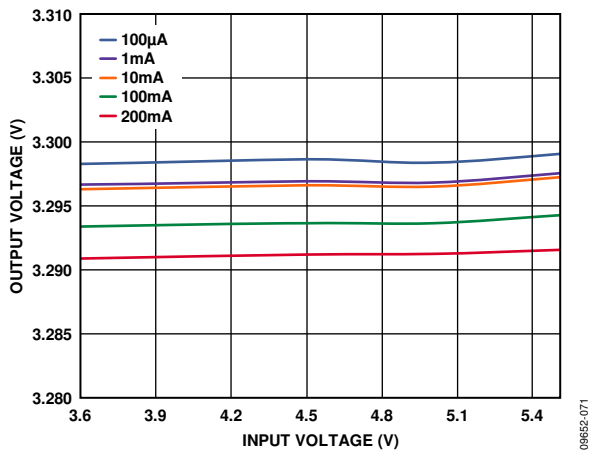


Figure 71. LDO1, LDO2 Line Regulation Across Input Voltage, $V_{OUT} = 3.3\text{ V}$

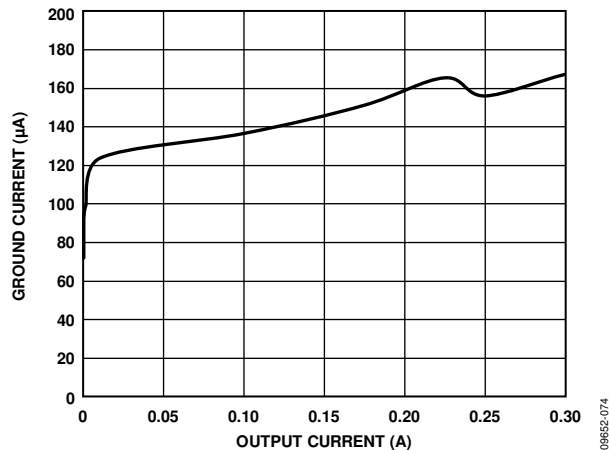


Figure 74. LDO1, LDO2 Ground Current vs. Output Current, $V_{OUT} = 3.3\text{ V}$

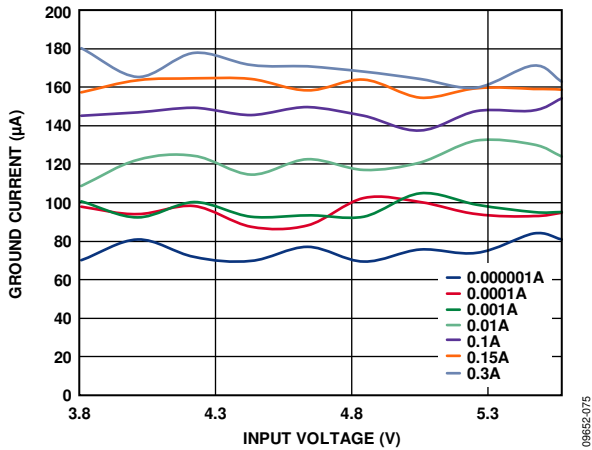


Figure 75. LDO1, LDO2 Ground Current vs. Input Voltage, Across Output Load (A), $V_{OUT} = 3.3\text{ V}$

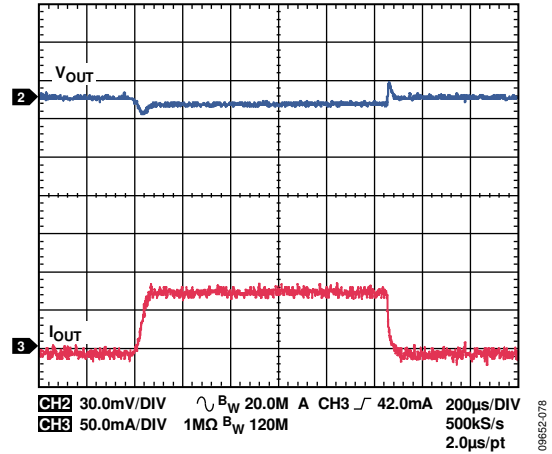


Figure 78. LDO1, LDO2 Response to Load Transient, I_{OUT} from 1 mA to 80 mA, $V_{OUT} = 3.3\text{ V}$

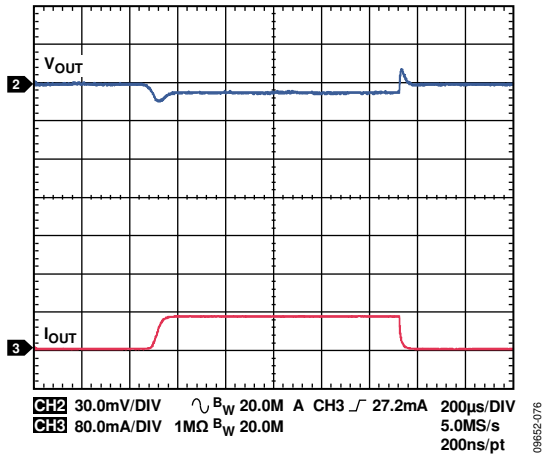


Figure 76. LDO1, LDO2 Response to Load Transient, I_{OUT} from 1 mA to 27.2 mA, $V_{OUT} = 4.7\text{ V}$

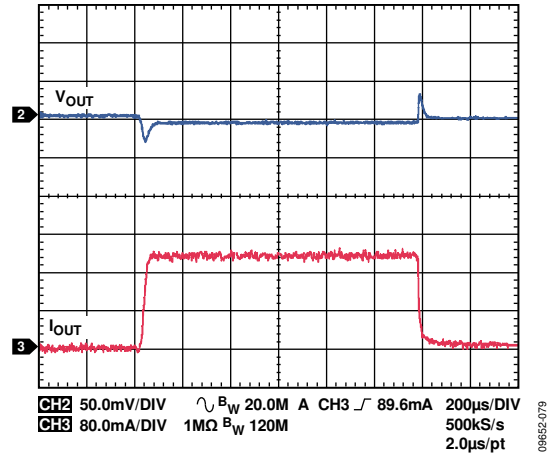


Figure 79. LDO1, LDO2 Response to Load Transient, I_{OUT} from 10 mA to 89.6 mA, $V_{OUT} = 3.3\text{ V}$

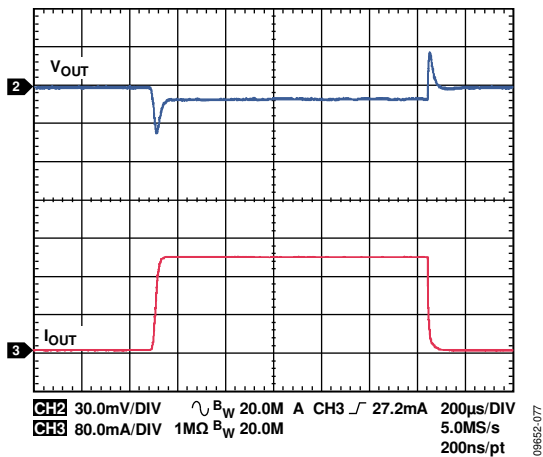


Figure 77. LDO1, LDO2 Response to Load Transient, I_{OUT} from 10 mA to 27.2 mA, $V_{OUT} = 4.7\text{ V}$

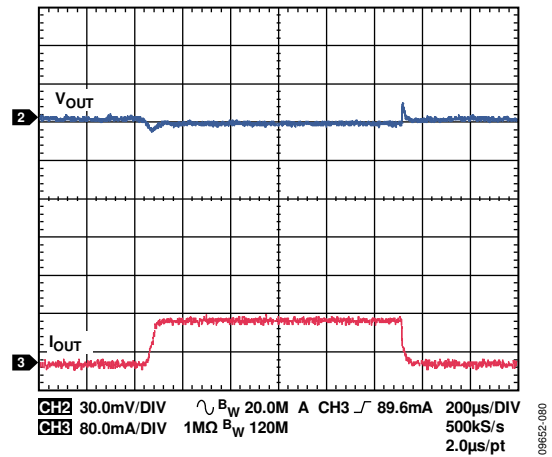


Figure 80. LDO1, LDO2 Response to Load Transient, I_{OUT} from 1 mA to 89.6 mA, $V_{OUT} = 1.8\text{ V}$

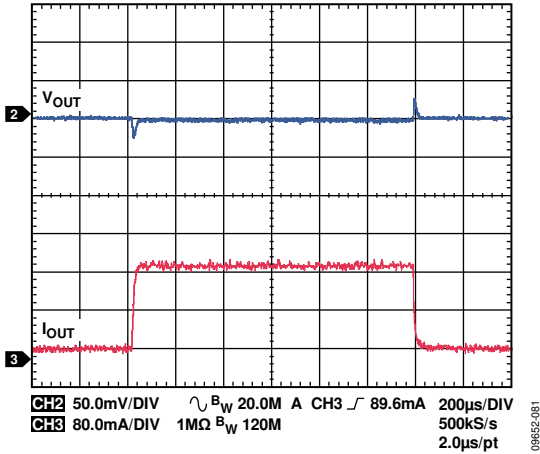


Figure 81. LDO1, LDO2 Response to Load Transient, I_{OUT} from 10 mA to 200 mA, $V_{OUT} = 1.8$ V

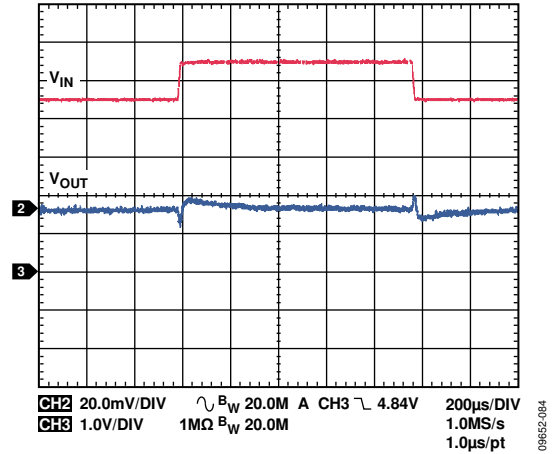


Figure 84. LDO1, LDO2 Response to Line Transient, Input Voltage from 4.5 V to 5.5 V, $V_{OUT} = 3.3$ V

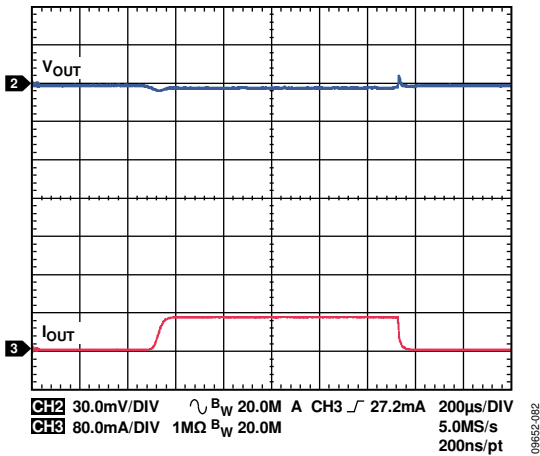


Figure 82. LDO1, LDO2 Response to Load Transient, I_{OUT} from 1 mA to 80 mA, $V_{OUT} = 1.2$ V

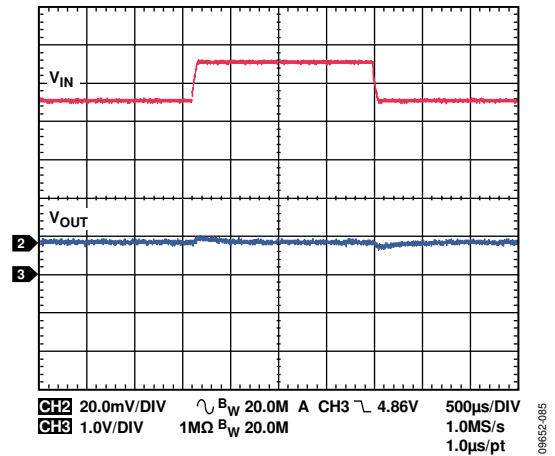


Figure 85. LDO1, LDO2 Response to Line Transient, Input Voltage from 4.5 V to 5.5 V, $V_{OUT} = 1.8$ V

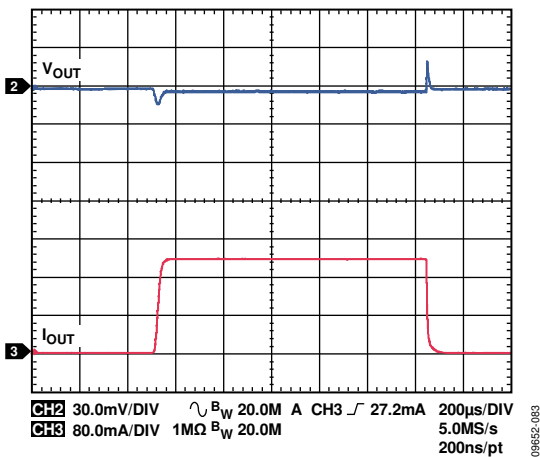


Figure 83. LDO1, LDO2 Response to Load Transient, I_{OUT} from 10 mA to 200 mA, $V_{OUT} = 1.2$ V

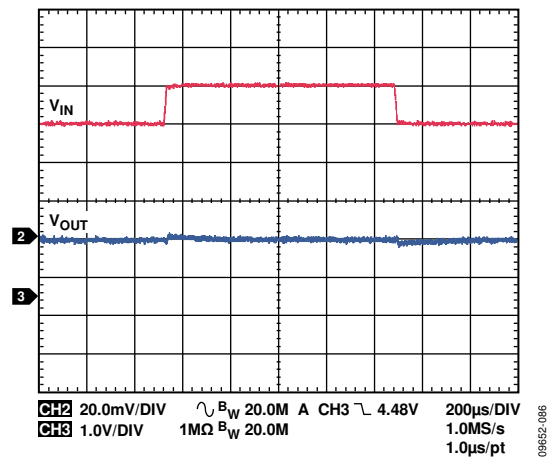


Figure 86. LDO1, LDO2 Response to Line Transient, Input Voltage from 4.5 V to 5.5 V, $V_{OUT} = 1.2$ V

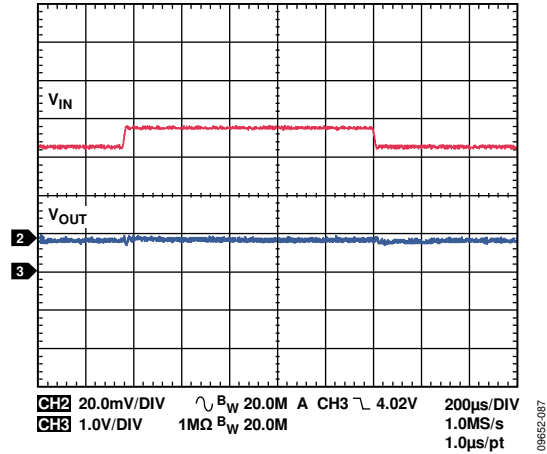


Figure 87. LDO1, LDO2 Response to Line Transient, Input Voltage from 3.3 V to 3.8 V, $V_{OUT} = 1.8$ V

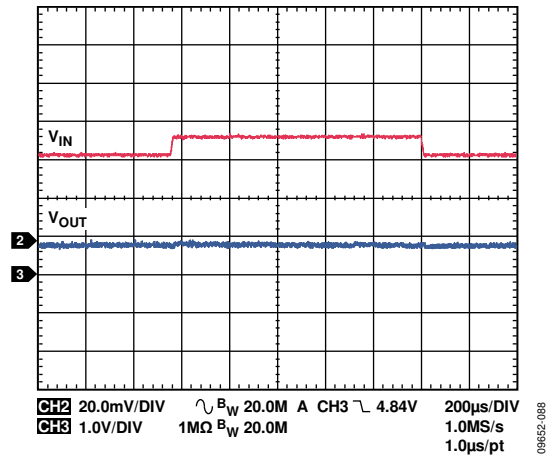


Figure 88. LDO1, LDO2 Response to Line Transient, Input Voltage from 3.3 V to 3.8 V, $V_{OUT} = 1.2$ V

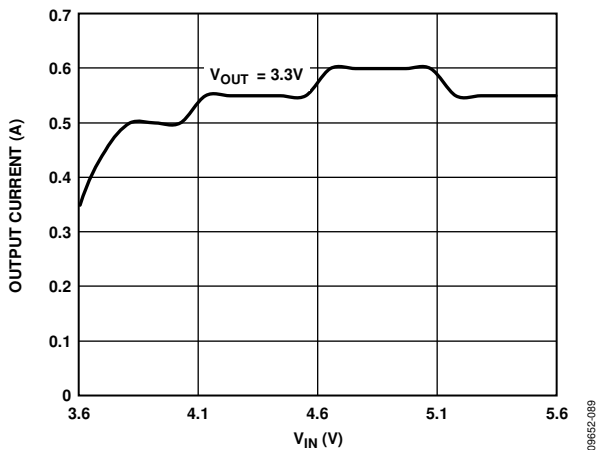


Figure 89. LDO1, LDO2 Output Current Capability vs. Input Voltage

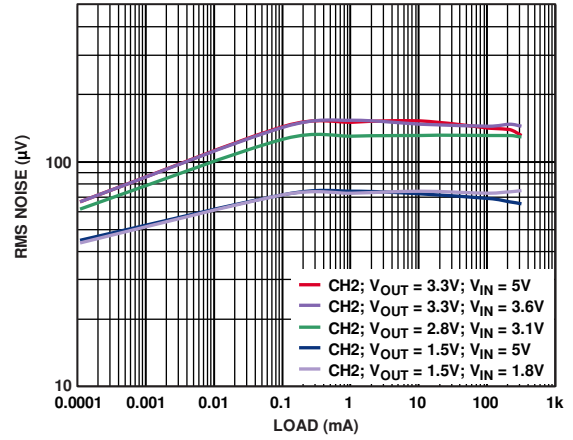


Figure 90. LDO1 Output Noise vs. Load Current, Across Input and Output Voltage

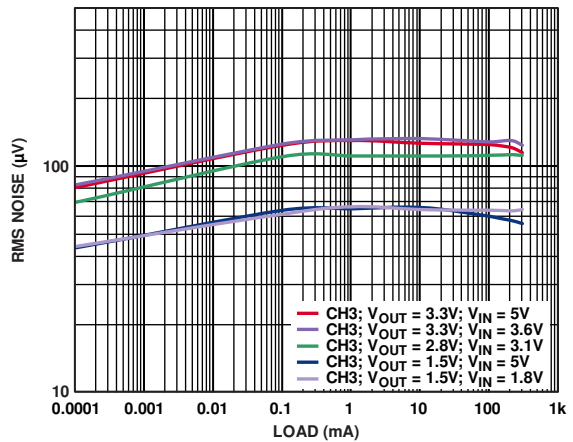


Figure 91. LDO2 Output Noise vs. Load Current, Across Input and Output Voltage

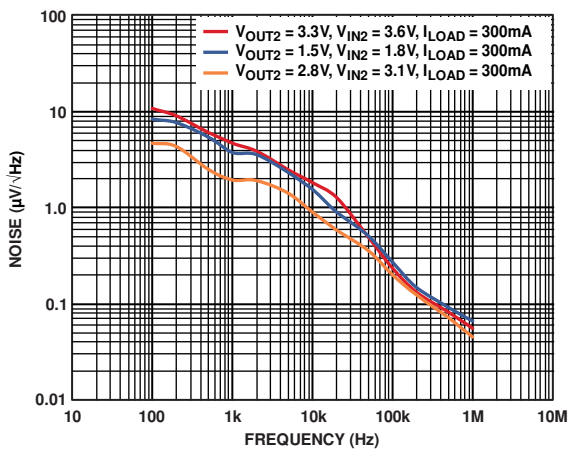


Figure 92. LDO1 Noise Spectrum Across Output Voltage, $V_{IN} = V_{OUT} + 0.3$ V

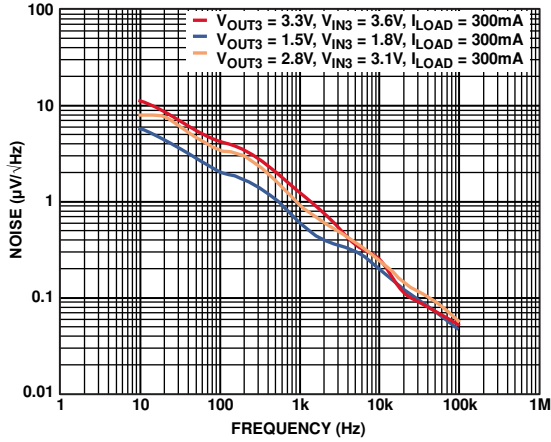


Figure 93. LDO2 Noise Spectrum Across Output Voltage, $V_{IN} = V_{OUT} + 0.3V$

09652-115

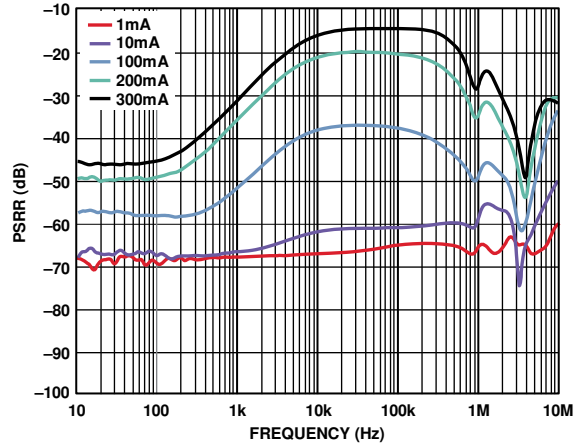


Figure 96. LDO2 PSRR Across Output Load, $V_{IN3} = 3.1V, V_{OUT3} = 2.8V$

09652-110

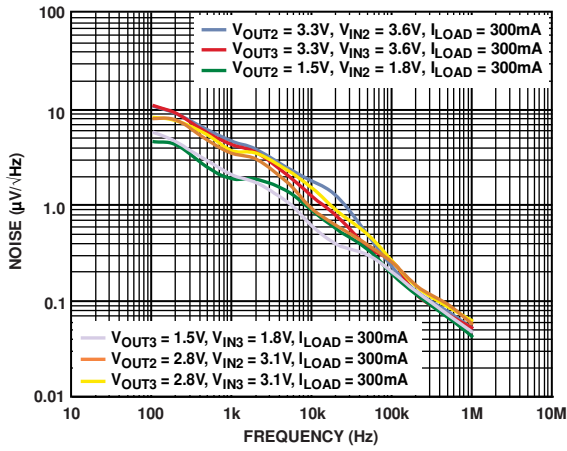


Figure 94. LDO1 vs. LDO2 Noise Spectrum

09652-108

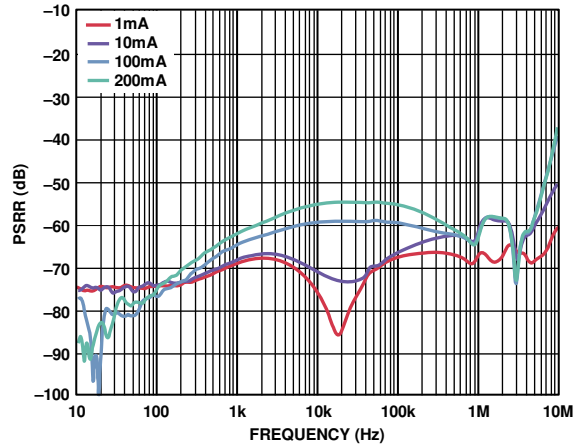


Figure 97. LDO2 PSRR Across Output Load, $V_{IN3} = 5.0V, V_{OUT3} = 3.3V$

09652-111

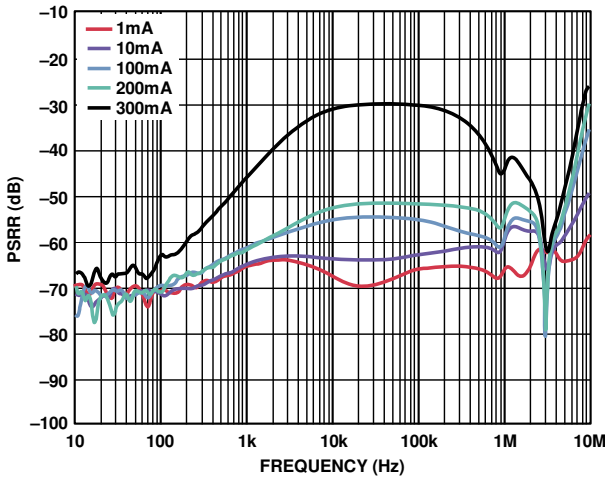


Figure 95. LDO2 PSRR Across Output Load, $V_{IN3} = 3.3V, V_{OUT3} = 2.8V$

09652-109

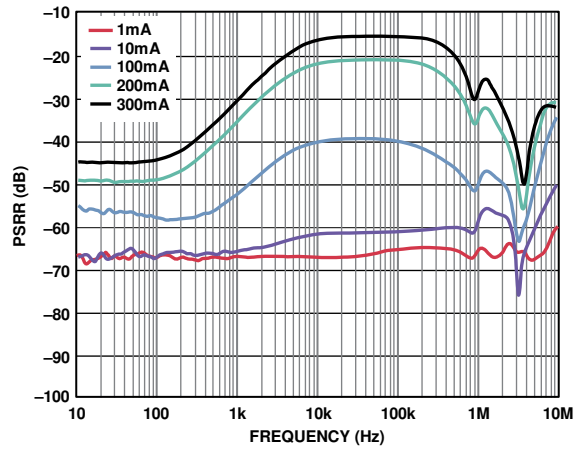


Figure 98. LDO2 PSRR Across Output Load, $V_{IN3} = 3.6V, V_{OUT3} = 3.3V$

09652-112