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5-Channel Integrated Power Solution with Quad Buck Regulators and 200 mA LDO Regulator

Data Sheet **ADP5050**

FEATURES

- Wide input voltage range: 4.5 V to 15 V
- ±1.5% output accuracy over full temperature range
- 250 kHz to 1.4 MHz adjustable switching frequency
- Adjustable/fixed output options via factory fuse or I²C interface
- I²C interface with interrupt on fault conditions
- Power regulation
  - Channel 1 and Channel 2: programmable 1.2 A/2.5 A/4 A sync buck regulators with low-side FET driver
  - Channel 3 and Channel 4: 1.2 A sync buck regulators
  - Channel 5: 200 mA low dropout (LDO) regulator
- Single 8 A output (Channel 1 and Channel 2 operated in parallel)
- Dynamic voltage scaling (DVS) for Channel 1 and Channel 4
- Precision enable with 0.8 V accurate threshold
- Active output discharge switch
- Programmable phase shift in 90° steps
- Individual channel FPWM/PSM mode selection
- Frequency synchronization input or output
- Optional latch-off protection on OVP/OCP failure
- Power-good flag on selected channels
- Low input voltage detection
- Overheat detection on junction temperature
- UVLO, OCP, and TSD protection
- 48-lead, 7 mm × 7 mm LFCSP package
- –40°C to +125°C junction temperature

APPLICATIONS

- Small cell base stations
- FPGA and processor applications
- Security and surveillance
- Medical applications

GENERAL DESCRIPTION

The ADP5050 combines four high performance buck regulators and one 200 mA low dropout (LDO) regulator in a 48-lead LFCSP package that meets demanding performance and board space requirements. The device enables direct connection to high input voltages up to 15 V with no preregulators.

Channel 1 and Channel 2 integrate high-side power MOSFETs and low-side MOSFET drivers. External NFETs can be used in low-side power devices to achieve an efficiency optimized solution and deliver a programmable output current of 1.2 A, 2.5 A, or 4 A. Combining Channel 1 and Channel 2 in a parallel configuration can provide a single output with up to 8 A of current.

Channel 3 and Channel 4 integrate both high-side and low-side MOSFETs to deliver output current of 1.2 A.

TYPICAL APPLICATION CIRCUIT

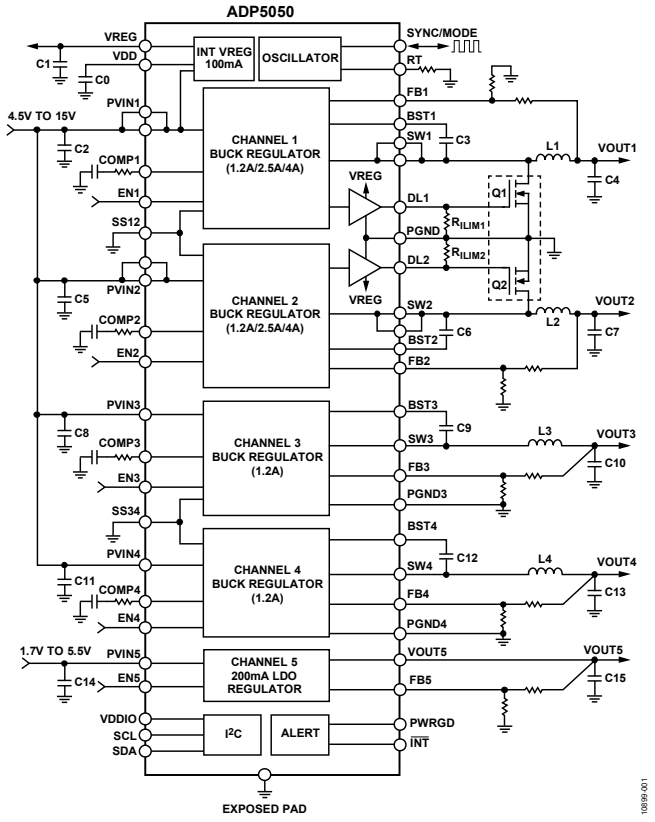

Figure 1.

Table 1. Family Models

Model	Channels	I²C	Package
ADP5050	Four bucks, one LDO	Yes	48-Lead LFCSP
ADP5051	Four bucks, supervisory	Yes	48-Lead LFCSP
ADP5052	Four bucks, one LDO	No	48-Lead LFCSP
ADP5053	Four bucks, supervisory	No	48-Lead LFCSP
ADP5054	Four high current bucks	No	48-Lead LFCSP

The switching frequency of the ADP5050 can be programmed or synchronized to an external clock. The ADP5050 contains a precision enable pin on each channel for easy power-up sequencing or adjustable UVLO threshold.

The ADP5050 integrates a general-purpose LDO regulator with low quiescent current and low dropout voltage that provides up to 200 mA of output current.

The optional I²C interface provides the user with flexible configuration options, including adjustable and fixed output voltage options, junction temperature overheat warning, low input voltage detection, and dynamic voltage scaling (DVS).

Rev. C
Document Feedback

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ADP5050* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADP5050 Evaluation Board

DOCUMENTATION

Data Sheet

- ADP5050: 5-Channel Integrated Power Solution with Quad Buck Regulators and 200 mA LDO Regulator Data Sheet

TOOLS AND SIMULATIONS

- ADIsimPower™ Voltage Regulator Design Tool
- ADP505x Buck Regulator Design Tool

REFERENCE MATERIALS

Press

- Tiny Integrated Solution Powers RF Agile Radio Applications and FPGAs

Solutions Bulletins & Brochures

- Integrated Power Solutions for Altera FPGAs
- Integrated, High Power Solutions for Xilinx FPGAs

DESIGN RESOURCES

- ADP5050 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADP5050 EngineerZone Discussions.

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REVISION HISTORY

10/2016—Rev. B to Rev. C

Deleted Factory Programmable Options Section and Table 52 to Table 65; Renumbered Sequentially 54
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Updated Outline Dimensions 55

9/2015—Rev. A to Rev. B

Changes to Figure 1 and Table 1 1

3/2014—Rev. 0 to Rev. A

Changed Pin 13 from nINT to $\overline{INT}$ .... Throughout
Added Table 1; Renumbered Sequentially 1
Changes to Figure 8 13
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Changes to Table 14 30
Updated Outline Dimensions (Exposed Paddle Changed for JEDEC Compliance) 57

5/2013—Revision 0: Initial Version

DETAILED FUNCTIONAL BLOCK DIAGRAM

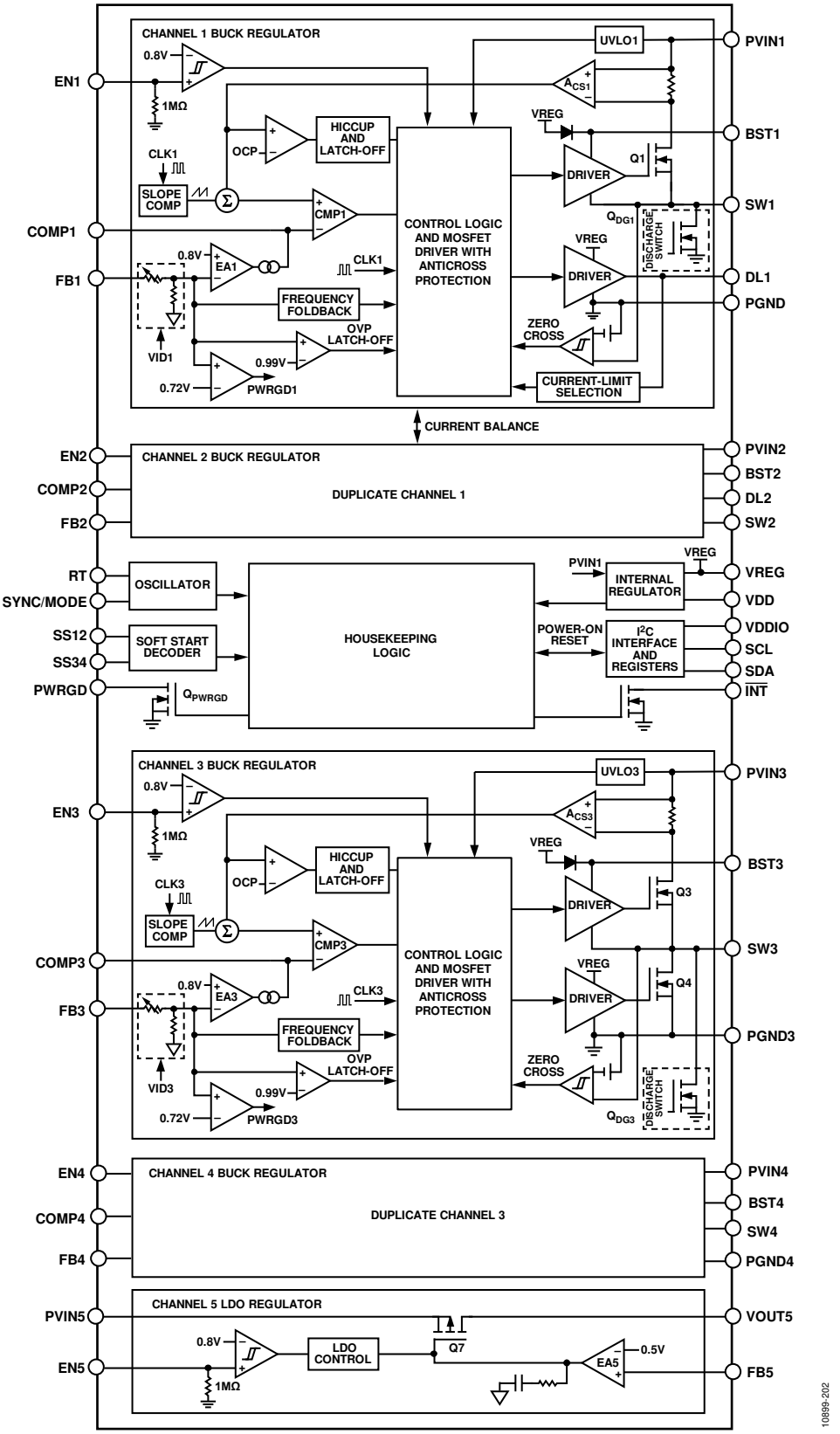

Figure 2.

SPECIFICATIONS

V_{IN} = 12 V, V_{VREG} = 5.1 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT SUPPLY VOLTAGE RANGE	V_{IN}	4.5		15.0	V	PVIN1, PVIN2, PVIN3, PVIN4 pins
QUIESCENT CURRENT						PVIN1, PVIN2, PVIN3, PVIN4 pins
Operating Quiescent Current	$I_{Q(4\text{-}BUCKS)}$		4.8	6.25	mA	No switching, all ENx pins high
	$I_{SHDN(4BUCKS+LDO)}$		25	65	µA	All ENx pins low
UNDERVOLTAGE LOCKOUT	UVLO					PVIN1, PVIN2, PVIN3, PVIN4 pins
Rising Threshold	$V_{UVLO\text{-}RISING}$		4.2	4.36	V	
Falling Threshold	$V_{UVLO\text{-}FALLING}$	3.6	3.78		V	
Hysteresis	V_{HYS}		0.42		V	
OSCILLATOR CIRCUIT						
Switching Frequency	f_{SW}	700	740	780	kHz	RT = 25.5 kΩ
Switching Frequency Range		250		1400	kHz	
SYNC Input						
Input Clock Range	f_{SYNC}	250		1400	kHz	
Input Clock Pulse Width						
Minimum On Time	$t_{SYNC\_MIN\_ON}$	100			ns	
Minimum Off Time	$t_{SYNC\_MIN\_OFF}$	100			ns	
Input Clock High Voltage	$V_{H(SYNC)}$	1.3			V	
Input Clock Low Voltage	$V_{L(SYNC)}$			0.4	V	
SYNC Output						
Clock Frequency	f_{CLK}		f_{SW}		kHz	
Positive Pulse Duty Cycle	$t_{CLK\_PULSE\_DUTY}$		50		%	
Rise or Fall Time	$t_{CLK\_RISE\_FALL}$		10		ns	
High Level Voltage	$V_{H(SYNC\_OUT)}$		V_{VREG}		V	
PRECISION ENABLING						EN1, EN2, EN3, EN4, EN5 pins
High Level Threshold	$V_{TH\_H(EN)}$		0.806	0.832	V	
Low Level Threshold	$V_{TH\_L(EN)}$	0.688	0.725		V	
Pull-Down Resistor	$R_{PULL\text{-}DOWN(EN)}$		1.0		MΩ	
POWER GOOD						
Internal Power-Good Rising Threshold	$V_{PWRGD(RISE)}$	86.3	90.5	95	%	
Internal Power-Good Hysteresis	$V_{PWRGD(HYS)}$		3.3		%	
Internal Power-Good Falling Delay	t_{PWRGD_FALL}		50		µs	
Rising Delay for PWRGD Pin	$t_{PWRGD\_PIN\_RISE}$		1		ms	
Leakage Current for PWRGD Pin	$I_{PWRGD\_LEAKAGE}$		0.1	1	µA	
Output Low Voltage for PWRGD Pin	V_{PWRGD_LOW}		50	100	mV	I_{PWRGD} = 1 mA
LOGIC INPUTS (SCL AND SDA PINS)						VDDIO = 3.3 V
High Level Threshold	V_{LOGIC_HIGH}	0.7 × VDDIO			V	
Low Level Threshold	V_{LOGIC_LOW}			0.3 × VDDIO	V	
LOGIC OUTPUTS						
Low Level Output Voltage						
SDA Pin	V_{SDA_LOW}			0.4	V	VDDIO = 3.3 V, I_{SDA} = 3 mA
$\overline{INT}$ Pin	$V_{\overline{INT}\_LOW}$			0.4	V	$I_{\overline{INT}}$ = 3 mA
INTERNAL REGULATORS						
VDD Output Voltage	V_{VDD}	3.2	3.305	3.4	V	I_{VDD} = 10 mA
VDD Current Limit	I_{LIM_VDD}	20	51	80	mA	
VREG Output Voltage	V_{VREG}	4.9	5.1	5.3	V	
VREG Dropout Voltage	$V_{DROPOUT}$		225		mV	I_{VREG} = 50 mA
VREG Current Limit	I_{LIM_VREG}	50	95	140	mA	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOW INPUT VOLTAGE DETECTION						
Low Input Voltage Threshold	$V_{LVIN-TH}$	4.07	4.236	4.39	V	LVIN_TH[3:0] = 0000
		10.05	10.25	10.4	V	LVIN_TH[3:0] = 1100
Low Input Voltage Threshold Range		4.2		11.2	V	I^2C programmable (4-bit value)
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SHDN}		150		°C	
Thermal Shutdown Hysteresis	T_{HYS}		15		°C	
THERMAL OVERHEAT WARNING						
Thermal Overheat Threshold	T_{HOT}		115		°C	TEMP_TH[1:0] = 10
Overheat Threshold Range		105		125	°C	I^2C programmable (2-bit value)
Thermal Overheat Hysteresis	$T_{HOT(HYS)}$		5		°C	

BUCK REGULATOR SPECIFICATIONS

V_{IN} = 12 V, V_{VREG} = 5.1 V, f_{SW} = 600 kHz for all channels, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL 1 SYNC BUCK REGULATOR						
FB1 Pin						
Fixed Output Options	V_{OUT1}	0.85		1.60	V	Fuse trim or I^2C interface (5-bit value)
Adjustable Feedback Voltage	V_{FB1}		0.800		V	
Feedback Voltage Accuracy	$V_{FB1(DEFAULT)}$	−0.55		+0.55	%	T_J = 25°C
		−1.25		+1.0	%	0°C ≤ T_J ≤ 85°C
		−1.5		+1.5	%	−40°C ≤ T_J ≤ +125°C
Feedback Bias Current	I_{FB1}			0.1	µA	Adjustable voltage
SW1 Pin						
High-Side Power FET On Resistance	$R_{DSON(1H)}$		100		mΩ	Pin-to-pin measurement
Current-Limit Threshold	$I_{TH(ILIM1)}$	3.50	4.4	5.28	A	R_{ILIM1} = floating
		1.91	2.63	3.08	A	R_{ILIM1} = 47 kΩ
		4.95	6.44	7.48	A	R_{ILIM1} = 22 kΩ
Minimum On Time	t_{MIN_ON1}		117	155	ns	f_{SW} = 250 kHz to 1.4 MHz
Minimum Off Time	t_{MIN_OFF1}		1/9 × t_{SW}		ns	f_{SW} = 250 kHz to 1.4 MHz
Low-Side Driver, DL1 Pin						
Rising Time	$t_{RISING1}$		20		ns	C_{ISS} = 1.2 nF
Falling Time	$t_{FALLING1}$		3.4		ns	C_{ISS} = 1.2 nF
Sourcing Resistor	$t_{SOURCING1}$		10		Ω	
Sinking Resistor	$t_{SINKING1}$		0.95		Ω	
Error Amplifier (EA), COMP1 Pin						
EA Transconductance	g_{m1}	310	470	620	µS	
Soft Start						
Soft Start Time	t_{SS1}		2.0		ms	SS12 connected to VREG
Programmable Soft Start Range		2.0		8.0	ms	
Hiccup Time	$t_{HICCUP1}$		7 × t_{SS1}		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS1}		250		Ω	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL 2 SYNC BUCK REGULATOR						
FB2 Pin						
Fixed Output Options	V_{OUT2}	3.3		5.0	V	Fuse trim or I²C interface (3-bit value)
Adjustable Feedback Voltage	V_{FB2}		0.800		V	
Feedback Voltage Accuracy	$V_{FB2(DEFAULT)}$	−0.55		+0.55	%	T_J = 25°C
		−1.25		+1.0	%	0°C ≤ T_J ≤ 85°C
		−1.5		+1.5	%	−40°C ≤ T_J ≤ +125°C
Feedback Bias Current	I_{FB2}			0.1	µA	Adjustable voltage
SW2 Pin						
High-Side Power FET On Resistance	$R_{DSON(2H)}$		110		mΩ	Pin-to-pin measurement
Current-Limit Threshold	$I_{TH(ILIM2)}$	3.50	4.4	5.28	A	R_{ILIM2} = floating
		1.91	2.63	3.08	A	R_{ILIM2} = 47 kΩ
		4.95	6.44	7.48	A	R_{ILIM2} = 22 kΩ
Minimum On Time	t_{MIN_ON2}		117	155	ns	f_{SW} = 250 kHz to 1.4 MHz
Minimum Off Time	t_{MIN_OFF2}		1/9 × t_{SW}		ns	f_{SW} = 250 kHz to 1.4 MHz
Low-Side Driver, DL2 Pin						
Rising Time	$t_{RISING2}$		20		ns	C_{ISS} = 1.2 nF
Falling Time	$t_{FALLING2}$		3.4		ns	C_{ISS} = 1.2 nF
Sourcing Resistor	$t_{SOURCING2}$		10		Ω	
Sinking Resistor	$t_{SINKING2}$		0.95		Ω	
Error Amplifier (EA), COMP2 Pin						
EA Transconductance	g_{m2}	310	470	620	µS	
Soft Start						
Soft Start Time	t_{SS2}		2.0		ms	SS12 connected to VREG
Programmable Soft Start Range		2.0		8.0	ms	
Hiccup Time	$t_{HICCUP2}$		7 × t_{SS2}		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS2}		250		Ω	
CHANNEL 3 SYNC BUCK REGULATOR						
FB3 Pin						
Fixed Output Options	V_{OUT3}	1.20		1.80	V	Fuse trim or I²C interface (3-bit value)
Adjustable Feedback Voltage	V_{FB3}		0.800		V	
Feedback Voltage Accuracy	$V_{FB3(DEFAULT)}$	−0.55		+0.55	%	T_J = 25°C
		−1.25		+1.0	%	0°C ≤ T_J ≤ 85°C
		−1.5		+1.5	%	−40°C ≤ T_J ≤ +125°C
Feedback Bias Current	I_{FB3}			0.1	µA	Adjustable voltage
SW3 Pin						
High-Side Power FET On Resistance	$R_{DSON(3H)}$		225		mΩ	Pin-to-pin measurement
Low-Side Power FET On Resistance	$R_{DSON(3L)}$		150		mΩ	Pin-to-pin measurement
Current-Limit Threshold	$I_{TH(ILIM3)}$	1.7	2.2	2.55	A	
Minimum On Time	t_{MIN_ON3}		90	120	ns	f_{SW} = 250 kHz to 1.4 MHz
Minimum Off Time	t_{MIN_OFF3}		1/9 × t_{SW}		ns	f_{SW} = 250 kHz to 1.4 MHz
Error Amplifier (EA), COMP3 Pin						
EA Transconductance	g_{m3}	310	470	620	µS	
Soft Start						
Soft Start Time	t_{SS3}		2.0		ms	SS34 connected to VREG
Programmable Soft Start Range		2.0		8.0	ms	
Hiccup Time	$t_{HICCUP3}$		7 × t_{SS3}		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS3}		250		Ω	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL 4 SYNC BUCK REGULATOR						
FB4 Pin						
Fixed Output Options	V_{OUT4}	2.5		5.5	V	Fuse trim or I^2C interface (5-bit value)
Adjustable Feedback Voltage	V_{FB4}		0.800		V	
Feedback Voltage Accuracy	$V_{FB4(DEFAULT)}$	−0.55		+0.55	%	T_J = 25°C
		−1.25		+1.0	%	0°C ≤ T_J ≤ 85°C
		−1.5		+1.5	%	−40°C ≤ T_J ≤ +125°C
Feedback Bias Current	I_{FB4}			0.1	µA	
SW4 Pin						
High-Side Power FET On Resistance	$R_{DSON(4H)}$		225		mΩ	Pin-to-pin measurement
Low-Side Power FET On Resistance	$R_{DSON(4L)}$		150		mΩ	Pin-to-pin measurement
Current-Limit Threshold	$I_{TH(ILIM4)}$	1.7	2.2	2.55	A	
Minimum On Time	t_{MIN_ON4}		90	120	ns	f_{SW} = 250 kHz to 1.4 MHz
Minimum Off Time	t_{MIN_OFF4}		1/9 × t_{SW}		ns	f_{SW} = 250 kHz to 1.4 MHz
Error Amplifier (EA), COMP4 Pin						
EA Transconductance	g_{m4}	310	470	620	µS	
Soft Start						
Soft Start Time	t_{SS4}		2.0		ms	SS34 connected to VREG
Programmable Soft Start Range		2.0		8.0	ms	
Hiccup Time	$t_{HICCUP4}$		7 × t_{SS4}		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS4}		250		Ω	

LDO REGULATOR SPECIFICATIONS

V_{IN5} = (VOUT5 + 0.5 V) or 1.7 V (whichever is greater) to 5.5 V; C_{IN} = C_{OUT} = 1 µF; T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT SUPPLY VOLTAGE RANGE	1.7		5.5	V	PVIN5 pin
OPERATIONAL SUPPLY CURRENT					
Bias Current for LDO Regulator		30	130	µA	I_{OUT5} = 200 µA
		60	170	µA	I_{OUT5} = 10 mA
		145	320	µA	I_{OUT5} = 200 mA
VOLTAGE FEEDBACK (FB5 PIN)					
Adjustable Feedback Voltage		0.500		V	
Feedback Voltage Accuracy	−1.0		+1.0	%	T_J = 25°C
	−1.6		+1.6	%	0°C ≤ T_J ≤ 85°C
	−2.0		+2.0	%	−40°C ≤ T_J ≤ +125°C
DROPOUT VOLTAGE					I_{OUT5} = 200 mA
		80		mV	VOUT5 = 3.3 V
		100		mV	VOUT5 = 2.5 V
		180		mV	VOUT5 = 1.5 V
CURRENT-LIMIT THRESHOLD	250	510		mA	Specified from the output voltage drop to 90% of the specified typical value
OUTPUT NOISE		92		µV rms	10 Hz to 100 kHz, V_{PVIN5} = 5 V, VOUT5 = 1.8 V
POWER SUPPLY REJECTION RATIO					V_{PVIN5} = 5 V, VOUT5 = 1.8 V, I_{OUT5} = 1 mA
		77		dB	10 kHz
		66		dB	100 kHz

I²C INTERFACE TIMING SPECIFICATIONS

T_A = 25°C, V_{VDD} = 3.3 V, V_{VDDIO} = 3.3 V, unless otherwise noted.

Table 5.

Parameter	Min	Typ	Max	Unit	Description
f_{SCL}			400	kHz	SCL clock frequency
t_{HIGH}	0.6			µs	SCL high time
t_{LOW}	1.3			µs	SCL low time
$t_{SU,DAT}$	100			ns	Data setup time
$t_{HD,DAT}$	0		0.9	µs	Data hold time[1]
$t_{SU,STA}$	0.6			µs	Setup time for a repeated start condition
$t_{HD,STA}$	0.6			µs	Hold time for a start or repeated start condition
t_{BUF}	1.3			µs	Bus free time between a stop condition and a start condition
$t_{SU,STO}$	0.6			µs	Setup time for a stop condition
t_R	20 + 0.1C_B[2]		300	ns	Rise time of SCL and SDA
t_F	20 + 0.1C_B[2]		300	ns	Fall time of SCL and SDA
t_{SP}	0		50	ns	Pulse width of suppressed spike
C_B[2]			400	pF	Capacitive load for each bus line

[1] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} minimum of the SCL signal) to bridge the undefined region of the SCL falling edge.
[2] C_B is the total capacitance of one bus line in picofarads (pF).

Timing Diagram

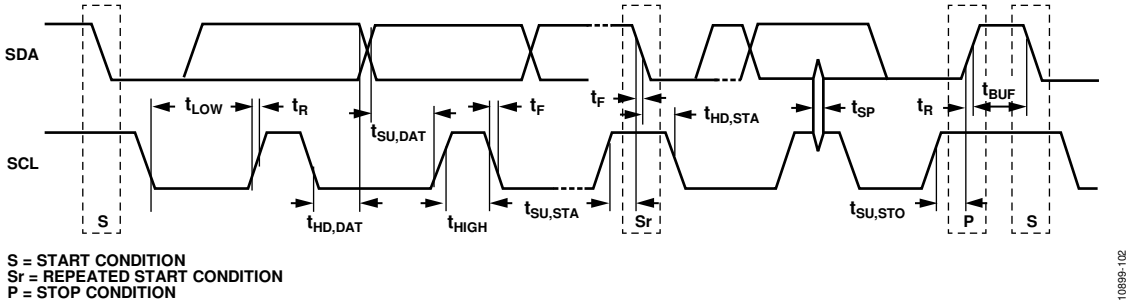

Figure 3. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
PVIN1 to PGND	−0.3 V to +18 V
PVIN2 to PGND	−0.3 V to +18 V
PVIN3 to PGND3	−0.3 V to +18 V
PVIN4 to PGND4	−0.3 V to +18 V
PVIN5 to GND	−0.3 V to +6.5 V
SW1 to PGND	−0.3 V to +18 V
SW2 to PGND	−0.3 V to +18 V
SW3 to PGND3	−0.3 V to +18 V
SW4 to PGND4	−0.3 V to +18 V
PGND to GND	−0.3 V to +0.3 V
PGND3 to GND	−0.3 V to +0.3 V
PGND4 to GND	−0.3 V to +0.3 V
BST1 to SW1	−0.3 V to +6.5 V
BST2 to SW2	−0.3 V to +6.5 V
BST3 to SW3	−0.3 V to +6.5 V
BST4 to SW4	−0.3 V to +6.5 V
DL1 to PGND	−0.3 V to +6.5 V
DL2 to PGND	−0.3 V to +6.5 V
SS12, SS34 to GND	−0.3 V to +6.5 V
EN1, EN2, EN3, EN4, EN5 to GND	−0.3 V to +6.5 V
VREG to GND	−0.3 V to +6.5 V
SYNC/MODE to GND	−0.3 V to +6.5 V
VOUT5, FB5 to GND	−0.3 V to +6.5 V
RT to GND	−0.3 V to +3.6 V
$\overline{\text{INT}}$, PWRGD to GND	−0.3 V to +6.5 V
FB1, FB2, FB3, FB4 to GND[1]	−0.3 V to +3.6 V
FB2 to GND[2]	−0.3 V to +6.5 V
FB4 to GND[2]	−0.3 V to +7 V
COMP1, COMP2, COMP3, COMP4 to GND	−0.3 V to +3.6 V
VDD, VDDIO to GND	−0.3 V to +3.6 V
SCL, SDA	−0.3 V to VDDIO + 0.3 V
Storage Temperate Range	−65°C to +150°C
Operational Junction Temperature Range	−40°C to +125°C

[1] This rating applies to the adjustable output voltage models of the ADP5050.
[2] This rating applies to the fixed output voltage models of the ADP5050.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
48-Lead LFCSP	27.87	2.99	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

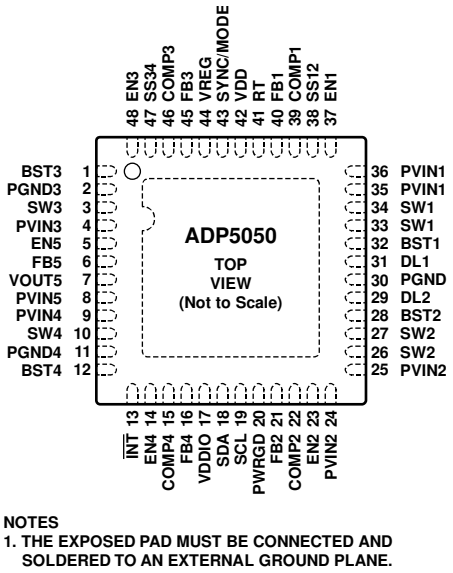

Figure 4. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BST3	High-Side FET Driver Power Supply for Channel 3.
2	PGND3	Power Ground for Channel 3.
3	SW3	Switching Node Output for Channel 3.
4	PVIN3	Power Input for Channel 3. Connect a bypass capacitor between this pin and ground.
5	EN5	Enable Input for Channel 5. An external resistor divider can be used to set the turn-on threshold.
6	FB5	Feedback Sensing Input for Channel 5.
7	VOUT5	Power Output for Channel 5.
8	PVIN5	Power Input for Channel 5. Connect a bypass capacitor between this pin and ground.
9	PVIN4	Power Input for Channel 4. Connect a bypass capacitor between this pin and ground.
10	SW4	Switching Node Output for Channel 4.
11	PGND4	Power Ground for Channel 4.
12	BST4	High-Side FET Driver Power Supply for Channel 4.
13	$\overline{\text{INT}}$	Interrupt Output on Fault Condition. Open-drain output port.
14	EN4	Enable Input for Channel 4. An external resistor divider can be used to set the turn-on threshold.
15	COMP4	Error Amplifier Output for Channel 4. Connect an RC network from this pin to ground.
16	FB4	Feedback Sensing Input for Channel 4.
17	VDDIO	Power Supply for the I^2C Interface.
18	SDA	Data Input/Output for the I^2C Interface. Open-drain I/O port.
19	SCL	Clock Input for the I^2C Interface.
20	PWRGD	Power-Good Signal Output. This open-drain output is the power-good signal for the selected channels. This pin can be programmed by the factory to set the I^2C address of the part; the I^2C address setting function replaces the power-good function on this pin. For more information, see the I^2C Addresses section.
21	FB2	Feedback Sensing Input for Channel 2.
22	COMP2	Error Amplifier Output for Channel 2. Connect an RC network from this pin to ground.
23	EN2	Enable Input for Channel 2. An external resistor divider can be used to set the turn-on threshold.
24, 25	PVIN2	Power Input for Channel 2. Connect a bypass capacitor between this pin and ground.
26, 27	SW2	Switching Node Output for Channel 2.
28	BST2	High-Side FET Driver Power Supply for Channel 2.
29	DL2	Low-Side FET Gate Driver for Channel 2. Connect a resistor from this pin to ground to program the current-limit threshold for Channel 2.

Pin No.	Mnemonic	Description
30	PGND	Power Ground for Channel 1 and Channel 2.
31	DL1	Low-Side FET Gate Driver for Channel 1. Connect a resistor from this pin to ground to program the current-limit threshold for Channel 1.
32	BST1	High-Side FET Driver Power Supply for Channel 1.
33, 34	SW1	Switching Node Output for Channel 1.
35, 36	PVIN1	Power Input for the Internal 5.1 V VREG Linear Regulator and the Channel 1 Buck Regulator. Connect a bypass capacitor between this pin and ground.
37	EN1	Enable Input for Channel 1. An external resistor divider can be used to set the turn-on threshold.
38	SS12	Connect a resistor divider from this pin to VREG and ground to configure the soft start time for Channel 1 and Channel 2 (see the Soft Start section). This pin is also used to configure parallel operation of Channel 1 and Channel 2 (see the Parallel Operation section).
39	COMP1	Error Amplifier Output for Channel 1. Connect an RC network from this pin to ground.
40	FB1	Feedback Sensing Input for Channel 1.
41	RT	Connect a resistor from RT to ground to program the switching frequency from 250 kHz to 1.4 MHz. For more information, see the Oscillator section.
42	VDD	Output of the Internal 3.3 V Linear Regulator. Connect a 1 µF ceramic capacitor between this pin and ground.
43	SYNC/MODE	Synchronization Input/Output (SYNC). To synchronize the switching frequency of the part to an external clock, connect this pin to an external clock with a frequency from 250 kHz to 1.4 MHz. This pin can also be configured as a synchronization output using the I^2C interface or by factory fuse. Forced PWM or Automatic PWM/PSM Selection Pin (MODE). When this pin is logic high, each channel operates in forced PWM or automatic PWM/PSM mode, as specified by the PSMx_ON bits in Register 6. When this pin is logic low, all channels operate in automatic PWM/PSM mode, and the PSMx_ON settings in Register 6 are ignored.
44	VREG	Output of the Internal 5.1 V Linear Regulator. Connect a 1 µF ceramic capacitor between this pin and ground.
45	FB3	Feedback Sensing Input for Channel 3.
46	COMP3	Error Amplifier Output for Channel 3. Connect an RC network from this pin to ground.
47	SS34	Connect a resistor divider from this pin to VREG and ground to configure the soft start time for Channel 3 and Channel 4 (see the Soft Start section).
48	EN3	Enable Input for Channel 3. An external resistor divider can be used to set the turn-on threshold.
	EPAD	Exposed Pad (Analog Ground). The exposed pad must be connected and soldered to an external ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

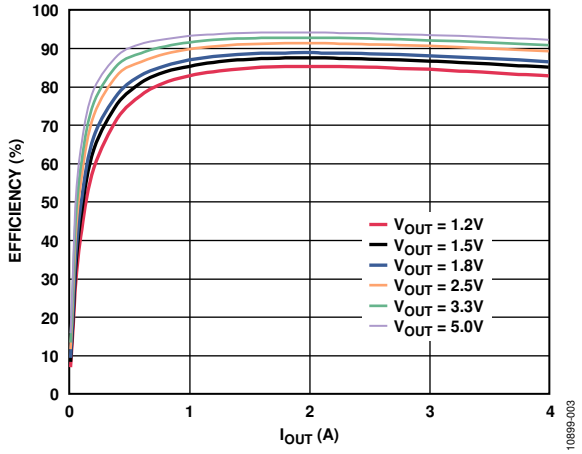

Figure 5. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM Mode

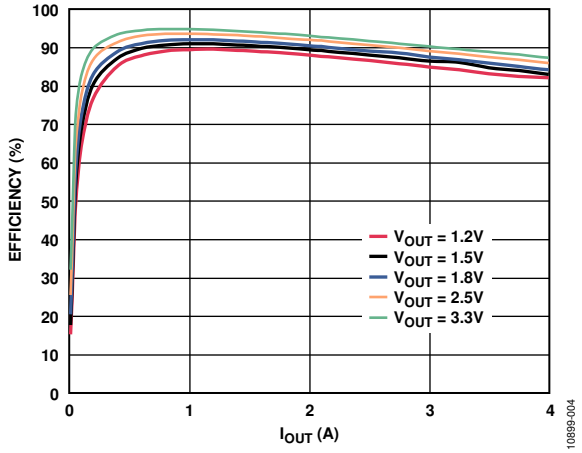

Figure 6. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 5.0 V, f_{SW} = 600 kHz, FPWM Mode

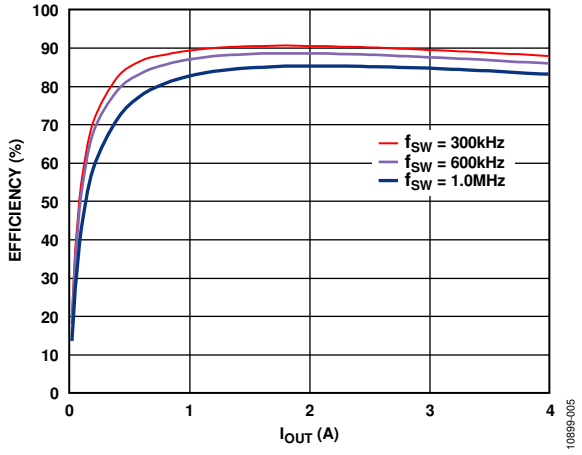

Figure 7. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 12 V, V_{OUT} = 1.8 V, FPWM Mode

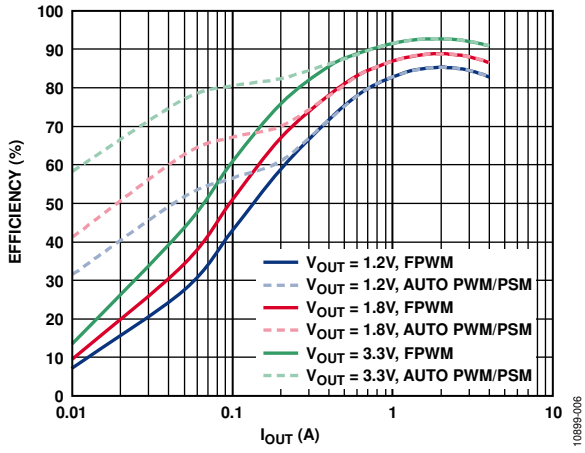

Figure 8. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM and Automatic PWM/PSM Modes

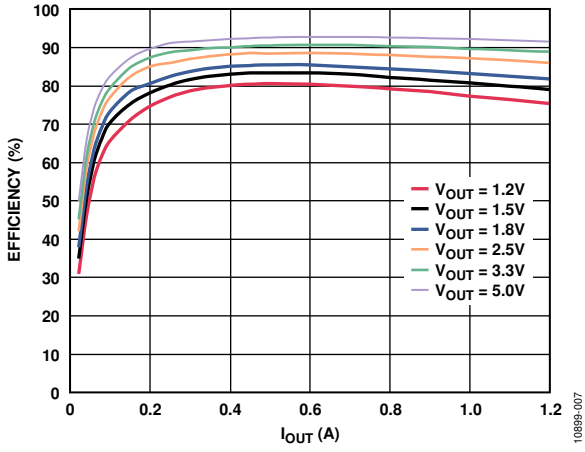

Figure 9. Channel 3/Channel 4 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM Mode

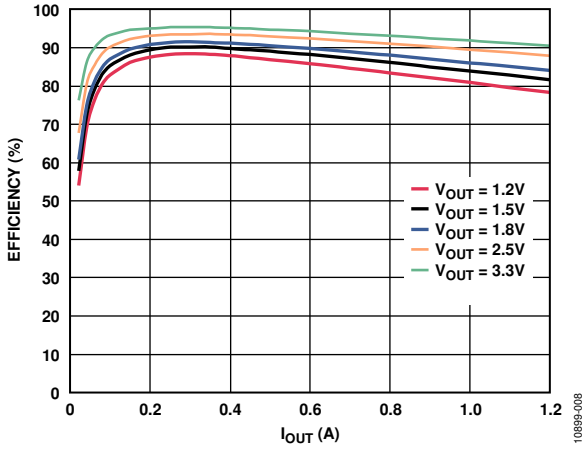

Figure 10. Channel 3/Channel 4 Efficiency Curve, V_{IN} = 5.0 V, f_{SW} = 600 kHz, FPWM Mode

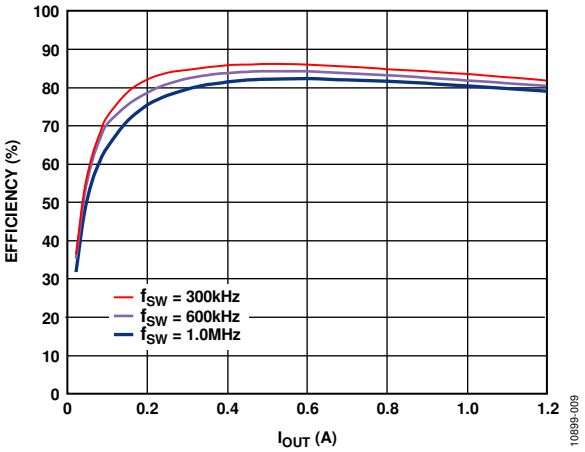

Figure 11. Channel 3/Channel 4 Efficiency Curve, V_{IN} = 12 V, V_{OUT} = 1.8 V, FPWM Mode

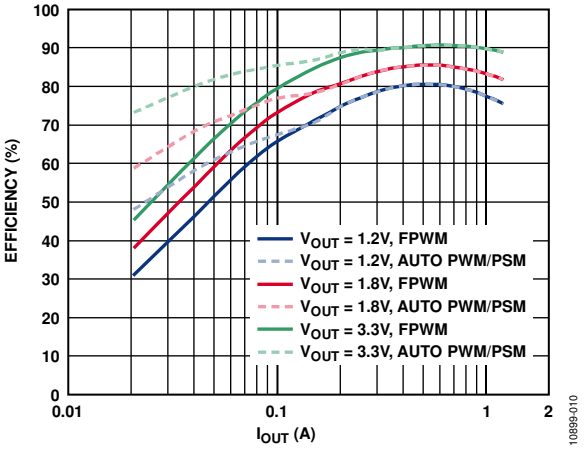

Figure 12. Channel 3/Channel 4 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM and and Automatic PWM/PSM Modes

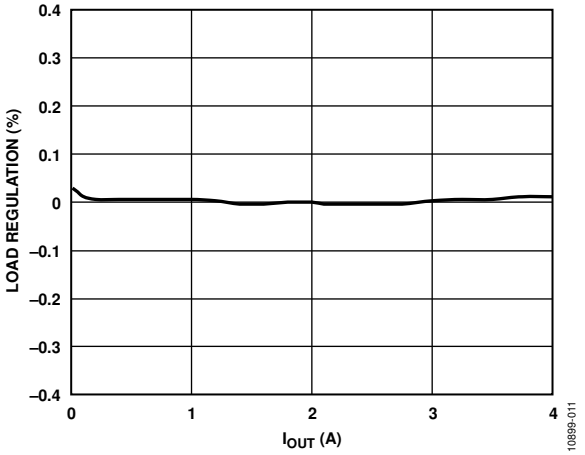

Figure 13. Channel 1 Load Regulation, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 600 kHz, FPWM Mode

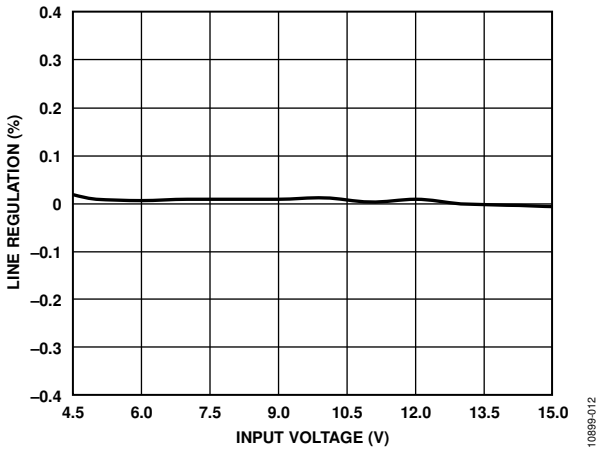

Figure 14. Channel 1 Line Regulation, V_{OUT} = 3.3 V, I_{OUT} = 4 A, f_{SW} = 600 kHz, FPWM Mode

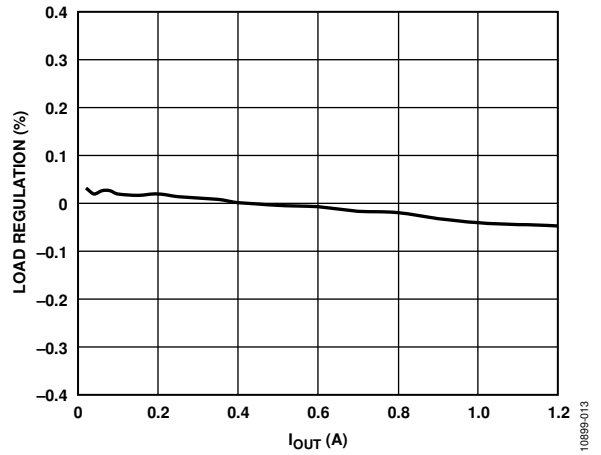

Figure 15. Channel 3 Load Regulation, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 600 kHz, FPWM Mode

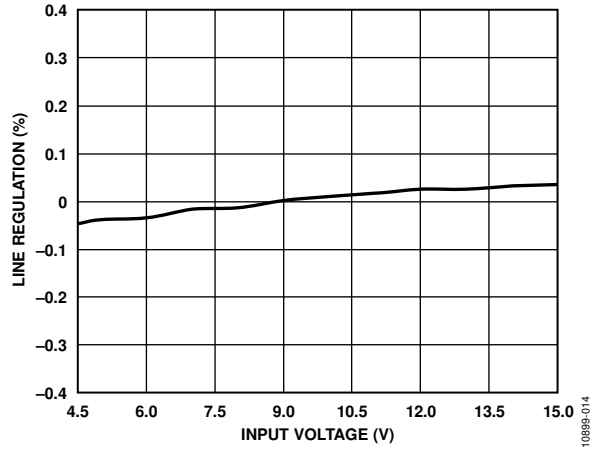

Figure 16. Channel 3 Line Regulation, V_{OUT} = 3.3 V, I_{OUT} = 1 A, f_{SW} = 600 kHz, FPWM Mode

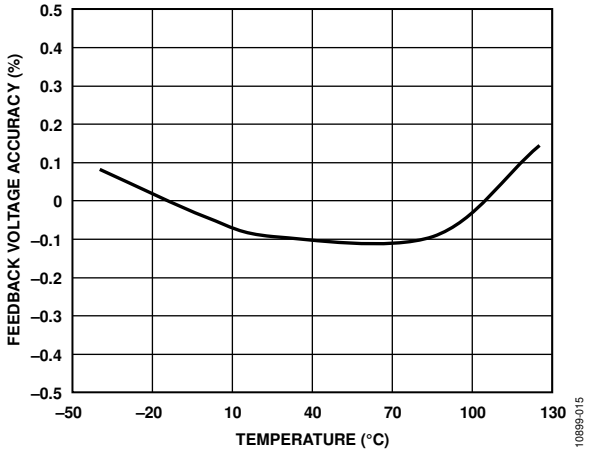

Figure 17. 0.8 V Feedback Voltage Accuracy vs. Temperature for Channel 1, Adjustable Output Model

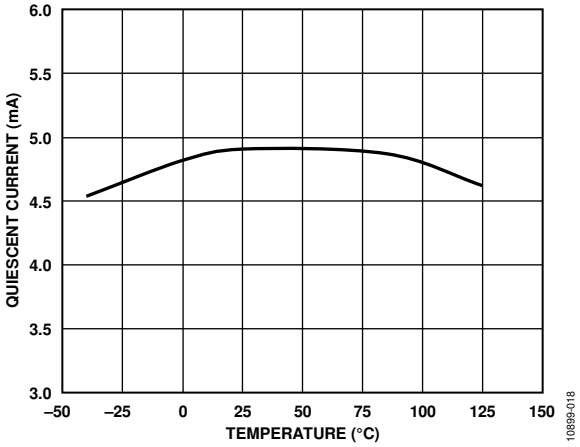

Figure 20. Quescient Current vs. Temperature (Includes PVIN1, PVIN2, PVIN3, and PVIN4)

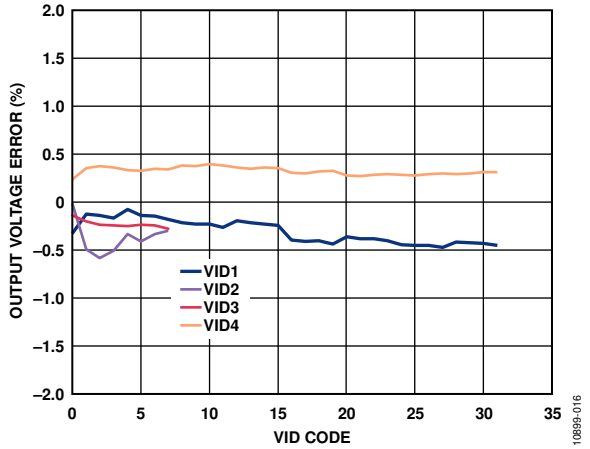

Figure 18. Output Voltage Error vs. VID Code, Adjustable Output Model

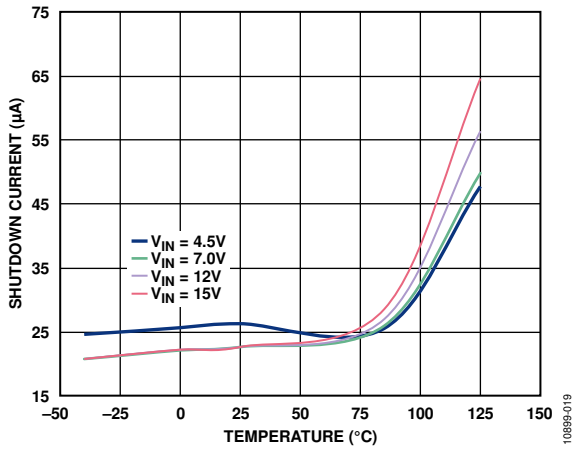

Figure 21. Shutdown Current vs. Temperature (EN1, EN2, EN3, EN4, and EN5 Low)

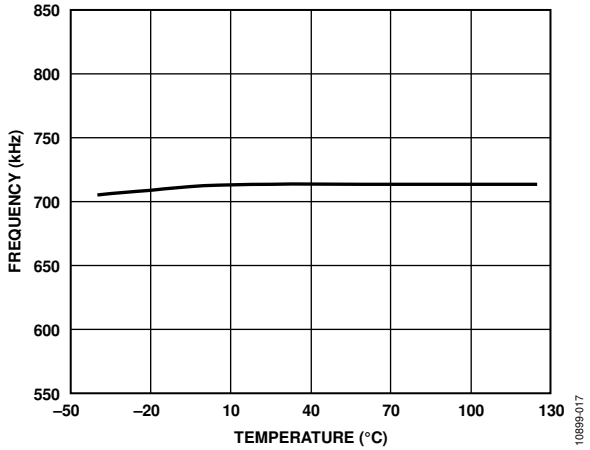

Figure 19. Frequency vs. Temperature, V_{IN} = 12 V

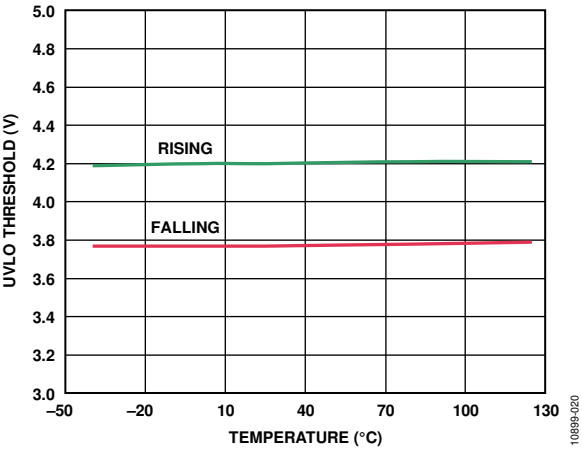

Figure 22. UVLO Threshold vs. Temperature

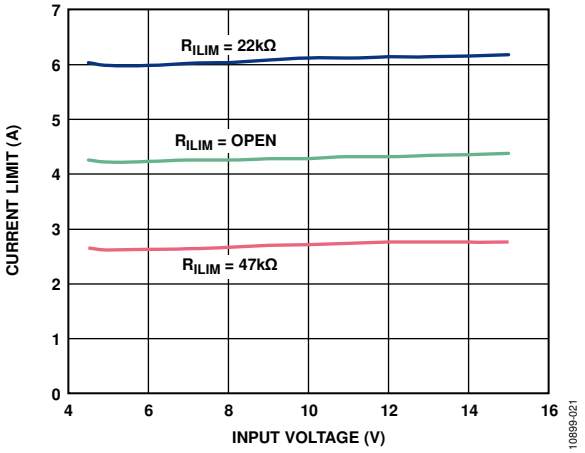

Figure 23. Channel 1/Channel 2 Current Limit vs. Input Voltage

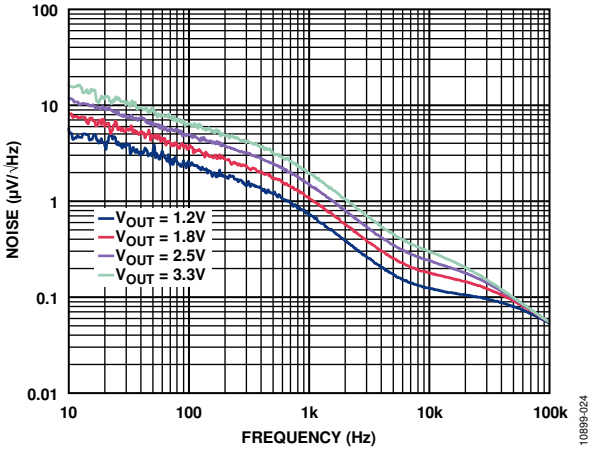

Figure 26. Channel 5 (LDO Regulator) Output Noise Spectrum, V_{IN} = 5 V, C_{OUT} = 1 μF, I_{OUT} = 10 mA

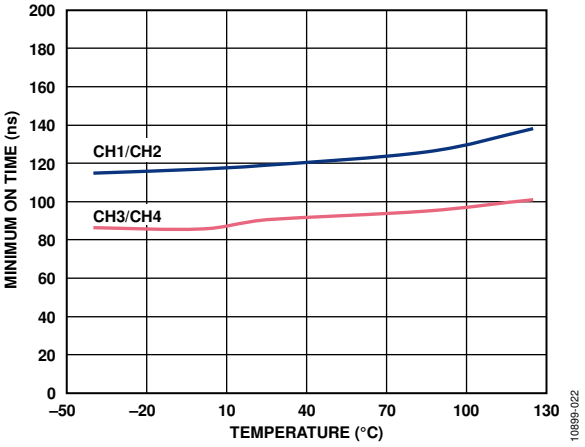

Figure 24. Minimum On Time vs. Temperature

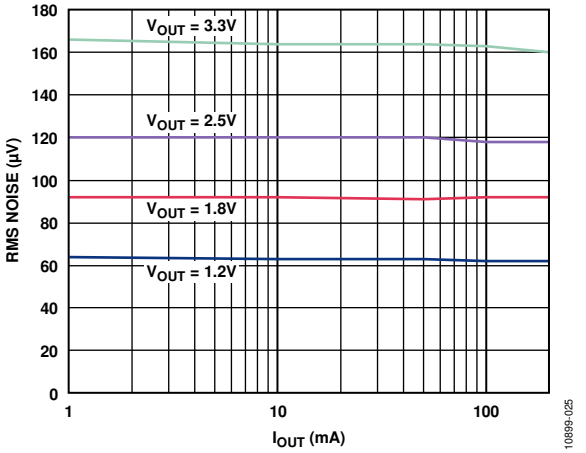

Figure 27. Channel 5 (LDO Regulator) Output Noise vs. Output Load, V_{IN} = 5 V, C_{OUT} = 1 μF

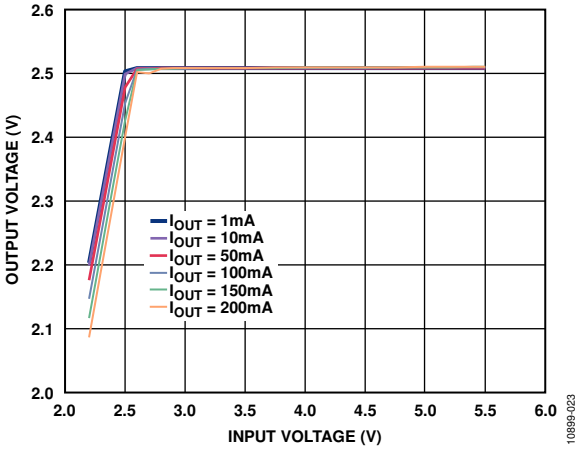

Figure 25. Channel 5 (LDO Regulator) Line Regulation over Output Load

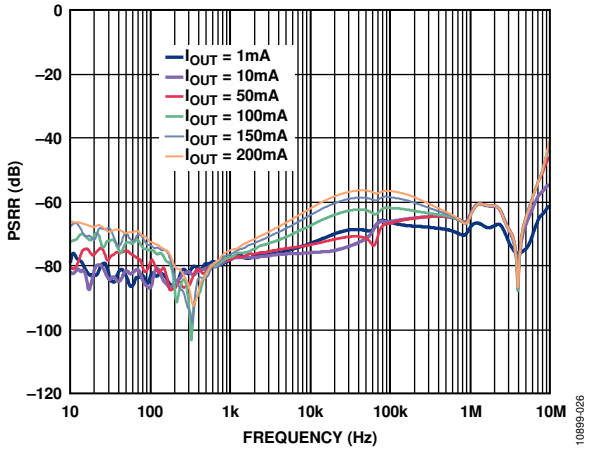

Figure 28. Channel 5 (LDO Regulator) PSRR over Output Load, V_{IN} = 5 V, V_{OUT} = 3.3 V, C_{OUT} = 1 μF

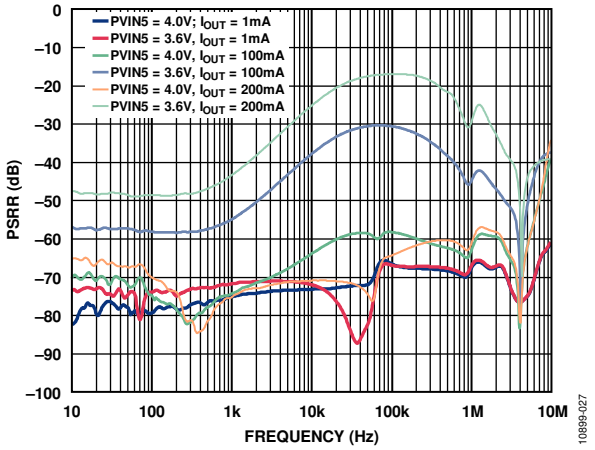

Figure 29. Channel 5 (LDO Regulator) PSRR over Various Loads and Dropout Voltages, V_{OUT} = 3.3 V, C_{OUT} = 1 µF

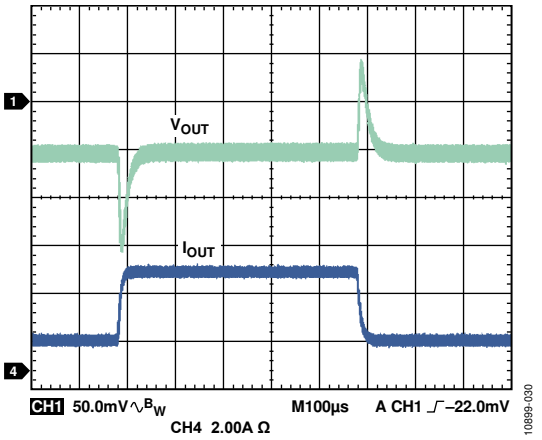

Figure 32. Channel 1/Channel 2 Load Transient, 1 A to 4 A, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 600 kHz, L = 2.2 µH, C_{OUT} = 47 µF × 2

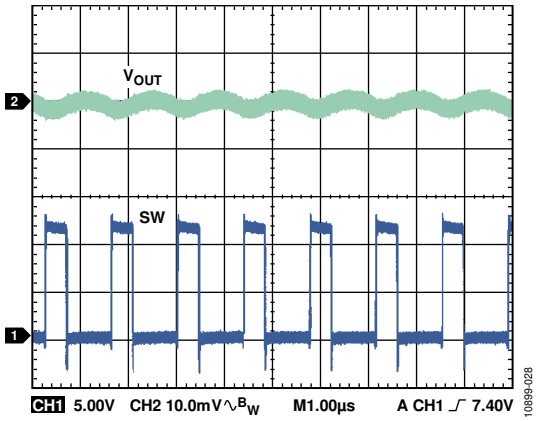

Figure 30. Steady State Waveform at Heavy Load, V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 3 A, f_{SW} = 600 kHz, L = 4.7 µH, C_{OUT} = 47 µF × 2, FPWM Mode

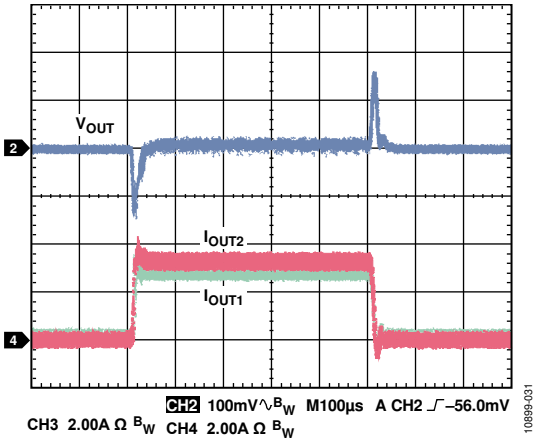

Figure 33. Load Transient, Channel 1/Channel 2 Parallel Output, 0 A to 6 A, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 600 kHz, L = 4.7 µH, C_{OUT} = 47 µF × 4

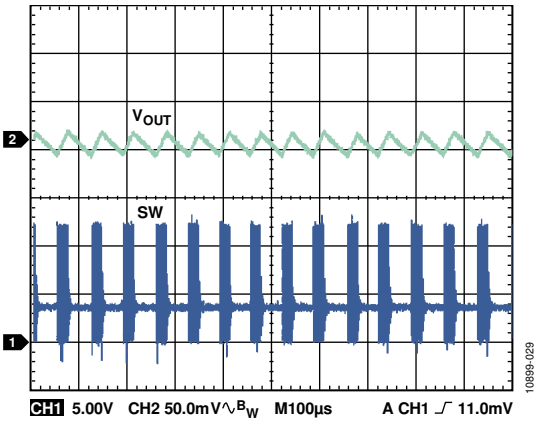

Figure 31. Steady State Waveform at Light Load, V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 30 mA, f_{SW} = 600 kHz, L = 4.7 µH, C_{OUT} = 47 µF × 2, Automatic PWM/PSM Mode

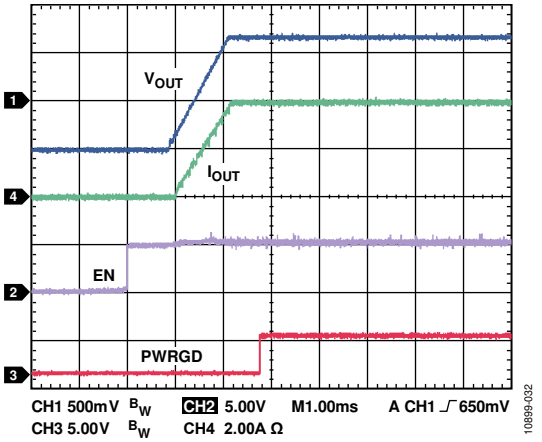

Figure 34. Channel 1/Channel 2 Soft Start with 4 A Resistance Load, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2

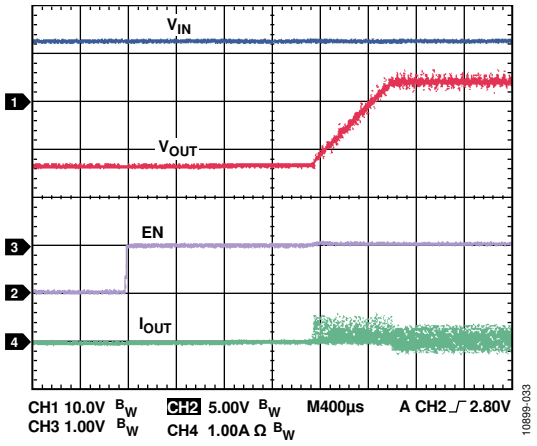

Figure 35. Startup with Precharged Output, V_{IN} = 12 V, V_{OUT} = 3.3 V

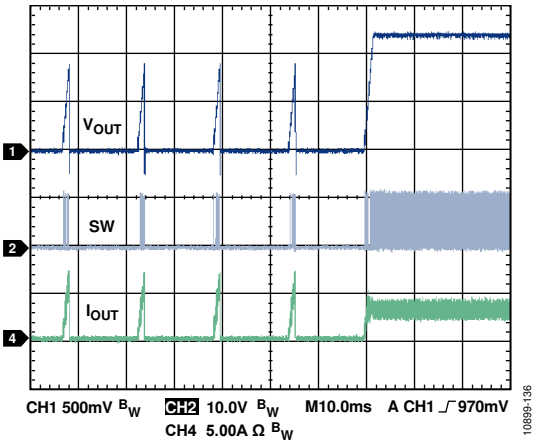

Figure 38. Short-Circuit Protection Recovery, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2

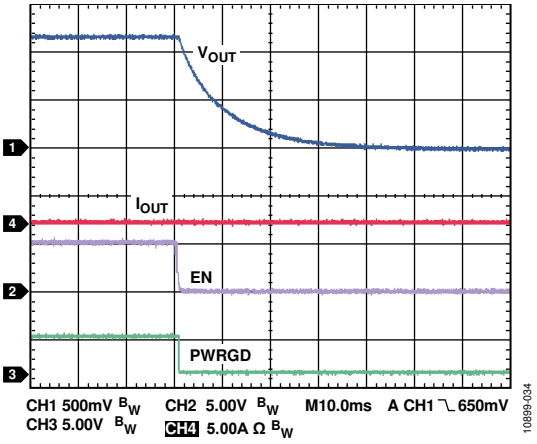

Figure 36. Channel 1/Channel 2 Shutdown with Active Output Discharge, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2

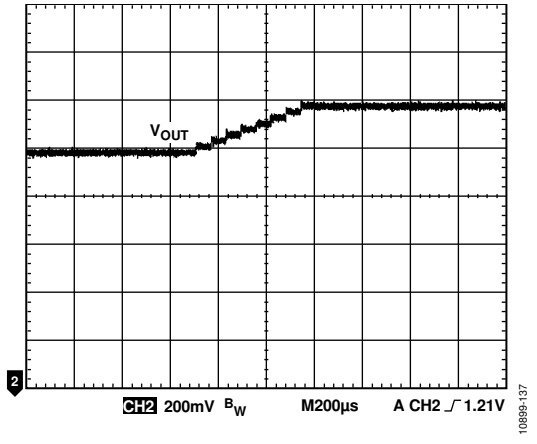

Figure 39. Channel 1 Dynamic Voltage Scaling (DVS) from 1.1 V to 1.3 V, 62.5 µs Interval, V_{IN} = 12 V, I_{OUT} = 4 A, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2

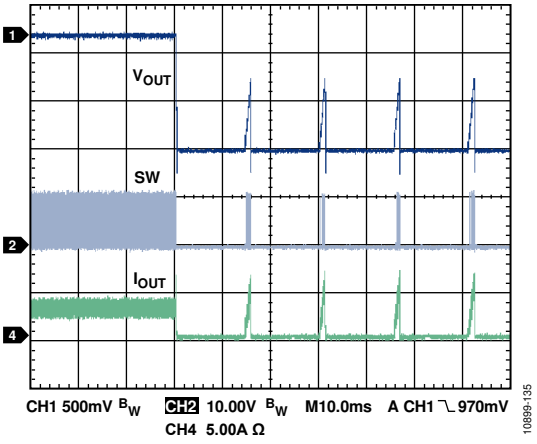

Figure 37. Short-Circuit Protection Entry, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2

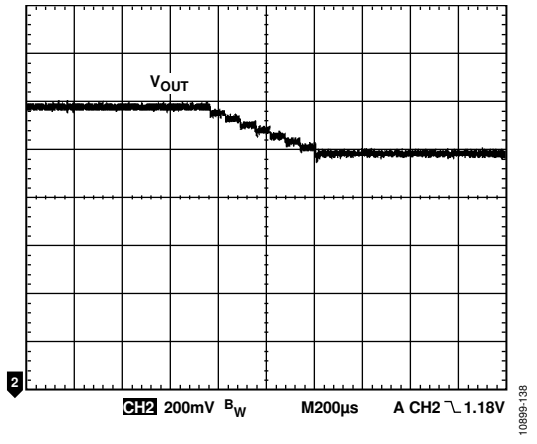

Figure 40. Channel 1 Dynamic Voltage Scaling (DVS) from 1.3 V to 1.1 V, 62.5 µs Interval, V_{IN} = 12 V, I_{OUT} = 4 A, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2

THEORY OF OPERATION

The ADP5050 is a micropower management unit that combines four high performance buck regulators with a 200 mA low dropout (LDO) regulator in a 48-lead LFCSP package to meet demanding performance and board space requirements. The device enables direct connection to high input voltages up to 15 V with no pre-regulators to make applications simpler and more efficient.

BUCK REGULATOR OPERATIONAL MODES

PWM Mode

In pulse-width modulation (PWM) mode, the buck regulators in the ADP5050 operate at a fixed frequency; this frequency is set by an internal oscillator that is programmed by the RT pin. At the start of each oscillator cycle, the high-side MOSFET turns on and sends a positive voltage across the inductor. The inductor current increases until the current-sense signal exceeds the peak inductor current threshold that turns off the high-side MOSFET; this threshold is set by the error amplifier output.

During the high-side MOSFET off time, the inductor current decreases through the low-side MOSFET until the next oscillator clock pulse starts a new cycle. The buck regulators in the ADP5050 regulate the output voltage by adjusting the peak inductor current threshold.

PSM Mode

To achieve higher efficiency, the buck regulators in the ADP5050 smoothly transition to variable frequency power save mode (PSM) operation when the output load falls below the PSM current threshold. When the output voltage falls below regulation, the buck regulator enters PWM mode for a few oscillator cycles until the voltage increases to within regulation. During the idle time between bursts, the MOSFET turns off, and the output capacitor supplies all the output current.

The PSM comparator monitors the internal compensation node, which represents the peak inductor current information. The average PSM current threshold depends on the input voltage (V_{IN}), the output voltage (V_{OUT}), the inductor, and the output capacitor. Because the output voltage occasionally falls below regulation and then recovers, the output voltage ripple in PSM operation is larger than the ripple in the forced PWM mode of operation under light load conditions.

Forced PWM and Automatic PWM/PSM Modes

The buck regulators can be configured to always operate in PWM mode using the SYNC/MODE pin and the I²C interface. In forced PWM (FPWM) mode, the regulator continues to operate at a fixed frequency even when the output current is below the PWM/PSM threshold. In PWM mode, efficiency is lower compared to PSM mode under light load conditions. The low-side MOSFET remains on when the inductor current falls to less than 0 A, causing the ADP5050 to enter continuous conduction mode (CCM).

The buck regulators can be configured to operate in automatic PWM/PSM mode using the SYNC/MODE pin and the I²C interface. In automatic PWM/PSM mode, the buck regulators operate in either PWM mode or PSM mode, depending on the output current. When the average output current falls below the PWM/PSM threshold, the buck regulator enters PSM mode operation; in PSM mode, the regulator operates with a reduced switching frequency to maintain high efficiency. The low-side MOSFET turns off when the output current reaches 0 A, causing the regulator to operate in discontinuous mode (DCM).

The user can alternate between forced PWM (FPWM) mode and automatic PWM/PSM mode during operation. The flexible configuration capability during operation of the device enables efficient power management.

When a logic high level is applied to the SYNC/MODE pin (or when SYNC/MODE is configured as a clock input or output), the operational mode of each channel is set by the PSMx_ON bit in Register 6. A value of 0 for the PSMx_ON bit configures the channel for forced PWM mode; a value of 1 configures the channel for automatic PWM/PSM mode.

When a logic low level is applied to the SYNC/MODE pin, the operational mode of all four buck regulators is automatic PWM/PSM mode, and the settings of the PSMx_ON bits in Register 6 are ignored.

Table 9 describes the function of the SYNC/MODE pin in setting the operational mode of the device.

Table 9. Configuring the Mode of Operation Using the SYNC/MODE Pin

SYNC/MODE Pin	Mode of Operation for Each Channel
High	Specified by the PSMx_ON bit setting in Register 6 (0 = forced PWM mode; 1 = automatic PWM/PSM mode)
Clock Input/Output	Specified by the PSMx_ON bit setting in Register 6 (0 = forced PWM mode; 1 = automatic PWM/PSM mode)
Low	Automatic PWM/PSM mode (PSMx_ON bit settings in Register 6 are ignored)

For example, with the SYNC/MODE pin high, write 1 to the PSM4_ON bit in Register 6 to configure automatic PWM/PSM mode operation for Channel 4, and write 0 to the PSM1_ON, PSM2_ON, and PSM3_ON bits to configure forced PWM mode for Channel 1, Channel 2, and Channel 3.

ADJUSTABLE AND FIXED OUTPUT VOLTAGES

The ADP5050 provides adjustable and fixed output voltage settings via the I²C interface or factory fuse. For the adjustable output settings, use an external resistor divider to set the desired output voltage via the feedback reference voltage (0.8 V for Channel 1 to Channel 4, and 0.5 V for Channel 5).

For the fixed output settings, the feedback resistor divider is built into the ADP5050, and the feedback pin (FBx) must be tied directly to the output. Each buck regulator channel can be programmed for a specific output voltage range using the VIDx bits in Register 2 to Register 4. Table 10 lists the fixed output voltage ranges configured by the VIDx bits.

Table 10. Fixed Output Voltage Ranges Set by the VIDx Bits

Channel	Fixed Output Voltage Range Set by the VIDx Bits
Channel 1	0.85 V to 1.6 V in 25 mV steps
Channel 2	3.3 V to 5.0 V in 300 mV or 200 mV steps
Channel 3	1.2 V to 1.8 V in 100 mV steps
Channel 4	2.5 V to 5.5 V in 100 mV steps

The output range can also be programmed by factory fuse. If a different output voltage range is required, contact your local Analog Devices, Inc., sales or distribution representative.

DYNAMIC VOLTAGE SCALING (DVS)

The ADP5050 provides a dynamic voltage scaling (DVS) function for Channel 1 and Channel 4; these outputs can be programmed in real time via the I²C interface (Register 5, DVS_CFG). The DVS_CFG register is used to enable DVS and to set the step interval during the transition (see Table 29).

It is recommended that the user enable the DVS function before setting the output voltage for Channel 1 or Channel 4. (The output voltage for Channel 1 is set using the VID1 bits in Register 2; the output voltage for Channel 4 is set using the VID4 bits in Register 4.) If DVS is enabled after the VID value is set, the output voltage changes rapidly to the next target voltage, which can result in problems such as a PWRGD failure or OVP and OCP events. Figure 41 shows the dynamic voltage scaling function.

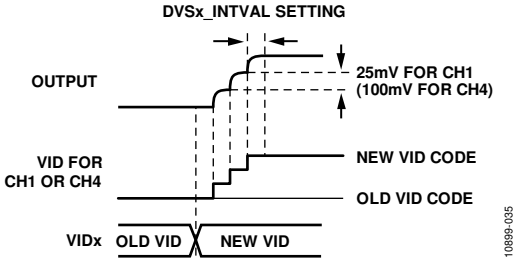

Figure 41. Dynamic Voltage Scaling

During the DVS transition period, the regulator is forced into PWM mode operation, and OVP latch-off, SCP latch-off, and hiccup protection are masked.

INTERNAL REGULATORS (VREG AND VDD)

The internal VREG regulator in the ADP5050 provides a stable 5.1 V power supply for the bias voltage of the MOSFET drivers. The internal VDD regulator in the ADP5050 provides a stable 3.3 V power supply for internal control circuits. Connect a 1.0 µF ceramic capacitor between VREG and ground, and connect another 1.0 µF ceramic capacitor between VDD and ground. The internal VREG and VDD regulators are active as long as PVIN1 is available.

The internal VREG regulator can provide a total load of 95 mA including the MOSFET driving current, and it can be used as an always alive 5.1 V power supply for a small system current demand. The current-limit circuit is included in the VREG regulator to protect the circuit when the part is heavily loaded.

The VDD regulator is for internal circuit use and is not recommended for other purposes.

SEPARATE SUPPLY APPLICATIONS

The ADP5050 supports separate input voltages for the four buck regulators. This means that the input voltages for the four buck regulators can be connected to different supply voltages.

The PVIN1 voltage provides the power supply for the internal regulators and the control circuitry. Therefore, if the user plans to use separate supply voltages for the buck regulators, the PVIN1 voltage must be above the UVLO threshold before the other channels begin to operate.

Precision enabling can be used to monitor the PVIN1 voltage and to delay the startup of the outputs to ensure that PVIN1 is high enough to support the outputs in regulation. For more information, see the Precision Enabling section.

The ADP5050 supports cascading supply operation for the four buck regulators. As shown in Figure 42, PVIN2, PVIN3, and PVIN4 are powered from the Channel 1 output. In this configuration, the Channel 1 output voltage must be higher than the UVLO threshold for PVIN2, PVIN3, and PVIN4.

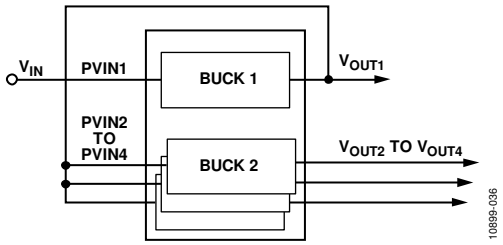

Figure 42. Cascading Supply Application

LOW-SIDE DEVICE SELECTION

The buck regulators in Channel 1 and Channel 2 integrate 4 A high-side power MOSFETs and low-side MOSFET drivers. The N-channel MOSFETs selected for use with the ADP5050 must be able to work with the synchronized buck regulators. In general, a low R_{DSON} N-channel MOSFET can be used to achieve higher efficiency; dual MOSFETs in one package (for both Channel 1 and Channel 2) are recommended to save space on the PCB. For more information, see the Low-Side Power Device Selection section.

BOOTSTRAP CIRCUITRY

Each buck regulator in the ADP5050 has an integrated bootstrap regulator. The bootstrap regulator requires a 0.1 µF ceramic capacitor (X5R or X7R) between the BSTx and SWx pins to provide the gate drive voltage for the high-side MOSFET.

ACTIVE OUTPUT DISCHARGE SWITCH

Each buck regulator in the ADP5050 integrates a discharge switch from the switching node to ground. This switch is turned on when its associated regulator is disabled, which helps to discharge the output capacitor quickly. The typical value of the discharge switch is 250 Ω for Channel 1 to Channel 4.

The discharge switch function can be enabled or disabled for each channel by factory fuse or by using the I²C interface (Register 6, OPT_CFG).

PRECISION ENABLING

The ADP5050 has an enable control pin for each regulator, including the LDO regulator. The enable control pin (ENx) features a precision enable circuit with a 0.8 V reference voltage. When the voltage at the ENx pin is greater than 0.8 V, the regulator is enabled. When the voltage at the ENx pin falls below 0.725 V, the regulator is disabled. An internal 1 MΩ pull-down resistor prevents errors if the ENx pin is left floating.

The precision enable threshold voltage allows easy sequencing of channels within the part, as well as sequencing between the ADP5050 and other input/output supplies. The ENx pin can also be used as a programmable UVLO input using a resistor divider (see Figure 43). For more information, see the Programming the UVLO Input section.

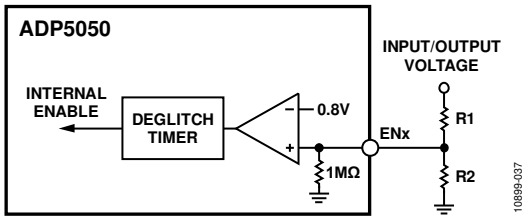

Figure 43. Precision Enable Diagram for One Channel

In addition to the ENx pins, the I²C interface (Register 1, PCTRL) can also be used to enable and disable each channel. The on/off status of a channel is controlled by the I²C enable bit for the channel (CHx_ON) and the external hardware enable pin for the channel (logical AND).

The default value of the I²C enable bit (CHx_ON = 1) specifies that the channel enable is controlled by the external hardware enable pin. Pulling the external ENx pin low resets the channel and forces the corresponding CHx_ON bit to the default value, 1, to support another startup when the external ENx pin is pulled high again.

OSCILLATOR

The switching frequency (f_{SW}) of the ADP5050 can be set to a value from 250 kHz to 1.4 MHz by connecting a resistor from the RT pin to ground. The value of the RT resistor can be calculated as follows:

$$R_{RT}\ (\text{k}\Omega) = [14{,}822/f_{SW}\ (\text{kHz})]^{1.081}$$

Figure 44 shows the typical relationship between the switching frequency (f_{SW}) and the RT resistor. The adjustable frequency allows users to make decisions based on the trade-off between efficiency and solution size.

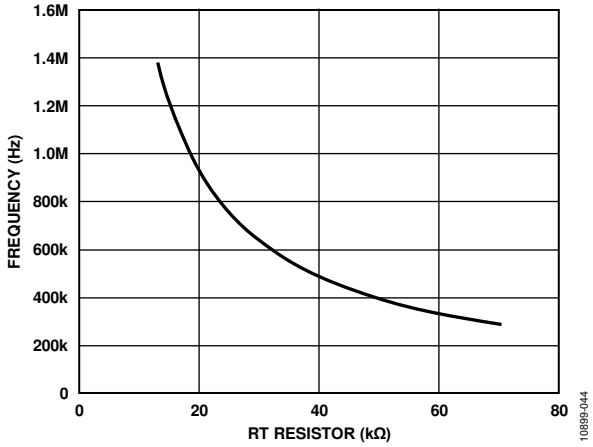

Figure 44. Switching Frequency vs. RT Resistor

For Channel 1 and Channel 3, the frequency can be set to half the master switching frequency set by the RT pin. This setting is configured using Register 8 (Bit 7 for Channel 3, and Bit 6 for Channel 1). If the master switching frequency is less than 250 kHz, this halving of the frequency for Channel 1 or Channel 3 is not recommended.

Phase Shift

By default, the phase shift between Channel 1 and Channel 2 and between Channel 3 and Channel 4 is 180° (see Figure 45). This value provides the benefits of out-of-phase operation by reducing the input ripple current and lowering the ground noise.

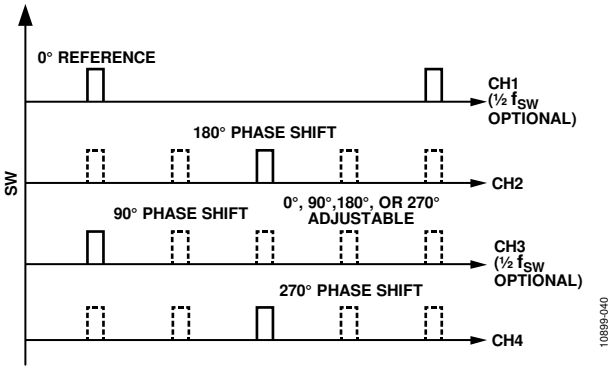

Figure 45. Phase Shift Diagram, Four Buck Regulators

For Channel 2 to Channel 4, the phase shift with respect to Channel 1 can be set to 0°, 90°, 180°, or 270° using Register 8, SW_CFG (see Figure 46). When parallel operation of Channel 1 and Channel 2 is configured, the switching frequency of Channel 2 is locked to a 180° phase shift with respect to Channel 1.

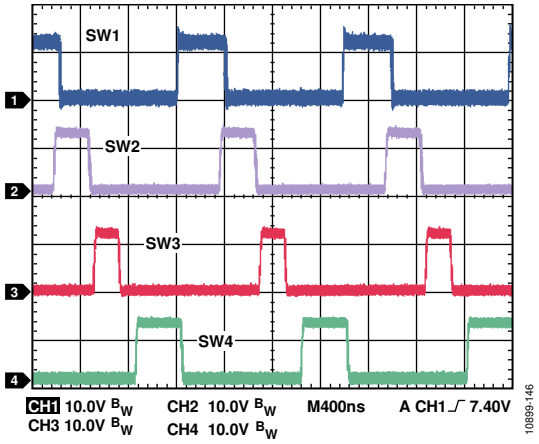

Figure 46. I²C Configurable 90° Phase Shift Waveforms, Four Buck Regulators

SYNCHRONIZATION INPUT/OUTPUT

The switching frequency of the ADP5050 can be synchronized to an external clock with a frequency range from 250 kHz to 1.4 MHz. The ADP5050 automatically detects the presence of an external clock applied to the SYNC/MODE pin, and the switching frequency transitions smoothly to the frequency of the external clock. When the external clock signal stops, the device automatically switches back to the internal clock and continues to operate.

Note that the internal switching frequency set by the RT pin must be programmed to a value that is close to the external clock value for successful synchronization; the suggested frequency difference is less than ±15% in typical applications.

The SYNC/MODE pin can be configured as a synchronization clock output by factory fuse or via the I²C interface (Register 10, HICCUP_CFG). A positive clock pulse with a 50% duty cycle is generated at the SYNC/MODE pin with a frequency equal to the internal switching frequency set by the RT pin. There is a short delay time (approximately 15% of t_{SW}) from the generated synchronization clock to the Channel 1 switching node.

Figure 47 shows two ADP5050 devices configured for frequency synchronization mode: one ADP5050 device is configured as the clock output to synchronize another ADP5050 device. It is recommended that a 100 kΩ pull-up resistor be used to prevent logic errors when the SYNC/MODE pin is left floating.

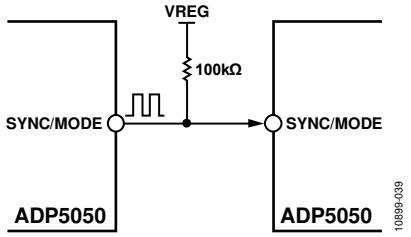

Figure 47. Two ADP5050 Devices Configured for Synchronization Mode

In the configuration shown in Figure 47, the phase shift between Channel 1 of the first ADP5050 device and Channel 1 of the second ADP5050 device is 0° (see Figure 48).

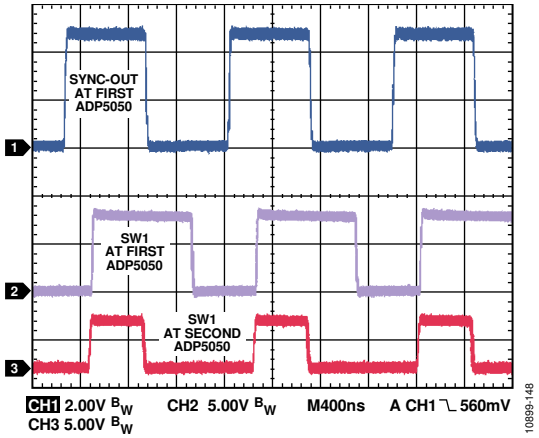

Figure 48. Waveforms of Two ADP5050 Devices Operating in Synchronization Mode

SOFT START

The buck regulators in the ADP5050 include soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current. The soft start time is typically fixed at 2 ms for each buck regulator when the SS12 and SS34 pins are tied to VREG.

To set the soft start time to a value of 2 ms, 4 ms, or 8 ms, connect a resistor divider from the SS12 or SS34 pin to the VREG pin and ground (see Figure 49). This configuration may be required to accommodate a specific start-up sequence or an application with a large output capacitor.

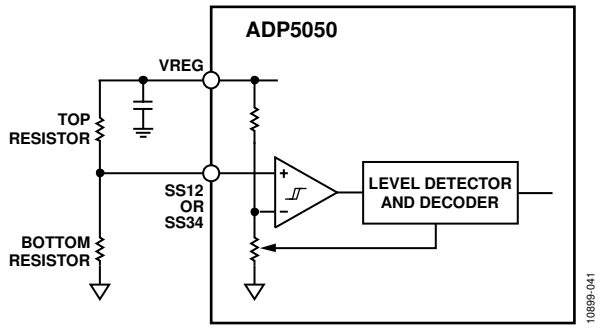

Figure 49. Level Detector Circuit for Soft Start

The SS12 pin can be used to program the soft start time and parallel operation for Channel 1 and Channel 2. The SS34 pin can be used to program the soft start time for Channel 3 and Channel 4. Table 11 provides the values of the resistors needed to set the soft start time.

Table 11. Soft Start Time Set by the SS12 and SS34 Pins

		Soft Start Time		Soft Start Time	
R_{TOP} (kΩ)	R_{BOT} (kΩ)	Channel 1	Channel 2	Channel 3	Channel 4
0	N/A	2 ms	2 ms	2 ms	2 ms
100	600	2 ms	Parallel	2 ms	4 ms
200	500	2 ms	8 ms	2 ms	8 ms
300	400	4 ms	2 ms	4 ms	2 ms
400	300	4 ms	4 ms	4 ms	4 ms
500	200	8 ms	2 ms	4 ms	8 ms
600	100	8 ms	Parallel	8 ms	2 ms
N/A	0	8 ms	8 ms	8 ms	8 ms

PARALLEL OPERATION

The ADP5050 supports two-phase parallel operation of Channel 1 and Channel 2 to provide a single output with up to 8 A of current. To configure Channel 1 and Channel 2 as a two-phase single output in parallel operation, do the following (see Figure 50):

- Use the SS12 pin to select parallel operation as specified in Table 11.
- Leave the COMP2 pin open.
- Use the FB1 pin to set the output voltage.
- Connect the FB2 pin to ground (FB2 is ignored).
- Connect the EN2 pin to ground (EN2 is ignored).

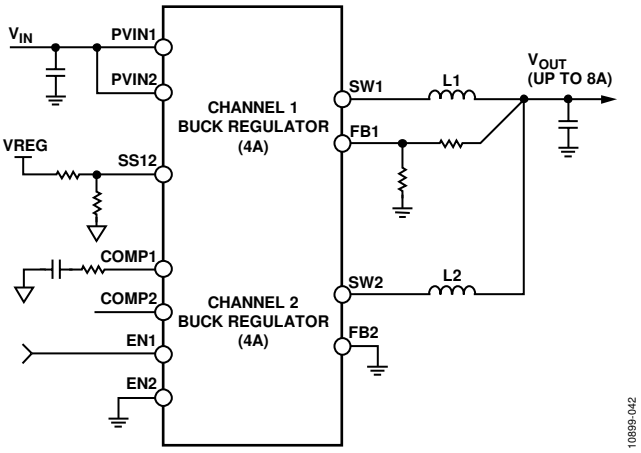

Figure 50. Parallel Operation for Channel 1 and Channel 2

When Channel 1 and Channel 2 are operated in the parallel configuration, configure the channels as follows:

- Set the input voltages and current-limit settings for Channel 1 and Channel 2 to the same values.
- Operate both channels in forced PWM mode.

Bits pertaining to Channel 2 in the configuration registers cannot be used. These bits include CH2_ON in Register 1, VID2 in Register 3, OVP2_ON and SCP2_ON in Register 7, PHASE2 in Register 8, and PWRG2 in Register 13.

Current balance in parallel configuration is well regulated by the internal control loop. Figure 51 shows the typical current balance matching in the parallel output configuration.

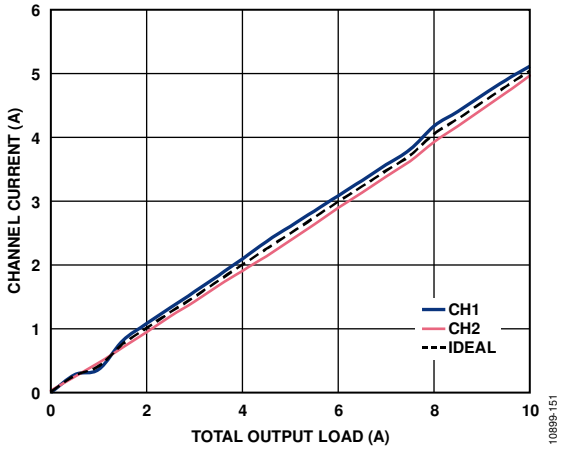

Figure 51. Current Balance in Parallel Output Configuration, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, FPWM Mode

STARTUP WITH PRECHARGED OUTPUT

The buck regulators in the ADP5050 include a precharged start-up feature to protect the low-side FETs from damage during startup. If the output voltage is precharged before the regulator is turned on, the regulator prevents reverse inductor current—which discharges the output capacitor—until the internal soft start reference voltage exceeds the precharged voltage on the feedback (FBx) pin.

CURRENT-LIMIT PROTECTION

The buck regulators in the ADP5050 include peak current-limit protection circuitry to limit the amount of positive current flowing through the high-side MOSFET. The peak current limit on the power switch limits the amount of current that can flow from the input to the output. The programmable current-limit threshold feature allows for the use of small size inductors for low current applications.

To configure the current-limit threshold for Channel 1, connect a resistor from the DL1 pin to ground; to configure the current-limit threshold for Channel 2, connect another resistor from the DL2 pin to ground. Table 12 lists the peak current-limit threshold settings for Channel 1 and Channel 2.

Table 12. Peak Current-Limit Threshold Settings for Channel 1 and Channel 2

R_{ILIM1} or R_{ILIM2}	Typical Peak Current-Limit Threshold
Floating	4.4 A
47 kΩ	2.63 A
22 kΩ	6.44 A

The buck regulators in the ADP5050 include negative current-limit protection circuitry to limit certain amounts of negative current flowing through the low-side MOSFET.

FREQUENCY FOLDBACK

The buck regulators in the ADP5050 include frequency foldback to prevent output current runaway when a hard short occurs on the output. Frequency foldback is implemented as follows:

- If the voltage at the FBx pin falls below half the target output voltage, the switching frequency is reduced by half.
- If the voltage at the FBx pin falls again to below one-fourth the target output voltage, the switching frequency is reduced to half its current value, that is, to one-fourth of f_{SW}.

The reduced switching frequency allows more time for the inductor current to decrease, but also increases the ripple current during peak current regulation. This results in a reduction in average current and prevents output current runaway.

Pulse Skip Mode Under Maximum Duty Cycle

Under maximum duty cycle conditions, frequency foldback maintains the output in regulation. If the maximum duty cycle is reached—for example, when the input voltage decreases—the PWM modulator skips every other PWM pulse, resulting in a switching frequency foldback of one-half. If the duty cycle increases further, the PWM modulator skips two of every three PWM pulses, resulting in a switching frequency foldback to one-third of the switching frequency. Frequency foldback increases the effective maximum duty cycle, thereby decreasing the dropout voltage between the input and output voltages.

HICCUP PROTECTION

The buck regulators in the ADP5050 include a hiccup mode for overcurrent protection (OCP). When the peak inductor current reaches the current-limit threshold, the high-side MOSFET turns off and the low-side MOSFET turns on until the next cycle.

When hiccup mode is active, the overcurrent fault counter is incremented. If the overcurrent fault counter reaches 15 and overflows (indicating a short-circuit condition), both the high-side and low-side MOSFETs are turned off. The buck regulator remains in hiccup mode for a period equal to seven soft start cycles and then attempts to restart from soft start. If the short-circuit fault has cleared, the regulator resumes normal operation; otherwise, it reenters hiccup mode after the soft start.

Hiccup protection is masked during the initial soft start cycle to enable startup of the buck regulator under heavy load conditions. Note that careful design and proper component selection are required to ensure that the buck regulator recovers from hiccup mode under heavy loads. The HICCUPx_OFF bits in Register 10 can be used to disable hiccup protection for each buck regulator. When hiccup protection is disabled, the frequency foldback feature is still available for overcurrent protection.

LATCH-OFF PROTECTION

The buck regulators in the ADP5050 have an optional latch-off mode to protect the device from serious problems such as short-circuit and overvoltage conditions. Latch-off mode can be enabled via the I^2C interface or by factory fuse.

Short-Circuit Latch-Off Mode

Short-circuit latch-off mode is enabled by factory fuse or by writing a 1 to the SCPx_ON bit in Register 7, LCH_CFG. When short-circuit latch-off mode is enabled and the protection circuit detects an overcurrent status after a soft start, the buck regulator enters hiccup mode and attempts to restart. If seven continuous restart attempts are made and the regulator remains in the fault condition, the regulator is shut down. This shutdown (latch-off) condition is cleared only by reenabling the channel or by resetting the channel power supply.

Figure 52 shows the short-circuit latch-off detection function.

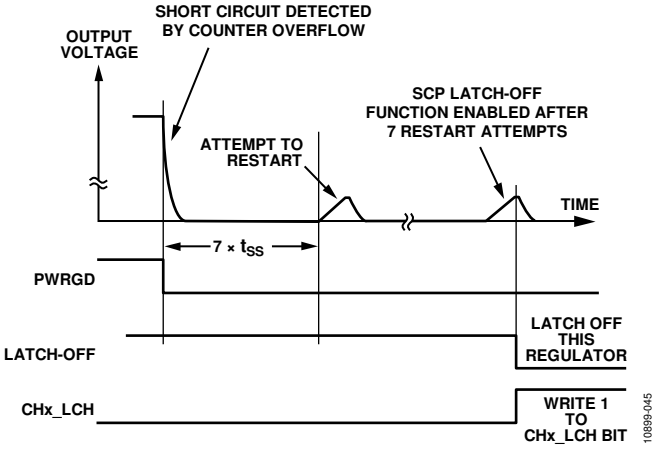

Figure 52. Short-Circuit Latch-Off Detection