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Linear LiFePO$_4$ Battery Charger with Power Path and USB Compatibility in LFCSP

Data Sheet

ADP5063

FEATURES

- Default charging termination voltage at 3.6 V
- Fully compatible with USB 3.0 and USB Battery Charging 1.2 Compliance Plan Specification
- Operating input voltage from 4 V to 6.7 V
- Tolerant input voltage from −0.5 V to +20 V (USB VBUS)
- Fully programmable via I²C
- Flexible digital control inputs
- Up to 2.1 A current from an ac charger in LDO mode
- Built-in current sensing and limiting
- As low as 55 mΩ battery isolation FET between battery and charger output
- Thermal regulation prevents overheating
- Compliant with JEITA1 and JEITA2 Li-Ion battery charging temperature specifications
- SYS_EN flag permits the system to be disabled until battery is at the minimum required level for guaranteed system start-up
- 4 mm × 4 mm LFCSP package

APPLICATIONS

- Single cell lithium iron phosphate (LiFePO$_4$) portable equipment
- Portable medical devices
- Portable instrumentation devices
- Portable consumer devices

GENERAL DESCRIPTION

The ADP5063 charger is fully compliant with USB 3.0 and the USB Battery Charging 1.2 Compliance Plan Specification, and enables charging via the mini USB VBUS pin from a wall charger, car charger, or USB host port.

The ADP5063 operates from a 4 V to 6.7 V input voltage range but is tolerant of voltages up to 20 V, thereby alleviating concerns about USB bus spikes during disconnection or connection scenarios.

The ADP5063 features an internal field effect transistor (FET) between the linear charger output and the battery. This permits battery isolation and, therefore, system powering under a dead battery or no battery scenario, which allows immediate system function upon connection to a USB power supply.

Based on the type of USB source, which is detected by an external USB detection chip, the ADP5063 can be set to apply the correct current limit for optimal charging and USB compliance.

The ADP5063 has three factory-programmable digital input/output pins that provide maximum flexibility for different systems. These digital input/output pins permit a combination of features, such as input current limits, charging enable and disable, charging current limits, and a dedicated interrupt output pin.

TYPICAL APPLICATION CIRCUIT

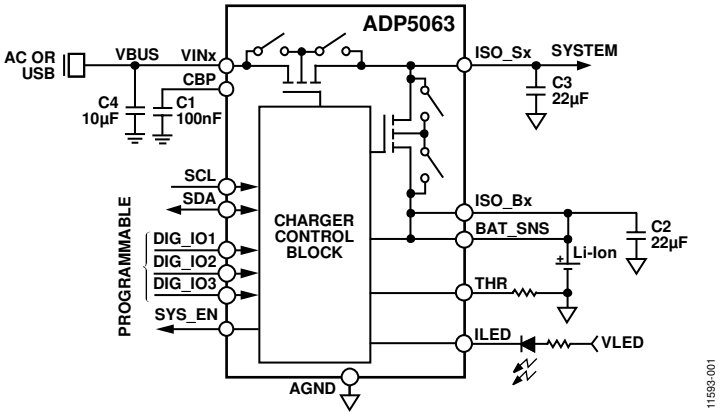

Figure 1.

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ADP5063* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADP5063 Evaluation Board

DOCUMENTATION

Data Sheet

- ADP5063: Linear LiFePO4 Battery Charger with Power Path and USB Compatibility in LFCSP Data Sheet

User Guides

- UG-595: Evaluating the ADP5063 Linear $LiFePO_4$ Battery Charger with Power Path and USB Compatibility in LFCSP

DESIGN RESOURCES

- ADP5063 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADP5063 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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Submit a technical question or find your regional support number.

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REVISION HISTORY

7/13—Revision 0: Initial Version

SPECIFICATIONS

$-40°C < T_J < +125°C$, $V_{VINx} = 5.0$ V, $R_{HOT\_RISE} < R_{THR} < R_{COLD\_FALL}$, $V_{BAT\_SNS} = 3.6$ V, $V_{ISO\_Bx} = V_{BAT\_SNS}$, $C_{VINx} = 10$ µF, $C_{ISO\_Sx} = 22$ µF, $C_{ISO\_Bx} = 22$ µF, $C_{CBP} = 100$ nF, all registers are at default values, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
GENERAL PARAMETERS						
Undervoltage Lockout	V_{UVLO}	2.25	2.35	2.5	V	Falling threshold, higher of V_{VINx} or V_{BAT_SNS}[1]
Hysteresis		50	100	150	mV	Hysteresis, higher of V_{VINx} or V_{BAT_SNS} rising[1]
Total Input Current	I_{LIM}	74	92	100	mA	Nominal USB initialized current level[2]
		114		150	mA	USB super speed
				300	mA	USB enumerated current level (specification for China)
		425	470	500	mA	USB enumerated current level
				900	mA	Dedicated charger input
				1500	mA	Dedicated wall charger
VINx Current Consumption	I_{QVIN}		2		mA	Charging or LDO mode
	$I_{QVIN\_SUSPEND}$		1.0	1.8	mA	DIS_LDO = high, $T_J = -40°C$ to $+85°C$
Battery Current Consumption	I_{QBATT}		20		µA	LDO mode, $V_{ISO\_Sx} > V_{BAT\_SNS}$
				5	µA	Standby, includes ISO_Sx pin leakage, $V_{VINx} = 0$ V, $T_J = -40°C$ to $+85°C$
			0.5	0.9	mA	Standby, battery monitor active
CHARGER						
Fast Charge Current Constant Current (CC) Mode	I_{CHG}		750		mA	
Fast Charge Current Accuracy		−9		+9	%	I_{CHG} = 400 mA to 1300 mA, $V_{ISO\_Bx} = 3.3$ V, $T_J = 0°C$ to $115°C$
Trickle Charge Current[2]	I_{TRK_DEAD}	16	20	25	mA	
Weak Charge Current[2, 3]	I_{CHG_WEAK}		$I_{TRK\_DEAD} + I_{CHG}$		mA	
Trickle to Weak Charge Threshold						
Dead Battery	V_{TRK_DEAD}	1.9	2.0	2.1	V	$V_{TRK\_DEAD} < V_{BAT\_SNS} < V_{WEAK}$[2, 4]
Hysteresis	ΔV_{TRK_DEAD}		100		mV	On BAT_SNS[2]
Weak Battery Threshold						
Weak to Fast Charge Threshold	V_{WEAK}	2.89	3.0	3.11	V	On BAT_SNS[2, 4]
	ΔV_{WEAK}		100		mV	
Battery Termination Voltage	V_{TRM}		3.600		V	
Termination Voltage Accuracy		−0.6		+0.6	%	On BAT_SNS, $T_J = 25°C$, $I_{END} = 52.5$ mA[2]
		−1.55		+1.45	%	$T_J = 0°C$ to $115°C$[2]
		−1.7		+1.7	%	$T_J = -40°C$ to $+125°C$
Battery Overvoltage Threshold	V_{BATOV}		$V_{IN} - 0.075$		V	Relative to VINx voltage, BAT_SNS rising
Charge Complete Current	I_{END}	15	52.5	98	mA	$V_{BAT\_SNS} = V_{TRM}$
Charging Complete Current Threshold Accuracy		17		83	mA	$I_{END} = 52.5$ mA, $T_J = 0°C$ to $115°C$[2]
		59		123	mA	$I_{END} = 92.5$ mA, $T_J = 0°C$ to $115°C$
Recharge Voltage Differential	V_{RCH}	160	260	390	mV	Relative to V_{TRM}, BAT_SNS falling[2]
Battery Node Short Threshold Voltage[2]	V_{BAT_SHR}	2.2	2.4	2.5	V	
Battery Short Detection Current	I_{TRK_SHORT}		20		mA	$I_{TRK\_SHORT} = I_{TRK\_DEAD}$[2]
Charging Start Voltage Limit	V_{CHG_VLIM}	3.1	3.2	3.3	V	Voltage limit is not active by default
Charging Soft Start Current	I_{CHG_START}	185	260	365	mA	$V_{BAT\_SNS} > V_{TRK\_DEAD}$
Charging Soft Start Time	t_{CHG_START}		3		ms	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
BATTERY ISOLATION FET						
Pin to Pin Resistance Between ISO_Sx and ISO_Bx	R_{DSON_ISO}		55	89	mΩ	On battery supplement mode, VINx = 0 V, V_{ISO_Bx} = 3.6 V, I_{ISO_Bx} = 500 mA
Regulated System Voltage: V_{BAT} Low	V_{ISO_SFC}	3.6	3.8	4.0	V	VTRM[5:0] programming ≥ 4.00 V
		3.2	3.4	3.5	V	VTRM[5:0] programming < 4.00 V
Battery Supplementary Threshold	V_{THISO}	0	5	12	mV	V_{ISO_Sx} < V_{ISO_Bx}, system voltage rising
LDO AND HIGH VOLTAGE BLOCKING						
Regulated System Voltage	V_{ISO_STRK}	4.214	4.3	4.386	V	VSYSTEM[2:0] = 000 (binary) = 4.3 V, I_{ISO_Sx} = 100 mA, LDO mode[2]
Load Regulation			−0.56		%/A	I_{ISO_Sx} = 0 mA to 1500 mA
High Voltage Blocking FET (LDO FET) On Resistance	$R_{DS(ON)HV}$		330	485	mΩ	I_{VINx} = 500 mA
Maximum Output Current			2.1		A	V_{ISO_Sx} = 4.3 V, LDO mode
VINx Input Voltage, Good Threshold Rising	$V_{VIN\_OK\_RISE}$	3.75	3.9	4.0	V	
VINx Falling	$V_{VIN\_OK\_FALL}$		3.6	3.7	V	
VINx Input Overvoltage Threshold	V_{VIN_OV}	6.7	6.9	7.2	V	
Hysteresis	ΔV_{VIN_OV}		0.1		V	
VINx Transition Timing	t_{VIN_RISE}	10			µs	Minimum rise time for VINx from 5 V to 20 V
	t_{VIN_FALL}	10			µs	Minimum fall time for VINx from 4 V to 0 V
THERMAL CONTROL						
Isothermal Charging Temperature	T_{LIM}		115		°C	
Thermal Early Warning Temperature	T_{SDL}		130		°C	
Thermal Shutdown Temperature	T_{SD}		140		°C	T_J rising
			110		°C	T_J falling
THERMISTOR CONTROL						
Thermistor Current						
10,000 NTC (Negative Temperature Coefficient) Resistor	I_{NTC_10k}			400	µA	
100,000 NTC Resistor	I_{NTC_100k}			40	µA	
Thermistor Capacitance	C_{NTC}		100		pF	
Cold Temperature Threshold	T_{NTC_COLD}		0		°C	No battery charging occurs
Resistance Thresholds						
Cool to Cold Resistance	R_{COLD_FALL}	20,500	25,600	30,720	Ω	
Cold to Cool Resistance	R_{COLD_RISE}		24,400		Ω	
Hot Temperature Threshold	T_{NTC_HOT}		60		°C	No battery charging occurs
Resistance Thresholds						
Hot to Typical Resistance	R_{HOT_FALL}		3700		Ω	
Typical to Hot Resistance	R_{HOT_RISE}	2750	3350	3950	Ω	
JEITA1 Li-ION BATTERY CHARGING SPECIFICATION DEFAULTS[5]						
JEITA Cold Temperature	T_{JEITA_COLD}		0		°C	No battery charging occurs
Resistance Thresholds						
Cool to Cold Resistance	R_{COLD_FALL}	20,500	25,600	30,720	Ω	
Cold to Cool Resistance	R_{COLD_RISE}		24,400		Ω	
JEITA Cool Temperature	T_{JEITA_COOL}		10		°C	Battery charging occurs at 50% of programmed level
Resistance Thresholds						
Typical to Cool Resistance	R_{TYP_FALL}	13,200	16,500	19,800	Ω	
Cool to Typical Resistance	R_{TYP_RISE}		15,900		Ω	
JEITA Warm Temperature	T_{JEITA_WARM}		45		°C	Battery termination voltage (V_{TRM}) is reduced by 100 mV
Resistance Thresholds						
Warm to Typical Resistance	R_{WARM_FALL}		5800		Ω	
Typical to Warm Resistance	R_{WARM_RISE}	4260	5200	6140	Ω	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
JEITA Hot Temperature	T_{JEITA_HOT}		60		°C	No battery charging occurs
Resistance Thresholds						
Hot to Warm Resistance	R_{HOT_FALL}		3700		Ω	
Warm to Hot Resistance	R_{HOT_RISE}	2750	3350	3950	Ω	
JEITA2 Li-ION BATTERY CHARGING SPECIFICATION DEFAULTS						
JEITA Cold Temperature	T_{JEITA_COLD}		0		°C	No battery charging occurs
Resistance Thresholds						
Cool to Cold Resistance	R_{COLD_FALL}	20,500	25,600	30,720	Ω	
Cold to Cool Resistance	R_{COLD_RISE}		24,400		Ω	
JEITA Cool Temperature	T_{JEITA_COOL}		10		°C	Battery termination voltage (V_{TRM}) is reduced by 100 mV
Resistance Thresholds						
Typical to Cool Resistance	R_{TYP_FALL}	13,200	16,500	19,800	Ω	
Cool to Typical Resistance	R_{TYP_RISE}		15,900		Ω	
JEITA Warm Temperature	T_{JEITA_WARM}		45		°C	Battery termination voltage (V_{TRM}) is reduced by 100 mV
Resistance Thresholds						
Warm to Typical Resistance	R_{WARM_FALL}		5800		Ω	
Typical to Warm Resistance	R_{WARM_RISE}	4260	5200	6140	Ω	
JEITA Hot Temperature	T_{JEITA_HOT}		60		°C	No battery charging occurs
Resistance Thresholds						
Hot to Warm Resistance	R_{HOT_FALL}		3700		Ω	
Warm to Hot Resistance	R_{HOT_RISE}	2750	3350	3950	Ω	
BATTERY DETECTION						
Sink Current	I_{SINK}	13	20	34	mA	
Source Current	I_{SOURCE}	7	10	13	mA	
Battery Threshold						
Low	V_{BATL}	1.8	1.9	2.0	V	
High	V_{BATH}		3.4		V	
Battery Detection Timer	t_{BATOK}		333		ms	
TIMERS						
Clock Oscillator Frequency	f_{CLK}	2.7	3	3.3	MHz	
Start Charging Delay	t_{START}		1		sec	
Trickle Charge	t_{TRK}		60		min	
Fast Charge	t_{CHG}		600		min	
Charge Complete	t_{END}		7.5		min	$V_{BAT\_SNS} = V_{TRM}$, $I_{CHG} < I_{END}$
Deglitch	t_{DG}		31		ms	Applies to V_{TRK_DEAD}, V_{RCH}, I_{END}, V_{WEAK}, $V_{VIN\_OK\_RISE}$, and $V_{VIN\_OK\_FALL}$
Watchdog[2]	t_{WD}		32		sec	
Safety	t_{SAFE}	36	40	44	min	
Battery Short[2]	t_{BAT_SHR}		30		sec	
ILED OUTPUT PINS						
Voltage Drop over ILED	V_{ILED}		200		mV	I_{ILED} = 20 mA
Maximum Operating Voltage over ILED	$V_{MAXILED}$			5.5	V	
SYS_EN OUTPUT Pin						
SYS_EN FET On Resistance	$R_{ON\_SYS\_EN}$		10		Ω	I_{SYS_EN} = 20 mA

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUT PINS						
Maximum Voltage on Digital Inputs	V_{DIN_MAX}			5.5	V	Applies to SCL, SDA, DIG_IO1, DIG_IO2, DIG_IO3
Maximum Logic Low Input Voltage	V_{IL}			0.5	V	Applies to SCL, SDA, DIG_IO1, DIG_IO2, DIG_IO3
Minimum Logic High Input Voltage	V_{IH}	1.2			V	Applies to SCL, SDA, DIG_IO1, DIG_IO2, DIG_IO3
Pull-Down Resistance		215	350	610	kΩ	Applies to DIG_IO1, DIG_IO2, DIG_IO3

[1] Undervoltage lockout generated normally from ISO_Sx or ISO_Bx; in certain transition cases, it can be generated from VINx.
[2] These values are programmable via I²C. Values are given with default register values.
[3] The output current during charging may be limited by the input current limit or by the isothermal charging mode.
[4] During weak charging mode, the charger provides at least 20 mA of charging current via the trickle charge branch to the battery unless trickle charging is disabled. Any residual current that is not required by the system is also used to charge the battery.
[5] Either JEITA1 (default) or JEITA2 can be selected in I²C, or both JEITA functions can be enabled or disabled in I²C.

RECOMMENDED INPUT AND OUTPUT CAPACITANCES

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CAPACITANCES						Effective capacitance
VINx	C_{VINx}	4		10	µF	
CBP	C_{CBP}	60	100	140	nF	
ISO_Sx	C_{ISO_Sx}	10	22	100	µF	
ISO_Bx	C_{ISO_Bx}	10	22		µF	

I²C-COMPATIBLE INTERFACE TIMING SPECIFICATIONS

Table 3.

Parameter[1]	Symbol	Min	Typ	Max	Unit
I²C-COMPATIBLE INTERFACE[2]					
Capacitive Load for Each Bus Line	C_S			400	pF
SCL Clock Frequency	f_{SCL}			400	kHz
SCL High Time	t_{HIGH}	0.6			µs
SCL Low Time	t_{LOW}	1.3			µs
Data Setup Time	$t_{SU, DAT}$	100			ns
Data Hold Time	$t_{HD, DAT}$	0		0.9	µs
Setup Time for Repeated Start	$t_{SU, STA}$	0.6			µs
Hold Time for Start/Repeated Start	$t_{HD, STA}$	0.6			µs
Bus Free Time Between a Stop and a Start Condition	t_{BUF}	1.3			µs
Setup Time for Stop Condition	$t_{SU, STO}$	0.6			µs
Rise Time of SCL/SDA	t_R	20		300	ns
Fall Time of SCL/SDA	t_F	20		300	ns
Pulse Width of Suppressed Spike	t_{SP}	0		50	ns

[1] Guaranteed by design.
[2] A master device must provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL (see Figure 2).

Timing Diagram

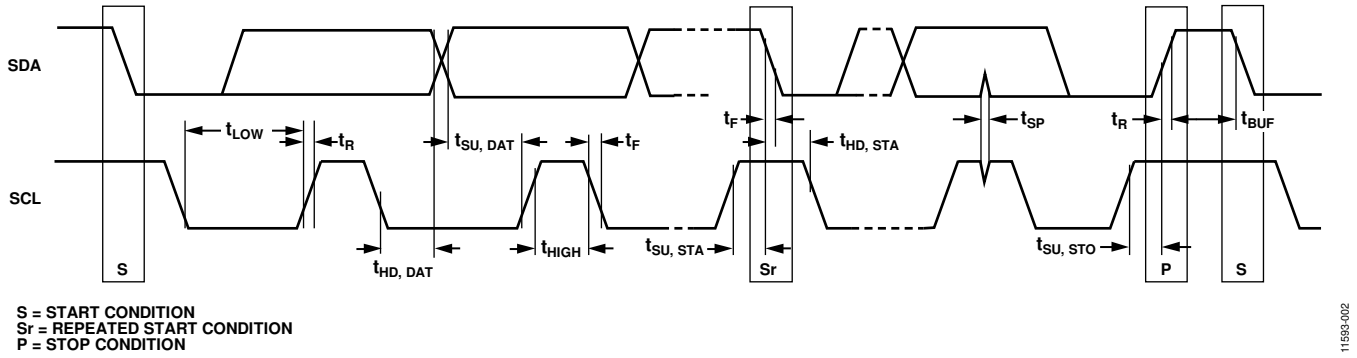

Figure 2. I²C Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VIN1, VIN2, VIN3 to AGND	−0.5 V to +20 V
All Other Pins to AGND	−0.3 V to +6 V
Continuous Drain Current, Battery Supplementary Mode, from ISO_Bx to ISO_Sx	2.1 A
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in a circuit board for surface-mount packages.

Table 5.

Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead LFCSP	35.6	3.65	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the ADP5063 package is limited by the associated rise in junction temperature (T_J) on the die. At a die temperature of approximately 150°C (the glass transition temperature), the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, thereby permanently shifting the parametric performance of the ADP5063. Exceeding a junction temperature of 175°C for an extended period can result in changes in the silicon devices, potentially causing failure.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

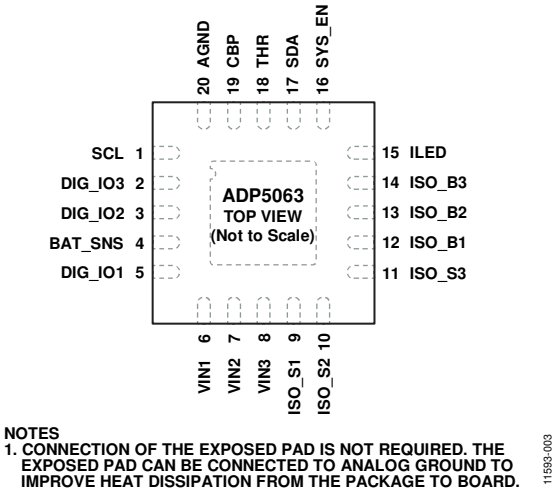

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Name	Type[1]	Description
1	SCL	I	I²C-Compatible Interface Serial Clock.
2	DIG_IO3	GPIO	Charging Enable. When DIG_IO3 = low or high-Z, charging is disabled. When DIG_IO3 = high, charging is enabled.[2, 3]
3	DIG_IO2	GPIO	Set Input Current Limit. When DIG_IO2 = low or high-Z, the input limit is defined by DIG_IO1 setting. When DIG_IO2 = high, the input limit is 1500 mA.[2, 3]
4	BAT_SNS	I	Battery Voltage Sense Pin.
5	DIG_IO1	GPIO	Set Input Current Limit. This pin sets the input current limit directly. When DIG_IO1 = low or high-Z, the input limit is 100 mA. When DIG_IO1 = high, the input limit is 500 mA.[2, 3]
6, 7, 8	VIN1, VIN2, VIN3	I/O	Power Connections to USB VBUS. These pins are high current inputs when in charging mode.
9, 10, 11	ISO_S1, ISO_S2, ISO_S3	I/O	Linear Charger Supply Side Input to Internal Isolation FET/Battery Current Regulation FET. High current input/output.
12, 13, 14	ISO_B1, ISO_B2, ISO_B3	I/O	Battery Supply Side Input to Internal Isolation FET/Battery Current Regulation FET.
15	ILED	O	Open-Drain Output to Indicator LED.
16	SYS_EN	O	System Enable. This pin is the battery OK flag/open-drain pull-down FET to enable the system when the battery reaches the V_{WEAK} level.
17	SDA	I/O	I²C-Compatible Interface Serial Data.
18	THR	I	Battery Pack Thermistor Connection. If this pin is not used, connect a dummy 10 kΩ resistor from THR to AGND.
19	CBP	I/O	Bypass Capacitor Input.
20	AGND	G	Analog Ground.
N/A[4]	EP	N/A[4]	Exposed Pad. Connection of the exposed pad is not required. The exposed pad can be connected to analog ground to improve heat dissipation from the package to the board.

[1] I is input, O is output, I/O is input/output, G is ground, and GPIO is the factory programmable general-purpose input/output.
[2] See the Digital Input and Output Options section for details.
[3] The DIG_IOx setting defines the initial state of the ADP5063. If the parameter or the mode that is related to each DIG_IOx pin setting is changed (by programming an equivalent I²C register bit or bits), the I²C register setting takes precedence over the DIG_IOx pin setting. VINx connection or disconnection resets control to the DIG_IOx pin.
[4] N/A = not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{VINx} = 5.0 V, C_{VINx} = 10 µF, C_{ISO_Sx} = 44 µF, C_{ISO_Bx} = 22 µF, C_{CBP} = 100 nF, all registers are at default values, unless otherwise noted.

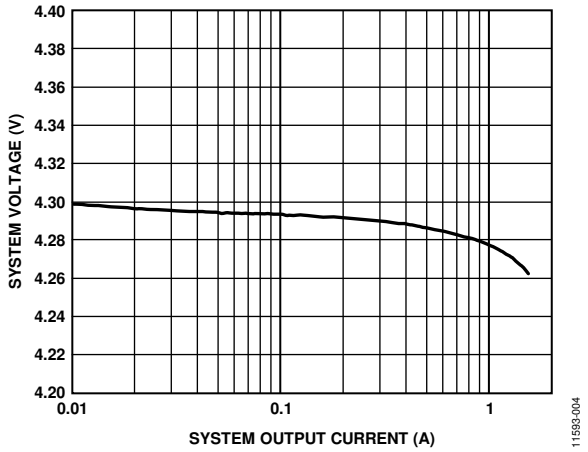

Figure 4. System Voltage vs. System Output Current, LDO Mode, VSYSTEM[2:0] = 000 (Binary) = 4.3 V

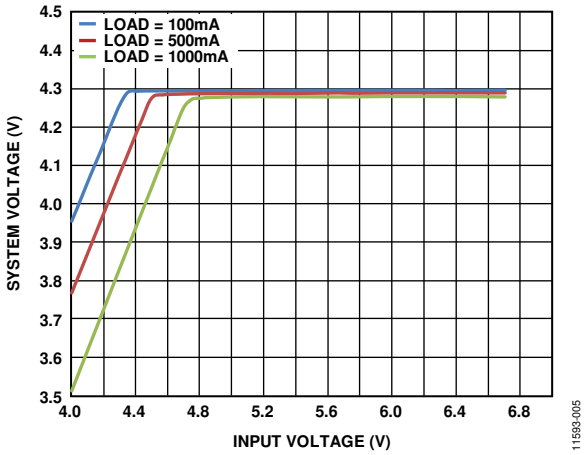

Figure 5. System Voltage vs. Input Voltage (in Dropout), LDO Mode, VSYSTEM[2:0] = 000 (Binary) = 4.3 V

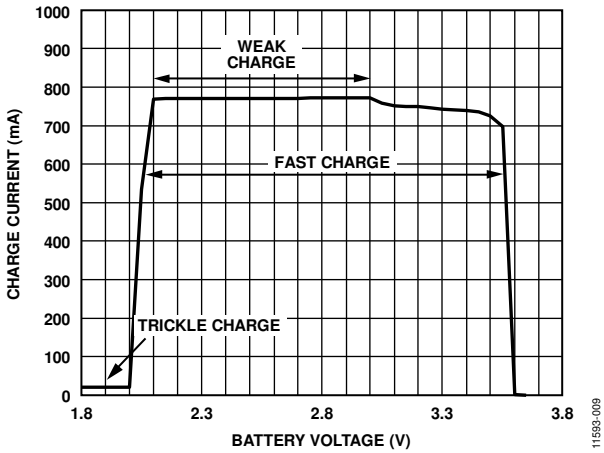

Figure 6. Battery Charge Current vs. Battery Voltage, ICHG[4:0] = 01001 (Binary) = 500 mA, ILIM[3:0] = 1111 (Binary) = 2100 mA

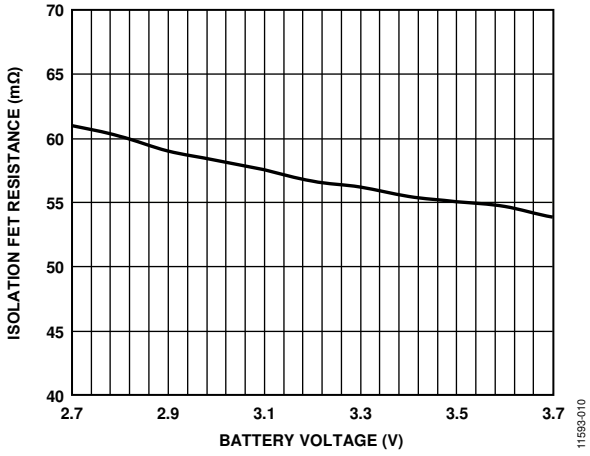

Figure 7. Ideal Diode R_{ON} vs. Battery Voltage, I_{ISO_Sx} = 500 mA, VINx Open

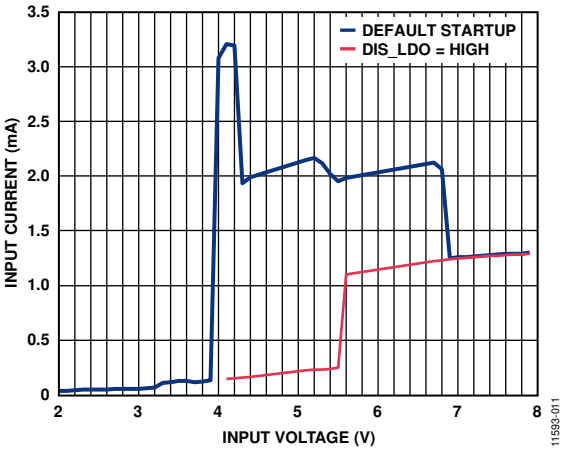

Figure 8. Input Current vs. Input Voltage, V_{ISO_Bx} = 3.3 V

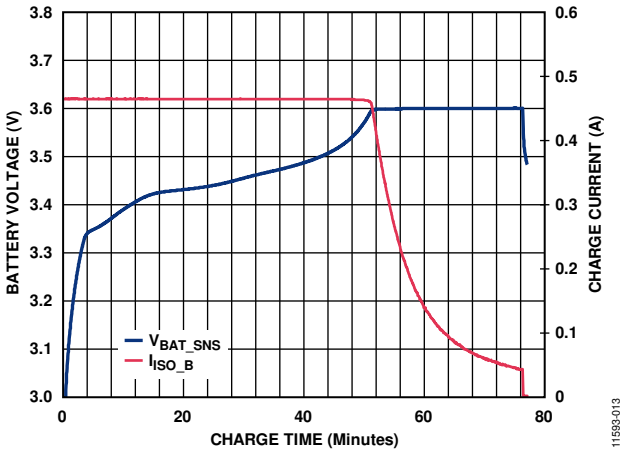

Figure 10. Charge Profile, ILIM[3:0] = 0110 (Binary) = 500 mA, $LiFePO_4$ Battery Capacity = 500 mAh

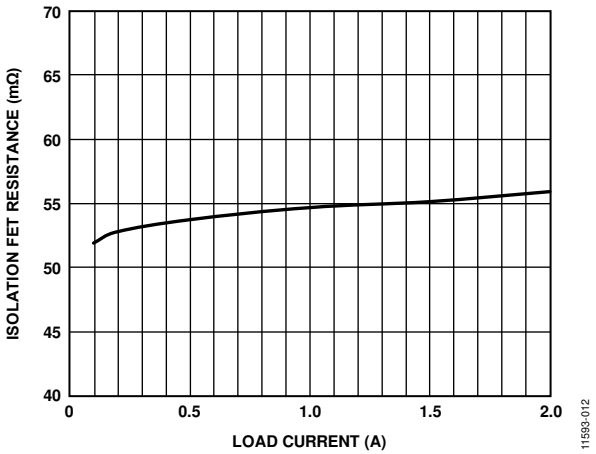

Figure 9. Ideal Diode R_{ON} vs. Load Current, V_{ISO_Bx} = 3.6 V

TEMPERATURE CHARACTERISTICS

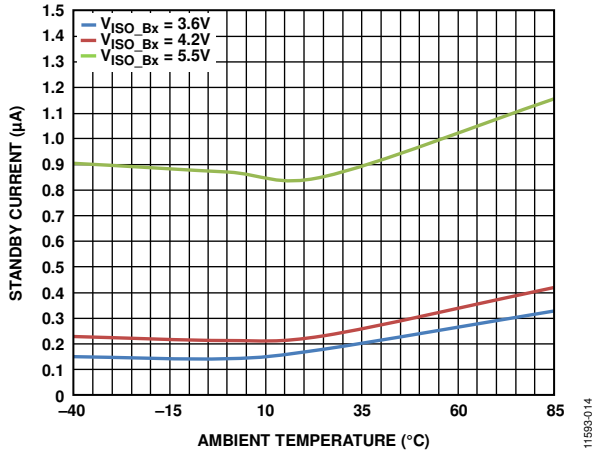

Figure 11. Battery Leakage (Standby) Current vs. Ambient Temperature, Standby Mode

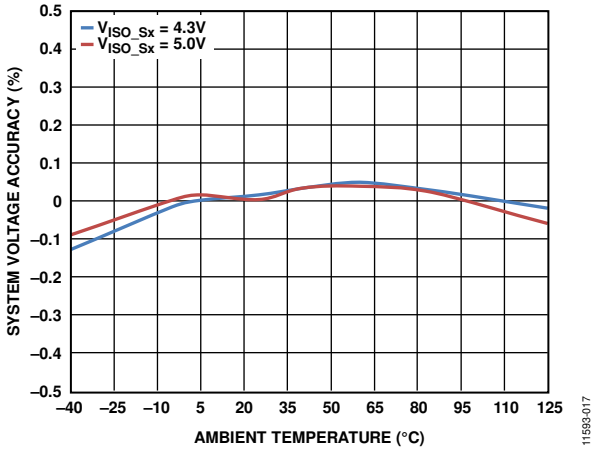

Figure 14. System Voltage Accuracy vs. Ambient Temperature, Trickle Charge Mode, V_{ISO_Sx} = 4.3 V and V_{VINx} = 5.0 V, or V_{ISO_Sx} = 5.0 V and V_{VINx} = 6.0 V

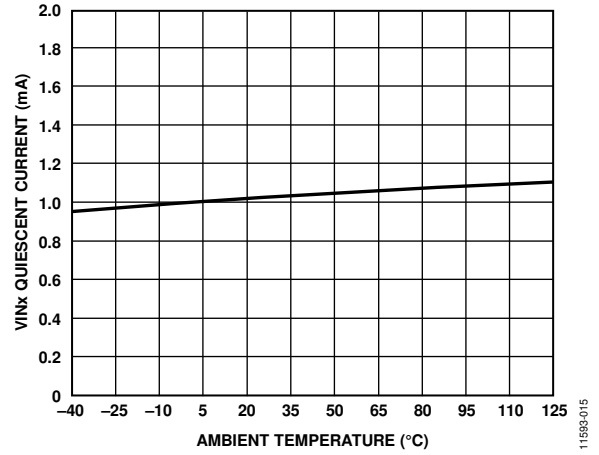

Figure 12. VINx Quiescent Current vs. Ambient Temperature, DIS_LDO = High

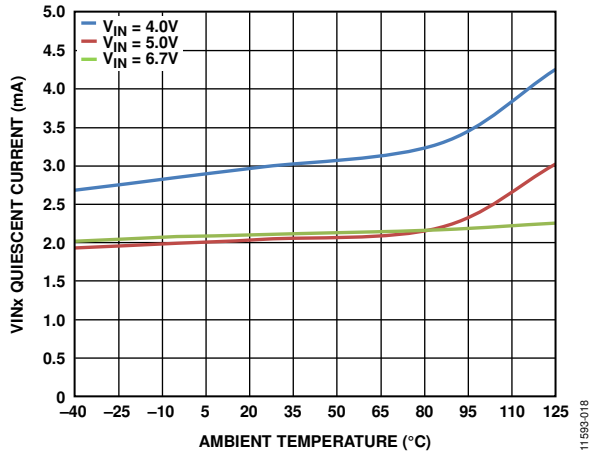

Figure 15. VINx Quiescent Current vs. Ambient Temperature, LDO Mode

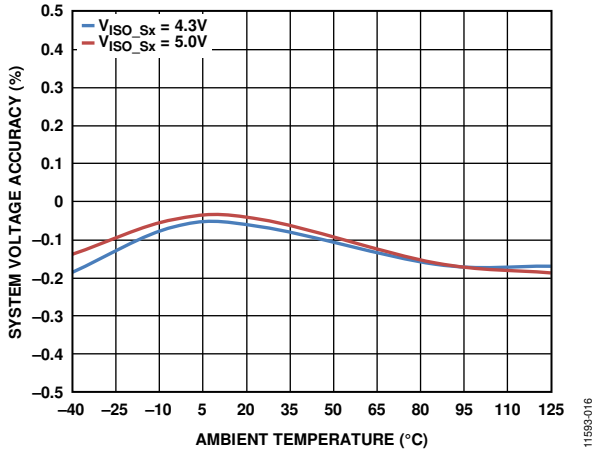

Figure 13. System Voltage Accuracy vs. Ambient Temperature, Load = 100 mA, V_{VINx} = 5.5 V

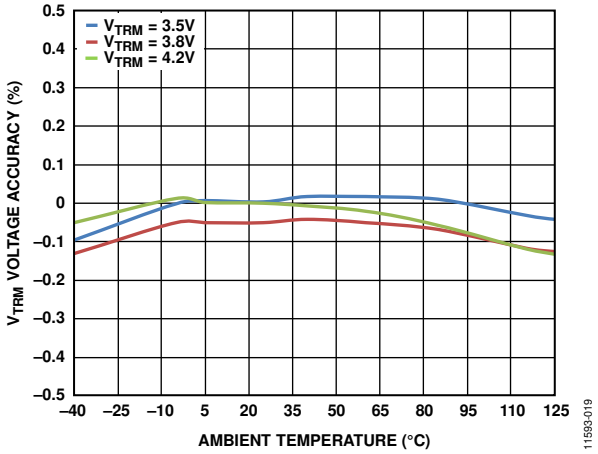

Figure 16. Termination (V_{TRM}) Voltage Accuracy vs. Ambient Temperature

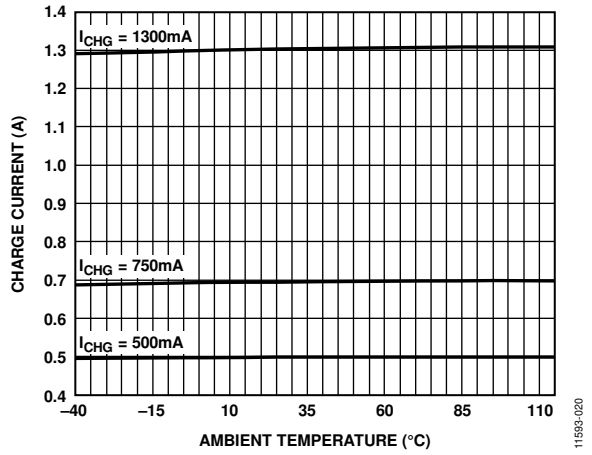

Figure 17. Fast Charge Current CC Mode vs. Ambient Temperature

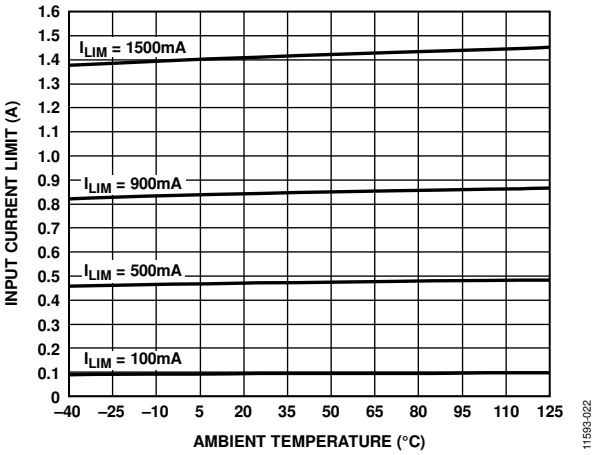

Figure 19. Input Current Limit vs. Ambient Temperature

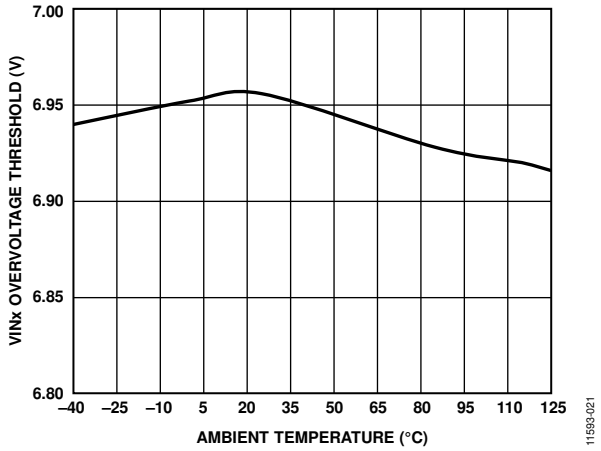

Figure 18. VINx Overvoltage Threshold vs. Ambient Temperature

TYPICAL WAVEFORMS

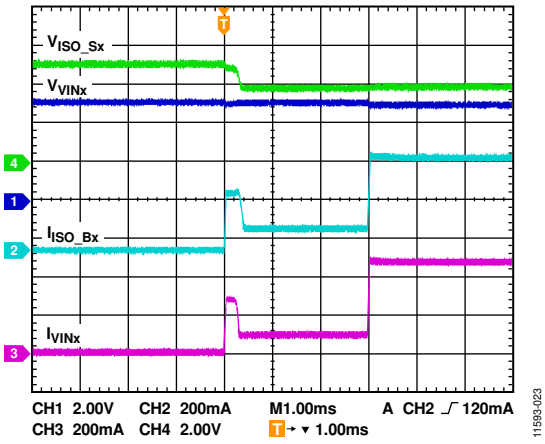

Figure 20. Charging Startup, V_{VINx} = 5.0 V, ILIM[3:0] = 0110 (Binary) = 500 mA, ICHG[4:0] = 01110 (Binary) = 750 mA

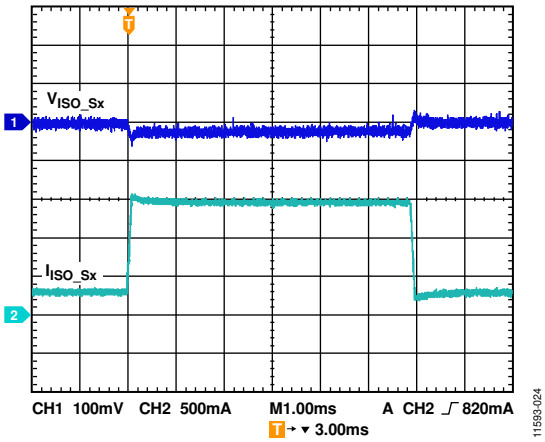

Figure 21. Load Transient, I_{ISO_Sx} Load = 300 mA to 1500 mA to 300 mA

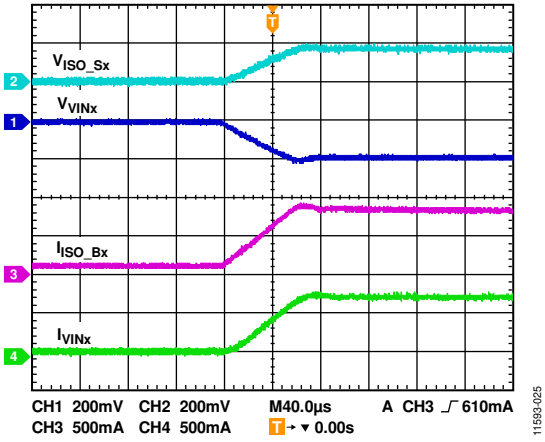

Figure 22. Input Current-Limit Transition from 100 mA to 900 mA, ISO_Sx Load = 66 Ω, Charging = 750 mA

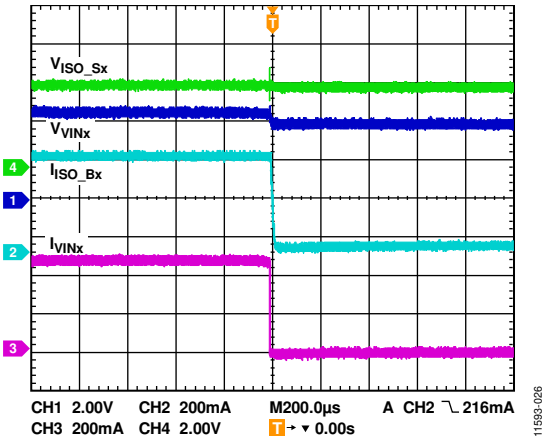

Figure 23. USB VBUS Disconnection

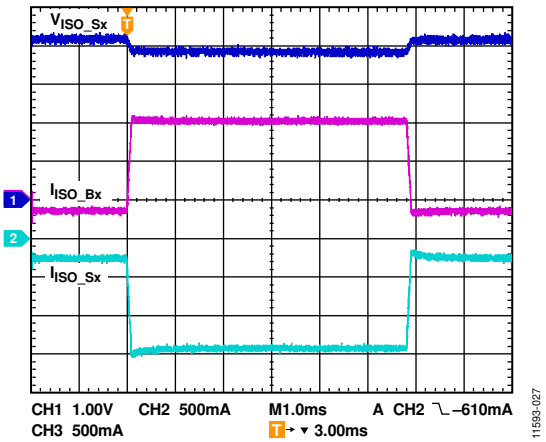

Figure 24. Load Transient, I_{ISO_Sx} Load = 300 mA to 1500 mA to 300 mA, EN_CHG = High, ILIM[3:0] = 0110 (Binary) = 500 mA

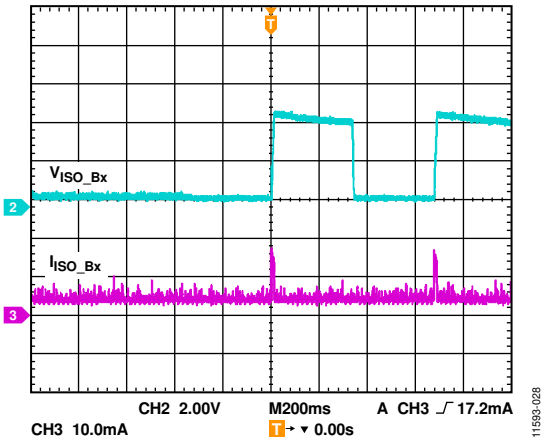

Figure 25. Battery Detection Waveform, VSYSTEM[2:0] = 000 (Binary) = 4.3 V, No Battery

THEORY OF OPERATION

SUMMARY OF OPERATION MODES

Table 7. Summary of Operation Modes

Mode Name	V_{VINx} Condition	Battery Condition	Trickle Charge	LDO FET State	Battery Isolation FET	System Voltage ISO_Sx	Additional Conditions[1]
IC Off, Standby	0 V	Any battery condition	Off	Off	On	Battery voltage or 0 V	
IC Off, Suspend	5 V	Any battery condition	Off	Off	On	Battery voltage	DIS_LDO = high
LDO Mode Off, Isolation FET On	5 V	Any battery condition	Off	Off	On	Battery voltage	Disable LDO and enable isolation FET
LDO Mode Off, Isolation FET Off (System Off)	5 V	Any battery condition	Off	Off	Off	0 V	Enable battery charging
LDO Mode, Charger Off	5 V	Any battery condition	Off	LDO	Off	4.3 V	Enable battery charging
Trickle Charge Mode	5 V	Battery < V_{TRK_DEAD}	On	LDO	Off	4.3 V	Enable battery charging
Weak Charge Mode	5 V	V_{TRK_DEAD} ≤ battery < V_{WEAK}	On	CHG	CHG	3.4 V	Enable battery charging
Fast Charge Mode	5 V	Battery ≥ V_{WEAK}	Off	CHG	CHG	3.4 V (minimum)	Enable battery charging
Charge Mode, No Battery	5 V	Open	Off	LDO	Off	4.3 V	Enable battery charging
Charge Mode, Battery (ISO_Bx) Shorted	5 V	Shorted	On	LDO	Off	4.3 V	Enable battery charging

[1] See Table 8 for details.

Table 8. Operation Mode Controls

Pin Configuration	DIG_IOx	Equivalent I²C Address, Data Bit(s)	Description
Enable Battery Charging	DIG_IO3	0x07, D0	Low = all charging modes disabled (fast, weak, trickle). High = all charging modes enabled (fast, weak, trickle).
Disable LDO and Enable Isolation FET	Not applicable	0x07, D3, D0	Low = LDO enabled. High = LDO disabled. In addition, when EN_CHG = low, the battery isolation FET is on; when EN_CHG = high, the battery isolation FET is off.

INTRODUCTION

The ADP5063 is a fully programmable I²C charger for single cell lithium ion or lithium polymer batteries, suitable for a wide range of portable applications.

The linear charger architecture enables up to 2.1 A output current at 4.3 V to 5.0 V (I²C programmable) on the system power supply, and up to 1.3 A of charge current into the battery from a dedicated charger.

The ADP5063 operates from an input voltage of 4 V up to 6.7 V but is tolerant of voltages of up to 20 V. The 20 V voltage tolerance alleviates the concerns of the USB bus spiking during disconnection or connection scenarios.

The ADP5063 features an internal FET between the linear charger output and the battery. This feature permits battery isolation and, therefore, system powering under a dead battery or no battery scenario, which allows immediate system function upon connection to a USB power supply.

The ADP5063 is fully compliant with USB 3.0 and the USB Battery Charging 1.2 Compliance Plan Specification. The ADP5063 is chargeable via the mini USB VBUS pin from a wall charger, car charger, or USB host port. Based on the type of USB source, which is detected by an external USB detection device, the ADP5063 can be set to apply the correct current limit for optimal charging and USB compliance. The USB charger permits correct operation under all USB compliant sources such as wall chargers, host chargers, hub chargers, and standard host and hubs.

A processor can control the USB charger using the I²C interface to program the charging current and numerous other parameters, including

- Trickle charge current level
- Trickle charge voltage threshold
- Weak charge (constant current) current level
- Fast charge (constant current) current level
- Fast charge (constant voltage) voltage level
- Fast charge safety timer period
- Watchdog safety timer parameters
- Weak battery threshold detection
- Charging complete threshold
- Recharge threshold
- Charging enable/disable
- Battery pack temperature detection and automatic charger shutdown

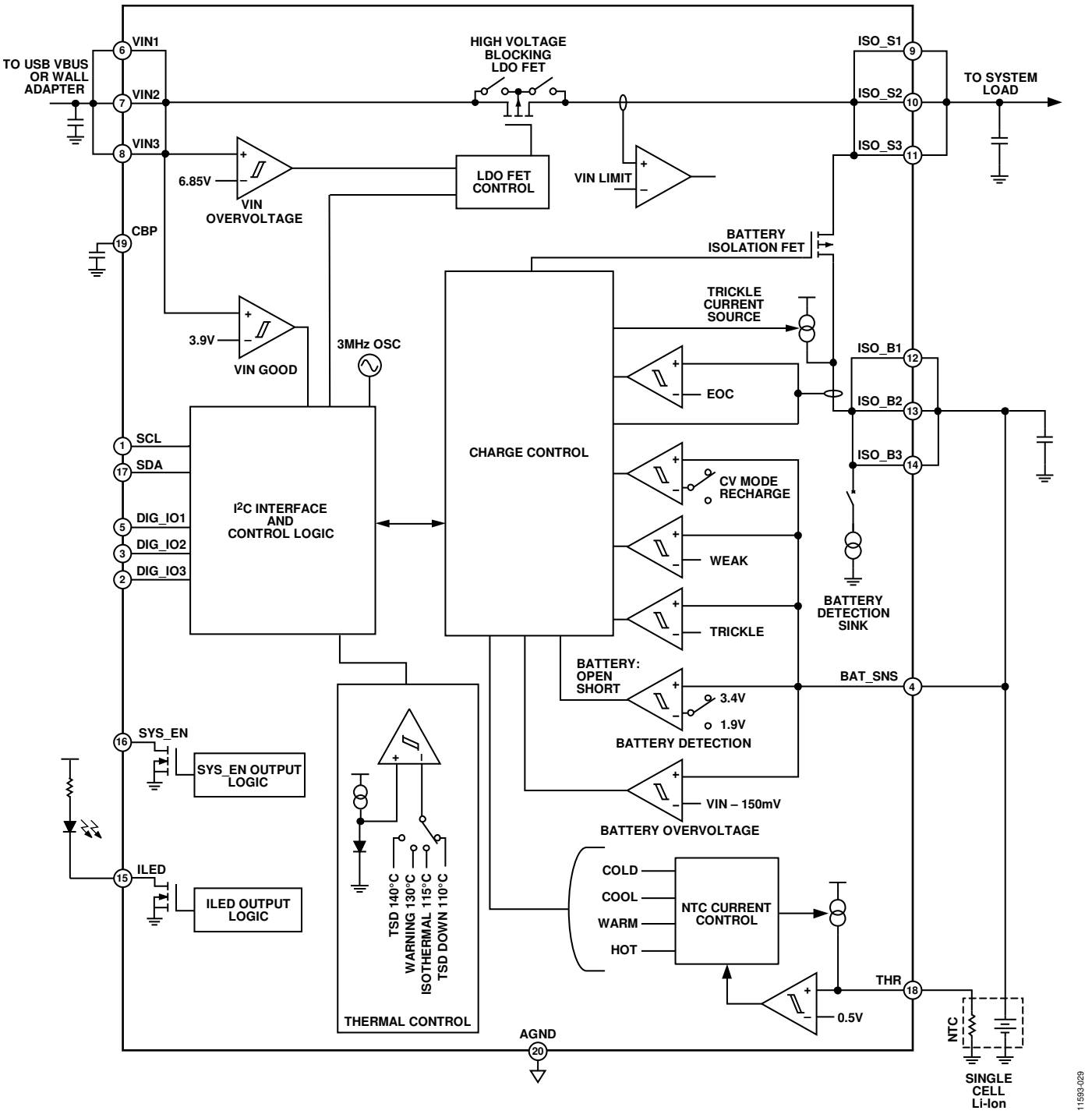

Figure 26. Block Diagram

The ADP5063 includes a number of significant features to optimize charging and functionality, including

- Thermal regulation for maximum performance.
- USB host current limits.
- Termination voltage accuracy: ±1.7%.
- Battery thermistor input with automatic charger shutdown in the event that the battery temperature exceeds limits (compliant with the JEITA Li-Ion battery charging temperature specification).
- Three external pins (DIG_IO1, DIG_IO2, and DIG_IO3) that directly control a number of parameters. These pins are factory programmable for maximum flexibility. They can be factory programmed for functions such as
  - Enable/disable charging.
  - Control of the 100 mA or 500 mA input current limit.
  - Control of the 1500 mA input current limit.
  - Control of the battery charge current.
  - An interrupt output pin.

See the Digital Input and Output Options section for details.

CHARGER MODES

Input Current Limit

The VINx input current limit is controlled via the internal I²C ILIM bits. The input current limit can also be controlled via the DIG_IO1 pin (if factory programmed to do so) as outlined in Table 9. Any change from the 100 mA I²C default takes precedence over the pin setting.

Table 9. DIG_IO1 Operation

DIG_IO1	Function
0	100 mA input current limit or I²C programmed value
1	500 mA input current limit or I²C programmed value (or reprogrammed I²C value from 100 mA default)

USB Compatibility

The ADP5063 features an I²C-programmable input current limit to ensure compatibility with the requirements listed in Table 10. The current limit defaults to 100 mA to allow compatibility with a USB host or hub that is not configured.

The I²C register default is 100 mA. An I²C write command to the ILIM bits overrides the DIG_IOx pins, and the I²C register default value can be reprogrammed for alternative requirements.

When the input current-limit feature is used, the available input current may be too low for the charger to meet the programmed charging current, I_{CHG}, thereby reducing the rate of charge and setting the VIN_ILIM flag.

When connecting voltage to VINx without the proper voltage level on the battery side, the high voltage blocking mechanism is in a state wherein it draws a current of <1 mA until V_{VINx} reaches the VIN_OK level.

The ADP5063 charger provides support for the following connections through the single connector VINx pin, as shown in Table 10.

Table 10. Input Current Compatibility with Standard USB Limits

Mode	Standard USB Limit	ADP5063 Function
USB (China Only)	100 mA limit for standard USB host or hub	100 mA input current limit or I²C programmed value
	300 mA limit for Chinese USB specification	300 mA input current limit or I²C programmed value
USB 2.0	100 mA limit for standard USB host or hub	100 mA input current limit or I²C programmed value
	500 mA limit for standard USB host or hub	500 mA input current limit or I²C programmed value
USB 3.0	150 mA limit for superspeed USB 3.0 host or hub	150 mA input current limit or I²C programmed value
	900 mA limit for superspeed, high speed USB host or hub charger	900 mA input current limit or I²C programmed value
Dedicated Charger	1500 mA limit for dedicated charger or low/full speed USB host or hub charger	1500 mA input current limit or I²C programmed value

Trickle Charge Mode

A deeply discharged Li-Ion cell can exhibit a very low cell voltage, making it unsafe to charge the cell at high current rates. The ADP5063 charger uses a trickle charge mode to reset the battery pack protection circuit and lift the cell voltage to a safe level for fast charging. A cell with a voltage below V_{TRK_DEAD} is charged with the trickle mode current, I_{TRK_DEAD}. During trickle charging mode, the CHARGER_STATUS[2:0] bits are set.

During trickle charging, the ISO_Sx node is regulated to V_{ISO_STRK} by the LDO and the battery isolation FET is off, which means that the battery is isolated from the system power supply.

Trickle Charge Mode Timer

The duration of trickle charge mode is monitored to ensure that the battery is revived from its deeply discharged state. If trickle charge mode runs for longer than 60 minutes without the cell voltage reaching V_{TRK_DEAD}, a fault condition is assumed and charging stops. The fault condition is asserted on the CHARGER_STATUS[2:0] bits, allowing the user to initiate the fault recovery procedure specified in the Fault Recovery section.

Weak Charge Mode (Constant Current)

When the battery voltage exceeds V_{TRK_DEAD} but is less than V_{WEAK}, the charger switches to intermediate charge mode.

During the weak charge mode, the battery voltage is too low to allow the full system to power up. Because of the low battery level, the USB transceiver cannot be powered and, therefore, cannot enumerate for more current from a USB host. Consequently, the USB limit remains at 100 mA.

The system microcontroller may or may not be powered by the charger output voltage (V_{ISO_SFC}), depending upon the amount of current that the microcontroller and/or the system architecture requires. When the ISO_Sx pins power the microcontroller, the battery charge current (I_{CHG_WEAK}) cannot be increased above 20 mA to ensure microcontroller operation (if doing so), nor can I_{CHG_WEAK} be increased above the 100 mA USB limit. Therefore, set the battery charging current as follows:

- Set the default 20 mA via the linear trickle charger branch (to ensure that the microprocessor remains alive if powered by the main charger output, ISO_Sx). Any residual current on the main charger output, ISO_Sx, is used to charge the battery.
- During weak current mode, other features may prevent the weak charging current from reaching its full programmed value. Isothermal charging mode or input current limiting for USB compatibility can affect the programmed weak charging current value under certain operating conditions. During weak charging, the ISO_Sx node is regulated to V_{ISO_SFC} by the battery isolation FET.

Fast Charge Mode (Constant Current)

When the battery voltage exceeds V_{TRK_DEAD} and V_{WEAK}, the charger switches to fast charge mode, charging the battery with the constant current, I_{CHG}. During fast charge mode (constant current), the CHARGER_STATUS[2:0] bits are set to 010.

During constant current mode, other features may prevent the current, I_{CHG}, from reaching its full programmed value. Isothermal charging mode or input current limiting for USB compatibility can affect the value of I_{CHG} under certain operating conditions. The voltage on ISO_Sx is regulated to stay at V_{ISO_SFC} by the battery isolation FET when $V_{ISO\_Bx} < V_{ISO\_SFC}$.

Fast Charge Mode (Constant Voltage)

As the battery charges, its voltage rises and approaches the termination voltage, V_{TRM}. The ADP5063 charger monitors the voltage on the BAT_SNS pin to determine when charging should end. However, the internal ESR of the battery pack combined with the printed circuit board (PCB) and other parasitic series resistances creates a voltage drop between the sense point at the BAT_SNS pin and the cell terminal. To compensate for this and to ensure a fully charged cell, the ADP5063 enters a constant voltage charging mode when the termination voltage is detected on the BAT_SNS pin. The ADP5063 reduces charge current gradually as the cell continues to charge, maintaining a voltage of V_{TRM} on the BAT_SNS pin. During fast charge mode (constant voltage), the CHARGER_ STATUS bits are set to 011.

Fast Charge Mode Timer

The duration of fast charge mode is monitored to ensure that the battery is charging correctly. If the fast charge mode runs for longer than t_{CHG} without the voltage at the BAT_SNS pin reaching V_{TRM}, a fault condition is assumed and charging stops. The fault condition is asserted on the CHARGER_STATUS[2:0] bits, allowing the user to initiate the fault recovery procedure as specified in the Fault Recovery section.

If the fast charge mode runs for longer than t_{CHG}, and V_{TRM} has been reached on the BAT_SNS pin but the charge current has not yet fallen below I_{END}, charging stops. No fault condition is asserted in this circumstance, and charging resumes as normal if the recharge threshold is breached.

Watchdog Timer

The ADP5063 charger features a programmable watchdog timer function to ensure that charging is under the control of the processor. The watchdog timer starts running when the ADP5063 charger determines that the processor should be operational, that is, when the processor sets the RESET_WD bit for the first time or when the battery voltage is greater than the weak battery threshold, V_{WEAK}. When the watchdog timer has been triggered, it must be reset regularly within the watchdog timer period, t_{WD}.

While in charger mode, if the watchdog timer expires without being reset, the ADP5063 charger assumes that there is a software problem and triggers the safety timer, t_{SAFE}. For more information see the Safety Timer section.

Safety Timer

While in charger mode, if the watchdog timer expires, the ADP5063 charger initiates the safety timer, t_{SAFE} (see the Watchdog Timer section). If the processor has programmed charging parameters by the time the charger initiates the safety timer, I_{LIM} is set to the default value. Charging continues for a period of t_{SAFE}, and then the charger switches off and sets the CHARGER_STATUS[2:0] bits.

Charge Complete

The ADP5063 charger monitors the charging current while in fast charge constant voltage mode. If the current falls below I_{END} and remains below I_{END} for t_{END}, charging stops and the CHDONE flag is set. If the charging current falls below I_{END} for less than t_{END} and then rises above I_{END} again, the t_{END} timer resets.

Recharge

After the detection of charge complete and the cessation of charging, the ADP5063 charger monitors the BAT_SNS pin as the battery discharges through normal use. If the BAT_SNS pin voltage falls to V_{RCH}, the charger reactivates charging. Under most circumstances, triggering the recharge threshold results in the charger starting directly in fast charge constant voltage mode.

The recharge function can be disabled in the I²C interface, but a status bit (Register Address 0x0C, Bit 3) informs the system that a recharge cycle is required.

IC Enable/Disable

The ADP5063 IC can be disabled by the DIG_IO2 digital input pin (if factory programmed to do so) or by the I²C registers. All internal control circuits are disabled when the IC is disabled. Disabling the IC1 option can also control the states of the LDO FET and the battery isolation FET.

It is critical to note that during the disable IC1 mode, a high voltage at VINx passes to the internal supply voltage because all of the internal control circuits are disabled. The VINx supply voltage must fulfill the following condition:

$$V_{ISO\_Bx} < VINx < 5.5\ V$$

Battery Charging Enable/Disable

The ADP5063 charging function can be disabled by setting the I²C EN_CHG bit to low. The LDO to the system still operates under this circumstance and can be set in I²C to the default or I²C programmed system voltage from 4.3 V to 5.0 V (see Table 26 for details).

The ADP5063 charging function can also be controlled via one of the external DIG_IOx pins (if factory programmed to do so). Any change in the I²C EN_CHG bit takes precedence over the pin setting.

Battery Voltage Limit to Prevent Charging

The battery monitor of the ADP5063 charger can be configured to monitor battery voltage and prevent charging when the battery voltage is higher than V_{CHG_VLIM} (typically 3.2 V) during charging start-up (enabled by EN_CHG or DIG_IO3). This function can prevent unnecessary charging of a half discharged battery and, as such, can extend the lifetime of the Li-Ion battery cell. Charging starts automatically when the battery voltage drops below V_{CHG_VLIM} and continues through full charge cycle until the battery voltage reaches V_{TRM} (typically 3.6 V).

By default, the charging voltage limit is disabled, and it can be enabled via I²C Register Address 0x08, Bit 5 (EN_CHG_VLIM).

SYS_EN Output

The ADP5063 features a SYS_EN open-drain FET to enable the system until the battery is at the minimum required level for guaranteed system startup. When there are minimum battery voltage and/or minimum battery charge level requirements, the operation of SYS_EN can be set by I²C programming. The SYS_EN operation can be factory programmed to four different operating conditions, as described in Table 11.

Table 11. SYS_EN Mode Descriptions

SYS_EN Mode Selection	Description
00	SYS_EN is activated when LDO is active and system voltage is available.
01	SYS_EN is activated by the ISO_Bx voltage, the battery charging mode.
10	SYS_EN is activated and the isolation FET is disabled when the battery drops below V_{WEAK}. This option is active when VINx = 0 V and the battery monitor is activated from Register 0x07, Bit 5 (EN_BMON).
11	SYS_EN is active in LDO mode when the charger is disabled. SYS_EN is active in charging mode when $V_{ISO\_Bx} \geq V_{WEAK}$.

Indicator LED Output (ILED)

The ILED is an open-drain output for an indicator LED connection. Optionally, the ILED output can be used as a status output for a microcontroller. Indicator LED modes are listed in Table 12.

Table 12. Indicator LED Operation Modes

ADP5063 Mode	ILED Mode	On/Off Time
IC Off	Off	
LDO Mode Off	Off	
LDO Mode On	Off	
Charge Mode	Continuously on	
Timer Error (t_{TRK}, t_{CHG}, t_{SAFE})	Blinking	167 ms/833 ms
Overtemperature (T_{SD})	Blinking	1 sec/1 sec

THERMAL MANAGEMENT

Isothermal Charging

The ADP5063 includes a thermal feedback loop that limits the charge current when the die temperature exceeds T_{LIM} (typically 115°C). As the on-chip power dissipation and die temperature increase, the charge current is automatically reduced to maintain the die temperature within the recommended range. As the die temperature decreases due to lower on-chip power dissipation or ambient temperature, the charge current returns to the programmed level. During isothermal charging, the THERM_LIM I^2C flag is set to high.

This thermal feedback control loop allows the user to set the programmed charge current based on typical rather than worst-case conditions.

The ADP5063 does not include a thermal feedback loop to limit ISO_Sx load current in LDO mode. If the power dissipated on chip during LDO mode causes the die temperature to exceed 130°C, an interrupt is generated. If the die temperature continues to rise beyond 140°C, the device enters thermal shutdown.

Thermal Shutdown and Thermal Early Warning

The ADP5063 charger features a thermal shutdown threshold detector. If the die temperature exceeds T_{SD}, the ADP5063 charger is disabled, and the TSD 140°C bit is set. The ADP5063 charger can be reenabled when the die temperature drops below the T_{SD} falling limit and the TSD 140°C bit is reset. To reset the TSD 140°C bit, write to the I^2C fault register, Register Address 0x0D (Bit 0) or cycle the power.

Before the die temperature reaches T_{SD}, the early warning bit is set if T_{SDL} is exceeded. This allows the system to accommodate power consumption before thermal shutdown occurs.

Fault Recovery

Before performing the following operation, it is important to ensure that the cause of the fault has been rectified.

To recover from a charger fault (when CHARGER_STATUS[2:0] = 110), cycle the power on VINx or write high to reset the I^2C fault bits in the fault register (Register Address 0x0D).

BATTERY ISOLATION FET

The ADP5063 charger features an integrated battery isolation FET for power path control. The battery isolation FET isolates a deeply discharged Li-Ion cell from the system power supply in both trickle and fast charge modes, thereby allowing the system to be powered at all times.

When VINx is below $V_{VIN\_OK\_RISE}$, the battery isolation FET is in full conducting mode.

The battery isolation FET is off during trickle charge mode. When the battery voltage exceeds V_{TRK_DEAD}, the battery isolation FET switches to the system voltage regulation mode. During system voltage regulation mode, the battery isolation FET maintains the V_{ISO_SFC} voltage on the ISO_Sx pins. When the battery voltage exceeds V_{ISO_SFG}, the battery isolation FET is in full conducting mode.

The battery isolation FET supplements the battery to support high current functions on the system power supply. When the voltage on ISO_Sx drops below V_{ISO_Bx}, the battery isolation FET enters into full conducting mode. When voltage on ISO_Sx rises above V_{ISO_Bx}, the isolation FET enters regulating mode or full conduction mode, depending on the Li-Ion cell voltage and the linear charger mode.

BATTERY DETECTION

Battery Voltage Level Detection

The ADP5063 charger features a battery detection mechanism to detect an absent battery. The charger actively sinks and sources current into the ISO_Bx node, and voltage vs. time is detected. The sink phase is used to detect a charged battery, whereas the source phase is used to detect a discharged battery.

The sink phase (see Figure 27) sinks I_{SINK} current from the ISO_Bx pins for a time period, t_{BATOK}. If ISO_Bx is below V_{BATL} when the t_{BATOK} timer expires, the charger assumes that no battery is present and starts the source phase. If the ISO_Bx pin exceeds the V_{BATL} voltage when the t_{BATOK} timer expires, the charger assumes that the battery is present and begins a new charge cycle.

The source phase sources I_{SOURCE} current to the ISO_Bx pins for a time period, t_{BATOK}. If ISO_Bx exceeds V_{BATH} before the t_{BATOK} timer expires, the charger assumes that no battery is present. If the ISO_Bx pin does not exceed the V_{BATH} voltage when the t_{BATOK} timer expires, the charger assumes that a battery is present and begins a new charge cycle.

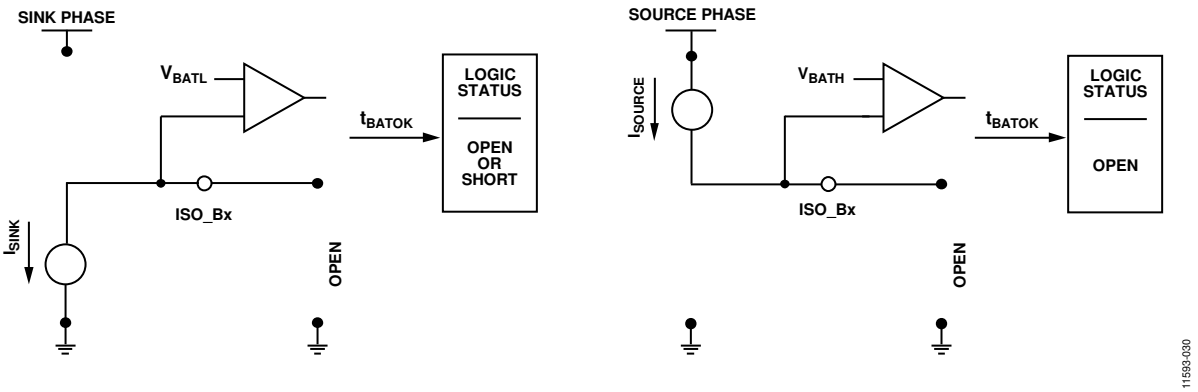

Figure 27. Sink Phase

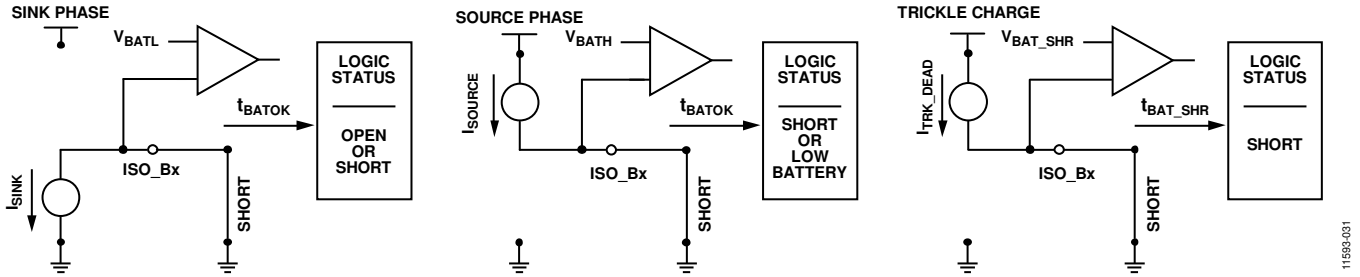

Figure 28. Trickle Charge

Battery (ISO_Bx) Short Detection

A battery short occurs under a damaged battery condition or when the battery protection circuitry is enabled.

On commencing trickle charging, the ADP5063 charger monitors the battery voltage. If this battery voltage does not exceed V_{BAT_SHR} within the specified timeout period, t_{BAT_SHR}, a fault is declared and the charger is stopped by turning the battery isolation FET off, but the system voltage is maintained at V_{ISO_STRK} by the linear regulator.

After source phase, if the ISO_Bx or BAT_SNS level remains below V_{BATH}, either the battery voltage is low or the battery node is shorted. Because the battery voltage is low, trickle charging mode is initiated (see Figure 28). If the BAT_SNS level remains below V_{BAT_SHR} after t_{BAT_SHR} has elapsed, the ADP5063 assumes that the battery node is shorted.

The trickle charge branch is active during the battery short scenario, and trickle charge current to the battery is maintained until the 60-minute trickle charge mode timer expires.

BATTERY PACK TEMPERATURE SENSING

Battery Thermistor Input

The ADP5063 charger features battery pack temperature sensing that precludes charging when the battery pack temperature is outside the specified range. The THR pin provides an on and off switching current source that must be connected directly to the battery pack thermistor terminal. The activation interval of the THR current source is 167 ms.

The battery pack temperature sensing can be controlled by I²C,using the conditions shown in Table 13. Note that the I²C register default setting for EN_THR (Register Address 0x07) is 0 = temperature sensing off.

Table 13. THR Input Function

Conditions		
VINx	**V_{ISO_Bx}**	**THR Function**
Open or V_{IN} = 0 V to 4.0 V	<2.5 V	Off
Open or V_{IN} = 0 V to 4.0 V	>2.5 V	Off, controlled by I²C
4 V to 6.7 V	Don't care	Always on

If the battery pack thermistor is not connected directly to the THR pin, a 10 kΩ (tolerance ±20%) dummy resistor must be connected between the THR input and AGND. Leaving the THR pin open results in a false detection of the battery temperature being <0°C, and charging is disabled.

The ADP5063 charger monitors the voltage in the THR pin and suspends charging when the current is outside the range of less than 0°C or greater than 60°C.

The ADP5063 charger is designed for use with an NTC thermistor in the battery pack with a nominal room temperature value of either 10 kΩ at 25°C or 100 kΩ at 25°C, which is selected by factory programming.

The ADP5063 charger is designed for use with an NTC thermistor in the battery pack with a temperature coefficient curve (beta). Factory programming supports eight beta values covering a range from 3150 to 4400 (see Table 43).

JEITA Li-Ion Battery Temperature Charging Specification

The ADP5063 is compliant with the JEITA1 and JEITA2 Li-Ion battery charging temperature specifications as outlined in Table 14 and Table 16, respectively.

JEITA function can be enabled via the I²C interface and, optionally, the JEITA1 or JEITA2 function can be selected via the I²C interface. Alternatively, the JEITA1 or JEITA2 function can be enabled as the default setting by factory programming.

When the ADP5063 identifies a hot or cold battery condition, the ADP5063 takes the following actions:

- Stops charging the battery.
- Connects or enables the battery isolation FET such that the ADP5063 continues in LDO mode.

Table 14. JEITA1 Specifications

Parameter	Symbol	Conditions	Min	Max	Unit
JEITA1 Cold Temperature Limits	I_{JEITA_COLD}	No battery charging occurs.		0	°C
JEITA1 Cool Temperature Limits	I_{JEITA_COOL}	Battery charging occurs at approximately 50% of the programmed level. See Table 15 for specific charging current reduction levels.	0	10	°C
JEITA1 Typical Temperature Limits	I_{JEITA_TYP}	Normal battery charging occurs at the default/programmed levels.	10	45	°C
JEITA1 Warm Temperature Limits	I_{JEITA_WARM}	Battery termination voltage (V_{TRM}) is reduced by 100 mV from the programmed value.	45	60	°C
JEITA1 Hot Temperature Limits	I_{JEITA_HOT}	No battery charging occurs.	60		°C

Table 15. JEITA1 Reduced Charge Current Levels, Battery Cool Temperature

ICHG[4:0] (Default)	ICHG JEITA1
00000 = 50 mA	50 mA
00001 = 100 mA	50 mA
00010 = 150 mA	50 mA
00011 = 200 mA	100 mA
00100 = 250 mA	100 mA
00101 = 300 mA	150 mA
00110 = 350 mA	150 mA
00111 = 400 mA	200 mA
01000 = 450 mA	200 mA
01001 = 500 mA	250 mA
01010 = 550 mA	250 mA
01011 = 600 mA	300 mA
01100 = 650 mA	300 mA
01101 = 700 mA	350 mA
01110 = 750 mA	350 mA
01111 = 800 mA	400 mA
10000 = 850 mA	400 mA
10001 = 900 mA	450 mA
10010 = 950 mA	450 mA
10011 = 1000 mA	500 mA
10100 = 1050 mA	500 mA
10101 = 1100 mA	550 mA
10110 = 1200 mA	600 mA
10111 to 11111 = 1300 mA	650 mA

Table 16. JEITA2 Specifications

Parameter	Symbol	Conditions	Min	Max	Unit
JEITA2 Cold Temperature Limits	I_{JEITA_COLD}	No battery charging occurs.		0	°C
JEITA2 Cool Temperature Limits	I_{JEITA_COOL}	Battery termination voltage (V_{TRM}) is reduced by 100 mV from the programmed value.	0	10	°C
JEITA2 Typical Temperature Limits	I_{JEITA_TYP}	Normal battery charging occurs at the default/programmed levels.	10	45	°C
JEITA2 Warm Temperature Limits	I_{JEITA_WARM}	Battery termination voltage (V_{TRM}) is reduced by 100 mV from the programmed value.	45	60	°C
JEITA2 Hot Temperature Limits	I_{JEITA_HOT}	No battery charging occurs.	60		°C

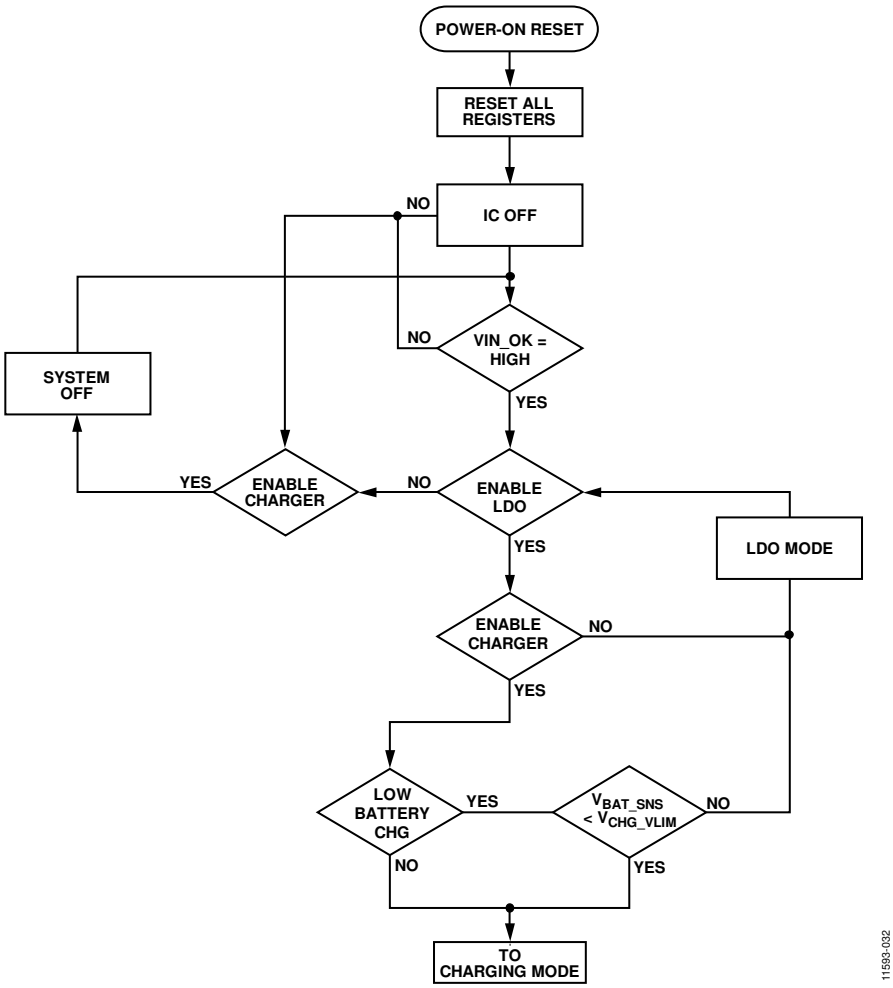

Figure 29. Simplified Battery and VINx Connect Flowchart