Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Fast Charge Battery Manager with Power Path and USB Compatibility

Data Sheet

ADP5065

FEATURES

- 3 MHz switch mode charger
- 1.25 A charge current from dedicated charger
- Up to 680 mA charging current from 500 mA USB host
- Operating input voltage from 4.0 V up to 5.5 V
- Tolerant input voltage −0.5 V to +20 V (USB VBUS)
- Dead battery isolation FET between battery and charger output
- Battery thermistor input with automatic charger shutdown for when battery temperature exceeds limits
- Compliant with the JEITA Li-Ion battery charging temperature specification
- SYS_EN_OK flag to hold off system turn-on until battery is at minimum required level for guaranteed system startup due to minimum battery voltage and/or minimum battery charge level requirements
- EOC programming with C/20, C/10 and specific current level selection

FUNCTIONAL BLOCK DIAGRAM

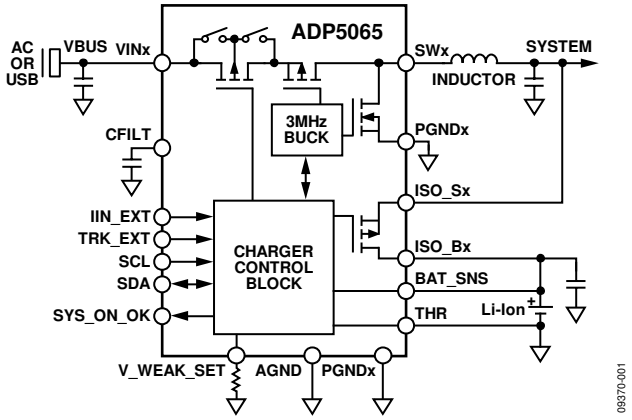

Figure 1.

APPLICATIONS

- Digital still cameras
- Digital video cameras
- Single cell Li-Ion portable equipment
- PDA, audio, GPS devices
- Mobile phones

GENERAL DESCRIPTION

The ADP5065 charger is fully compliant with the USB 2.0, USB 3.0, and USB Battery Charging Specification 1.1 and enables charging via the mini USB VBUS pin from a wall charger, car charger, or USB host port.

The ADP5065 operates from a 4 V to 5.5 V input voltage range but is tolerant of voltages of up to 20 V. This alleviates the concerns about the USB bus spiking during disconnect or connect scenarios.

The ADP5065 also features an internal FET between the dc-to-dc charger output and the battery. This permits battery isolation and, hence, system powering under a dead battery or no battery scenario, which allows for immediate system function on connection to a USB power supply.

Based on the type of USB source, which is detected by an external USB detection chip, the ADP5065 can be set to apply the correct current limit for optimal charging and USB compliance.

The ADP5065 comes in a very small and low profile 20-lead WLCSP (0.5 mm pitch spacing) package.

The overall solution requires only five small, low profile external components consisting of four ceramic capacitors (one of which is the battery filter capacitor), one multilayer inductor. In addition to these components, there is one optional dead battery situation default setting resistor. This configuration enables a very small PCB area to provide an integrated and performance enhancing solution to USB battery charging and power rail provision.

Rev. D
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

ADP5065* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADP5065 Evaluation Board

DOCUMENTATION

Data Sheet

- ADP5065: Fast Charge Battery Manager with Power Path and USB Compatibility Data Sheet

User Guides

- UG-415: ADP5065 Evaluation Board Manual

REFERENCE DESIGNS

- CN0352

DESIGN RESOURCES

- ADP5065 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADP5065 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

2/13—Rev. C to Rev. D

Changed Maximum Duty Cycle from 93% to 96% ... 3
Changed Bit[3:0] Default Value from 0100 to 0101, Table 16 ... 26
Changed Bit 5 and Bit 2 Default Values from 1 to 0, Table 21 ... 29
Deleted Disconnecting Supply Voltage at VINx Section ... 34

9/12—Rev. B to Rev. C

Changed Bit[3:0] Default Value from 0011 to 0100, Table 16 ... 27
Added Disconnecting Supply Voltage at VINx Section ... 34

4/12—Rev. A to Rev. B

Changes to Features Section and General Description Section ... 1
Changes to Table 1 ... 3
Changes to VIN1, VIN2 to PGND1, PGND2 Parameter, Table 4 ... 7
Changes to Introduction Section ... 15

11/11—Rev. 0 to Rev. A

Changes to Figure 10 ... 10
Changes to Figure 17 and Figure 18 ... 11
Changes to Figure 41 ... 36

10/11—Revision 0: Initial Version

SPECIFICATIONS

$-40°C < T_J < 125°C$, $V_{IN} = 5.0$ V, $V_{ISO\_S} > 3.0$ V, $V_{HOT} < V_{THR} < V_{COLD}$, $V_{BAT\_SNS} = 3.6$ V, $C_{VIN} = 2.2$ µF, $C_{DCDC} = 22$ µF, $C_{BAT} = 22$ µF, $C_{CFILT} = 4.7$ µF, $L_{OUT} = 1$ µH, all registers are at default values, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
GENERAL PARAMETERS						
Undervoltage Lockout	V_{UVLO}	2.25	2.35	2.45	V	Falling threshold, higher of V_{CFILT} and V_{BAT_SNS}
		50	100	150	mV	Hysteresis, higher of V_{CFILT} and V_{BAT_SNS} rising
Total Input Current	I_{VIN}	86	92	100	mA	Nominal USB initialized current level[1]
				150	mA	USB super speed
				300	mA	USB enumerated current level (specification for China)
		460	475	500	mA	USB enumerated current level
				900	mA	Dedicated charger input
				1500	mA	Dedicated wall charger
Current Consumption						
VINx	I_{QVIN}		15		mA	No battery, no ISO_Sx load, switching 3 MHz
Battery, Standby	I_{QISO_B}		0.22	2	µA	$T_J = -40°C$ to $+85°C$
SWxPin Leakage Current	$-I_{OUT}$			2	µA	$V_{VIN} = 0$ V, $T_J = -40°C$ to $+85°C$
CHARGING PARAMETERS						
Fast Charge Current, CC Mode (Battery Voltage > V_{TRK_DEAD})	I_{CHG}		1250		mA	$V_{CFILT} > V_{BAT\_SNS} + V_{CCDROP}$[1, 2]
Fast Charge Current Accuracy	$I_{CHG(TOL)}$	−7		+5	%	$T_j = 25°C$, $I_{CHG} = 550$ mA to 1250 mA
		−8		+8	%	$I_{CHG} = 550$ mA to 1150 mA, fast charge current accuracy is guaranteed at temperatures from $T_j = 0°C$ to isothermal regulation limit (typically $T_j = 115°C$)
		−17		+8	%	$I_{CHG} = 1250$ mA, $T_j = 0°C$ to isothermal regulation limit (typically $T_j = 115°C$)
Trickle Charge Current[1, 2]	I_{TRK_DEAD}	16	20	25	mA	
Weak Charge Current	I_{CHG_WEAK}		$I_{CHG} + 20$		mA	When $V_{TRK\_DEAD} < V_{BAT\_SNS} < V_{WEAK}$[1, 3]
Dead Battery						
Trickle to Weak Charge Threshold	V_{TRK_DEAD}	2.4	2.5	2.6	V	On BAT_SNS[1]
Trickle to Weak Charge Threshold Hysteresis	ΔV_{TRK_DEAD}		90		mV	
Weak Battery						
Weak to Fast Charge Threshold	V_{WEAK}	2.9	3.0	3.1	V	On BAT_SNS[1, 3]
Weak Battery Threshold Hysteresis	ΔV_{WEAK}		90		mV	
Battery Termination Voltage	V_{TRM}	4.158	4.200	4.242	V	On BAT_SNS, $T_J = 0°C$ to $115°C$[1]
Battery Termination Voltage Accuracy		−0.3		+0.3	%	On BAT_SNS, $T_J = 25°C$, $I_{END} = 52.5$ mA[1]
Battery Overvoltage Threshold	V_{BATOV}		$V_{CFILT} - 0.15$		V	Relative to CFILT voltage, BAT_SNS rising
Charge Complete Current	I_{END}		52.5		mA	$V_{BAT\_SNS} = V_{TRM}$[1]
Charge Complete Current Threshold Accuracy		−25		+25	%	$I_{END} = 72.5$ mA or 92.5 mA, $T_J = 0°C$ to $115°C$
		−35		+35	%	$I_{END} = 52.5$ mA, $T_J = 0°C$ to $115°C$
		−55		+55	%	$I_{END} = 32.5$ mA, $T_J = 0°C$ to $115°C$
Recharge Voltage Differential	V_{RCH}		260		mV	Relative to V_{TRM}, BAT_SNS falling[1]
Battery Node Short Threshold Voltage[1]	V_{BAT_SHR}	2.3	2.4	2.5	V	
CHARGER DC-to-DC CONVERTER						
Switching Frequency	f_{SWCHG}	2.8	3	3.2	MHz	
Maximum Duty Cycle	D_{MAX}		96		%	
Peak Inductor Current	$I_{L(PK)}$	1500	1750	2000	mA	
Regulated System Voltage	V_{ISO_STRK}	3.21	3.3	3.39	V	$V_{BAT\_SNS} < V_{TRK\_DEAD}$, trickle charging mode
Load Regulation			5		mV/A	
DC-to-DC Power						
PMOS On Resistance	$R_{DS(ON)P}$		220	285	mΩ	
NMOS On Resistance	$R_{DS(ON)N}$		160	210	mΩ	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
BATTERY ISOLATION FET						
Bump to Bump Resistance Between ISO_Bx and ISO_Sx Bumps	$R_{DSONISO}$		76	115	mΩ	Includes bump resistances and battery isolation PMOS on resistance; on battery supplement mode, V_{IN} = 0 V, V_{ISO_B} = 3.6 V, I_{ISO_B} = 500 mA
Regulated System Voltage	V_{ISO_SFC}	3.15	3.3	3.45	V	$V_{TRK\_DEAD} < V_{BAT\_SNS}$, fast charging CC mode
Battery Supplementary Threshold	V_{THISO}	0	5	10	mV	$V_{ISO\_S[1:2]} < V_{ISO\_B[1:2]}$, V_{SYS} rising
HIGH VOLTAGE BLOCKING FET						
VINx Input						
High Voltage Blocking FET On Resistance	R_{DSONHV}		340	455	mΩ	I_{IN} = 500 mA
Current, Suspend Mode	$I_{SUSPEND}$		1.3	2.5	mA	EN_CHG = low
Input Voltage						
Good Threshold						
Rising	$V_{VIN\_OK\_RISE}$	3.78	3.9	4.0	V	
Falling	$V_{VIN\_OK\_FALL}$		3.6	3.67	V	
Overvoltage Threshold	V_{VIN_OV}	5.35	5.42	5.5	V	
Overvoltage Threshold Hysteresis			75		mV	
VINx Transition Timing						
Minimum Rise Time for VINx from 5 V to 20 V	t_{VIN_RISE}	10			µs	
Minimum Fall Time for VINx from 4 V to 0 V	t_{VIN_FALL}	10			µs	
THERMAL CONTROL						
Isothermal Charging Temperature	T_{LIM}		115		°C	
Thermal Early Warning Temperature	T_{SDL}		130		°C	
Thermal Shutdown Temperature	T_{SD}		140		°C	T_J rising
			110		°C	T_J falling
THERMISTOR CONTROL						
Thermistor Current						
10,000 NTC	I_{NTC_10k}			400	µA	
100,000 NTC	I_{NTC_100k}			40	µA	
Thermistor Capacitance	C_{NTC}			100	pF	
Cold Temperature Threshold	T_{NTC_COLD}		0		°C	No battery charging occurs
Resistance Thresholds						
Cool to Cold Resistance	R_{COLD_FALL}	24,050	27,300	30,600	Ω	
Cold to Cool Resistance	R_{COLD_RISE}	23,100	26,200	29,400	Ω	
Hot Temperature Threshold	T_{NTC_HOT}		60		°C	No battery charging occurs
Resistance Thresholds						
Hot to Typical Resistance	R_{HOT_FALL}	2990	3310	3640	Ω	
Typical to Hot Resistance	R_{HOT_RISE}	2730	3030	3330	Ω	
JEITA SPECIFICATION[4]						
JEITA Cold Temperature	T_{JEITA_COLD}		0		°C	No battery charging occurs
Resistance Thresholds						
Cool to Cold Resistance	R_{COLD_FALL}	24,050	27,300	30,600	Ω	
Cold to Cool Resistance	R_{COLD_RISE}	23,100	26,200	29,400	Ω	
JEITA Cool Temperature	T_{JEITA_COOL}		10		°C	Battery charging occurs at 50% of programmed level
Resistance Thresholds						
Typical to Cool Resistance	R_{TYP_FALL}	15,200	17,800	20,400	Ω	
Cool to Typical Resistance	R_{TYP_RISE}	14,500	17,000	19,500	Ω	
JEITA Typical Temperature	T_{JEITA_TYP}				°C	Normal battery charging occurs at default/programmed levels
Resistance Thresholds						
Warm to Typical Resistance	R_{WARM_FALL}	4710	5400	6100	Ω	
Typical to Warm Resistance	R_{WARM_RISE}	4320	4950	5590	Ω	
JEITA Warm Temperature	T_{JEITA_WARM}		45		°C	Battery termination voltage (V_{TRM}) is reduced by 100 mV
Resistance Thresholds						
Hot to Warm Resistance	R_{HOT_FALL}	2990	3310	3640	Ω	
Warm to Hot Resistance	R_{HOT_RISE}	2730	3030	3330	Ω	
JEITA Hot Temperature	T_{JEITA_HOT}		60		°C	No battery charging occurs

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
BATTERY DETECTION						
Sink Current	I_{SINK}	13	20	34	mA	
Source Current	I_{SOURCE}	7	10	13	mA	
Battery Threshold						
Low	V_{BATL}	1.8	1.9	2.0	V	
High	V_{BATH}		3.4		V	
No Battery Threshold	V_{NOBAT}		3.3		V	$V_{TRM} \geq 3.7$ V, valid after charge complete (see Figure 38)
			3.0		V	$V_{TRM} < 3.7$ V, valid after charge complete (see Figure 38)
Battery Detection Timer	t_{BATOK}		333		ms	
TIMERS						
Start Charging Delay Timer	t_{START}		1		sec	
Trickle Charge Timer	t_{TRK}		60		min	
Fast Charge Timer	t_{CHG}		600		min	
Charge Complete Timer	t_{END}		7.5		min	$V_{BAT\_SNS} = V_{TRM}$, $I_{CHG} < I_{END}$
Deglitch Timer	t_{DG}		31		ms	Applies to V_{TRK}, V_{RCH}, I_{END}, V_{DEAD}, V_{VIN_OK}
Watchdog Timer[1]	t_{WD}		32		sec	
Safety Timer	t_{SAFE}	36	40	44	min	
Battery Node Short Timer[1]	t_{BAT_SHR}		30		sec	
LOGIC INPUTS						
Maximum Voltage on Digital Inputs	V_{DIN_MAX}			5.5	V	
Maximum Logic Low Input Voltage	V_{IL}			0.5	V	Applies to SCL, SDA, TRK_EXT, IIN_EXT
Minimum Logic High Input Voltage	V_{IH}	1.2			V	Applies to SCL, SDA, TRK_EXT, IIN_EXT
Pull-Down Resistance		215	350	610	kΩ	Applies to TRK_EXT, IIN_EXT

[1] These values are programmable via I²C. Values are given with default register values.
[2] The output current during charging can be limited by I_{BUS} or by the isothermal charging mode.
[3] Programmable via external resistor programming, if required.
[4] JEITA can be enabled or disabled in I²C.

RECOMMENDED INPUT AND OUTPUT CAPACITANCE

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CAPACITANCE					
VINx Capacitance	1.0			µF	Effective capacitance
CFILT Pin Total External Capacitance	2.0	4.7	5.0	µF	Effective capacitance
ISO_Sx Pin Total Capacitance	10		50	µF	Effective capacitance
ISO_Bx Pin Total Capacitance	10			µF	Effective capacitance

I²C-COMPATIBLE INTERFACE TIMING SPECIFICATIONS

Table 3.

Parameter[1]	Symbol	Min	Typ	Max	Unit
I²C-COMPATIBLE INTERFACE[2]					
Capacitive Load, Each Bus Line	C_S			400	pF
SCL Clock Frequency	f_{SCL}			400	kHz
SCL High Time	t_{HIGH}	0.6			µs
SCL Low Time	t_{LOW}	1.3			µs
Data Setup Time	t_{SUDAT}	100			ns
Data Hold Time	t_{HDDAT}	0		0.9	µs
Setup Time for Repeated Start	t_{SUSTA}	0.6			µs
Hold Time for Start/Repeated Start	t_{HDSTA}	0.6			µs
Bus Free Time Between a Stop and a Start Condition	t_{BUF}	1.3			µs
Setup Time for Stop Condition	t_{SUSTO}	0.6			µs
Rise Time of SCL/SDA	t_R	20		300	ns
Fall Time of SCL/SDA	t_F	20		300	ns
Pulse Width of Suppressed Spike	t_{SP}	0		50	ns

[1] Guaranteed by design.
[2] A master device must provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL. See Figure 2, the I²C timing diagram.

Timing Diagram

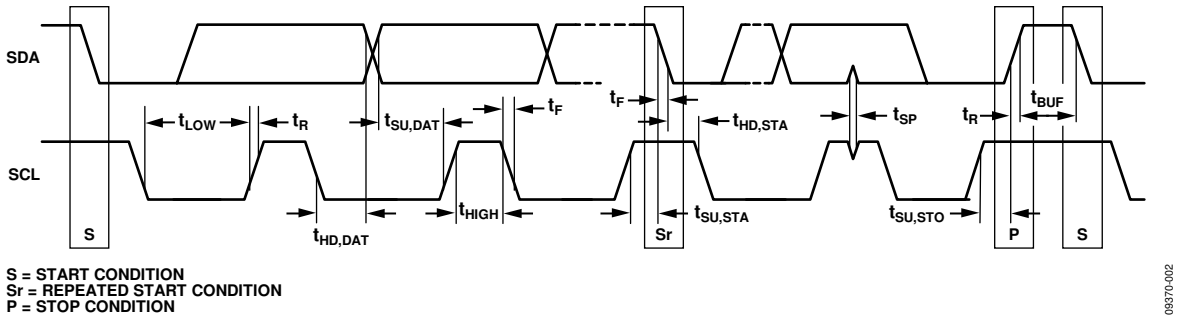

Figure 2. I²C Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VIN1, VIN2 to PGND1, PGND2	−0.5 V to +20 V
All Other Pins to AGND	−0.3 V to +6 V
Continuous Drain Current, Battery Supplementary Mode, from ISO_Bx to ISO_Sx	
$T_J \leq 85°C$	2.2 A
$T_J = 125°C$	1.1 A
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	θ_{JB}	Unit
20-Lead WLCSP[1]	46.8	0.7	9.2	°C/W

[1] 5 × 4 array, 0.5 mm pitch (2.75 mm × 2.08 mm); based on a JEDEC, 2S2P, 4-layer board with 0 m/sec airflow.

Maximum Power Dissipation

The maximum safe power dissipation in the ADP5065 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADP5065. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in the silicon devices that potentially cause failure.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

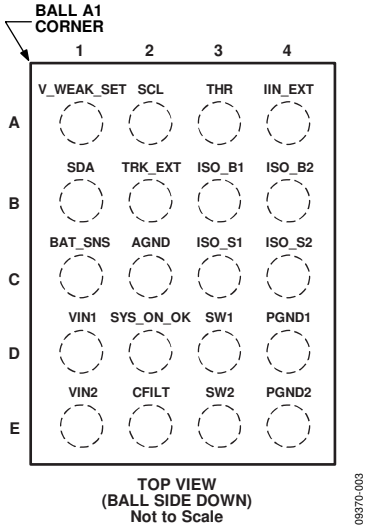

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
D3, E3	SW1, SW2	I/O	DC-to-DC Converter Inductor Connection. These pins are high current outputs when in charging mode.
D1, E1	VIN1, VIN2	I/O	Power Connection to USB VBUS. These pins are high current inputs when in charging mode.
D4, E4	PGND1, PGND2	G	Charger Power Ground. These pins are high current inputs when in charging mode.
C2	AGND	G	Analog Ground.
E2	CFILT	I/O	4.7 µF Filter Capacitor Connection. This pin is a high current input/output when in charging mode.
C3, C4	ISO_S1, ISO_S2	I/O	Charger Supply Side Input to Internal Isolation FET/Battery Current Regulation FET.
B3, B4	ISO_B1, ISO_B2	I/O	Battery Supply Side Input to Internal Isolation FET/Battery Current Regulation FET.
A2	SCL	I	I^2C-Compatible Interface Serial Clock.
B1	SDA	I/O	I^2C-Compatible Interface Serial Data.
A4	IIN_EXT	I	Set Input Current Limit. This pin sets the input current limit directly. When IIN_EXT = low or high-Z, the input limit is 100 mA. When IIN_EXT = high, the input limit is 500 mA.
B2	TRK_EXT	I	Enable Trickle Charge Function. When TRK_EXT = low or high-Z, the trickle charge is enabled. When TRK_EXT = high, the trickle charge is disabled.
A3	THR	I	Battery Pack Thermistor Connection. If not used, connect a dummy 10 kΩ resistor from THR to GND.
C1	BAT_SNS	I	Battery Voltage Sense Pin.
D2	SYS_ON_OK	O	Battery Okay Open-Drain Output Flag. Active low. This pin enables the system when the battery reaches V_{WEAK}.
A1	V_WEAK_SET	I/O	External Resistor Setting Pin for V_WEAK threshold. The use of this pin is optional. When not in use, connect to GND.

[1] I is input, O is output, I/O is input/output, and G is ground.

TYPICAL PERFORMANCE CHARACTERISTICS

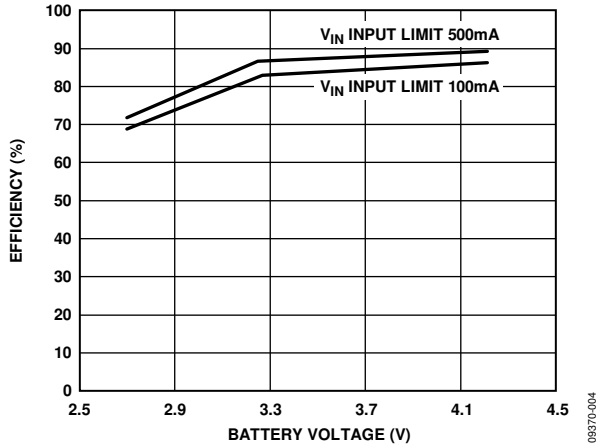

Figure 4. Battery Charger Efficiency vs. Battery Voltage, V_{IN} = 5.0 V

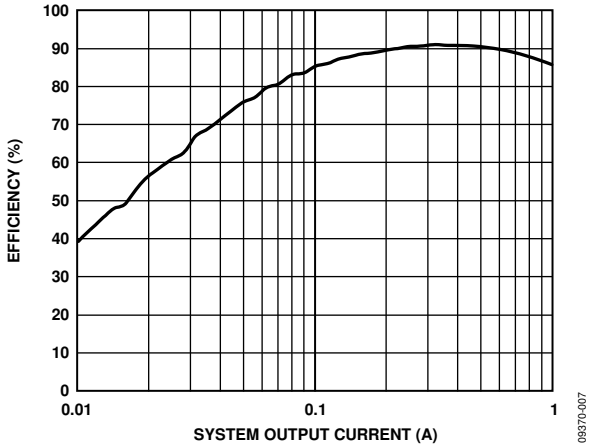

Figure 7. System Voltage Efficiency vs. Output Current, V_{IN} = 5.0 V

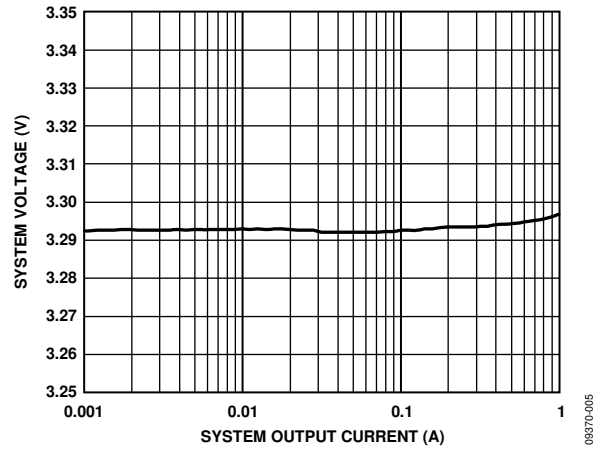

Figure 5. System Voltage Regulation vs. Output Current, V_{IN} = 5.0 V

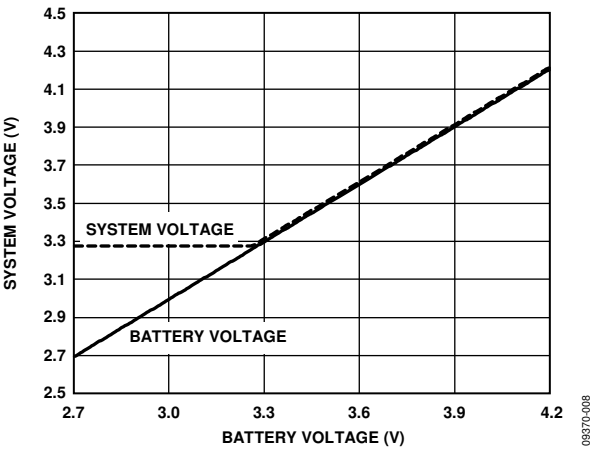

Figure 8. System Voltage vs. Battery Voltage, V_{IN} = 5.0 V, ILIM = 100 mA

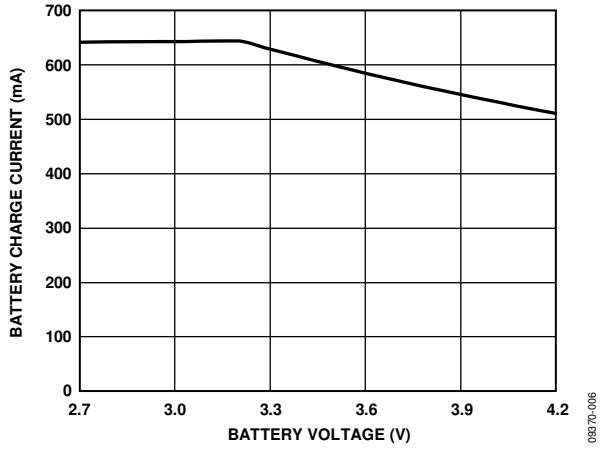

Figure 6. USB Compliant Charge Current vs. Battery Voltage, V_{IN} = 5.0 V, ILIM = 500 mA

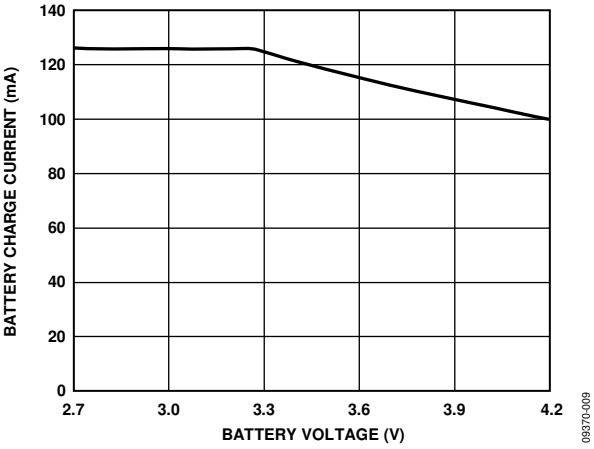

Figure 9. USB Limited Battery Charge Current vs. Battery Voltage, V_{IN} = 5.0 V, ILIM = 100 mA

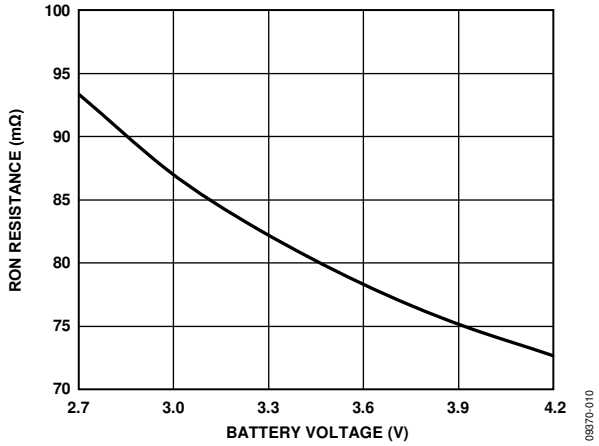

Figure 10. Battery Isolation FET Resistance vs. Battery Voltage, V_{IN} = 5.0 V, Load Current = 1.0 A

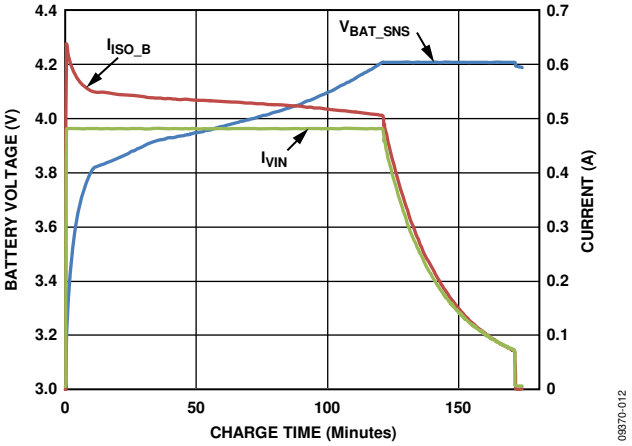

Figure 12. Charge Profile, V_{IN} = 5.0 V, ILIM = 500 mA, Battery Capacity = 1320 mAh

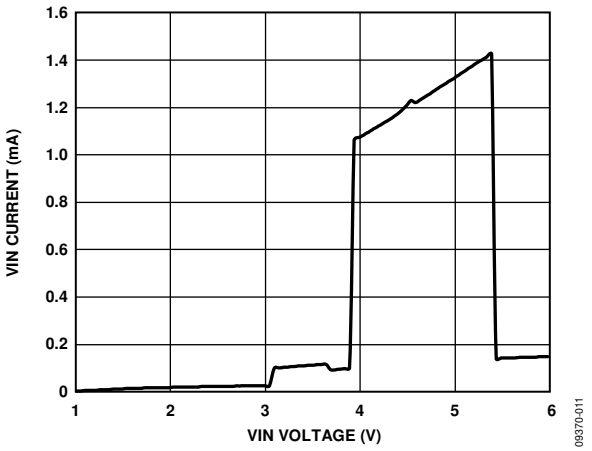

Figure 11. VINx Current vs. VINx Voltage, Suspend Mode (EN_CHG = 0)

TEMPERATURE CHARACTERISTICS

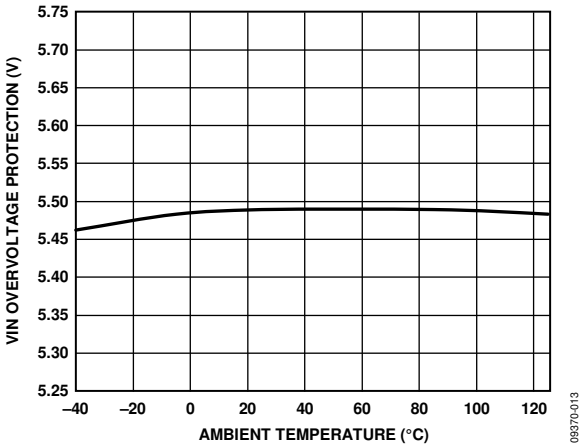

Figure 13. VINx Overvoltage Protection Rising Threshold vs. Ambient Temperature

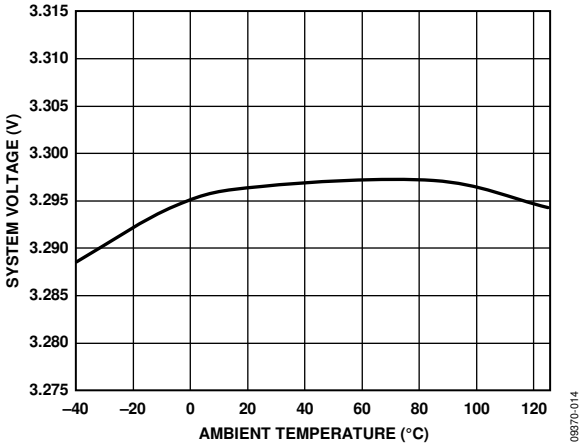

Figure 14. System Voltage vs. Ambient Temperature, V_{IN} = 5.0 V, R_{LOAD} = 33 Ω

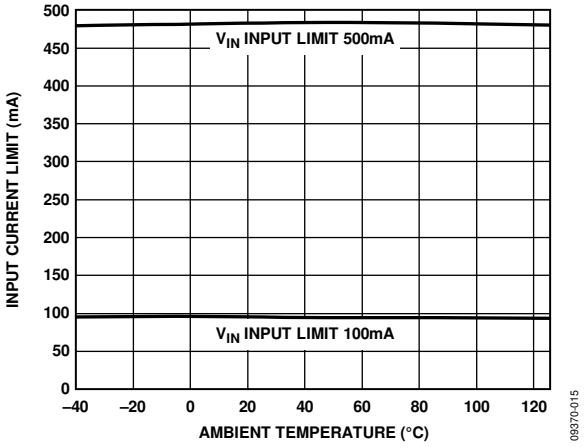

Figure 15. Input Current Limit vs. Ambient Temperature, V_{IN} = 5.0 V

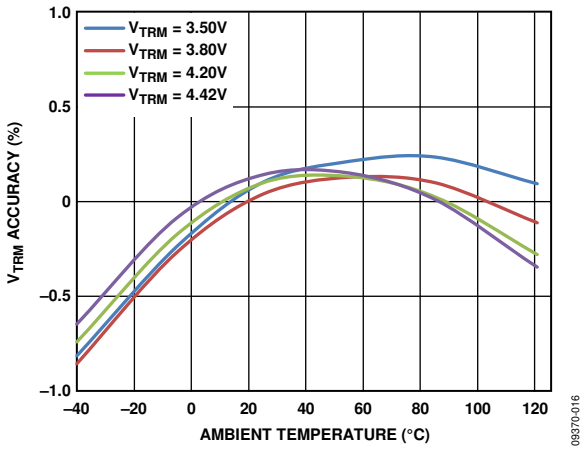

Figure 16. Termination Voltage vs. Ambient Temperature, V_{IN} = 5.0 V, V_{TRM} Programming 3.50 V, 3.80 V, 4.20 V, and 4.42 V

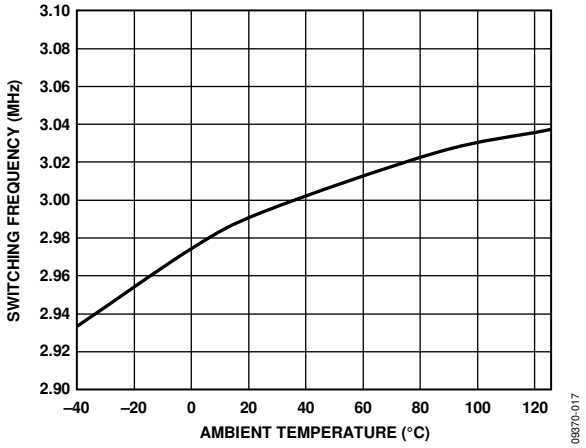

Figure 17. Switching Frequency vs. Ambient Temperature, V_{IN} = 5.0 V

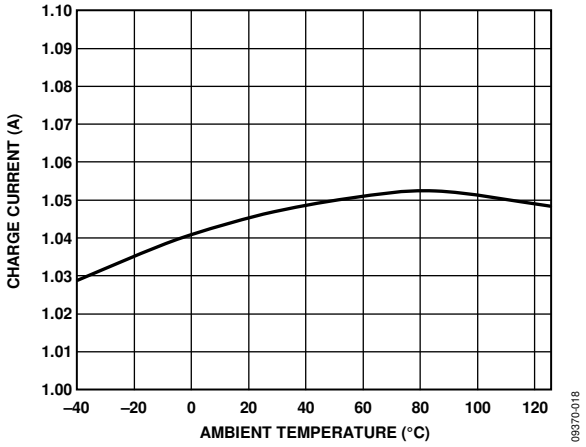

Figure 18. Fast Charge Current vs. Ambient Temperature, V_{IN} = 5.0 V, V_{ISO_B} = 3.6 V, I_{CHG} = 1050 mA

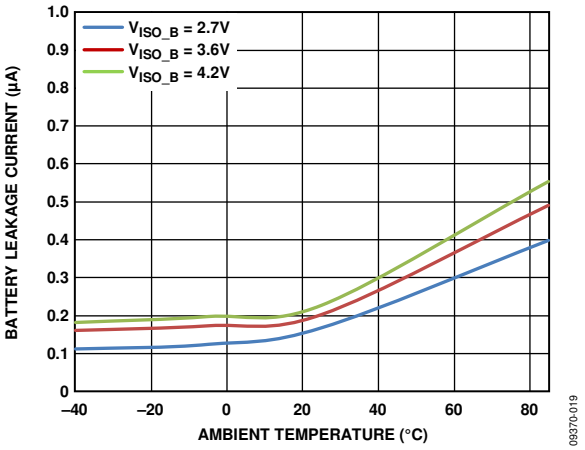

Figure 19. Battery Leakage Current vs. Ambient Temperature

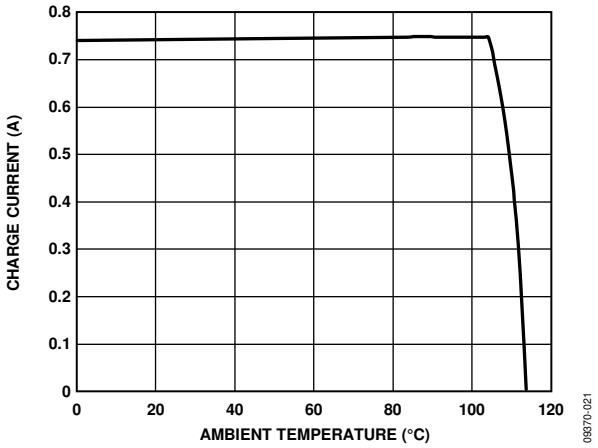

Figure 21. Isothermal Regulation of Charge Current vs. Ambient Temperature, I_{CHG} = 750 mA, V_{IN} = 5.0 V, V_{ISO_B} = 3.6 V

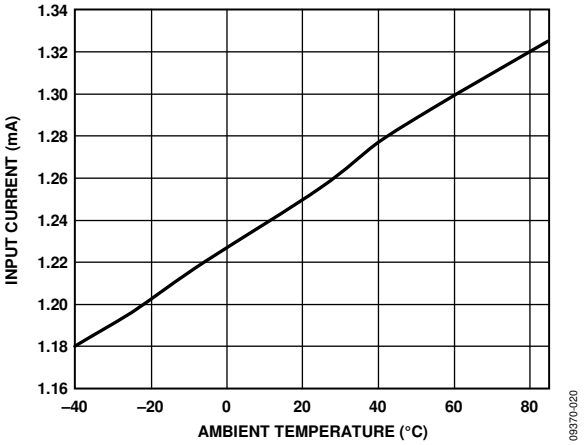

Figure 20. VINx Quiescent Current vs. Temperature, V_{IN} = 5.0 V, Suspend Mode (EN_CHG = 0)

TYPICAL WAVEFORMS

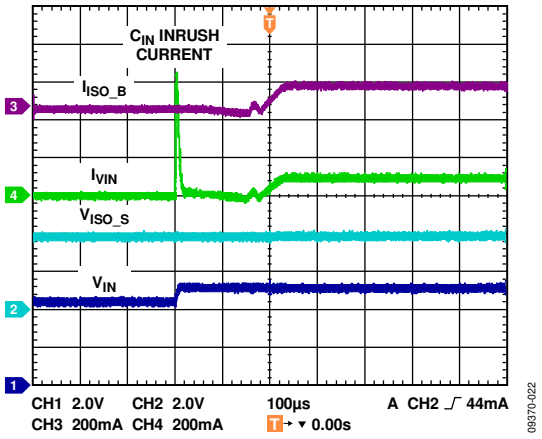

Figure 22. Typical Waveforms, VINx Connect From High Impedance to VBUS, ILIM = 100 mA

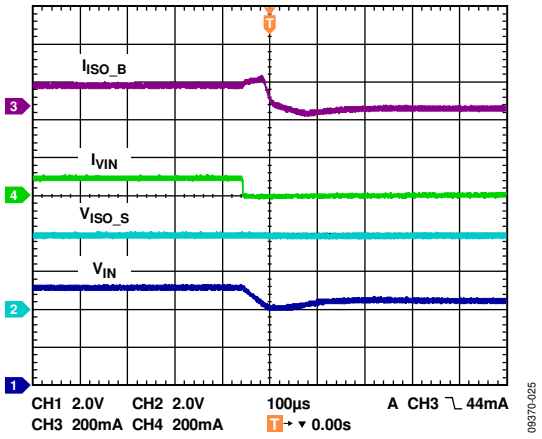

Figure 25. Typical Waveforms, VINx Disconnect from VBUS to High Impedance, ILIM = 100 mA

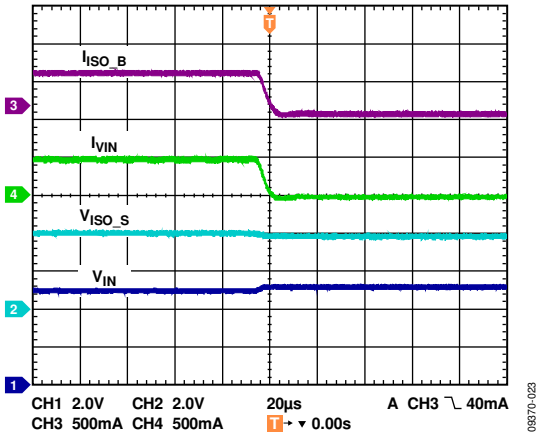

Figure 23. Mode Change, Fast Charge to Suspend (EN_CHG from High to Low), ILIM = 500 mA, R_{LOAD} = 33 Ω

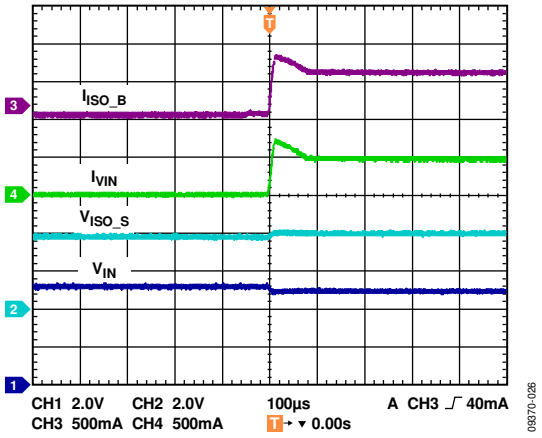

Figure 26. Mode Change, Suspend to Fast Charge (EN_CHG from Low to High), ILIM = 500 mA, R_{LOAD} = 33 Ω

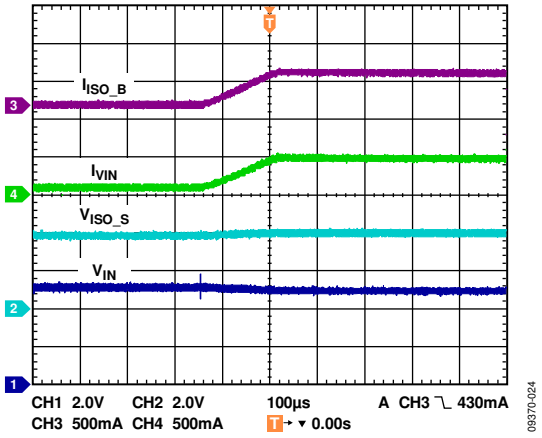

Figure 24. VINx Current Limit Change from 100 mA to 500 mA, EN_CHG = High, V_{IN} = 5.0 V, R_{LOAD} = 33 Ω

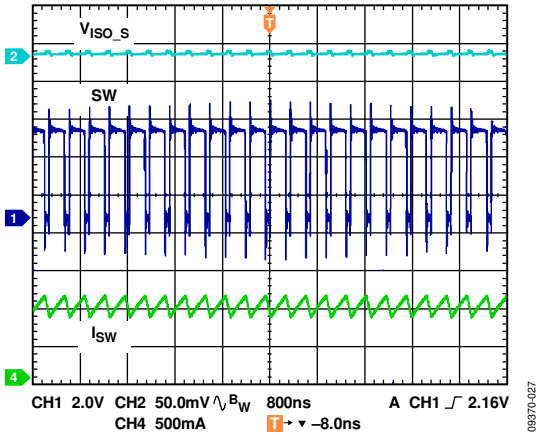

Figure 27. Typical Waveforms, Heavy Load, V_{IN} = 5.0 V, I_{ISO_S} = 1000 mA

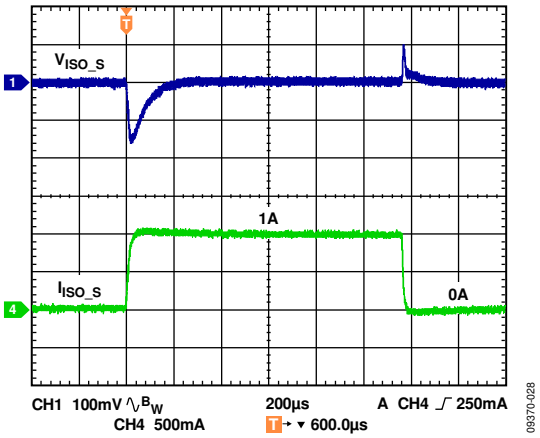

Figure 28. System Voltage Load Transient, V_{IN} = 5.0 V, No Battery

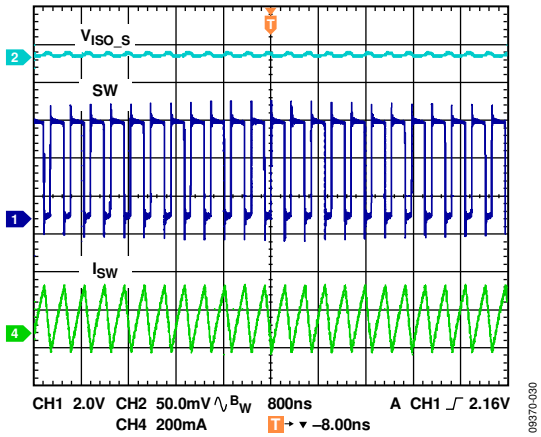

Figure 30. Typical Waveforms, Light Load, V_{IN} = 5.0 V, I_{ISO_S} = 100 mA

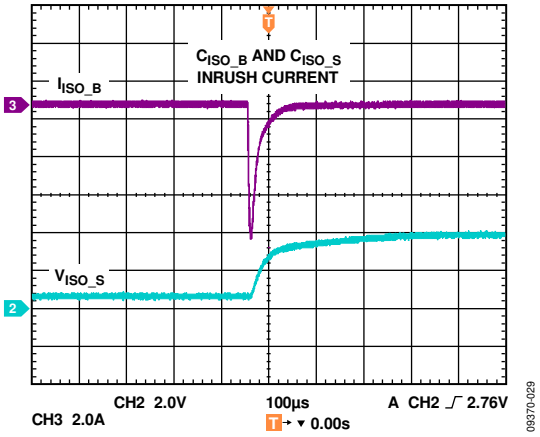

Figure 29. Battery Connect

THEORY OF OPERATION

INTRODUCTION

The ADP5065 is a fully I²C-programmable charger for single-cell lithium-ion or lithium-polymer batteries suitable for a wide range of portable applications.

The highly efficient switcher dc-to-dc architecture enables higher charging currents as well as a lower temperature charging operation that results in faster charging times because of the following features:

- 3 MHz switch mode charger.
- 1.25 A charge current from dedicated charger.
- Up to 680 mA of charging current from a 500 mA USB host.

The ADP5065 operates from an input voltage from 4 V to 5.5 V but is tolerant of voltages of up to 20 V. This alleviates the concern about USB bus spiking during disconnection or connection scenarios.

The ADP5065 features an internal FET between the dc-to-dc charger output and the battery. This permits battery isolation and, hence, system powering in a dead battery or no battery scenario, which allows for immediate system function on connection to a USB power supply.

The ADP5065 is fully compliant with the USB 3.0 battery charging specification and enables charging via the mini USB VBUS pin from a wall charger, car charger, or USB host port. Based on the type of USB source, which is detected by an external USB detection device, the ADP5065 can be set to apply the correct current limit for optimal charging and USB compliance. The USB charger permits correct operation under all USB compliant sources such as, wall chargers, host chargers, hub chargers, and standard hosts and hubs.

A processor is able to control the USB charger using the I²C to program the charging current and numerous other parameters including

- Trickle charge current level.
- Trickle charge voltage threshold.
- Weak charge (constant current) charge current level.
- Fast charge (constant current) charge current level.
- Fast charge (constant voltage) charge voltage level at 1% accuracy.
- Fast charge safety timer period.
- Watchdog safety timer parameters.
- Weak battery threshold detection.
- Charge complete threshold.
- Recharge threshold.
- Charge enable/disable.
- Battery pack temperature detection and automatic charger shutdown.

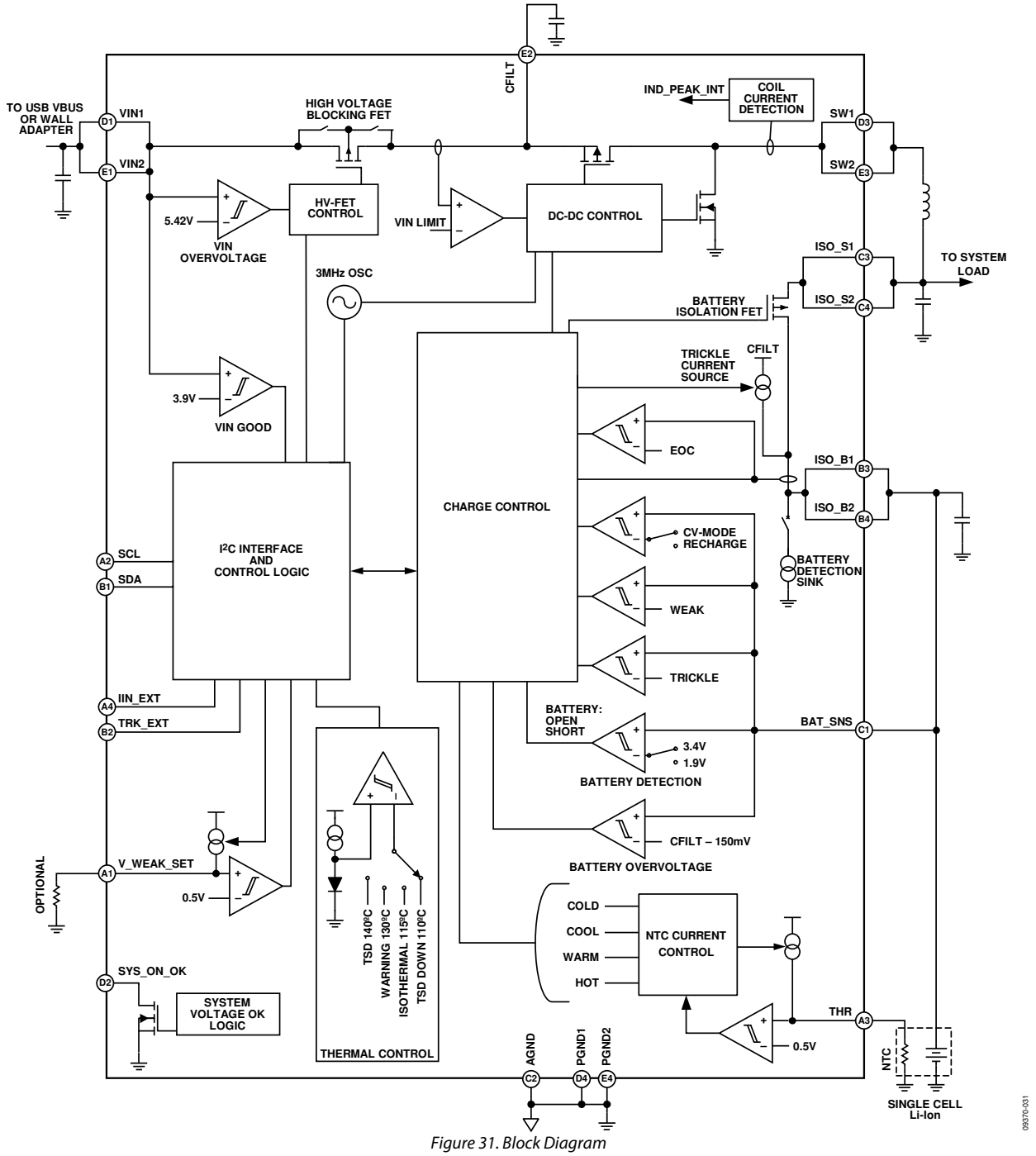

Figure 31. Block Diagram

The ADP5065 also includes a number of significant features to optimize charging and functionality, including

- Thermal regulation for maximum performance.
- USB host current-limit accuracy: ±5 %.
- Termination voltage accuracy: ±1 %.
- Battery thermistor input with automatic charger shutdown in the event that the battery temperature exceeds limits. (Compliant with the JEITA Li-Ion battery charging temperature specification.)
- Offloads processor to manage external pin (TRK_EXT) control to enable/disable trickle charging.
- Direct external pin (IIN_EXT) control of 100 mA or 500 mA input current limit.
- Optional external resistor programming input, V_WEAK_SET, which is used for setting the V_{WEAK} threshold. When the battery reaches the V_{WEAK} threshold, the ADP5065 pulls down the SYS_EN_OK open-drain output flag. The flag can be used to hold off system turn on until the battery is at the minimum required level for a guaranteed system startup.

CHARGER MODES

Input Current Limit

The VINx input current limit is controlled via an internal I²C ILIM register. The input current limit can also be controlled via the IIN_EXT pin as outlined in Table 7. Any change in the I²C default from 100 mA dominates over the pin setting.

Table 7. IIN_EXT Operation

IIN_EXT	Function
0	100 mA input current limit or I²C programmed value
1	500 mA input current limit or I²C programmed value (or reprogrammed I²C value from 100 mA default)

USB Compatibility

The ADP5065 charger provides support for the following connections through the single connector VINx pin.

The ADP5065 features a programmable input current limit to ensure compatibility with the requirements listed in Table 8. The current limit defaults to 100 mA to allow compatibility with a USB host or hub that is not configured.

The I²C register default is 100 mA. An I²C write command to the ILIM register overrides the IIN_EXT pin and the I²C register default value can be reprogrammed for alternative requirements.

When the input current limiting feature is used, the available input current may be too low for the charger to meet the programmed charging current, I_{CHG}, and the rate of charge is reduced. In this case, the VIN_ILIM flag is set.

When connecting voltage to VINx without having the proper voltage level on the battery side, the HV blocking part is in a state wherein it draws only 1.3 mA (typical) of current until the V_{IN} has reached the VIN_OK level.

Table 8. Input Current Compatibility with Standard USB Limits

Mode	Standard USB Limit	ADP5065 Function
USB (China Only)	100 mA limit for standard USB host or hub	100 mA input current limit or I²C programmed value
	300 mA limit for Chinese USB specification	300 mA input current limit or I²C programmed value
USB 2.0	100 mA limit for standard USB host or hub	100 mA input current limit or I²C programmed value
	500 mA limit for standard USB host or hub	500 mA input current limit or I²C programmed value
USB 3.0	150 mA limit for super speed USB 3.0 host or hub	150 mA input current limit or I²C programmed value
	900 mA limit for super speed, high speed USB host or hub charger	900 mA input current limit or I²C programmed value
Dedicated Charger	1500 mA limit for dedicated charger or low/full speed USB host or hub charger	1500 mA input current limit or I²C programmed value

Trickle Charge Mode

A deeply discharged Li-Ion cell may exhibit a very low cell voltage making it unsafe to charge the cell at high current rates. The ADP5065 charger uses a trickle charge mode to reset the battery pack protection circuit and lift the cell voltage to a safe level for fast charging. A cell with a voltage below V_{TRK_DEAD} is charged with the trickle mode current, I_{TRK_DEAD}. During trickle charging mode, the CHARGER_STATUS register is set.

During trickle charging, the ISO_Sx node is regulated to V_{ISO_STRK} by the dc-to-dc converter and the battery isolation FET is off, which means the battery is isolated from the system power supply.

Trickle charging can be controlled via the TRK_EXT external pin (see Table 9). Note that any change in the I²C EN_TRK bit dominates over the pin setting.

Table 9. TRK_EXT Operation

TRK_EXT	Function
0	Trickle charge enabled
1	Trickle charge disabled

Trickle Charge Mode Timer

The duration of trickle charge mode is monitored to ensure the battery is revived from its deeply discharged state. If trickle charge mode runs for longer than 60 minutes without the cell voltage reaching V_{TRK_DEAD}, a fault condition is assumed and charging stops. The fault condition is asserted on the CHARGER_STATUS register, allowing the user to initiate the fault recovery procedure specified in the Fault Recovery section.

Weak Charge Mode (Constant Current)

When the battery voltage exceeds V_{TRK_DEAD} but is less than V_{WEAK}, the charger switches to the intermediate charge mode.

During the weak charge mode, the battery voltage is too low to allow the full system to power-up. Due to the low level of the battery, the USB transceiver cannot be powered and, therefore, cannot enumerate for more current from a USB host. Consequently, the USB limit remains at 100 mA.

The system microcontroller may or may not be powered by the charger output voltage (V_{ISO_SFC}) depending upon the amount of current required by the microcontroller and/or the system architecture. In this case, the battery charge current (I_{CHG_WEAK}) cannot be increased above 20 mA to ensure the microcontroller can still operate (if doing so) nor increased above the 100 mA USB limit. Thus, set the battery charging current as follows:

- Set the default 20 mA via the linear trickle charger branch (to ensure that the microprocessor remains alive if powered by the main switching charger output, ISO_Sx). Any residual current on the main switching charger output, ISO_Sx, is used to charge the battery at up to the preprogrammed level in the I^2C for I_{CHG} (fast charge current limit) or I_{LIM} (input current limit).
- During weak current mode, other features may prevent the actual programmed weak charging current from reaching its full programmed value. Isothermal charging mode or input current limiting for USB compatibility may affect the programmed weak charging current value under certain operating conditions. During weak charging, the ISO_Sx node is regulated to V_{ISO_SFC} by the battery isolation FET.

Fast Charge Mode (Constant Current)

When the battery voltage exceeds V_{TRK_DEAD} and V_{WEAK}, the charger switches to fast charge mode, charging the battery with the constant current, I_{CHG}. During fast charge mode (constant current), the CHARGER_STATUS register is set.

During constant current mode, other features may prevent the current, I_{CHG}, from reaching its full programmed value. Isothermal charging mode or input current limiting for USB compatibility may affect the value of I_{CHG} under certain operating conditions. The voltage on ISO_Sx is regulated to stay at V_{ISO_SFC} by the battery isolation FET when $V_{ISO\_B} < V_{ISO\_SFC}$.

Fast Charge Mode (Constant Voltage)

As the battery charges, its voltage rises and approaches the termination voltage, V_{TRM}. The ADP5065 charger monitors the voltage on the BAT_SNS pin to determine when charging should end. However, the internal ESR of the battery pack combined with PCB and other parasitic series resistances creates a voltage drop between the sense point at the BAT_SNS pin and the cell terminal itself. To compensate for this and ensure a fully charged cell, the ADP5065 enters a constant voltage charging mode when the termination voltage is detected on the BAT_SNS pin. The ADP5065 reduces charge current gradually as the cell continues to charge, maintaining a voltage of V_{TRM} on the BAT_SNS pin. During fast charge mode (constant voltage), the CHARGER_ STATUS register is set.

Fast Charge Mode Timer

The duration of fast charge mode is monitored to ensure that the battery is charging correctly. If the fast charge mode runs for longer than t_{CHG} without the voltage at the BAT_SNS pin reaching V_{TRM}, a fault condition is assumed and charging stops. The fault condition is asserted on the CHARGER_STATUS register allowing the user to initiate the fault recovery procedure specified in the Fault Recovery section.

If the fast charge mode runs for longer than t_{CHG}, and V_{TRM} has been reached on the BAT_SNS pin but the charge current has not yet fallen below I_{END}, charging stops. No fault condition is asserted in this circumstance and charging resumes as normal if the recharge threshold is breached.

Watchdog Timer

The ADP5065 charger features a programmable watchdog timer function to ensure charging is under the control of the processor. The watchdog timer starts running when the ADP5065 charger determines that the processor should be operational, that is, when the processor sets the RESET_WD bit for the first time or when the battery voltage is greater than the weak battery threshold, V_{WEAK}. When the watchdog timer has been triggered, it must be reset regularly within the watchdog timer period, t_{WD}.

If the watchdog timer expires without being reset while in charger mode, the ADP5065 charger assumes there is a software problem and triggers the safety timer, t_{SAFE}. For more information see the Safety Timer section.

Safety Timer

If the watchdog timer (see the Watchdog Timer section for more information) expires while in charger mode, the ADP5065 charger initiates the safety timer, t_{SAFE}. If the processor has programmed charging parameters by this time, the I_{LIM} is set to the default value. Charging continues for a period of t_{SAFE}, then the charger switches off and sets the CHARGER_STATUS register.

Charge Complete

The ADP5065 charger monitors the charging current while in constant voltage fast charge mode. If the current falls below I_{END} and remains below I_{END} for t_{END}, charging stops and the CHDONE flag is set. If the charging current falls below I_{END} for less than t_{END} and then rises above I_{END} again, the t_{END} timer resets.

Recharge

After the detection of charge complete, and the cessation of charging, the ADP5065 charger monitors the BAT_SNS pin as the battery discharges through normal use. If the BAT_SNS pin voltage falls to V_{RCH}, the charger reactivates charging. Under most circumstances, triggering the recharge threshold results in the charger starting directly into fast charge constant voltage mode.

Battery Charging Enable/Disable

The ADP5065 charging function can be disabled by setting the I^2C EN_CHG bit to low.

THERMAL MANAGEMENT

Isothermal Charging

To assist with the thermal management of the ADP5065 charger, the battery charger provides an isothermal charging function. As the on-chip power dissipation and die temperature increase, the ADP5065 charger monitors die temperature and limits output current when the temperature reaches T_{LIM} (typically at 115°C). The die temperature is maintained at T_{LIM} through the control of the charging current into the battery. A reduction in power dissipation or ambient temperature may allow the charging current to return to its original value, and the die temperature subsequently drops below T_{LIM}. During isothermal charging, the THERM_LIM flag is set to high.

Thermal Shutdown and Thermal Early Warning

The ADP5065 switching charger features a thermal shutdown threshold detector. If the die temperature exceeds T_{SD}, the ADP5065 charger is disabled, and the TSD 140°C bit is set. The ADP5065 charger can be reenabled when the die temperature drops below the T_{SD} falling limit and the TSD 140°C bit is reset. To reset the TSD 140°C bit, write to the I^2C Fault Register 0x0D or cycle the power.

Before die temperature reaches T_{SD}, the early warning bit is set if T_{SDL} is exceeded. This allows the system to accommodate power consumption before thermal shutdown occurs.

Fault Recovery

Before performing the following operation, it is important to ensure that the cause of the fault has been rectified.

To recover from a charger fault (when the CHARGER_STATUS equals 110), cycle power on VINx or write high to reset the I^2C fault bits in the fault register.

BATTERY ISOLATION FET

The ADP5065 charger features an integrated battery isolation FET for power path control. The battery isolation FET isolates a deeply discharged Li-Ion cell from the system power supply in both trickle and fast charge modes, thereby allowing the system to be powered at all times.

When VINx is below V_{VIN_OK}, the battery isolation FET is in full conducting mode.

The battery isolation FET is off during trickle charge mode. When the battery voltage exceeds V_{TRK}, the battery isolation FET switches to the system voltage regulation mode. During system voltage regulation mode, the battery isolation FET maintains the V_{ISO_SFC} voltage on the ISO_Sx pins. When the battery voltage exceeds V_{ISO_SFC}, the battery isolation FET is in full conducting mode.

The battery isolation FET supplements the battery to support high current functions on the system power supply.

When voltage on ISO_Sx drops below ISO_Bx, the battery isolation FET enters into full conducting mode.

When voltage on ISO_Sx rises above ISO_Bx, the isolation FET enters regulating mode or full conduction mode, depending on the Li-Ion cell voltage and the dc-to-dc charger mode.

BATTERY DETECTION

Battery Level Detection

The ADP5065 charger features a battery detection mechanism to detect an absent battery. The charger actively sinks and sources current into the ISO_Bx/BAT_SNS node, and voltage vs. time is detected. The sink phase is used to detect a charged battery, whereas the source phase is used to detect a discharged battery.

The sink phase (see Figure 32) sinks I_{SINK} current from the ISO_Bx/ BAT_SNS pins for a time, t_{BATOK}. If the BAT_SNS pin is below V_{BATL} when the t_{BATOK} timer expires, the charger assumes no battery is present, and starts the source phase. If the BAT_SNS exceeds the V_{BATL} voltage when the t_{BATOK} timer expires, the charger assumes the battery is present, and begins a new charge cycle.

The source phase sources I_{SOURCE} current to ISO_Bx or the BAT_SNS pins for a time, t_{BATOK}. If the BAT_SNS pin exceeds V_{BATH} before the t_{BATOK} timer expires, the charger assumes that no battery is present. If the BAT_SNS does not exceed the V_{BATH} voltage when the t_{BATOK} timer expires, the charger assumes that a battery is present, and begins a new charge cycle.

Battery (ISO_Bx) Short Detection

A battery short occurs under a damaged battery condition or when the battery protection circuitry is enabled.

On commencing trickle charging, the ADP5065 charger monitors the battery voltage. If this battery voltage does not exceed V_{BAT_SHR} within the specified timeout period, t_{BAT_SHR}, a fault is declared and the charger is stopped by turning the battery isolation FET off but the system voltage is maintained at V_{ISO_STRK} by the linear regulator.

The trickle charge branch is active during the battery short scenario, and trickle charge current to the battery is maintained until the 60 minute trickle charge mode timer expires.

After source phase, if the ISO_Bx or BAT_SNS level remains below V_{BATH}, either the battery voltage is low or the battery node can be shorted. As a result of the battery voltage being low, trickle charging mode is initiated (see Figure 33). If the BAT_SNS level remains below V_{BAT_SHR} after t_{BAT_SHR} has elapsed, the ADP5065 assumes that the battery node is shorted.

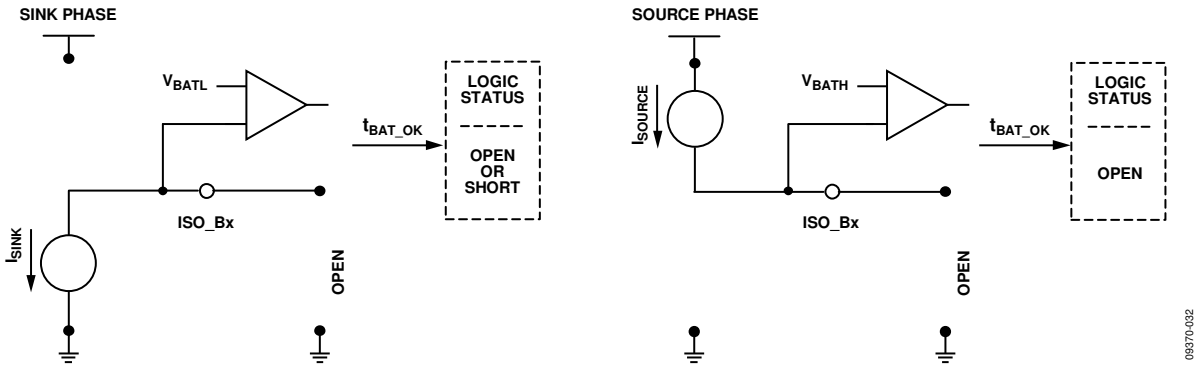

Figure 32. Battery Detection Sequence

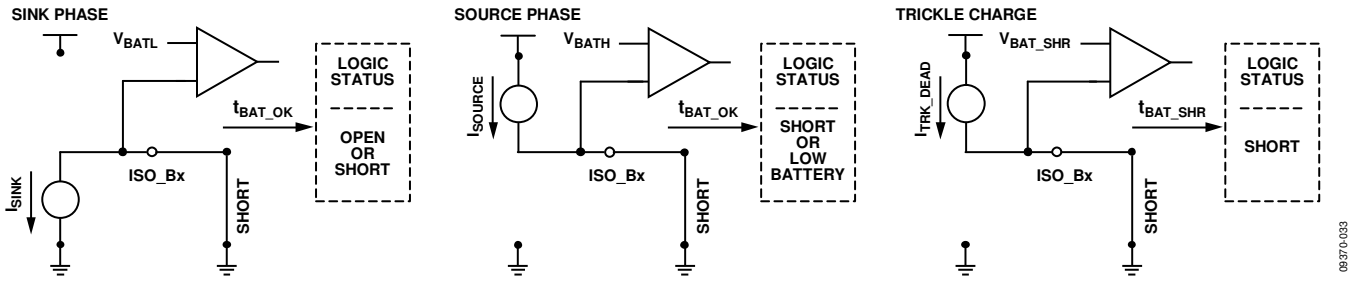

Figure 33. Battery Short Detection Sequence

BATTERY PACK TEMPERATURE SENSING

Battery Thermistor Input

The ADP5065 charger features battery pack temperature sensing that precludes charging when the battery pack temperature is outside the specified range. The THR pin provides an on and off switching current source, which should be connected directly to the battery pack thermistor terminal. The activation interval of the THR current source is 167 ms.

The battery pack temperature sensing can be controlled by I²C using the conditions shown in Table 10. Note that the I²C register default setting for EN_THR (Register 0x07) is 0 = temperature sensing off.

Table 10. THR Input Function

Conditions		
VINx	**V_{ISO_B}**	**THR Function**
Open or V_{IN} = 0 V to 4.0 V	<2.5 V	Off
Open or V_{IN} = 0 V to 4.0 V	>2.5 V	Off, controlled by I²C
4.0 V to 5.5 V	Don't care	Always on

If the battery pack thermistor is not connected directly to the ADP5065 THR pin, a 10 kΩ (tolerance ±20%) dummy resistor must be connected between the THR input and GND. Leaving the THR pin open results in a false detection of the battery temperature being <0°C and charging is disabled.

The ADP5065 charger monitors the voltage in the THR pin and suspends charging if the current is outside the range of less than 0°C or greater than 60°C. For temperatures greater than 0°C, the THR_STATUS register is set accordingly, and for temperatures lower than 60°C, the THR_STATUS register is, likewise, set accordingly.

The ADP5065 charger is designed for use with an NTC thermistor in the battery pack with a nominal room temperature value of either 10 kΩ at 25°C or 100 kΩ at 25°C, which is selected by a fuse.

The ADP5065 charger is designed for use with an NTC thermistor in the battery pack with a temperature coefficient curve (beta). Fuse-selectable beta programming is supported by eight steps covering a range from 3150 to 4400 (see Table 34).

JEITA Li-Ion Battery Temperature Charging Specification

The ADP5065 is compliant with the JEITA Li-Ion battery charging temperature specifications as outlined in Table 11.

The JEITA function can be enabled via the I²C interface. When the ADP5065 detects a JEITA cool condition, charging current is reduced according to Table 12.

When the ADP5065 identifies a hot or cold battery condition, the ADP5065 takes the following actions:

- Stops charging the battery.
- Connects/enables the battery isolation FET such that the system power supply node is connected to the battery.

Table 11. JEITA Li-Ion Battery Charging Specification Defaults

Parameter	Symbol	Conditions	Min	Max	Unit
JEITA Cold Temperature Limits	I_{JEITA_COLD}	No battery charging occurs.		0	°C
JEITA Cool Temperature Limits	I_{JEITA_COOL}	Battery charging occurs at approximately 50% of programmed level. See Table 12 for specific charging current reduction levels.	0	10	°C
JEITA Typical Temperature Limits	I_{JEITA_TYP}	Normal battery charging occurs at default/programmed levels.	10	45	°C
JEITA Warm Temperature Limits	I_{JEITA_WARM}	Battery termination voltage (V_{TRM}) is reduced by 100 mV from programmed value.	45	60	°C
JEITA Hot Temperature Limits	I_{JEITA_HOT}	No battery charging occurs.	60		°C

Table 12. JEITA Reduced Charge Current Levels

JEITA Cool Temperature Limit—Reduced Charge Current Levels	
ICHG[2:0] (Default)	**ICHG JEITA (mA)**
000 = 550 mA	250
001 = 650 mA	300
010 = 750 mA	350
011 = 850 mA	400
100 = 950 mA	450
101 = 1050 mA	500
110 = 1150 mA	550
111 = 1250 mA	600

EXTERNAL RESISTOR FOR V_WEAK_SET

The ADP5065 charger features a V_{WEAK} threshold, which can be used for enabling the main PMU system. When battery voltage at the BAT_SNS pin exceeds the V_{WEAK} level, the ADP5065 pulls down the SYS_ON_OK open-drain flag.

The V_{WEAK} threshold can be programmed set either by I^2C or by an external resistor connected between the V_WEAK_SET pin and GND. Recommended resistor values for each threshold are listed in Table 13.

If an external resistor is not used, it is recommended to tie the V_WEAK_SET pin to AGND for V_{WEAK} to obtain its default value.

Table 13. Resistor Values for V_WEAK_SET Pin

Target Resistor Value E24 (kΩ)	Actual Threshold (kΩ)	V_{WEAK} Voltage (Rising Threshold)	V_{WEAK} Voltage (Falling Threshold)
Short to GND	Not applicable	I^2C (3.0 V default)	I^2C programmed − 100 mV
15	13.2	2.7 V	2.6 V
20	17.8	2.8 V	2.7 V
27	23.5	2.9 V	2.8 V
36	31.0	3.0 V	2.9 V
47	41.3	3.1 V	3.0 V
68	56.2	3.2 V	3.1 V
100	79.7	3.3 V	3.2 V
Open	122.4	3.4 V	3.3 V

I²C INTERFACE

The ADP5065 includes an I²C-compatible serial interface for control of the charging and for a readback of system status registers. The I²C chip address is 0x28 in write mode and 0x29 in read mode.

Register values are reset to the default values, when the supply voltage at the VINx pin falls below the V_{VIN_OK} falling voltage threshold. The I²C registers are also reset when the battery is disconnected and V_{IN} is 0 V.

See Figure 34 for an example of the I²C write sequence to a single register. The subaddress content selects which one of the five ADP5065 registers is written to first. The ADP5065 sends an acknowledgement to the master after the 8-bit data byte has been written. The ADP5065 increments the subaddress automatically and starts receiving a data byte to the following register until the master sends an I²C stop as shown in Figure 35.

Figure 36 shows the I²C read sequence of a single register. ADP5065 sends the data from the register denoted by the subaddress and increments the subaddress automatically, sending data from the next register until the master sends an I²C stop condition as shown in Figure 37.

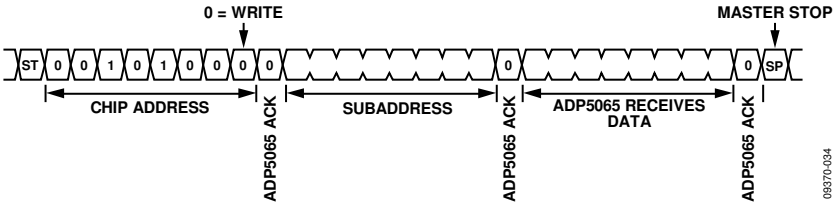

Figure 34. I²C Single Register Write Sequence

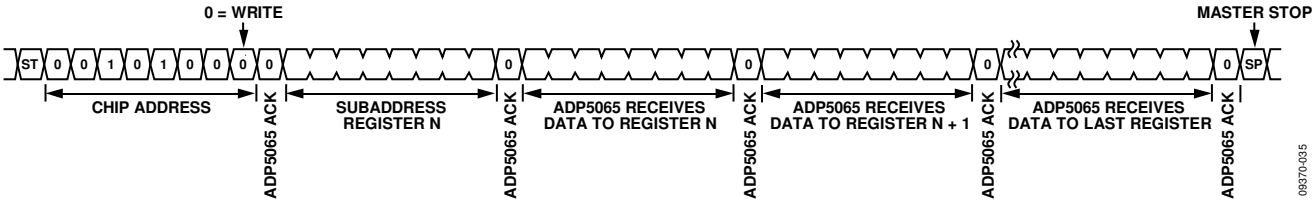

Figure 35. I²C Multiple Register Write Sequence

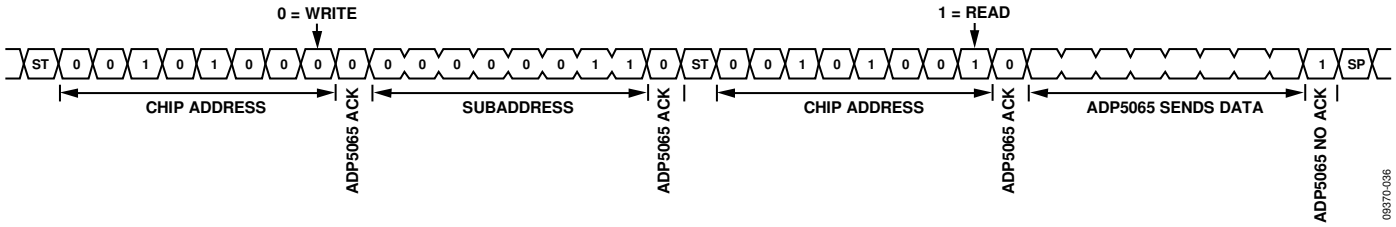

Figure 36. I²C Single Register Read Sequence

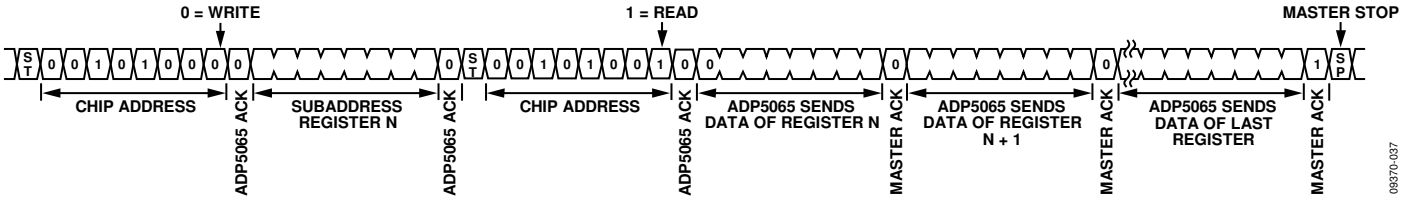

Figure 37. I²C Multiple Register Read Sequence

CHARGER OPERATIONAL FLOWCHART

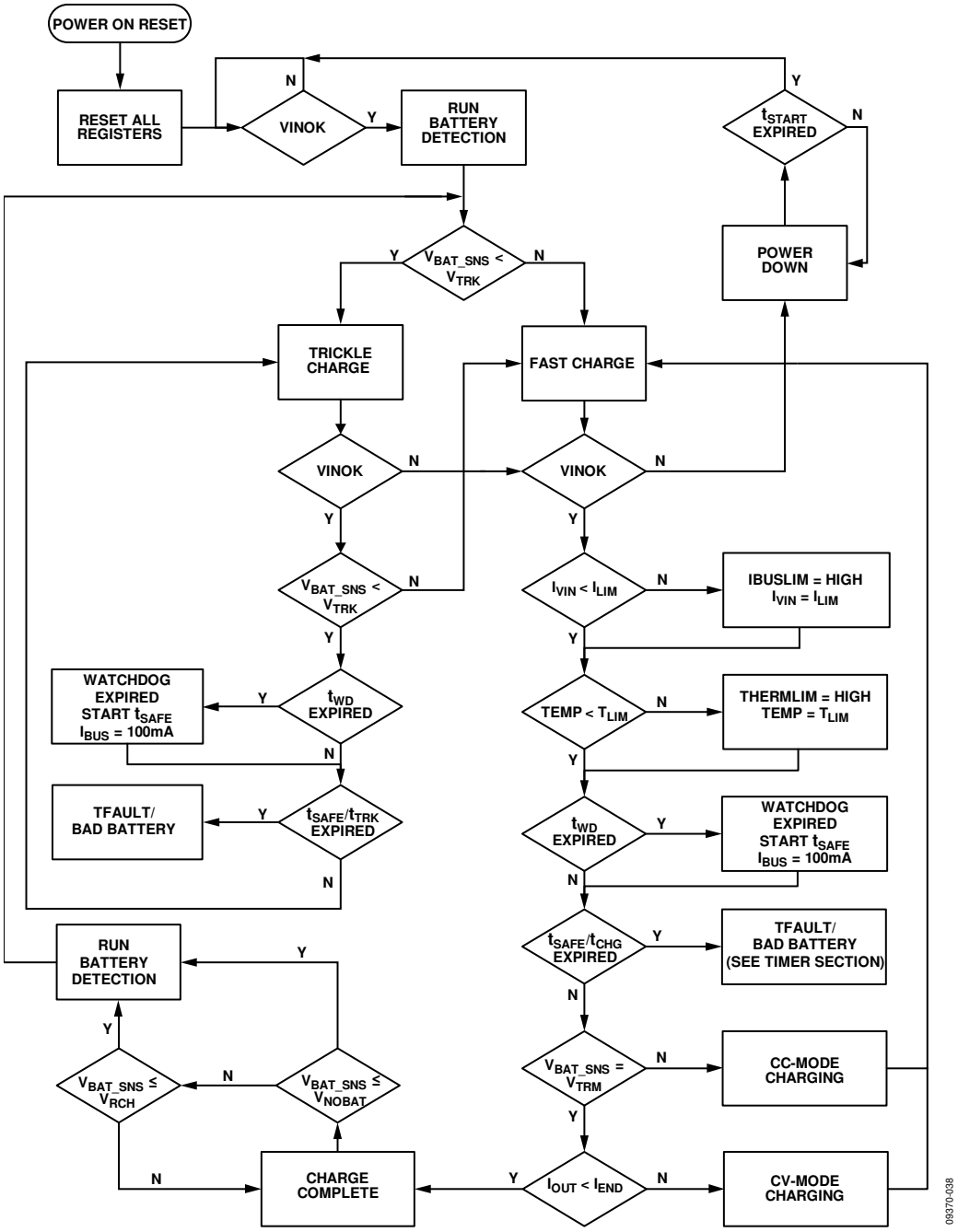

Figure 38. ADP5065 Operational Flowchart