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High Efficiency Integrated Power Solution for Multicell Lithium Ion Applications

Data Sheet **ADP5080**

FEATURES

- Wide input voltage range: 4.0 V to 15 V
- High efficiency architecture
- Up to 2 MHz switching frequency
- 6 synchronous rectification dc-to-dc converters
  - Channel 1 buck regulator: 3 A maximum
  - Channel 2 buck regulator: 1.15 A maximum
  - Channel 3 buck regulator: 1.5 A maximum
  - Channel 4 buck regulator: 0.8 A maximum
  - Channel 5 buck regulator: 2 A maximum
  - Channel 6 configurable buck or buck boost regulator
    - 2 A maximum for buck regulator configuration
    - 1.5 A maximum for buck boost regulator configuration
  - Channel 7 high voltage, high performance LDO regulator: 30 mA maximum
- 2 low quiescent current keep-alive LDO regulators
  - LDO1 regulator: 400 mA maximum
  - LDO2 regulator: 300 mA maximum
- Control circuit
  - Charge pump for internal switching driver power supply
  - I²C-programmable output levels and power sequencing
- Package: 72-ball, 4.5 mm × 4.0 mm × 0.6 mm WLCSP (0.5 mm pitch)

APPLICATIONS

- DSLR cameras
- Non-reflex (mirrorless) cameras
- Portable instrumentation

FUNCTIONAL BLOCK DIAGRAM

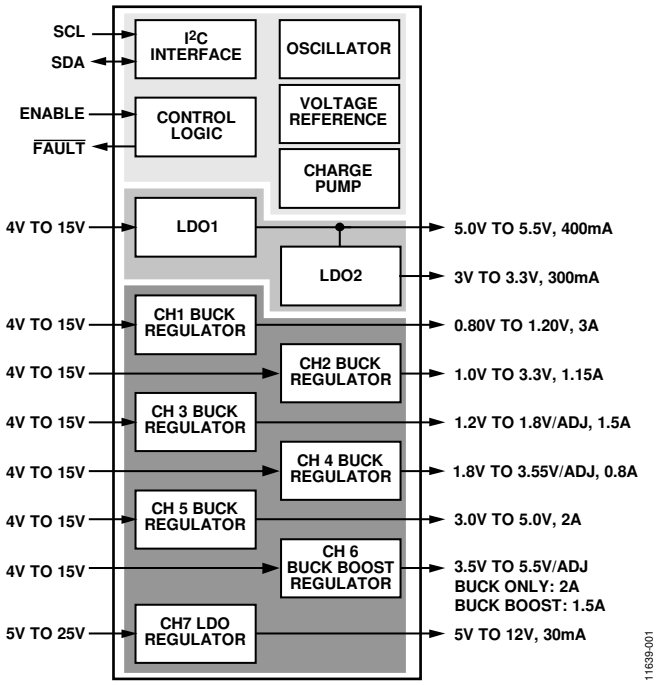

Figure 1.

GENERAL DESCRIPTION

The ADP5080 is a fully integrated, high efficiency power solution for multicell lithium ion battery applications. The device can connect directly to the battery, which eliminates the need for preregulators and, therefore, increases the battery life of the system.

The ADP5080 integrates two keep-alive LDO regulators, five synchronous buck regulators, a configurable four-switch buck boost regulator, and a high voltage LDO regulator. The ADP5080 is a highly integrated power solution that incorporates all power MOSFETs, feedback loop compensation, voltage setting resistor dividers, and discharge switches, as well as a charge pump to generate a global bootstrap voltage.

All these features help to minimize the number of external components and PCB space required, providing significant advantages for portable applications. The switching frequency is selectable on each channel from 750 kHz to 2 MHz.

Key functions for power applications, such as soft start, selectable preset output voltage, and flexible power-up and power-down sequences, are provided on chip and are programmable via the I²C interface with fused factory defaults. The ADP5080 is available in a 72-ball WLCSP 0.5 mm pitch package.

Rev. A

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COMPARABLE PARTS

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EVALUATION KITS

- ADP5080 Evaluation Board

DOCUMENTATION

Data Sheet

- ADP5080: High Efficiency Integrated Power Solution for Multicell Lithium Ion Applications Data Sheet

User Guides

- UG-752: Operating the ADP5080 High Efficiency, 6-Channel PMU Evaluation Board
- UG-773: Installing the ADP5080 Evaluation Board Hardware and Software

TOOLS AND SIMULATIONS

- ADIsimPower™ Voltage Regulator Design Tool

DESIGN RESOURCES

- ADP5080 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADP5080 EngineerZone Discussions.

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REVISION HISTORY

4/14—Revision A: Initial Version

SPECIFICATIONS

T_J = 25°C, V_{VBATT} = 7.2 V, V_{VREG1} = V_{VDRx} = 5 V, V_{VREG2} = V_{VDDIO} = 3.3 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT SUPPLY VOLTAGE RANGE						
VBATT	V_{VBATT}	4.0		15	V	Applies to PVIN1, PVIN2, PVIN3, PVIN4, PVIN5, and PVIN6
VILDO7	V_{VILDO7}	5		25	V	
VDDIO	V_{VDDIO}	1.6		3.6	V	
QUIESCENT CURRENT						
Operating Quiescent Current	$I_{Q\ (VIN)}$		8	11	mA	All channels on, nonswitching
VDDIO	$I_{Q\ (VDDIO\_OP)}$		0.2		µA	V_{VDDIO} = V_{SCL} = V_{SDA} = 3.3 V
Standby Current	$I_{Q\ (VBATT\_STNBY1)}$		12	20	µA	Includes LDO1 and LDO2, EN low
	$I_{Q\ (VBATT\_STNBY2)}$		1.25		mA	All channels off, EN high, SEL_FSW = 1, FREQ_CP = 01
UNDERVOLTAGE LOCKOUT	UVLO					
UVLO Rising Threshold	$V_{UVLO\ (R)}$	3.45	3.7	3.85	V	At PVIN1
UVLO Falling Threshold	$V_{UVLO\ (F)}$		3.45	3.55	V	At PVIN1
VBATT UVLO Threshold	$V_{UVLO\ (BATT)}$		3.3		V	At VBATT, falling
Reset Threshold	$V_{UVLO\ (POR)}$		2.4		V	At VREG2, falling
OSCILLATOR CIRCUIT						
Switching Frequency	f_{SW}	1.98	2.0	2.02	MHz	R_{OSC} = 100 kΩ, SEL_FSW = 0
		1.48	1.5	1.52	MHz	R_{OSC} = 100 kΩ, SEL_FSW = 1
SYNC Pin, Input Clock						
Frequency Range	f_{SYNC}	0.5		2.0	MHz	R_{OSC} = 100 kΩ
Minimum On Pulse Width	$t_{SYNC\_MIN\_ON}$	100			ns	
Minimum Off Pulse Width	$t_{SYNC\_MIN\_OFF}$	100			ns	
High Logic	$V_{H\ (SYNC)}$			0.8 × V_{VREG2}	V	V_{VREG2} = 3.3 V, −25°C ≤ T_J ≤ +85°C
Low Logic	$V_{L\ (SYNC)}$	0.3 × V_{VREG2}			V	V_{VREG2} = 3.3 V, −25°C ≤ T_J ≤ +85°C
LOGIC INPUTS						
EN Pin						
High Level Threshold	$V_{IH\ (EN)}$			2.15	V	V_{VREG2} = 3.3 V, −25°C ≤ T_J ≤ +85°C
Low Level Threshold	$V_{IL\ (EN)}$	1.45			V	V_{VREG2} = 3.3 V, −25°C ≤ T_J ≤ +85°C
EN34 Pin						
High Level Threshold	$V_{IH\ (EN34)}$			1.25	V	V_{VREG2} = 3.3 V, −25°C ≤ T_J ≤ +85°C
Low Level Threshold	$V_{IL\ (EN34)}$	0.70			V	V_{VREG2} = 3.3 V, −25°C ≤ T_J ≤ +85°C
SCL and SDA Pins						
High Level Threshold	$V_{IH\ (I2C)}$			0.75 × V_{VDDIO}	V	V_{VDDIO} = 3.3 V, −25°C ≤ T_J ≤ +85°C
Low Level Threshold	$V_{IL\ (I2C)}$	0.3 × V_{VDDIO}			V	V_{VDDIO} = 3.3 V, −25°C ≤ T_J ≤ +85°C
LOGIC OUTPUTS						
SDA Pin						
Low Level Output Voltage	$V_{OL\ (SDA)}$			0.4	V	3.0 mA sink current, −25°C ≤ T_J ≤ +85°C
Leakage Current	$I_{LEAK\ (SDA)}$		10		nA	V_{SDA} = 3.3 V
CLKO Pin						
High Level Output Voltage	$V_{OH\ (CLKO)}$	V_{VREG2} − 0.4			V	3.0 mA sink current, −25°C ≤ T_J ≤ +85°C
Low Level Output Voltage	$V_{OL\ (CLKO)}$			0.4	V	3.0 mA sink current, −25°C ≤ T_J ≤ +85°C
$\overline{\text{FAULT}}$ Pin						
Low Level Output Voltage	$V_{OL\ (\overline{FAULT})}$			0.4	V	3.0 mA source current, −25°C ≤ T_J ≤ +85°C
Leakage Current	$I_{LEAK\ (\overline{FAULT})}$		10		nA	$V_{\overline{FAULT}}$ = 3.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER GOOD						
Rising Threshold	$V_{PGOOD\ (R)}$		83		%	Measured at V_{OUT}
Falling Threshold	$V_{PGOOD\ (F)}$		79		%	Measured at V_{OUT}
OVERVOLTAGE/UNDERVOLTAGE						
OVP Threshold	V_{OVP}		125	137	%	Measured at V_{OUT}
UVP Threshold	V_{UVP}	48	65		%	Measured at V_{OUT}
THERMAL SHUTDOWN	TSD					
Rising Threshold	T_{TSD}		165		°C	
Hysteresis	T_{TSD_HYS}		15		°C	

HOUSEKEEPING BLOCK SPECIFICATIONS

T_J = 25°C, V_{VBATT} = 7.2 V, V_{VREG1} = V_{VDRx} = 5 V, V_{VREG2} = V_{VDDIO} = 3.3 V, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LDO1						
Output Voltage (VREG1 Pin)						
Fixed Voltage Range, 1 Bit	V_{VREG1}	5.0		5.5	V	V_{VBATT} = V_{VREG1} + 0.5 V, I_{VREG1} = 10 mA
Voltage Accuracy	$V_{VREG1\ (DEFAULT)}$	−2		+2	%	V_{VBATT} = V_{VREG1} + 0.5 V, I_{VREG1} = 10 mA
Load Regulation	$\Delta V_{VREG1}/I_{VREG1}$		3.5		%/A	I_{VREG1} = 4 mA to 95 mA
Line Regulation	$\Delta V_{VREG1}/V_{VBATT}$		0.03		%/V	V_{VBATT} = (V_{VREG1} + 0.5 V) to 15 V
Current-Limit Threshold	I_{LDO1_ILIM}	390	550		mA	V_{VREG1} = 90% of nominal
Dropout Voltage			0.15		V	I_{VREG1} = 100 mA, V_{VREG1} = 5 V
Input Select Switch On Resistance	R_{DSON_VISW1}		795		mΩ	V_{VISW1} = 5 V
C_{OUT} Discharge Switch On Resistance	R_{DIS_LDO1}		1		kΩ	V_{VREG1} = 1 V
LDO2						
Output Voltage (VREG2 Pin)						
Fixed Voltage Range, 2 Bits	V_{VREG2}	3.0		3.3	V	I_{VREG2} = 10 mA
Voltage Accuracy	$V_{VREG2\ (DEFAULT)}$	−2		+2	%	I_{VREG2} = 10 mA
Load Regulation	$\Delta V_{VREG2}/I_{VREG2}$		5.5		%/A	I_{VREG2} = 4 mA to 95 mA
Current-Limit Threshold	I_{LDO2_ILIM}	290	400		mA	V_{VREG2} = 90% of nominal
Input Select Switch On Resistance	R_{DSON_VISW2}		1409		mΩ	V_{VISW2} = 3.3 V
C_{OUT} Discharge Switch On Resistance	R_{DIS_LDO2}		12		Ω	V_{VREG2} = 1 V
CHARGE PUMP						
C+ Switch On Resistance						
Low-Side	R_{DSON_C+SW1}		1.1		Ω	Source, PVINCP to C+
High-Side	R_{DSON_C+SW2}		1.0		Ω	Sink, C+ to BSTCP
C− Switch On Resistance						
High-Side	R_{DSON_C-SW1}		1.0		Ω	Source, VDR5 to C−
Low-Side	R_{DSON_C-SW2}		785		mΩ	Sink, C− to PGND5
Shunt Switch On Resistance	R_{DSON_CP}		3.3		Ω	BSTCP to PVINCP, EN low
Charge Pump Start-Up Threshold	CP_{START}		4.0		V	At VBATT

DC-TO-DC CONVERTER BLOCK SPECIFICATIONS

T_J = 25°C, V_{VBATT} = 7.2 V, V_{VREG1} = V_{VDRx} = 5 V, V_{VREG2} = V_{VDDIO} = 3.3 V, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL 1 SYNC BUCK REGULATOR						
Channel 1 Output Voltage (FB1 Pin)						
Fixed Voltage Range, 5 Bits	V_{FB1}	0.89		1.20	V	REDUCE_VOUT1 = 0
		0.80		1.11	V	REDUCE_VOUT1 = 1
Feedback Voltage Accuracy at Default VID Code	$V_{FB1\ (DEFAULT)}$	−0.8		+0.8	%	
		−1.3		+1.3	%	−25°C ≤ T_J ≤ +85°C
Load Regulation	$\Delta V_{FB1}/I_{LOAD1}$		0.15		%/A	I_{LOAD1} = 20 mA to 2 A, AUTO-PSM1 = 0
Line Regulation	$\Delta V_{FB1}/V_{PVIN1}$		0.004		%/V	V_{PVIN1} = 5 V to 15 V, I_{LOAD} = 1 A
SW1A Pin						
High-Side Power FET On Resistance	R_{DSON_1AH}		250		mΩ	I_D = 100 mA
Low-Side Power FET On Resistance	R_{DSON_1AL}		130		mΩ	I_D = 100 mA
SW1B Pin						
High-Side Power FET On Resistance	R_{DSON_1BH}		175		mΩ	I_D = 100 mA, GATE_SCAL1 = 0
Low-Side Power FET On Resistance	R_{DSON_1BL}		95		mΩ	I_D = 100 mA
SW1A and SW1B Pins						
Switch Current Limit	I_{CL1}	3.1	4.0		A	Valley current, −25°C ≤ T_J ≤ +85°C
Minimum Off Time	$t_{OFF1\ (MIN)}$		115		ns	
Minimum Duty Cycle	D_{MIN1}		0		%	
Soft Start Time	t_{SS1}		4		ms	SS1 = 10
C_{OUT} Discharge Switch On Resistance	R_{DIS1}		125		Ω	V_{FB1} = 1 V
CHANNEL 2 SYNC BUCK REGULATOR						
Channel 2 Output Voltage (FB2 Pin)						
Fixed Voltage Range, 4 Bits	V_{FB2}	1.0		3.3	V	
Feedback Voltage Accuracy at Default VID Code	$V_{FB2\ (DEFAULT)}$	−0.8		+0.8	%	
		−1.3		+1.3	%	−25°C ≤ T_J ≤ +85°C
Load Regulation	$\Delta V_{FB2}/I_{LOAD2}$		0.25		%/A	I_{LOAD2} = 10 mA to 1.0 A, AUTO-PSM2 = 0
Line Regulation	$\Delta V_{FB2}/V_{PVIN2}$		0.004		%/V	V_{PVIN2} = 5 V to 15 V, I_{LOAD2} = 500 mA
SW2 Pins						
High-Side Power FET On Resistance	R_{DSON_2H}		235		mΩ	I_D = 100 mA
Low-Side Power FET On Resistance	R_{DSON_2L}		165		mΩ	I_D = 100 mA
Switch Current Limit	I_{CL2}	1.2	1.8		A	Valley current, −25°C ≤ T_J ≤ +85°C
Minimum Off Time	$t_{OFF2\ (MIN)}$		100		ns	
Minimum Duty Cycle	D_{MIN2}		0		%	
Soft Start Time	t_{SS2}		4		ms	SS2 = 10
C_{OUT} Discharge Switch On Resistance	R_{DIS2}		125		Ω	V_{FB2} = 1 V
CHANNEL 3 SYNC BUCK REGULATOR						
Channel 3 Output Voltage (FB3 Pin)						
Fixed Voltage Range, 3 Bits	V_{FB3}	1.2		1.8	V	
Minimum Adjustable Voltage			0.8		V	VID3 = 111
Feedback Voltage Accuracy at Default VID Code	$V_{FB3\ (DEFAULT)}$	−0.8		+0.8	%	
		−1.3		+1.3	%	−25°C ≤ T_J ≤ +85°C
Load Regulation	$\Delta V_{FB3}/I_{LOAD3}$		0.17		%/A	I_{LOAD3} = 15 mA to 1.5 A, AUTO-PSM3 = 0
Line Regulation	$\Delta V_{FB3}/V_{PVIN3}$		0.003		%/V	V_{PVIN3} = 5 V to 15 V, I_{LOAD3} = 700 mA

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SW3 Pins						
High-Side Power FET On Resistance	R_{DSON_3H}		155		mΩ	I_D = 100 mA
Low-Side Power FET On Resistance	R_{DSON_3L}		100		mΩ	I_D = 100 mA
Switch Current Limit	I_{CL3}	2.05	2.8		A	Valley current, −25°C ≤ T_J ≤ +85°C
Minimum Off Time	$t_{OFF3\ (MIN)}$		90		ns	
Minimum Duty Cycle	D_{MIN3}		0		%	
Soft Start Time	t_{SS3}		4		ms	SS3 = 10
C_{OUT} Discharge Switch On Resistance	R_{DIS3}		125		Ω	V_{FB3} = 1 V
CHANNEL 4 SYNC BUCK REGULATOR						
Channel 4 Output Voltage (FB4 Pin)						
Fixed Voltage Range, 3 Bits	V_{FB4}	1.8		3.55	V	
Minimum Adjustable Voltage			0.8		V	VID4 = 111
Feedback Voltage Accuracy at Default VID Code	$V_{FB4\ (DEFAULT)}$	−1		+1	%	
		−2		+2	%	−25°C ≤ T_J ≤ +85°C
Load Regulation	$\Delta V_{FB4}/I_{LOAD4}$		0.10		%/A	I_{LOAD4} = 10 mA to 800 mA, AUTO-PSM4 = 0
Line Regulation	$\Delta V_{FB4}/V_{PVIN4}$		0.003		%/V	V_{PVIN4} = 5 V to 15 V, I_{LOAD4} = 400 mA
SW4 Pin						
High-Side Power FET On Resistance	R_{DSON_4H}		350		mΩ	I_D = 100 mA
Low-Side Power FET On Resistance	R_{DSON_4L}		345		mΩ	I_D = 100 mA
Switch Current Limit	I_{CL4}	0.96	1.4		A	Peak current, −25°C ≤ T_J ≤ +85°C
Minimum On Time	$t_{ON4\ (MIN)}$		75		ns	
Maximum Duty Cycle	D_{MAX4}		100		%	
Soft Start Time	t_{SS4}		4		ms	SS4 = 10
C_{OUT} Discharge Switch On Resistance	R_{DIS4}		125		Ω	V_{FB4} = 1 V
CHANNEL 5 SYNC BUCK REGULATOR						
Channel 5 Output Voltage (FB5 Pin)						
Fixed Voltage Range, 3 Bits	V_{FB5}	3.0		5.0	V	
Feedback Voltage Accuracy at Default VID Code	$V_{FB5\ (DEFAULT)}$	−1		+1	%	
		−2		+2	%	−25°C ≤ T_J ≤ +85°C
Load Regulation	$\Delta V_{FB5}/I_{LOAD5}$		0.05		%/A	I_{LOAD5} = 20 mA to 2 A, AUTO-PSM5 = 0
Line Regulation	$\Delta V_{FB5}/V_{PVIN5}$		0.001		%/V	V_{PVIN5} = 5 V to 15 V, I_{LOAD5} = 1 A
SW5 Pins						
High-Side Power FET On Resistance	R_{DSON_5H}		200		mΩ	I_D = 100 mA
Low-Side Power FET On Resistance	R_{DSON_5L}		120		mΩ	I_D = 100 mA
Switch Current Limit	I_{CL5}	2.4	3		A	Peak current, −25°C ≤ T_J ≤ +85°C
Minimum On Time	$t_{ON5\ (MIN)}$		75		ns	
Maximum Duty Cycle	D_{MAX5}		100		%	
Soft Start Time	t_{SS5}		4		ms	SS5 = 10
C_{OUT} Discharge Switch On Resistance	R_{DIS5}		125		Ω	V_{FB5} = 1 V
CHANNEL 6 BUCK BOOST REGULATOR						
Channel 6 Output Voltage (FB6 Pin)						
Fixed Voltage Range, 4 Bits	V_{FB6}	3.5		5.5	V	
Minimum Adjustable Voltage			0.8		V	VID6 = 1111
Accuracy at Default VID Code	$V_{VOUT6\ (DEFAULT)}$	−1		+1	%	
		−2		+2	%	−25°C ≤ T_J ≤ +85°C
Load Regulation	$\Delta V_{VOUT6}/I_{LOAD6}$		0.05		%/A	Buck boost configuration, I_{LOAD6} = 15 mA to 1.5 A, AUTO-PSM6 = 0
Line Regulation	$\Delta V_{VOUT6}/V_{PVIN6}$		0.001		%/V	V_{PVIN6} = 5 V to 15 V, I_{LOAD6} = 700 mA

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SW6A Pins						
Low-Side Power FET On Resistance	R_{DSON_6AL}		95		mΩ	I_D = 100 mA, V_{VDR6} = 5 V
High-Side Power FET On Resistance	R_{DSON_6AH}		60		mΩ	I_D = 100 mA, V_{VDR6} = 5 V
High-Side Switch Current Limit	I_{CL6A}	3.2	4.4		A	Peak current, −25°C ≤ T_J ≤ +85°C
Minimum On Time	$t_{ON6\ (MIN)}$		80		ns	SW6A high-side on time
SW6B Pins						
Low-Side Power FET On Resistance	R_{DSON_6BL}		50		mΩ	I_D = 100 mA
High-Side Power FET On Resistance	R_{DSON_6BH}		55		mΩ	I_D = 100 mA
Boost Minimum Duty Cycle	D_{MIN6B}		0		%	SW6B low-side duty cycle
Soft Start Time	t_{SS6}		4		ms	SS6 = 10
C_{OUT} Discharge Switch On Resistance	R_{DIS6}		110		Ω	V_{VOUT6} = 1 V

LINEAR REGULATOR BLOCK SPECIFICATIONS

T_J = 25°C, V_{VBATT} = 7.2 V, V_{VREG1} = V_{VDRx} = 5 V, V_{VREG2} = V_{VDDIO} = 3.3 V, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL 7 LDO REGULATOR						
Channel 7 Output Voltage	V_{VOLDO7}	5		12	V	V_{VILDO7} = V_{VOLDO7} + 0.5 V
Voltage Accuracy	$V_{VOLDO7\ (DEFAULT)}$	−1.5		+1.5	%	V_{VILDO7} = V_{VOLDO7} + 0.5 V, I_{LOAD7} = 1 mA
		−2.5		+2.5	%	V_{VILDO7} = V_{VOLDO7} + 0.5 V, I_{LOAD7} = 1 mA, −25°C ≤ T_J ≤ +85°C
Load Regulation	$\Delta V_{VOLDO7}/I_{LOAD7}$		0.005		%/mA	V_{VILDO7} = V_{VOLDO7} + 0.5 V, I_{LOAD7} = 1 mA to 20 mA
Line Regulation	$\Delta V_{VOLDO7}/V_{VILDO7}$		0.007		%/V	V_{VILDO7} = (V_{VOLDO7} + 0.5 V) to 25 V, I_{LOAD7} = 1 mA
Dropout Voltage[1]	V_{DROP}		75		mV	V_{VOLDO7} programmed to 12 V, I_{VOLDO7} = 10 mA
Current Limit	I_{CL7}	30	50		mA	V_{VOLDO7} = 95% of nominal
Soft Start Time	t_{SS7}		4		ms	SS7 = 1
C_{OUT} Discharge Switch On Resistance	R_{DIS7}		1		kΩ	V_{VOLDO7} = 1 V

[1] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage.

I²C INTERFACE TIMING SPECIFICATIONS

T_J = 25°C, V_{VBATT} = 7.2 V, V_{VDRx} = 5 V, V_{VREG2} = V_{VDDIO} = 3.3 V, unless otherwise noted.

Table 5.

Parameter	Min	Typ	Max	Unit	Description
f_{SCL}			400	kHz	SCL clock frequency
t_{HIGH}	0.6			µs	SCL high time
t_{LOW}	1.3			µs	SCL low time
$t_{SU,DAT}$	100			ns	Data setup time
$t_{HD,DAT}$	0		0.9	µs	Data hold time[1]
$t_{SU,STA}$	0.6			µs	Setup time for repeated start
$t_{HD,STA}$	0.6			µs	Hold time for start or repeated start
t_{BUF}	1.3			µs	Bus free time between a stop condition and a start condition
$t_{SU,STO}$	0.6			µs	Setup time for a stop condition
t_R	20 + 0.1 × C_B[2]		300	ns	Rise time of SCL and SDA
t_F	20 + 0.1 × C_B[2]		300	ns	Fall time of SCL and SDA
t_{SP}	0		50	ns	Pulse width of suppressed spike
C_B[2]			400	pF	Capacitive load for each bus line

[1] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} minimum of the SCL signal) to bridge the undefined region of the SCL falling edge.
[2] C_B is the total capacitance of one bus line in picofarads (pF).

Timing Diagram

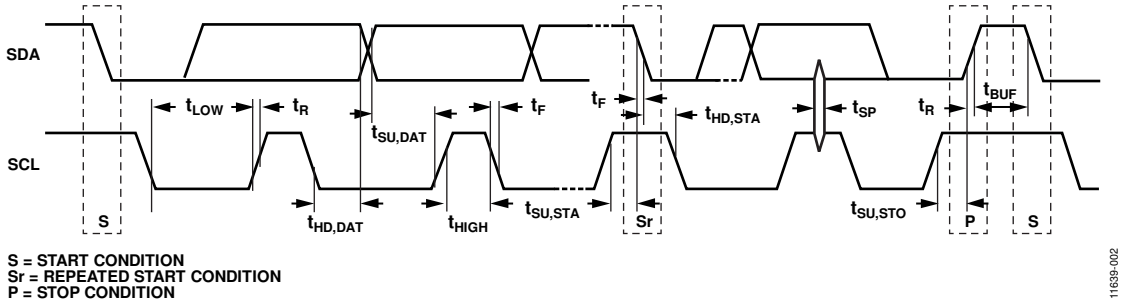

Figure 2. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
VBATT to GND	−0.3 V to +18 V
VDDIO to GND	−0.3 V to +4.0 V
VISW1 to GND	−0.3 V to +6.5 V
VISW2 to GND	−0.3 V to +4.0 V
VREG1 to GND	−0.3 V to +6.5 V
VREG2 to GND	−0.3 V to +4.0 V
EN to GND	−0.3 V to +18 V
EN34 to GND	−0.3 V to +6.5 V
$\overline{\text{FAULT}}$ to GND	−0.3 V to +4.0 V
BSTCP to PVINCP	−0.3 V to +6.5 V
BSTCP to GND	−0.3 V to +23 V
C+ to PVINCP	−0.3 V to (V_{VDR5} + 0.3 V)
C− to PGND5	−0.3 V to (V_{VDR5} + 0.3 V)
PVINx to PGNDx	−0.3 V to +18 V
VDRx to PGNDx	−0.3 V to +6.5 V
BST16, BST23, BST45 to PVINx	−0.3 V to +6.5 V
FB1, FB2, FB3 to GND	−0.3 V to +4.0 V
FB4, FB5, FB6 to GND	−0.3 V to +6.5 V
VOUT6 to PGND6	−0.3 V to +6.5 V
SW1A, SW1B to PGND1	−2.0 V to +18 V
SW2 to PGND2	−2.0 V to +18 V
SW3 to PGND3	−2.0 V to +18 V
SW4 to PGND4	−2.0 V to +18 V
SW5 to PGND5	−2.0 V to +18 V
SW6A to PGND6	−2.0 V to +18 V
SW6B to PGND6	−0.5 V to (V_{VOUT6} + 2.0 V) or +6.5 V, whichever is lower
PGNDx to GND	−0.3 V to +0.3 V
VILDO7 to GND	−0.3 V to +28 V
VOLDO7 to GND	−0.3 V to +18 V
FREQ to GND	−0.3 V to (V_{VREG2} + 0.3 V)
SYNC to GND	−0.3 V to +4.0 V
CLKO to GND	−0.3 V to (V_{VREG2} + 0.3 V)
SCL to GND	−0.3 V to +4.0 V
SDA to GND	−0.3 V to +4.0 V
Storage Temperature Range	−65°C to +150°C
Operating Ambient Temperature Range	−25°C to +85°C
Operating Junction Temperature Range	−25°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for worst-case conditions; that is, a device soldered in a circuit board for surface-mount packages. Note that actual θ_{JA} depends on the application environment.

Table 7. Thermal Resistance

PCB Type[1]	θ_{JA}[2]	θ_{JB}[2]	Unit
1S0P	60.6	7.3	°C/W
2S2P	26.9	4.5	°C/W

[1] PCB type conforms to JEDEC JESD51-9 standard.
[2] 1.25 W power dissipation with zero airflow.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

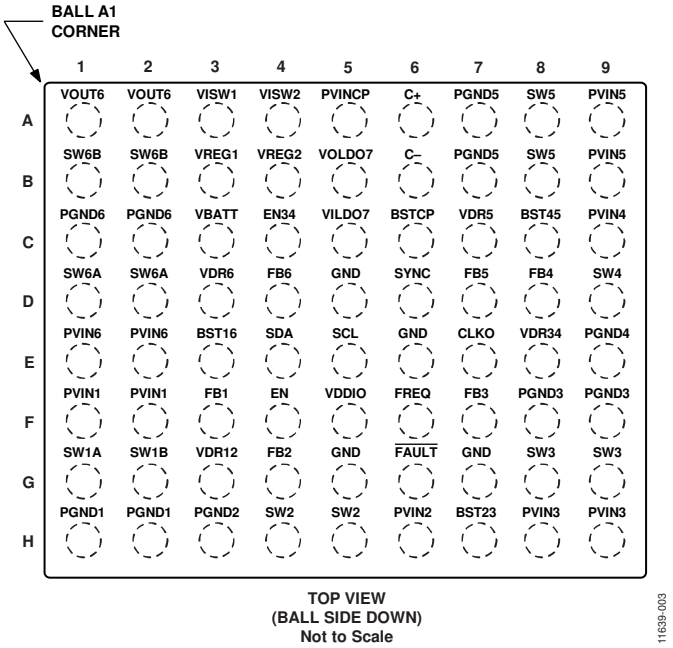

Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1A	VOUT6	Output Voltage for Channel 6.
2A	VOUT6	Output Voltage for Channel 6.
3A	VISW1	Input for an External Regulator Output. A 5.0 V to 5.5 V regulator connected to the VISW1 pin can take over from LDO1 to supply the internal circuit of the ADP5080 and the VREG1 load. If this pin is not used, connect it to GND.
4A	VISW2	Input for an External Regulator Output. A 3.0 V to 3.3 V regulator connected to the VISW2 pin can take over from LDO2 to supply the internal circuit of the ADP5080 and the VREG2 load. If this pin is not used, connect it to GND.
5A	PVINCP	Input Power Supply for the Charge Pump.
6A	C+	Flying Capacitor Terminal for the Charge Pump.
7A	PGND5	Power Ground for Channel 5.
8A	SW5	Switching Node for Channel 5.
9A	PVIN5	Input Power Supply for Channel 5.
1B	SW6B	Secondary Side Boost Switching Node for Channel 6.
2B	SW6B	Secondary Side Boost Switching Node for Channel 6.
3B	VREG1	Output Voltage for LDO1.
4B	VREG2	Output Voltage for LDO2.
5B	VOLDO7	Output Voltage for Channel 7. Leave this pin open if not used.
6B	C–	Flying Capacitor Terminal for the Charge Pump.
7B	PGND5	Power Ground for Channel 5.
8B	SW5	Switching Node for Channel 5.
9B	PVIN5	Input Power Supply for Channel 5.
1C	PGND6	Power Ground for Channel 6.
2C	PGND6	Power Ground for Channel 6.
3C	VBATT	Power Supply Input for the Internal Circuits. Connect this pin to the battery.
4C	EN34	Independent Enable Input for Channel 3 and Channel 4. If this pin is not used, connect it to GND.
5C	VILDO7	Input Power Supply for Channel 7. If this pin is not used, connect it to VBATT.
6C	BSTCP	Output Voltage for Charge Pump.
7C	VDR5	Low-Side FET Driver Power Supply for Channel 5. Connect this pin to VREG1.
8C	BST45	High-Side FET Driver Power Supply for Channel 4 and Channel 5.

Pin No.	Mnemonic	Description
9C	PVIN4	Input Power Supply for Channel 4.
1D	SW6A	Primary Side Switching Node for Channel 6.
2D	SW6A	Primary Side Switching Node for Channel 6.
3D	VDR6	Low-Side FET Driver Power Supply for Channel 6. Connect this pin to VREG1.
4D	FB6	Feedback Node for Channel 6.
5D	GND	Ground. All GND pins must be connected.
6D	SYNC	External Clock Input (CMOS Input Port). If this pin is not used, connect it to GND.
7D	FB5	Feedback Node for Channel 5.
8D	FB4	Feedback Node for Channel 4.
9D	SW4	Switching Node for Channel 4.
1E	PVIN6	Input Power Supply for Channel 6.
2E	PVIN6	Input Power Supply for Channel 6.
3E	BST16	High-Side FET Driver Power Supply for Channel 1 and Channel 6.
4E	SDA	Data Input/Output for I^2C Interface. Open-drain I/O port.
5E	SCL	Clock Input for I^2C Interface. For start-up requirements, see the I^2C Interface section.
6E	GND	Ground. All GND pins must be connected.
7E	CLKO	Clock Output (CMOS Output Port). CLKO replicates the Channel 1 switching clock. This output is not available when the SYNC pin is driven by an external clock. If this pin is not used, leave it open.
8E	VDR34	Low-Side FET Driver Power Supply for Channel 3 and Channel 4. Connect this pin to VREG1.
9E	PGND4	Power Ground for Channel 4.
1F	PVIN1	Input Power Supply for Channel 1.
2F	PVIN1	Input Power Supply for Channel 1.
3F	FB1	Feedback Node for Channel 1.
4F	EN	Enable Control Input.
5F	VDDIO	Supply Voltage for I^2C Interface. Typically, this pin is connected externally to VREG2 or to the host I/O voltage.
6F	FREQ	Frequency Pin for the Internal Oscillator. To select the internal clock source oscillator, connect an external 100 kΩ resistor from the FREQ pin to GND.
7F	FB3	Feedback Node for Channel 3.
8F	PGND3	Power Ground for Channel 3.
9F	PGND3	Power Ground for Channel 3.
1G	SW1A	Switching Node for Channel 1.
2G	SW1B	Switching Node for Channel 1.
3G	VDR12	Low-Side FET Driver Power Supply for Channel 1 and Channel 2. Connect this pin to VREG1.
4G	FB2	Feedback Node for Channel 2.
5G	GND	Ground. All GND pins must be connected.
6G	$\overline{\text{FAULT}}$	Fault Status Output Pin. This open-drain output port goes low when a fault occurs. Leave open if not used.
7G	GND	Ground. All GND pins must be connected.
8G	SW3	Switching Node for Channel 3.
9G	SW3	Switching Node for Channel 3.
1H	PGND1	Power Ground for Channel 1.
2H	PGND1	Power Ground for Channel 1.
3H	PGND2	Power Ground for Channel 2.
4H	SW2	Switching Node for Channel 2.
5H	SW2	Switching Node for Channel 2.
6H	PVIN2	Input Power Supply for Channel 2.
7H	BST23	High-Side FET Driver Power Supply for Channel 2 and Channel 3.
8H	PVIN3	Input Power Supply for Channel 3.
9H	PVIN3	Input Power Supply for Channel 3.

TYPICAL PERFORMANCE CHARACTERISTICS

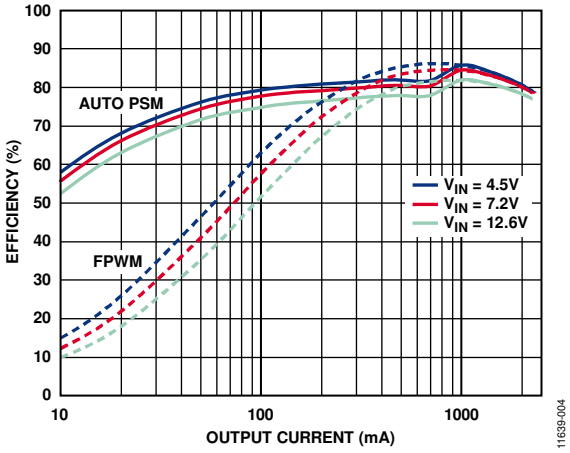

Figure 4. Channel 1 Efficiency, V_{OUT} = 1.1 V

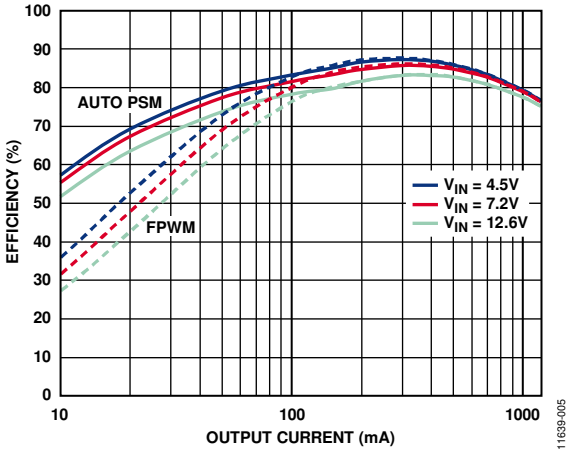

Figure 5. Channel 2 Efficiency, V_{OUT} = 1.2 V

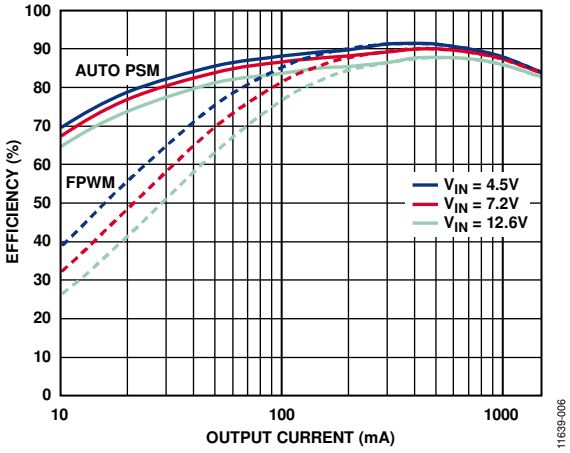

Figure 6. Channel 3 Efficiency, V_{OUT} = 1.8 V

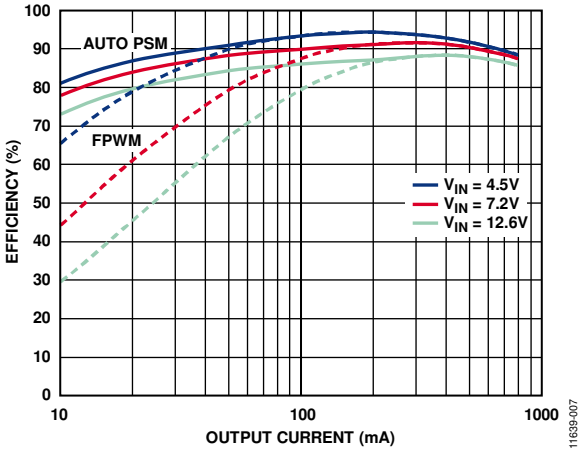

Figure 7. Channel 4 Efficiency, V_{OUT} = 3.3 V

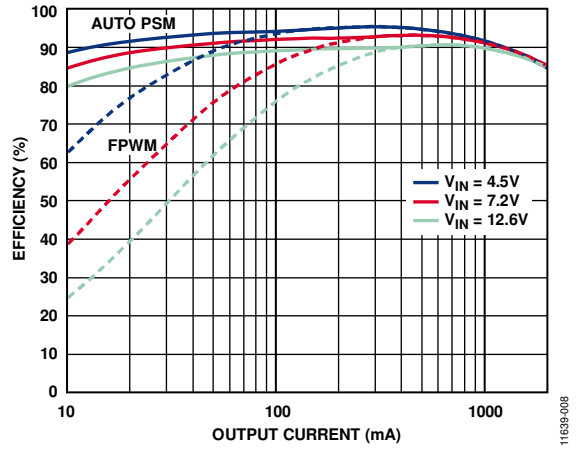

Figure 8. Channel 5 Efficiency, V_{OUT} = 3.3 V

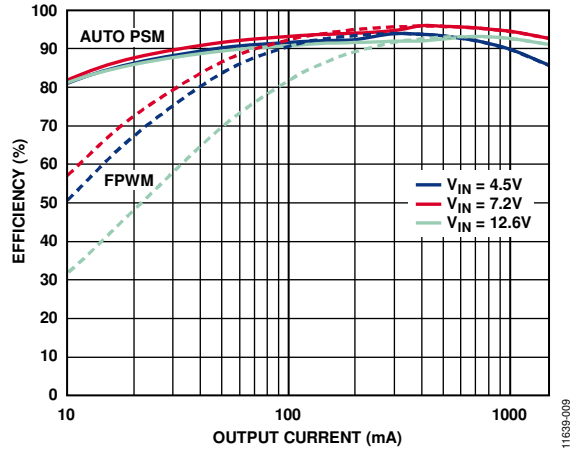

Figure 9. Channel 6 Efficiency, V_{OUT} = 5 V

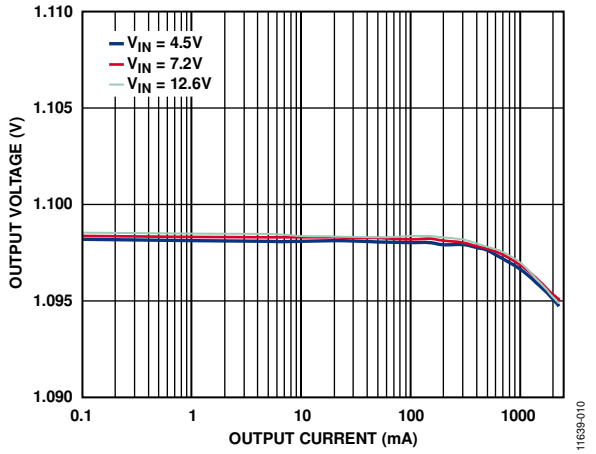

Figure 10. Channel 1 Load Regulation

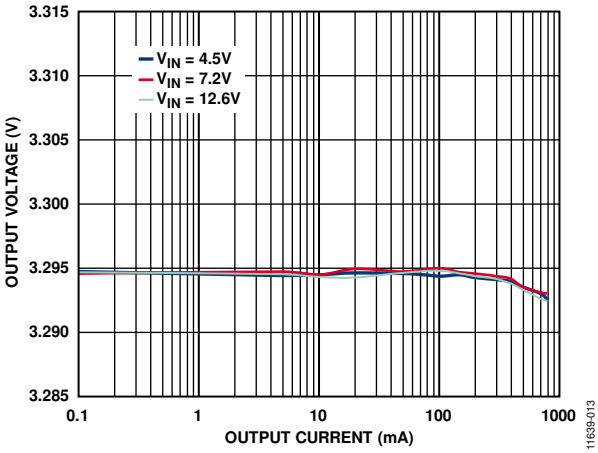

Figure 13. Channel 4 Load Regulation

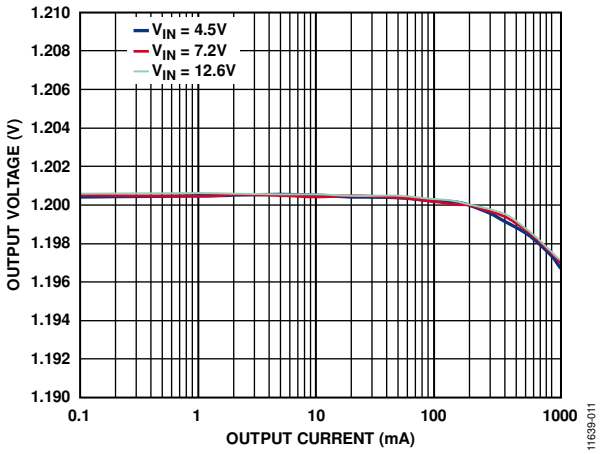

Figure 11. Channel 2 Load Regulation

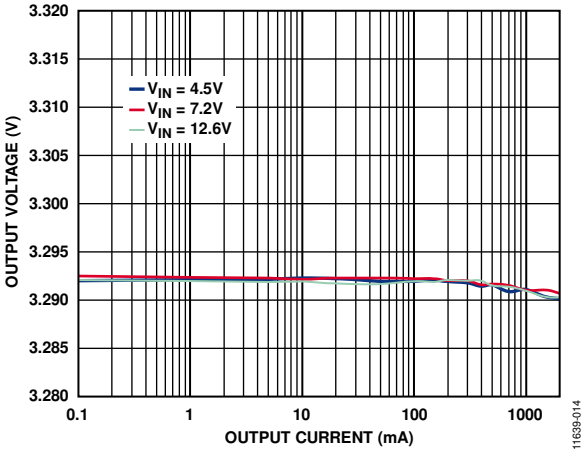

Figure 14. Channel 5 Load Regulation

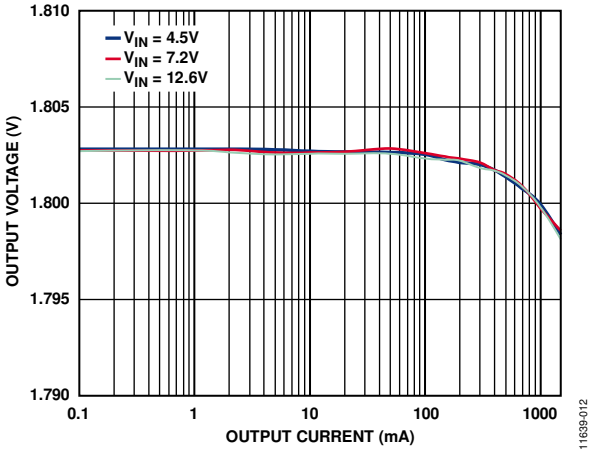

Figure 12. Channel 3 Load Regulation

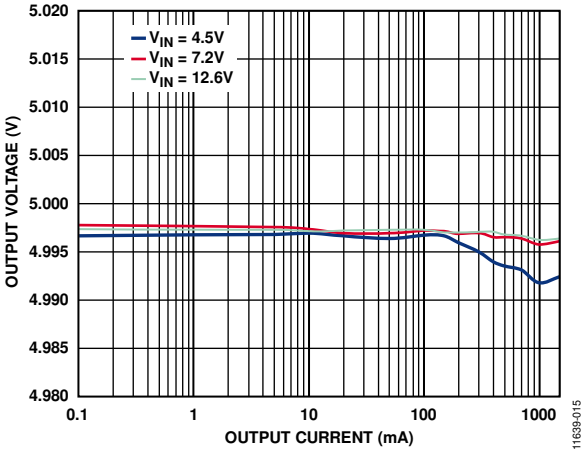

Figure 15. Channel 6 Load Regulation

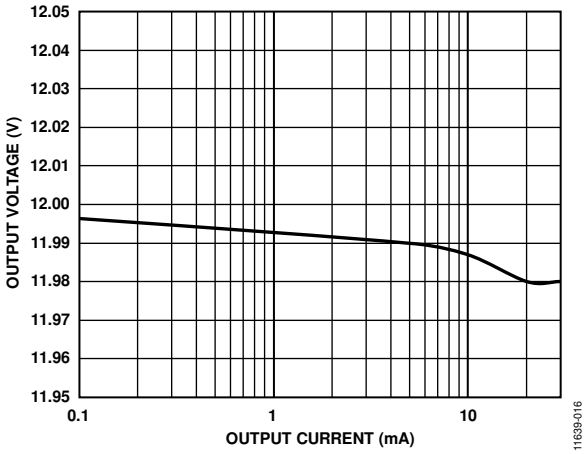

Figure 16. Channel 7 Load Regulation, VILDO7 = 16 V

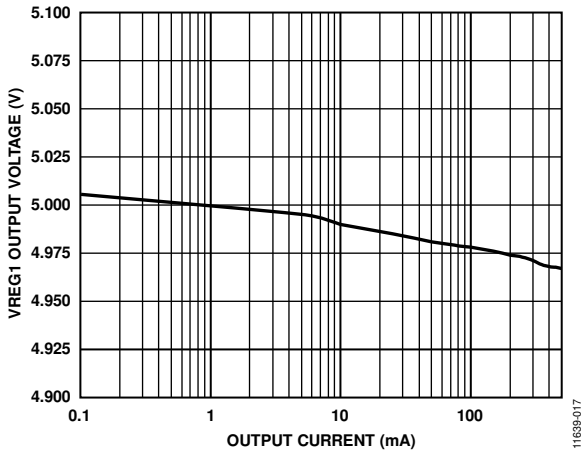

Figure 17. VREG1 Load Regulation

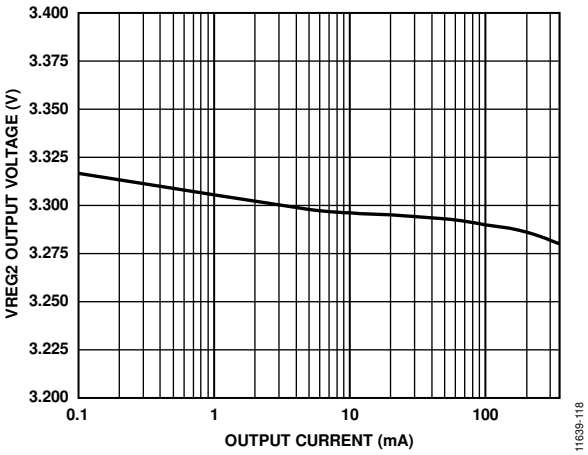

Figure 18. VREG2 Load Regulation

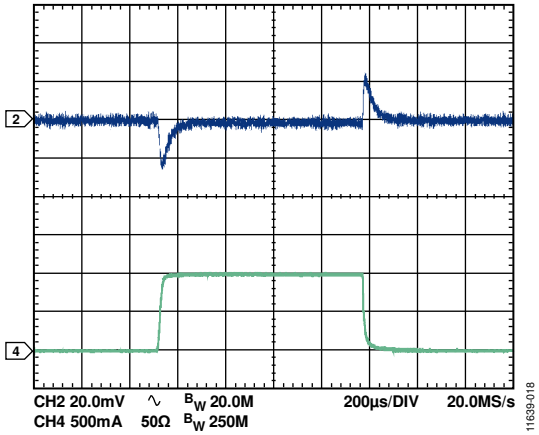

Figure 19. Channel 1 Load Transient, V_{OUT} = 1.1 V, FPWM Mode

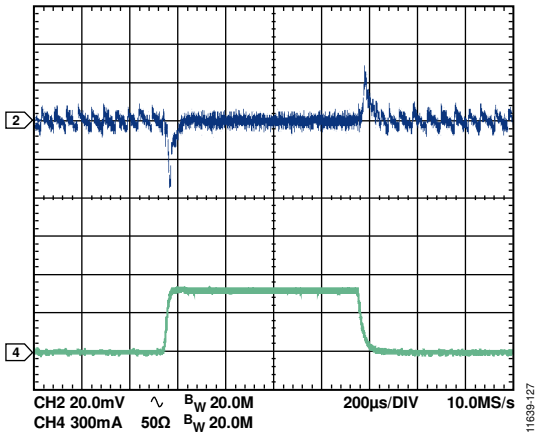

Figure 20. Channel 1 Load Transient, V_{OUT} = 1.1 V, Auto PSM Mode

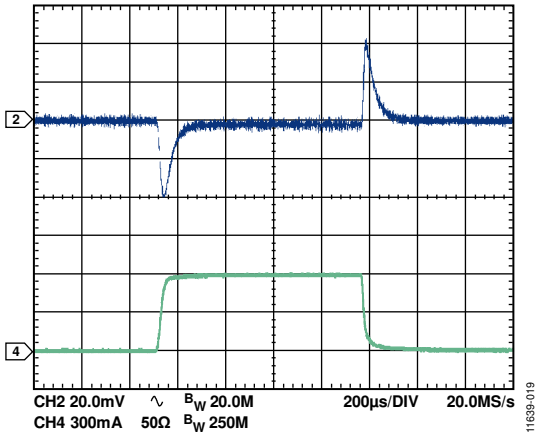

Figure 21. Channel 2 Load Transient, V_{OUT} = 1.2 V, FPWM Mode

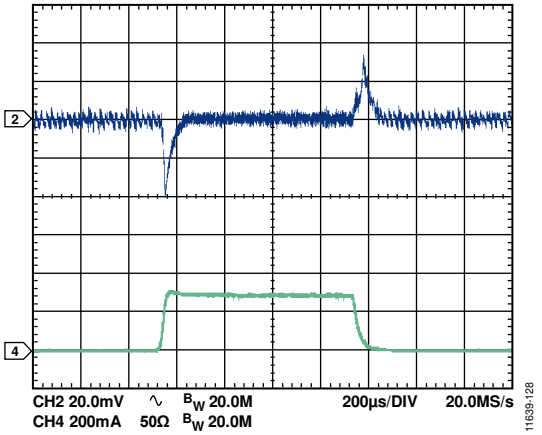

Figure 22. Channel 2 Load Transient, V_{OUT} = 1.2 V, Auto PSM Mode

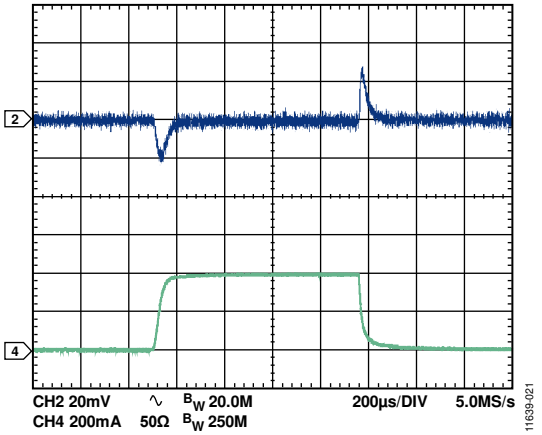

Figure 25. Channel 4 Load Transient, V_{OUT} = 3.3 V, FPWM Mode

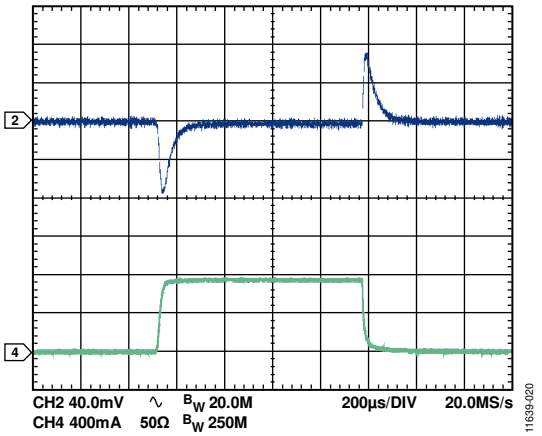

Figure 23. Channel 3 Load Transient, V_{OUT} = 1.8 V, FPWM Mode

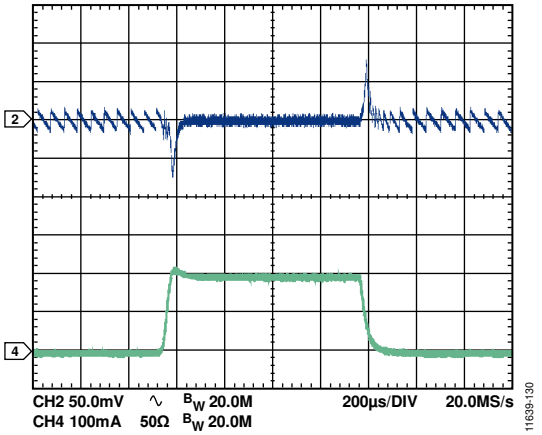

Figure 26. Channel 4 Load Transient, V_{OUT} = 3.3 V, Auto PSM Mode

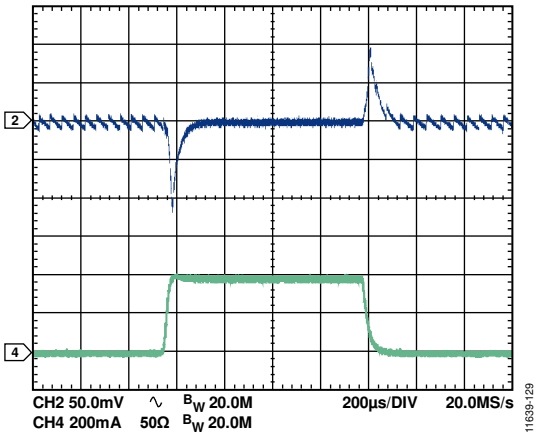

Figure 24. Channel 3 Load Transient, V_{OUT} = 1.8 V, Auto PSM Mode

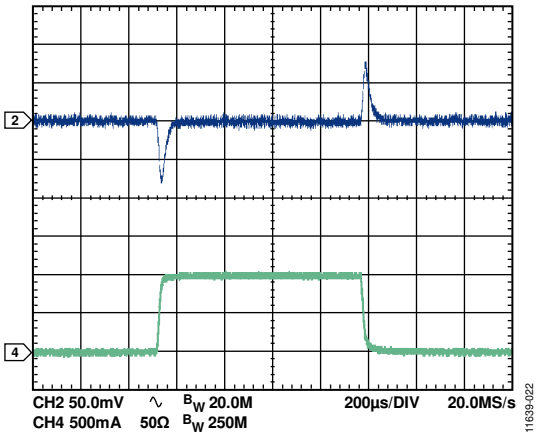

Figure 27. Channel 5 Load Transient, V_{OUT} = 3.3 V, FPWM Mode

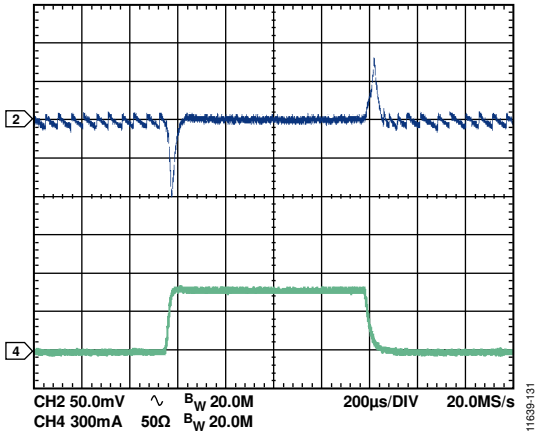

Figure 28. Channel 5 Load Transient, V_{OUT} = 3.3 V, Auto PSM Mode

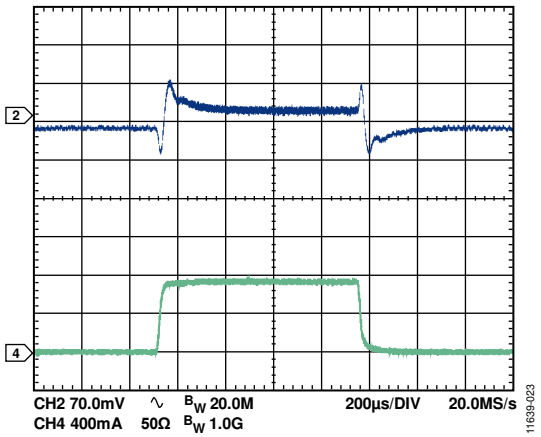

Figure 29. Channel 6 Load Transient, V_{OUT} = 5 V, FPWM Mode

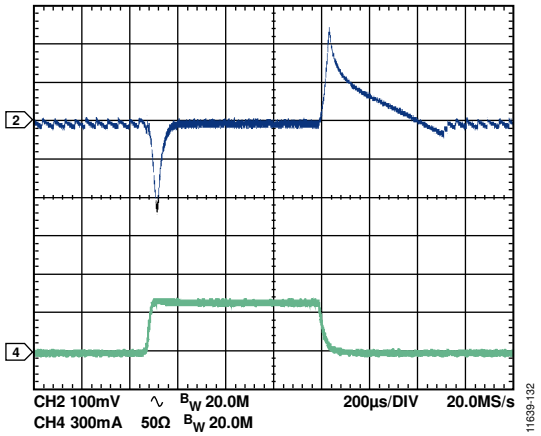

Figure 30. Channel 6 Load Transient, V_{OUT} = 5 V, Auto PSM Mode

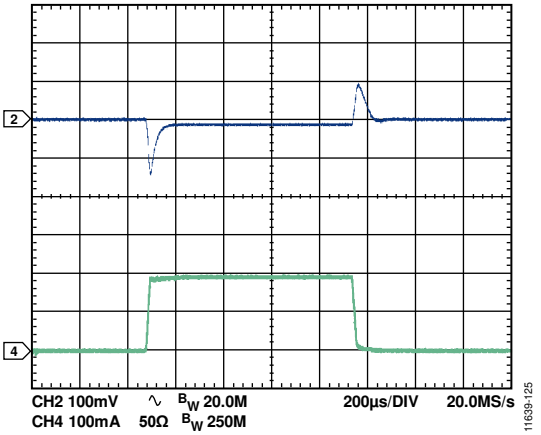

Figure 31. VREG1 Load Transient, VREG1 = 5 V

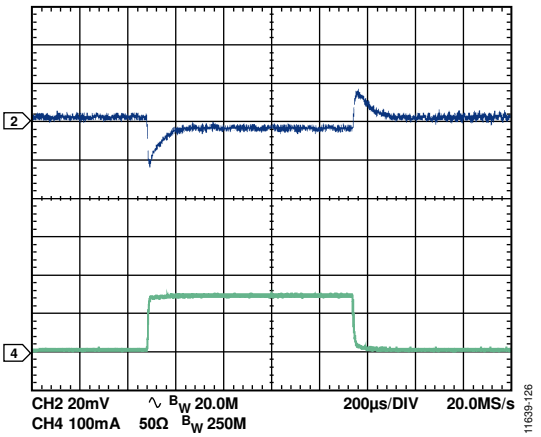

Figure 32. VREG2 Load Transient, VREG2 = 3.3 V

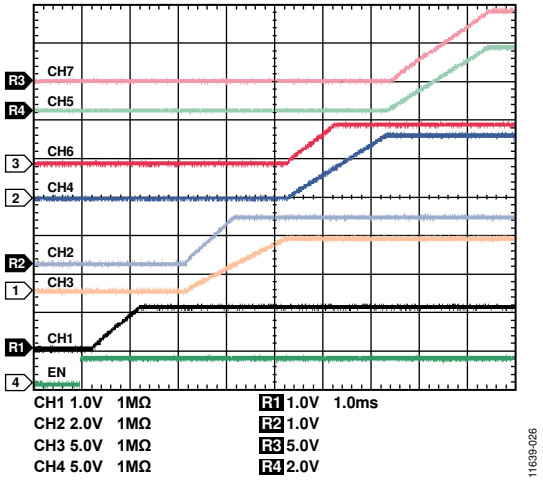

Figure 33. Startup

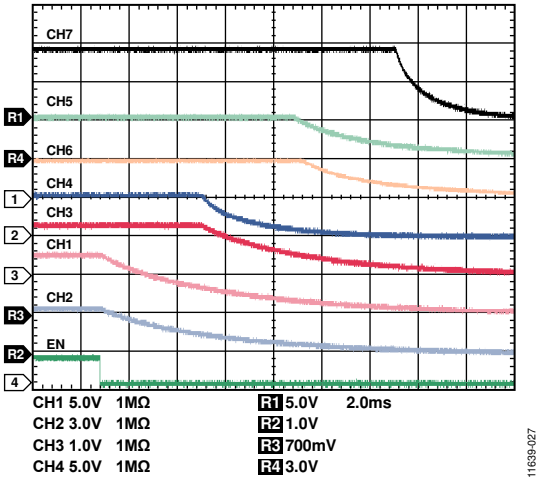

Figure 34. Shutdown

APPLICATION CIRCUIT

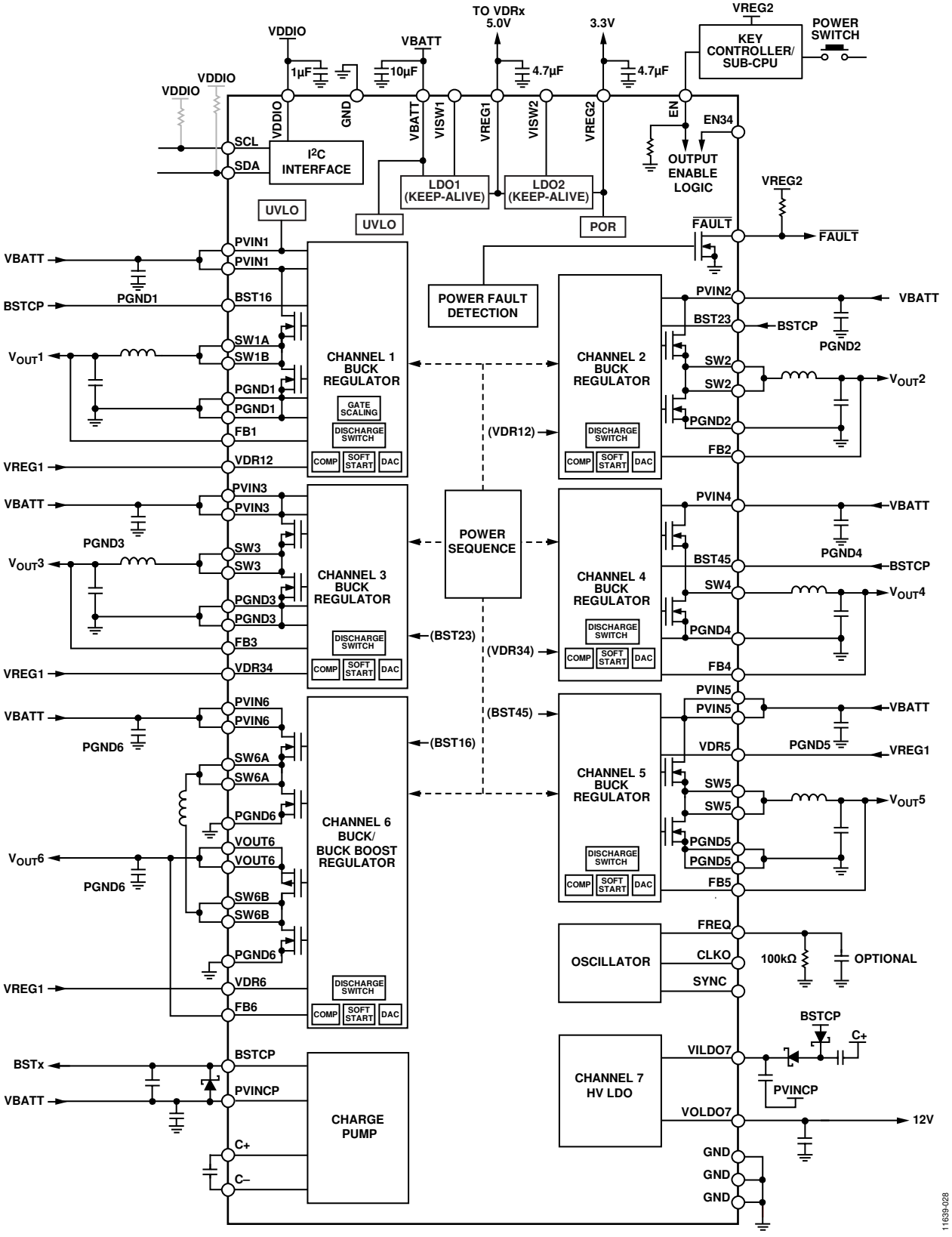

Figure 35. Typical Application Circuit

THEORY OF OPERATION

The ADP5080 is a fully integrated, high efficiency power solution for multicell lithium ion battery applications. The device can connect directly to the battery, which eliminates the need for preregulators and increases the battery life of the system.

The ADP5080 integrates two keep-alive LDO regulators, five synchronous buck regulators, one configurable buck boost regulator, and one high voltage LDO regulator. An integrated charge pump provides the switch driver power supply. Along with the integrated power FETs and drivers, integrated compensation, soft start, and FB dividers contribute to minimize the number of external components and the PCB layout space, providing significant advantages for portable applications.

Factory programming sets the default values for the output voltages, fault behavior, switching frequency, start-up time, and other functions. These values can also be programmed via the I^2C interface. The ADP5080 features a built-in sequencer that provides automatic startup and shutdown timing based on these settings.

UVLO AND POR

The undervoltage lockout (UVLO) and power-on reset (POR) functions prevent abnormal behavior and force a smooth shutdown when input voltages fall below the minimum required levels. The ADP5080 incorporates UVLO on VBATT, PVIN1, and VDR12; it incorporates POR on VREG2. The thresholds are low enough to ensure normal operation down to 4 V at VBATT with ample hysteresis to avoid chattering.

Undervoltage Lockout (UVLO)

If the PVIN1 voltage of Channel 1 falls below the UVLO threshold ($V_{UVLO\ (F)}$), all channels, as well as the charge pump, are turned off. However, LDO1 and LDO2 remain operational.

As the input voltage rises, the regulator channels do not restart automatically. EN must be toggled after a UVLO event to restart channels in sequencer mode or manual mode. For more information about enabling channels using sequencer mode and manual mode, see the Enabling and Disabling the Output Channels section.

The VDRx pins provide the gate drive voltage to the internal power FETs. If the VDR12 voltage falls below 2.9 V (typical), all channels except LDO1 and LDO2 shut down to prevent malfunction of the power FETs. As with a PVIN UVLO event, EN must be toggled to restart channel operation.

Power-On Reset (POR)

If the VBATT voltage falls below its UVLO threshold ($V_{UVLO\ (BATT)}$), all channels, including LDO1 and LDO2, are shut down. This event forces a power-on reset.

VREG2 is the voltage supply for the internal digital circuit blocks. If the VREG2 voltage falls below the power-on reset threshold ($V_{UVLO\ (POR)}$) of 2.4 V typical, the ADP5080 shuts down, and all registers are reset to their default values.

DISCHARGE SWITCH

The ADP5080 integrates discharge switches for Channel 1 to Channel 7. These switches help to discharge the output capacitors quickly when a channel is turned off. The discharge switches are turned on when the EN signal goes low or when a channel is manually turned off via I^2C control, provided that the discharge function was enabled by setting the DSCGx_ON bit (x is 1 to 7) in Register 1. The default values for the discharge switches are factory fuse programmed.

KEEP-ALIVE LDO REGULATORS

The keep-alive LDO linear regulators (LDO1 and LDO2) are kept alive as long as a valid supply voltage is applied to the VBATT pin. The LDO regulators are used to power the internal control block of the ADP5080 so that the device is ready for the enable (EN) signal. The outputs of LDO1 and LDO2 are also available via the VREG1 and VREG2 pins for external circuits that are also kept alive during system standby.

When VBATT initially rises above the UVLO threshold, LDO1 begins operation, followed by LDO2. When all UVLO thresholds are cleared, the ADP5080 is in standby mode and ready to be enabled. If an external voltage is used to drive VDDIO, VDDIO can be on before VBATT; otherwise, LDO2 provides power to VDDIO via the VREG2 output.

LDO1

LDO1 regulates the supply voltage applied to the VBATT pin to either 5.0 V or 5.5 V and is capable of providing up to 400 mA. LDO1 internally supplies LDO2, as well as external circuits, including the VDRx pins supplied through the VREG1 pin.

The LDO1 output is enabled when the VBATT pin voltage rises above the UVLO threshold and is disabled when the VBATT pin voltage falls below the UVLO threshold.

VISW1 Input

A 5.0 V to 5.5 V regulator connected to the VISW1 pin can take over from LDO1 to supply the internal circuit of the ADP5080 and the VREG1 load. To enable this feature, set the SEL_INP_LDO1 bit (Bit 0 in Register 33) high after the VISW1 pin voltage settles above 4.7 V.

If the VISW1 pin voltage falls below 4.5 V, LDO1 resumes control automatically. However, if the VISW1 source is disabled, it is recommended that the SEL_INP_LDO1 bit be reset to 0 before turning off the VISW1 pin source.

The use of an external regulator connected to the VISW1 pin is intended to achieve better system power efficiency by allowing a switching power supply to take over the LDO1 linear regulator when the system is powered up to operation. If the VISW1 input is not used, tie it to GND. The VISW1 input is not active until EN is high.

Current Limit for LDO1

LDO1 is rated to a maximum load current of 400 mA. Above this level, the current-limit feature limits the current to protect the device.

The VISW1 input has an independent current-limit circuit with a typical threshold of 500 mA. If this overcurrent threshold is exceeded, the VISW1 input is immediately disconnected and LDO1 takes over to supply the VREG1 current. After the VISW1 input is turned off due to a current-limit event, it can be reset only by toggling the EN pin.

Discharge Switch for LDO1

A discharge switch at the VREG1 pin turns on during low VBATT pin voltage (3.5 V ± 0.1 V hysteresis), removing the charge of the external capacitor via a 1 kΩ resistor.

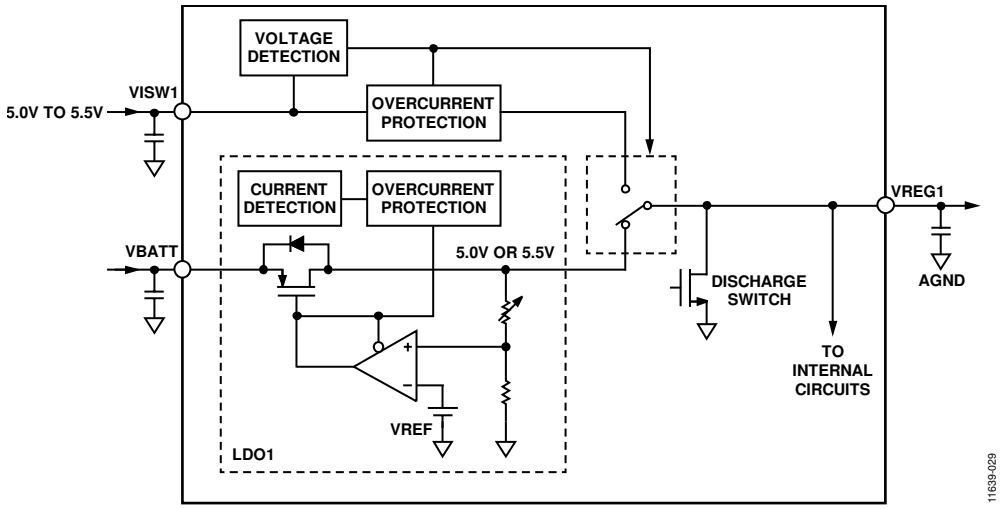

Figure 36. VREG1, LDO1, and VISW1

LDO2

LDO2 regulates the internally routed VREG2 pin voltage to 3 V, 3.15 V, 3.2 V, or 3.3 V and is capable of providing up to 300 mA. LDO2 internally supplies the control block of the ADP5080, as well as external circuits supplied through the VREG2 pin.

The LDO2 output is enabled when the VBATT pin voltage rises above the UVLO threshold and is disabled when the VBATT pin voltage falls below the UVLO threshold.

VISW2 Input

A 3.0 V to 3.3 V regulator connected to the VISW2 pin can take over from LDO2 to supply the internal circuit of the ADP5080 and the VREG2 load. To enable this feature, set the SEL_INP_LDO2 bit (Bit 4 in Register 33) high after the VISW2 pin voltage settles above 2.7 V.

If the VISW2 pin voltage falls below 2.55 V, LDO2 resumes control automatically. However, if the VISW2 source is disabled, it is recommended that the SEL_INP_LDO2 bit be reset to 0 before turning off the VISW2 pin source.

The use of an external regulator connected to the VISW2 pin is intended to achieve better system power efficiency by allowing a switching power supply to take over the LDO2 linear regulator when the system is powered up to operation. If the VISW2 input is not used, tie it to GND. The VISW2 input is not active until EN is high.

Because the VISW2 input supplies VREG2 with no regulation, the maximum voltage that can be applied to VISW2 is 3.3 V. The VISW2 input has a relatively high resistance compared to the LDO2 path. As a result, VISW2 regulation may not be sufficient when used to supply heavier loads.

Current Limit for LDO2

LDO2 is rated to a maximum load current of 300 mA. Above this level, the current-limit feature limits the current to protect the device.

The VISW2 input has an independent current-limit circuit with a typical threshold of 300 mA. If this overcurrent threshold is exceeded, the VISW2 input is immediately disconnected and LDO2 takes over to supply the VREG2 current. After the VISW2 input is turned off due to a current-limit event, it can be reset only by toggling the EN pin.

Discharge Switch for LDO2

A discharge switch at the VREG2 pin turns on during low VBATT pin voltage (3.5 V ± 0.1 V hysteresis), removing the residual charge of the external capacitor via a 12 Ω resistor.

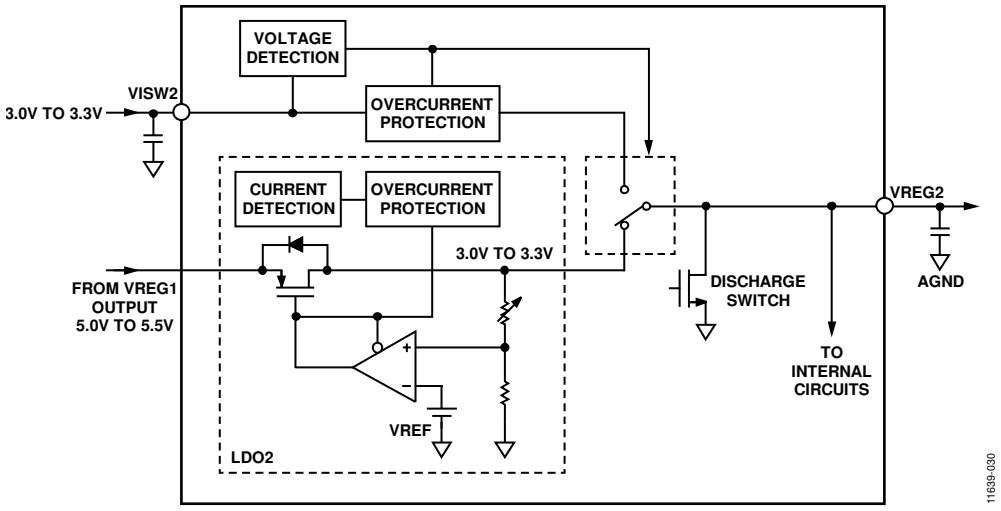

Figure 37. VREG2, LDO2, and VISW2

DC-TO-DC CONVERTER CHANNELS

The ADP5080 integrates five buck regulators and a configurable buck only/buck boost regulator. These regulators can be configured for various functions including auto PSM, auto DCM, DVS, and gate scaling. Each function is included only in the channels where it is most effective (see Table 9).

Channel 1, Channel 2, and Channel 3: Buck Regulators with Flex-Mode Architecture

Channel 1, Channel 2, and Channel 3 feature Flex-Mode™ current mode control, which eliminates minimum on time requirements and allows duty cycles as low as 0%. Flex-Mode uses a unique adaptive control architecture that maintains stable operation over a wide range of application conditions. With Flex-Mode control, very high step-down ratios can be achieved while maintaining high efficiency and excellent transient performance.

Selecting the Output Voltage, Channel 1 to Channel 3

The output voltage of Channel 1, Channel 2, or Channel 3 is selected from one of the preset values available in the VIDx bits, where x is 1, 2, or 3 (see Table 39 and Table 41). The default output voltage value is factory fuse programmed.

Channel 3 has an adjustable mode option that can be selected using the VID3 bits. When the adjustable output voltage mode is selected, the output voltage is set by an external feedback resistor divider. Select resistor values such that the desired output voltage is divided down to 0.8 V and the paralleled resistance seen from the dividing node does not exceed 25 kΩ (see the Setting the Output Voltage (Adjustable Mode Channels) section). Channel 1 can also be used in adjustable output mode by setting the VID1 bits to 0.8 V and using external feedback resistors with values less than 1 kΩ. When using the adjustable mode for Channel 1 or Channel 3, be aware of the minimum off time restriction, which may limit the range of available output voltages.

Channel 1, Channel 2, and Channel 3 are designed for very low duty cycle operation. However, at very high duty cycle, these channels have a limited range due to the minimum off time restriction (see Table 3). The minimum input voltage capability for a given output voltage can be determined using the following equation:

$$V_{IN\_MIN} = V_{OUT}/(1 - t_{OFF\_MIN} \times f_{SW})$$

If the input voltage falls below this level, the output voltage droops below its nominal value.

Current-Limit Protection, Channel 1 to Channel 3

Channel 1, Channel 2, and Channel 3 use valley mode current limit (see Figure 38). In valley mode current-limit protection, inductor current is sensed during the low-side on cycle, immediately before the high-side FET turns on. If the inductor current is above the current-limit threshold at this point, the next switching pulse is skipped.

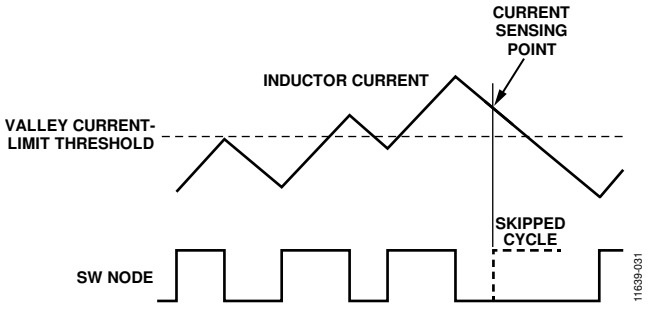

Figure 38. Valley Mode Current Limit

Switching does not resume until the current falls below the limit threshold. This behavior creates an inherent frequency foldback feature, which makes valley mode current-limit protection very robust against runaway inductor current. Because this type of current limit senses current before switching, it is also relatively immune to switching noise.

Table 3 provides the valley current threshold specifications. The actual load current-limit threshold varies with inductor value, frequency, and input and output voltage.

When the current-limit threshold is exceeded, load current is not allowed to increase further. Therefore, as the load impedance is reduced, the current limit forces the output voltage to fall. The falling output voltage in turn toggles the PWRGx, UVx, and $\overline{\text{FAULT}}$ error flags.

In the extreme event of an output voltage short circuit, the UVP function protects the device against excessive current during the on cycle (see the Undervoltage Protection (UVP) section).

Table 9. DC-to-DC Converter Specifications and Functions

Channel	Regulator Type	V_{IN} Range (V)	V_{OUT} Range (V)	Adjustable Mode (V)	I_{OUT} (A)	Auto PSM	Auto DCM	DVS	Gate Scaling
1	Buck	4 to 15	0.8 to 1.2[1]	0.8 to 1.2	3	Yes	N/A	Yes	Yes
2	Buck	4 to 15	1.0 to 3.3	N/A	1.15	Yes	N/A	Yes	N/A
3	Buck	4 to 15	1.2 to 1.8	0.8 to 3.6	1.5	Yes	N/A	N/A	N/A
4	Buck	4 to 15	1.8 to 3.55	1.0 to 5.0	0.8	Yes	N/A	N/A	N/A
5	Buck	4 to 15	3.0 to 5.0	N/A	2	Yes	Yes	N/A	N/A
6	Buck or buck boost	4 to 15	3.5 to 5.5	1.0 to 5.0	2 (buck) 1.5 (buck boost)	Yes	Yes	N/A	N/A

[1] Channel 1 has two available voltage ranges.

Discharge Switch, Channel 1 to Channel 3

Each channel incorporates a discharge switch. For Channel 1 and Channel 2, the discharge switch is located at the FB1 and FB2 pins, respectively; for Channel 3, the discharge switch is located at the SW3 pin. The discharge switch can be turned on when the corresponding channel output is turned off, removing the residual charge of the external capacitor via a 125 Ω resistor. The discharge switch can be enabled by setting the appropriate DSCGx_ON bit in Register 1.

Gate Scaling (Channel 1 Only)

Channel 1 features a gate scaling function, which improves efficiency in light load conditions. When enabled by setting the GATE_SCAL1 bit in Register 32, gate scaling halves the size of the Channel 1 switching FETs, reducing the gate charge-up current—which is a non-negligible loss element in light load conditions—while allowing increased R_{DSON}, whose effect is less significant in these conditions. When gate scaling is enabled, only SW1A is used for the Channel 1 switch node because it is assumed that the load current is light.

Dynamic Voltage Scaling (DVS) Function

Channel 1 and Channel 2 incorporate a dynamic voltage scaling (DVS) function. DVS provides a stair-step transition in output voltage when the preset value for the output voltage is reprogrammed on the fly (see Figure 39).

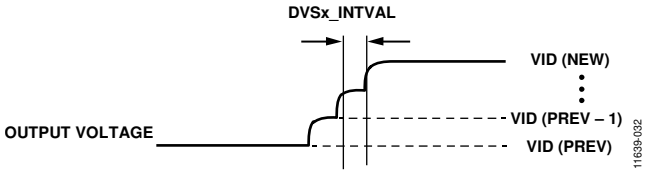

Figure 39. DVS Operation

The output voltage for Channel 1 is programmed using the VID1 bits in Register 12; the output voltage for Channel 2 is programmed using the VID2 bits in Register 13. When the DVS function is enabled, the voltage transition takes place according to the steps set by the VID1 or VID2 bits (see Table 39 and Table 41). The transition time from one step to the next is specified by the interval programmed in Register 17 using the DVSx_INTVAL bits (where x is 1 or 2). The DVS function is enabled by setting the EN_DVSx bit in Register 17.

For Channel 2, DVS operation is limited to an output voltage range of 1.0 V to 1.25 V.

When Channel 1 or Channel 2 is configured for DVS operation, toggling EN low does not immediately reset the VID code to its initial state. Instead Channel 1 or Channel 2 returns to its configured output voltage according to the steps set by the VID1 or VID2 bits (see Table 39 and Table 41, respectively).

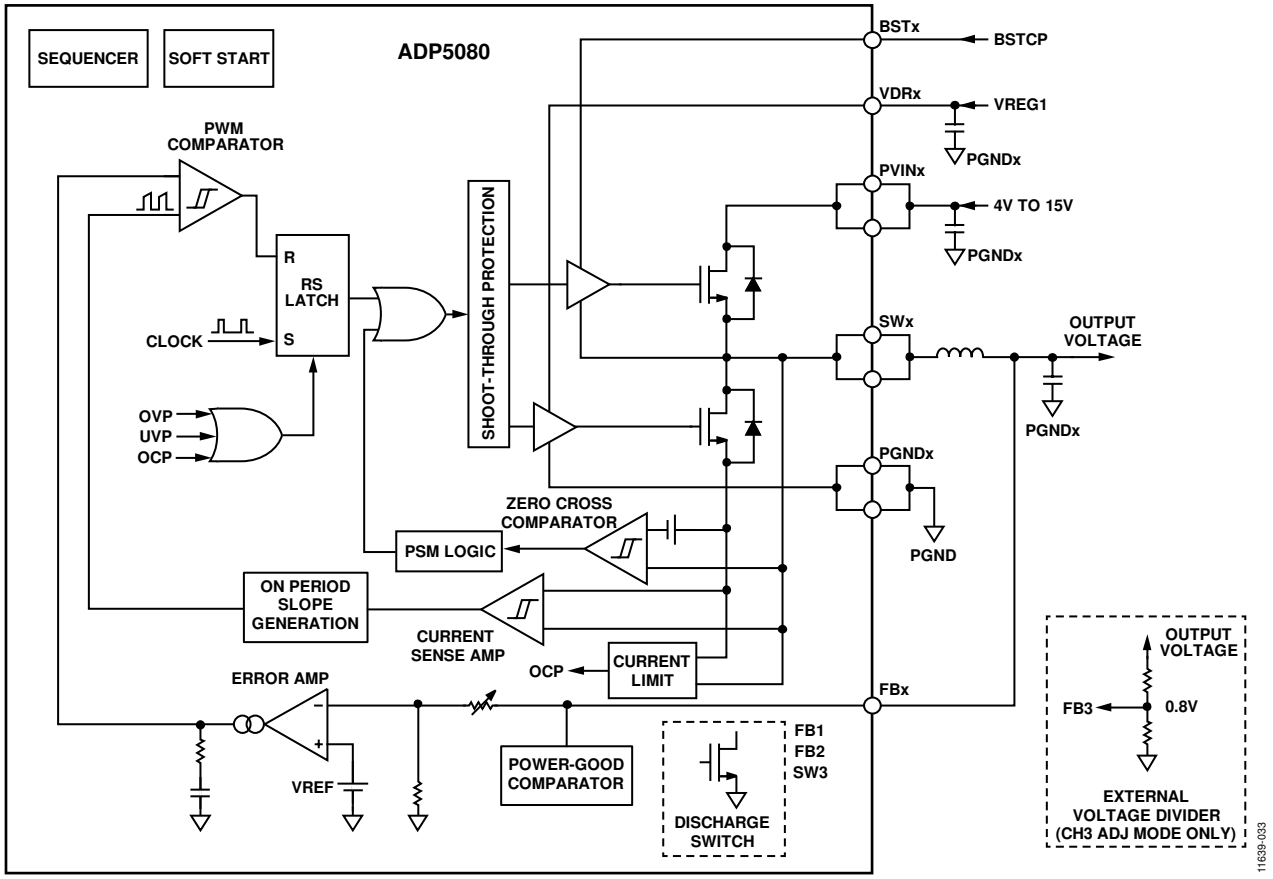

Figure 40. Buck Regulator Block Diagram: Channel 1, Channel 2, and Channel 3

Channel 4 and Channel 5: Current Mode Buck Regulators

Channel 4 and Channel 5 are internally compensated current mode control buck regulators (see Figure 41). Combined with the integrated charge pump, these channels are designed to operate at high duty cycles up to 100%.

Selecting the Output Voltage, Channel 4 and Channel 5

The output voltage of Channel 4 or Channel 5 is selected from one of the preset values available in the VIDx bits, where x is 4 or 5 (see Table 43). The default output voltage value is factory fuse programmed.

Channel 4 has an adjustable mode option that can be selected using the VID4 bits. When the adjustable output voltage mode is selected, the output voltage is set by an external feedback resistor divider. Select resistor values such that the desired output voltage is divided down to 0.8 V and the paralleled resistance seen from the dividing node does not exceed 25 kΩ (see the Setting the Output Voltage (Adjustable Mode Channels) section). When using the adjustable mode for Channel 4, be aware of the minimum on time restriction, which may limit the range of available output voltages.

Channel 4 and Channel 5 are designed for very high duty cycle operation. However, at very low duty cycle, these channels have a limited range due to the minimum on time restriction (75 ns typical) inherent in current mode control. The maximum input voltage capability for a given output voltage can be determined using the following equation:

$$V_{IN\_MAX} = V_{OUT}/(t_{ON\_MIN} \times f_{SW})$$

If the input voltage rises above this level, the output voltage continues to be regulated; however, switching pulses are skipped, which may increase output voltage ripple.

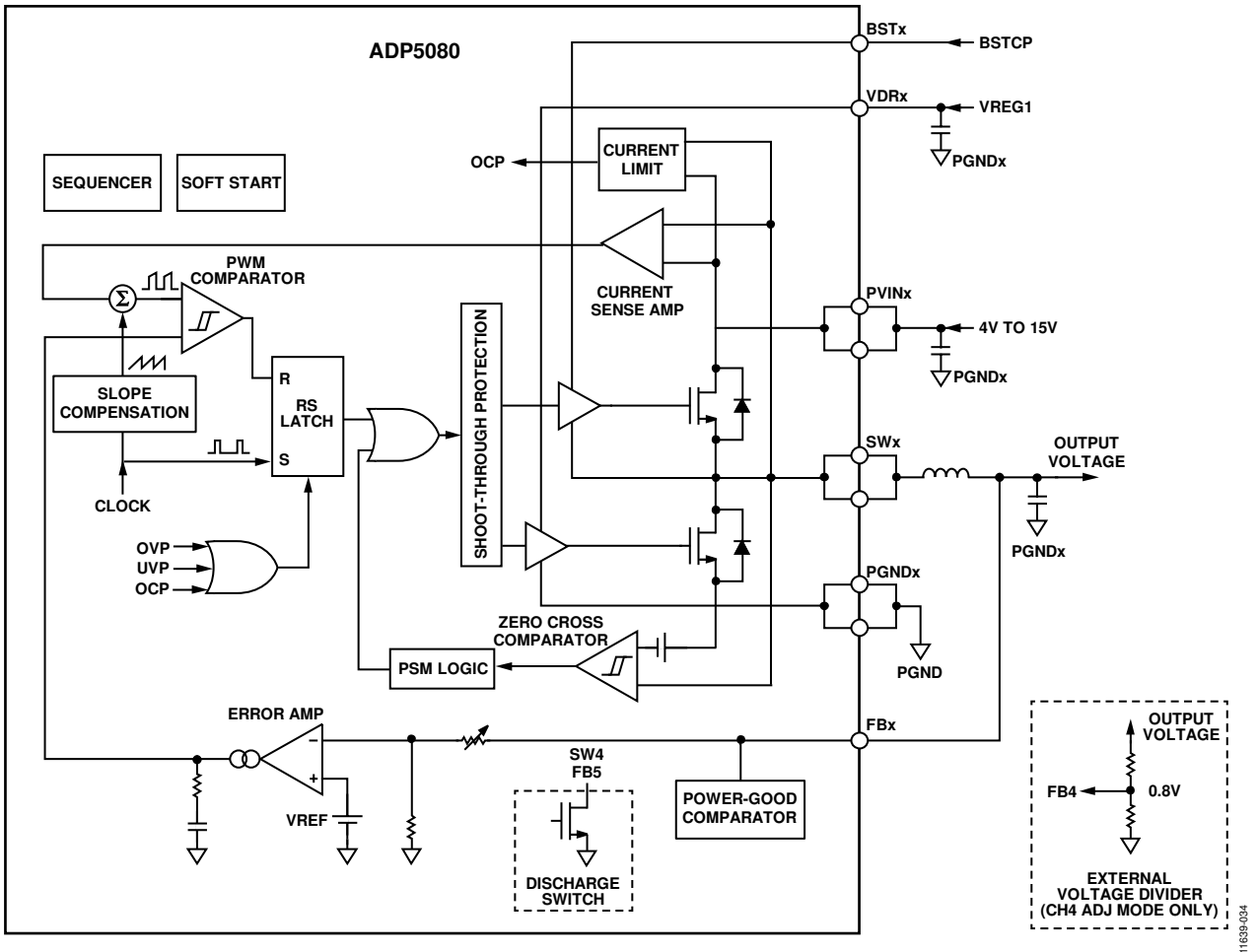

Figure 41. Buck Regulator Block Diagram: Channel 4 and Channel 5