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Dual 3 MHz, 1200 mA Buck Regulators and Two 300 mA LDO Regulators With Precision Enable and Power-Good Output

Data Sheet

ADP5134

FEATURES

- Main input voltage range of 2.5 V to 5.5 V
- Two 1200 mA buck regulators and two 300 mA LDO regulators
- 24-lead, 4 mm × 4 mm LFCSP package
- Regulator accuracy of ±1.8%
- Factory programmable or external adjustable VOUTx
- Precision enable pins for easier power sequencing
- Factory selectable power-good pin
- 3 MHz buck operation with forced PWM and automatic PWM/PSM modes
- BUCK1/BUCK2: output voltage range from 0.8 V to 3.8 V
- LDO1/LDO2: output voltage range from 0.8 V to 5.2 V
- LDO1/LDO2: input voltage range from 1.7 V to 5.5 V
- LDO1/LDO2: high PSRR and low output noise

APPLICATIONS

- Power for processors, application specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), and radio frequency (RF) chipsets
- Portable instrumentation and medical devices
- Space constrained devices

TYPICAL APPLICATION CIRCUIT

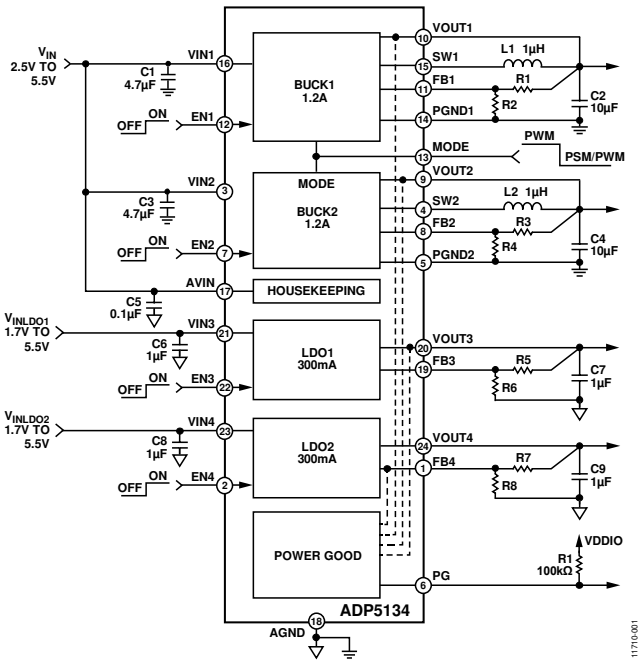

Figure 1.

GENERAL DESCRIPTION

The ADP5134 combines two high performance buck regulators and two low dropout (LDO) regulators. It is available in a 24-lead 4 mm × 4 mm LFCSP.

The high switching frequency of the buck regulators enables tiny multilayer external components and minimizes the board space. When the MODE pin is set to high, the buck regulators operate in forced pulse-width modulation (PWM) mode. When the MODE pin is set to low, the buck regulators operate in PWM mode when the load is above a predefined threshold. When the load current falls below a predefined threshold, the regulator operates in power save mode (PSM), improving the light load efficiency.

The two buck regulators operate out of phase to reduce the input capacitor requirement. The low quiescent current, low dropout voltage, and wide input voltage range of the ADP5134 LDO regulators extend the battery life of portable devices. The ADP5134 LDO regulators maintain power supply rejection greater than 60 dB for frequencies as high as 10 kHz while operating with a low headroom voltage of 500 mV.

Regulators in the ADP5134 are activated through dedicated enable pins. The default output voltages can be externally set in the adjustable version or factory programmable to a wide range of preset values in the fixed voltage version.

Table 1. Family Models

Model	Channels	Maximum Current	Package
ADP5023	2 Bucks, 1 LDO	800 mA, 300 mA	LFCSP (CP-24-10)
ADP5024	2 Bucks, 1 LDO	1.2 A, 300 mA	LFCSP (CP-24-10)
ADP5034	2 Bucks, 2 LDOs	1.2 A, 300 mA	LFCSP (CP-24-10), TSSOP (RE-28-1)
ADP5037	2 Bucks, 2 LDOs	800 mA, 300 mA	LFCSP (CP-24-10)
ADP5033	2 Bucks, 2 LDOs with 2 ENx pins	800 mA, 300 mA	WLCSP (CB-16-8)
ADP5040	1 Bucks, 2 LDOs	1.2 A, 300 mA	LFCSP (CP-20-10)
ADP5041	1 Bucks, 2 LDOs with supervisory circuit, watchdog function, and manual reset	1.2 A, 300 mA	LFCSP (CP-20-10)

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- ADP5134 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1311: Complex Power Supply Sequencing Made Easy

Data Sheet

- ADP5134: Dual 3 MHz, 1200 mA Buck Regulators and Two 300 mA LDO Regulators With Precision Enable and Power-Good Output Data Sheet

User Guides

- UG-591: Evaluating the ADP5134 Micropower Management Unit (PMU)

TOOLS AND SIMULATIONS

- 5V uPMU BuckDesigner
- ADIsimPower™ Voltage Regulator Design Tool

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Integrated Power Solutions for Altera FPGAs

DESIGN RESOURCES

- ADP5134 Material Declaration
- PCN-PDN Information
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REVISION HISTORY

10/13—Revision 0: Initial Version

SPECIFICATIONS

GENERAL SPECIFICATIONS

V_{AVIN} = V_{VIN1} = V_{VIN2} = 2.5 V to 5.5 V, V_{VIN3} = V_{VIN4} = 1.7 V to 5.5 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{AVIN}, V_{VIN1}, V_{VIN2}		2.5		5.5	V
THERMAL SHUTDOWN						
Threshold	TS_{SD}	T_J rising		150		°C
Hysteresis	TS_{SD-HYS}			20		°C
START-UP TIME[1]						
BUCK1	t_{START1}			650		µs
BUCK2	t_{START2}			750		µs
LDO1, LDO2 (Fast Soft Start)	t_{START3}			650		µs
LDO1, LDO2 (Slow Soft Start)	t_{START4}			900		µs
START-UP TIME, BUCK2 First						
BUCK2	t_{START5}			750		µs
BUCK1	t_{START6}			300		µs
LDO1, LDO2 (Fast Soft Start)	t_{START7}			300		µs
LDO1, LDO2 (Slow Soft Start)	t_{START8}			600		µs
SHUTDOWN CONTROL		All ENx pins below V_{IL_EN} level to achive $I_{SHUTDOWN}$				
Level High	V_{IH_EN}	T_J = −40°C to +85°C	0.9			V
Level Low	V_{IL_EN}				0.35	V
PRECISION ENABLE PINS (ENx)		Regulator(s) activation/deactivation thresholds				
Analog Activation Threshold	V_{ENR}	Device out of shutdown (V_{ENx} > V_{IH_EN})	0.94	0.97	1	V
Hysteresis (Regulator Deactivation)	V_{ENH}			80		mV
Input Leakage Current	$V_{I-LEAKAGE}$			0.05	1	µA
POWER-GOOD PIN (PG)		Monitors V_{OUT} falling out of regulation				
Power-Good Falling Threshold	V_{PGLOW}	At V_{OUT}		90		%
Power-Good Rising Threshold	V_{PGHYS}	At V_{OUT}	91	94	97	%
Power-Good Delay	t_{PGDLY}			15		µs
Power-Good Leakage Current	I_{PGIQ}	V_{PG} = V_{IN}			1	µA
Power-Good Output Voltage Low	V_{PGOL}	Load current (I_{LOADx}) = 1 mA		0.02	0.15	V
MODE PIN						
Level High	V_{IH_MOD}		1.1			V
Level Low	V_{IL_MOD}				0.4	V
INPUT CURRENT						
All Channels Enabled	$I_{STBY-NOSW}$	No load, no buck switching		113	182	µA
All Channels Disabled	$I_{SHUTDOWN}$	T_J = −40°C to +85°C		0.3	1	µA
VIN1 UNDERVOLTAGE LOCKOUT						
Low UVLO Input Voltage Rising	$UVLO_{VIN1RISE}$				2.45	V
Low UVLO Input Voltage Falling	$UVLO_{VIN1FALL}$		1.95			V

[1] Start-up time is defined as the time from EN1 = EN2 = EN3 = EN4 at 0 V to V_{AVIN} to VOUT1, VOUT2, VOUT3, and VOUT4 reaching 90% of their nominal level. Start-up times are shorter for individual channels if another channel is already enabled. See the Typical Performance Characteristics section for more information.

BUCK1 AND BUCK2 SPECIFICATIONS

V_{AVIN} = V_{VIN1} = V_{VIN2} = 2.5 V to 5.5 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
Output Voltage Accuracy	$\Delta V_{VOUT1}/V_{VOUT1}$, $\Delta V_{VOUT2}/V_{VOUT2}$	PWM mode, I_{LOAD1} = I_{LOAD2} = 0 mA	−1.8		+1.8	%
Line Regulation	$(\Delta V_{VOUT1}/V_{VOUT1})/\Delta V_{VIN1}$, $(\Delta V_{VOUT2}/V_{VOUT2})/\Delta V_{VIN2}$	PWM mode		−0.05		%/V
Load Regulation	$(\Delta V_{VOUT1}/V_{VOUT1})/\Delta I_{VOUT1}$, $(\Delta V_{VOUT2}/V_{VOUT2})/\Delta I_{VOUT2}$	I_{LOAD} = 0 mA to 1200 mA, PWM mode		−0.1		%/A
VOLTAGE FEEDBACK	V_{FB1}, V_{FB2}	Models with adjustable outputs	0.491	0.5	0.509	V
OPERATING SUPPLY CURRENT	I_{IN}	MODE = ground				
BUCK1 Only		I_{LOAD1} = 0 mA, device not switching, all other channels disabled		44		µA
BUCK2 Only		I_{LOAD2} = 0 mA, device not switching, all other channels disabled		55		µA
BUCK1 and BUCK2		I_{LOAD1} = I_{LOAD2} = 0 mA, device not switching, LDO channels disabled		67		µA
PSM CURRENT THRESHOLD	I_{PSM}	PSM to PWM operation		100		mA
SWx CHARACTERISTICS						
SWx On Resistance	R_{NFET}	V_{VIN1} = V_{VIN2} = 3.6 V		155	240	mΩ
	R_{PFET}	V_{VIN1} = V_{VIN2} = 3.6 V		205	310	mΩ
	R_{NFET}	V_{VIN1} = V_{VIN2} = 5.5 V		137	204	mΩ
	R_{PFET}	V_{VIN1} = V_{VIN2} = 5.5 V		162	243	mΩ
Current Limit	I_{LIMIT1}, I_{LIMIT2}	PFET switch peak current limit	1600	1950	2300	mA
ACTIVE PULL-DOWN	R_{PDWN-B}	V_{VIN1} = V_{VIN2} = 3.6 V, channels disabled		75		Ω
OSCILLATOR FREQUENCY	f_{SW}		2.5	3.0	3.5	MHz

LDO1 AND LDO2 SPECIFICATIONS

V_{VIN3} = (V_{VOUT3} + 0.5 V) or 1.7 V (whichever is greater) to 5.5 V, V_{VIN4} = (V_{VOUT4} + 0.5 V) or 1.7 V (whichever is greater) to 5.5 V, C_{IN} = C_{OUT} = 1 µF, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{VIN3}, V_{VIN4}		1.7		5.5	V
OPERATING SUPPLY CURRENT						
Bias Current per LDO[1]	$I_{VIN3BIAS}/I_{VIN4BIAS}$	I_{VOUT3} = I_{VOUT4} = 0 µA		10	30	µA
		I_{VOUT3} = I_{VOUT4} = 10 mA		60	100	µA
		I_{VOUT3} = I_{VOUT4} = 300 mA		165	245	µA
Total System Input Current	I_{IN}	Includes all current into AVIN, VIN1, VIN2, VIN3, and VIN4				
LDO1 or LDO2 Only		I_{VOUT3} = I_{VOUT4} = 0 µA, all other channels disabled		63		µA
LDO1 and LDO2		I_{VOUT3} = I_{VOUT4} = 0 µA, buck channels disabled		84		µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
Output Voltage Accuracy	$\Delta V_{VOUT3}/V_{VOUT3}$, $\Delta V_{VOUT4}/V_{VOUT4}$	$I_{VOUT3} = I_{VOUT4} = 1$ mA	−1.8		+1.8	%
Line Regulation	$(\Delta V_{VOUT3}/V_{VOUT3})/\Delta V_{VIN3}$, $(\Delta V_{VOUT4}/V_{VOUT4})/\Delta V_{VIN4}$	$I_{VOUT3} = I_{VOUT4} = 1$ mA	−0.03		+0.03	%/V
Load Regulation[2]	$(\Delta V_{VOUT3}/V_{VOUT3})/\Delta I_{VOUT3}$, $(\Delta V_{VOUT4}/V_{VOUT4})/\Delta I_{VOUT4}$	$I_{VOUT3} = I_{VOUT4} = 1$ mA to 300 mA		0.001	0.003	%/mA
VOLTAGE FEEDBACK	V_{FB3}, V_{FB4}		0.491	0.5	0.509	V
DROPOUT VOLTAGE[3]	$V_{DROPOUT}$	$V_{VOUT3} = V_{VOUT4} = 5.2$ V, $I_{VOUT3} = I_{VOUT4} = 300$ mA		50		mV
		$V_{VOUT3} = V_{VOUT4} = 3.3$ V, $I_{VOUT3} = I_{VOUT4} = 300$ mA		75	140	mV
		$V_{VOUT3} = V_{VOUT4} = 2.5$ V, $I_{VOUT3} = I_{VOUT4} = 300$ mA		100		mV
		$V_{VOUT3} = V_{VOUT4} = 1.8$ V, $I_{VOUT3} = I_{VOUT4} = 300$ mA		180		mV
CURRENT-LIMIT THRESHOLD[4]	I_{LIMIT3}, I_{LIMIT4}		335	600		mA
ACTIVE PULL-DOWN	R_{PDWN-L}	Channels disabled		600		Ω
OUTPUT NOISE						
Regulator LDO1	$NOISE_{LDO1}$	10 Hz to 100 kHz, $V_{VIN3} = 5$ V, $V_{VOUT3} = 2.8$ V		100		μV rms
Regulator LDO2	$NOISE_{LDO2}$	10 Hz to 100 kHz, $V_{VIN4} = 5$ V, $V_{VOUT4} = 1.2$ V		60		μV rms
POWER SUPPLY REJECTION RATIO	PSRR					
Regulator LDO1		10 kHz, $V_{VIN3} = 3.3$ V, $V_{VOUT3} = 2.8$ V, $I_{VOUT3} = 1$ mA		60		dB
		100 kHz, $V_{VIN3} = 3.3$ V, $V_{VOUT3} = 2.8$ V, $I_{VOUT3} = 1$ mA		62		dB
		1 MHz, $V_{VIN3} = 3.3$ V, $V_{VOUT3} = 2.8$ V, $I_{VOUT3} = 1$ mA		63		dB
Regulator LDO2		10 kHz, $V_{VIN4} = 1.8$ V, $V_{VOUT4} = 1.2$ V, $I_{VOUT4} = 1$ mA		54		dB
		100 kHz, $V_{VIN4} = 1.8$ V, $V_{VOUT4} = 1.2$ V, $I_{VOUT4} = 1$ mA		57		dB
		1 MHz, $V_{VIN4} = 1.8$ V, $V_{VOUT4} = 1.2$ V, $I_{VOUT4} = 1$ mA		64		dB

[1] This is the input current into VIN3 or VIN4 that is not delivered to the output load. If LDO1 is only activated, it is the current into VIN3. If LDO2 is only activated, it is the current into VIN4.
[2] Based on an endpoint calculation using 1 mA and 300 mA loads.
[3] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only to output voltages greater than 1.7 V.
[4] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V, or 2.7 V.

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

$T_A = -40°C$ to $+125°C$, unless otherwise specified.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit
NOMINAL INPUT AND OUTPUT CAPACITOR RATINGS					
BUCK1, BUCK2 Input Capacitor Ratings	C_{MIN1}, C_{MIN2}	4.7		40	μF
BUCK1, BUCK2 Output Capacitor Ratings	C_{MIN1}, C_{MIN2}	10		40	μF
LDO1, LDO2[1] Input and Output Capacitor Ratings	C_{MIN3}, C_{MIN4}	1.0			μF
CAPACITOR ESR	R_{ESR}	0.001		1	Ω

[1] The minimum input and output capacitance must be greater than 1.0 μF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R type and X5R type capacitors are recommended, and Y5V and Z5U capacitors are not recommended for use because of their poor temperature and dc bias characteristics.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVIN to AGND	−0.3 V to +6 V
VIN1, VIN2 to AVIN	−0.3 V to +0.3 V
PGND1, PGND2 to AGND	−0.3 V to +0.3 V
VIN3, VIN4, VOUT1, VOUT2, FB1, FB2, FB3, FB4, EN1, EN2, EN3, EN4, MODE, PG to AGND	−0.3 V to (AVIN + 0.3 V)
VOUT3 to AGND	−0.3 V to (VIN3 + 0.3 V)
VOUT4 to AGND	−0.3 V to (VIN4 + 0.3 V)
SW1 to PGND1	−0.3 V to (VIN1 + 0.3 V)
SW2 to PGND2	−0.3 V to (VIN2 + 0.3 V)
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

For detailed information on power dissipation, see the Power Dissipation and Thermal Considerations section.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
24-Lead, 0.5 mm Pitch LFCSP	35	3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

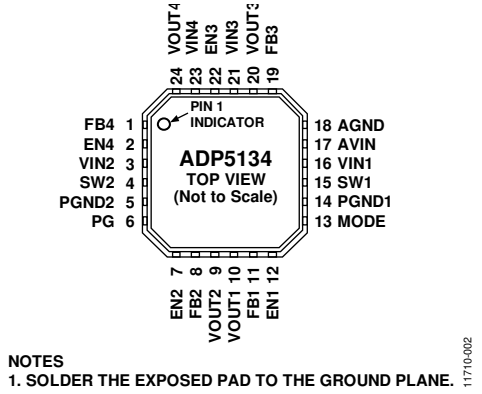

Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FB4	LDO2 Feedback Input. For device models with an adjustable output voltage, connect this pin to the middle of the LDO2 resistor divider. For device models with a factory programmed output voltage, connect FB4 to the top of the capacitor on VOUT4.
2	EN4	LDO2 Enable Pin. When EN4 is set to high, it turns the regulator on. When EN4 is set to low, it turns the regulator off.
3	VIN2	BUCK2 Input Supply (2.5 V to 5.5 V). Connect VIN2 to VIN1 and AVIN.
4	SW2	BUCK2 Switching Node.
5	PGND2	Dedicated Power Ground for BUCK2.
6	PG	Power-Good Pin Output. Factory selectable to monitor the output voltage of up to four regulators.
7	EN2	BUCK2 Enable Pin. When EN2 is set to high, it turns the regulator on. When EN2 is set to low, it turns the regulator off.
8	FB2	BUCK2 Feedback Input. For device models with an adjustable output voltage, connect this pin to the middle of the BUCK2 resistor divider. For device models with a fixed output voltage, leave this pin unconnected.
9	VOUT2	BUCK2 Output Voltage Sensing Input. Connect VOUT2 to the top of the BUCK2 output capacitor.
10	VOUT1	BUCK1 Output Voltage Sensing Input. Connect VOUT1 to the top of the BUCK1 output capacitor.
11	FB1	BUCK1 Feedback Input. For device models with an adjustable output voltage, connect this pin to the middle of the BUCK1 resistor divider. For device models with a fixed output voltage, leave this pin unconnected.
12	EN1	BUCK1 Enable Pin. When EN1 is set to high, it turns the regulator on. When EN1 is set to low, it turns the regulator off.
13	MODE	BUCK1/BUCK2 Operating Mode. When MODE is set to high, the device is set to forced PWM operation. When MODE is set to low, the device is automatically set to PWM/PSM operation.
14	PGND1	Dedicated Power Ground for BUCK1.
15	SW1	BUCK1 Switching Node.
16	VIN1	BUCK1 Input Supply (2.5 V to 5.5 V). Connect VIN1 to VIN2 and AVIN.
17	AVIN	Analog Input Supply (2.5 V to 5.5 V). Connect AVIN to VIN1 and VIN2.
18	AGND	Analog Ground.
19	FB3	LDO1 Feedback Input. For device models with an adjustable output voltage, connect this pin to the middle of the LDO1 resistor divider. For device models with a factory programmed output voltage, connect FB3 to the top of the capacitor on VOUT3.
20	VOUT3	LDO1 Output Voltage.
21	VIN3	LDO1 Input Supply (1.7 V to 5.5 V).
22	EN3	LDO1 Enable Pin. When EN3 is set to high, it turns on the regulator, and when EN3 is set to low, it turns off the regulator.
23	VIN4	LDO2 Input Supply (1.7 V to 5.5 V).
24	VOUT4	LDO2 Output Voltage.
	EP	Exposed Pad. Solder the exposed pad to the ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{VIN1} = V_{VIN2} = V_{VIN3} = V_{VIN4} = 3.6$ V, $T_A = 25°C$, unless otherwise noted.

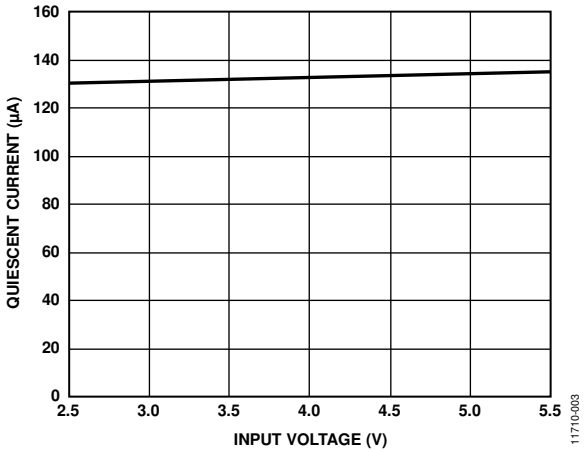

Figure 3. System Quiescent Current vs. Input Voltage, $V_{VOUT1} = 3.3$ V, $V_{VOUT2} = 1.8$ V, $V_{VOUT3} = 1.2$ V, $V_{VOUT4} = 3.3$ V, All Channels Unloaded

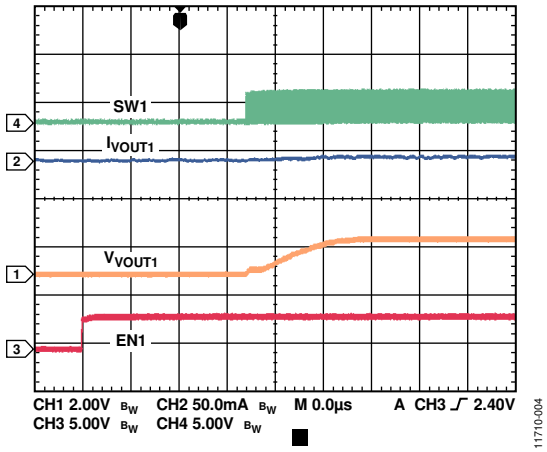

Figure 4. BUCK1 Startup, $V_{VIN1} = 4.2$ V, $V_{VOUT1} = 1.8$ V, $I_{VOUT1} = 5$ mA

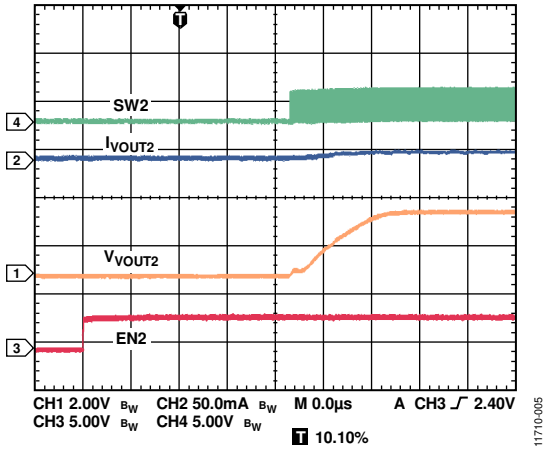

Figure 5. BUCK2 Startup, $V_{VIN2} = 4.2$ V, $V_{VOUT2} = 3.3$ V, $I_{VOUT2} = 10$ mA

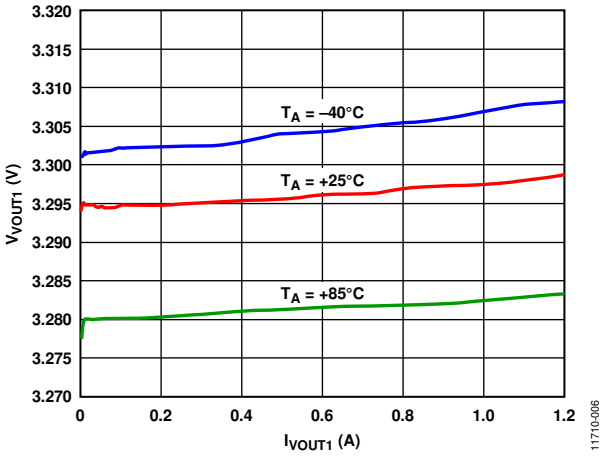

Figure 6. BUCK1 Load Regulation Across Temperature, $V_{VIN1} = 4.2$ V, $V_{VOUT1} = 3.3$ V, PWM Mode

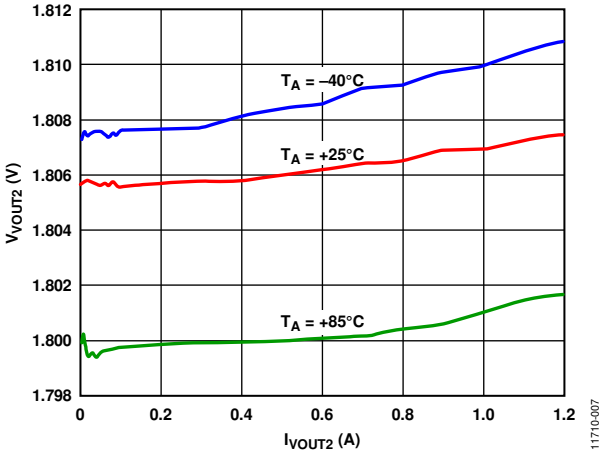

Figure 7. BUCK2 Load Regulation Across Temperature, $V_{VIN2} = 3.6$ V, $V_{VOUT2} = 1.8$ V, PWM Mode

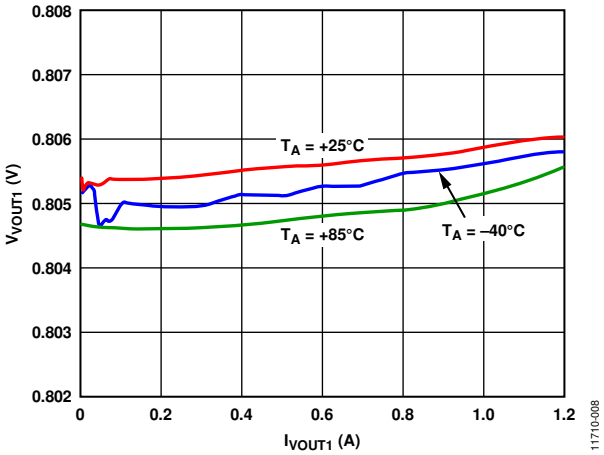

Figure 8. BUCK1 Load Regulation Across Input Voltage, $V_{VIN1} = 3.6$ V, $V_{VOUT1} = 0.8$ V, PWM Mode

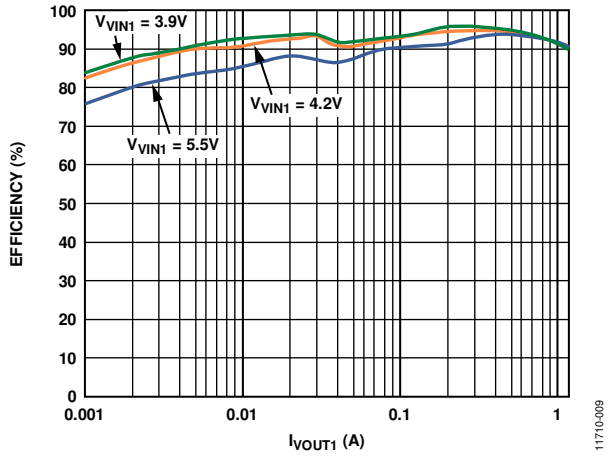

Figure 9. BUCK1 Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 3.3 V, Auto Mode

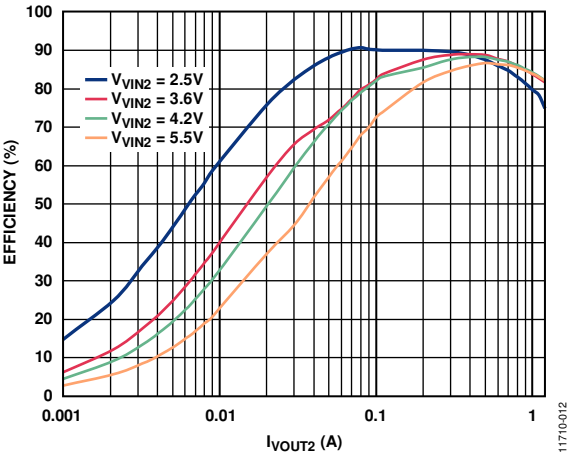

Figure 12. BUCK2 Efficiency vs. Load Current, Across Input Voltage, V_{OUT2} = 1.8 V, PWM Mode

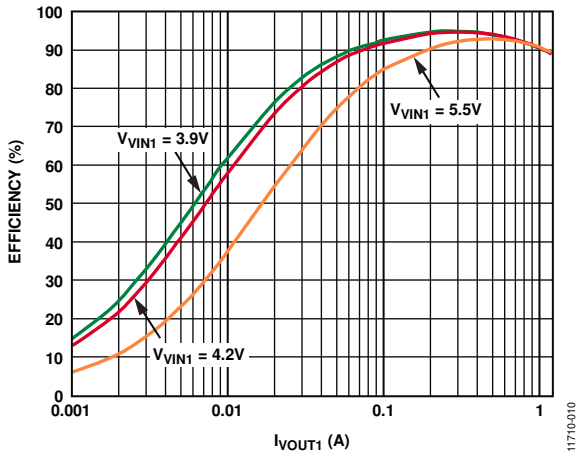

Figure 10. BUCK1 Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 3.3 V, PWM Mode

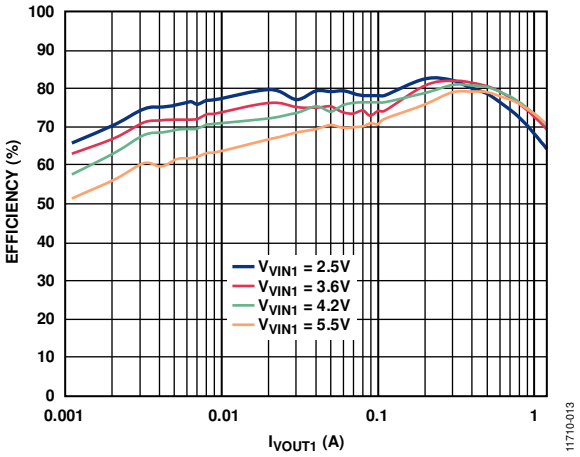

Figure 13. BUCK1 Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 0.8 V, Auto Mode

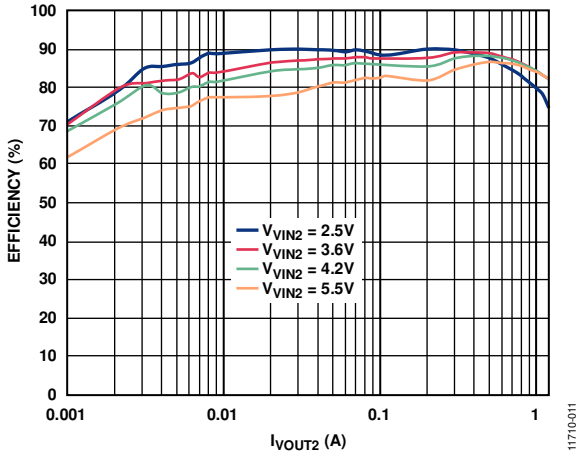

Figure 11. BUCK2 Efficiency vs. Load Current, Across Input Voltage, V_{OUT2} = 1.8 V, Auto Mode

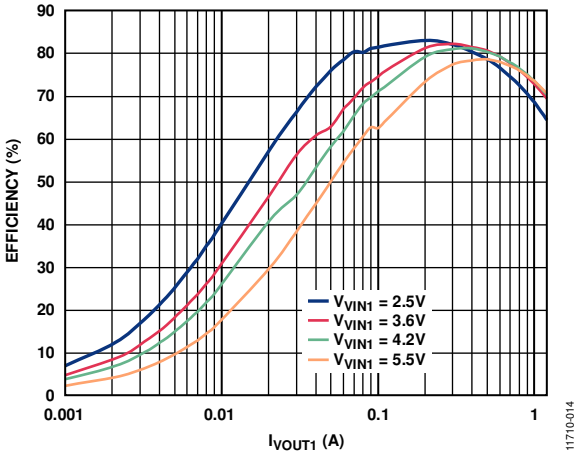

Figure 14. BUCK1 Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 0.8 V, PWM Mode

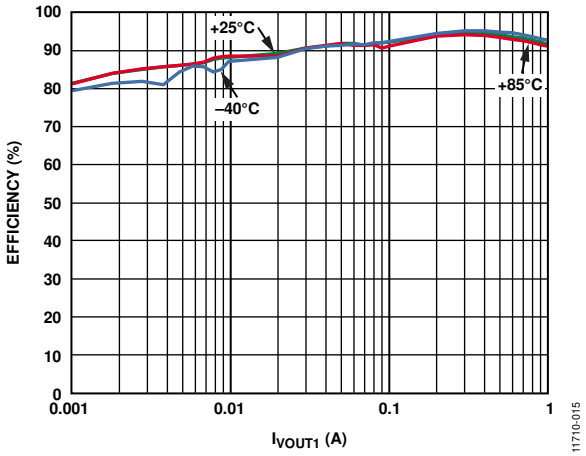

Figure 15. BUCK1 Efficiency vs. Load Current, Across Temperature, V_{VIN1} = 3.9 V, V_{VOUT1} = 3.3 V, Auto Mode

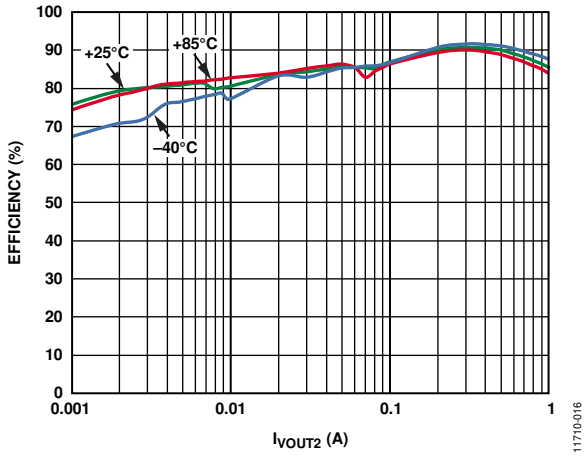

Figure 16. BUCK2 Efficiency vs. Load Current, Across Temperature, V_{VOUT2} = 1.8 V, Auto Mode

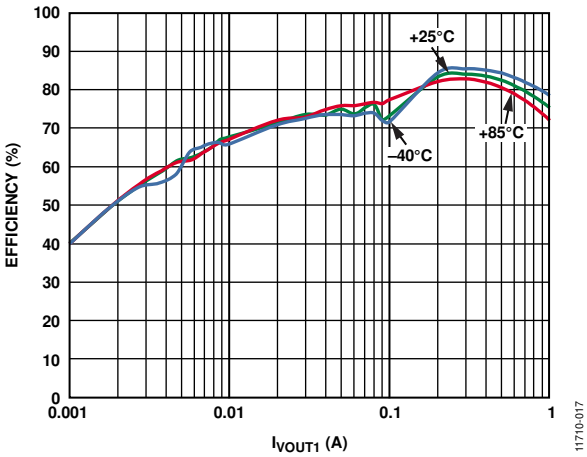

Figure 17. BUCK1 Efficiency vs. Load Current, Across Temperature, V_{VOUT1} = 0.8 V, Auto Mode

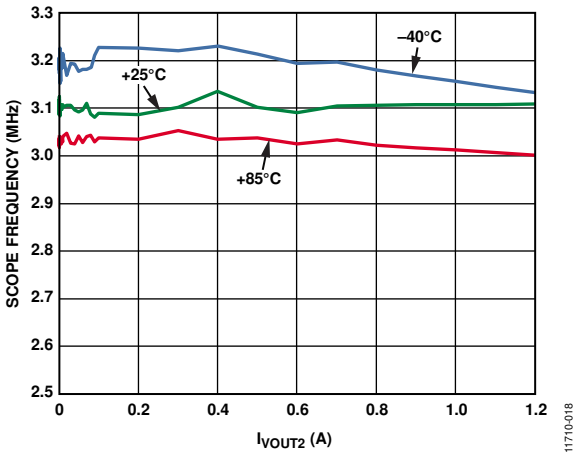

Figure 18. BUCK2 Switching Frequency vs. Output Current, Across Temperature, V_{VOUT2} = 1.8 V, PWM Mode

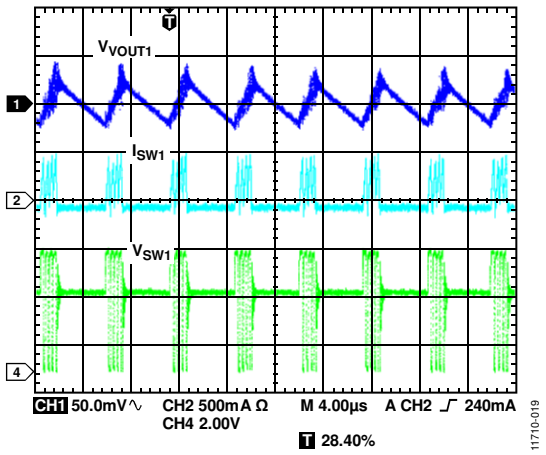

Figure 19. Typical Waveforms, V_{VOUT1} = 3.3 V, I_{VOUT1} = 30 mA, Auto Mode

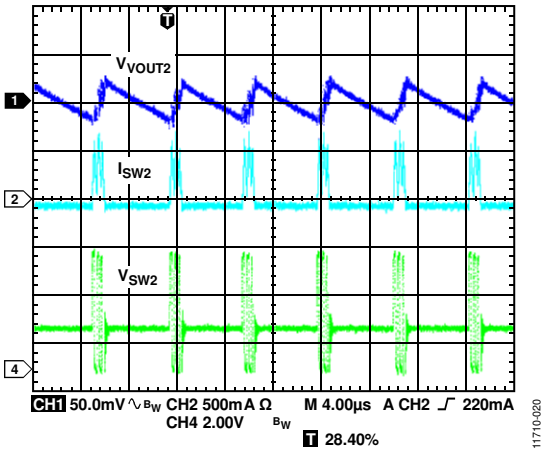

Figure 20. Typical Waveforms, V_{VOUT2} = 1.8 V, I_{VOUT2} = 30 mA, Auto Mode

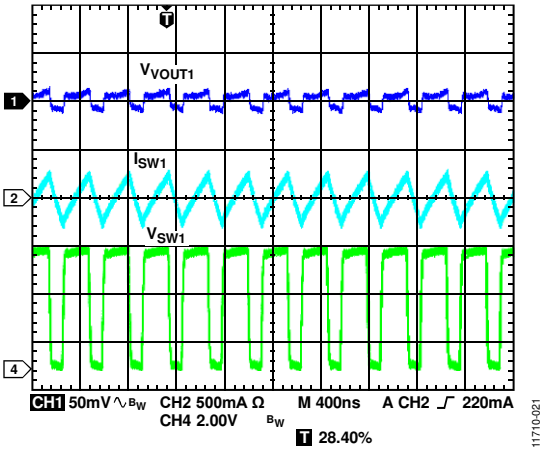

Figure 21. Typical Waveforms, V_{VOUT1} = 3.3 V, I_{VOUT1} = 30 mA, PWM Mode

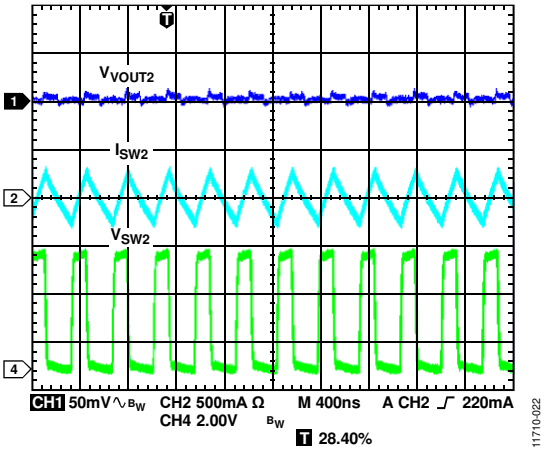

Figure 22. Typical Waveforms, V_{VOUT2} = 1.8 V, I_{VOUT2} = 30 mA, PWM Mode

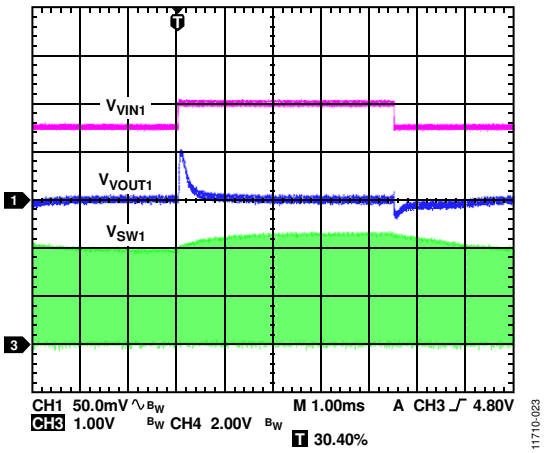

Figure 23. BUCK1 Response to Line Transient, Input Voltage from 4.5 V to 5.0 V, V_{VOUT1} = 3.3 V, PWM Mode

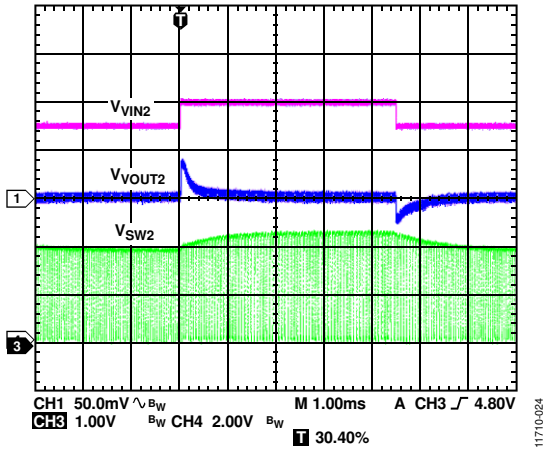

Figure 24. BUCK2 Response to Line Transient, V_{VIN2} = 4.5 V to 5.0 V, V_{VOUT2} = 1.8 V, PWM Mode

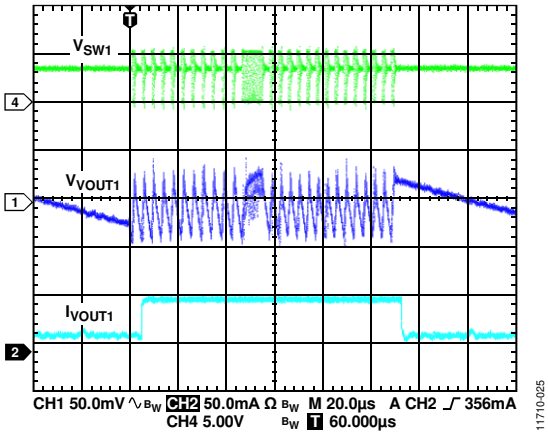

Figure 25. BUCK1 Response to Load Transient, I_{VOUT1} from 1 mA to 50 mA, V_{VOUT1} = 3.3 V, Auto Mode

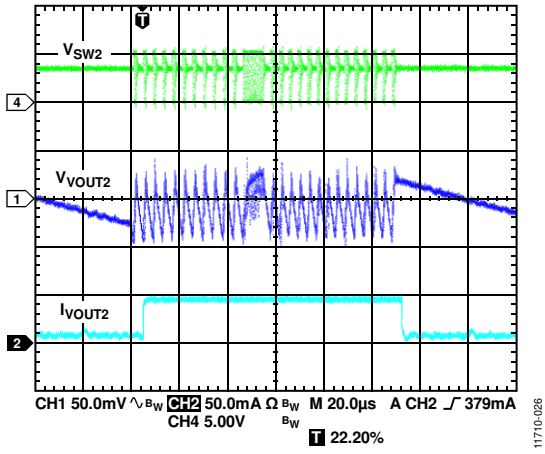

Figure 26. BUCK2 Response to Load Transient, I_{VOUT2} from 1 mA to 50 mA, V_{VOUT2} = 1.8 V, Auto Mode

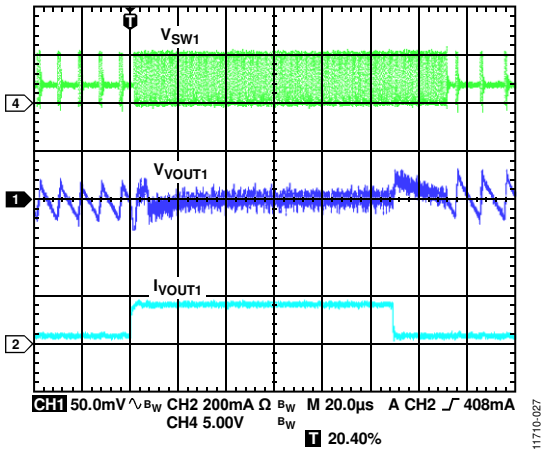

Figure 27. BUCK1 Response to Load Transient, I_{VOUT1} from 20 mA to 180 mA, V_{VOUT1} = 3.3 V, Auto Mode

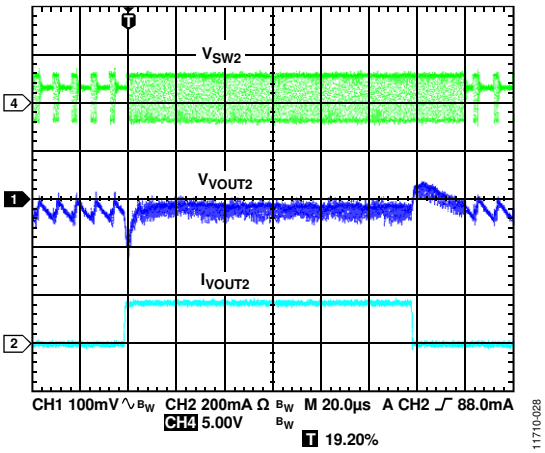

Figure 28. BUCK2 Response to Load Transient, I_{VOUT2} from 20 mA to 180 mA, V_{VOUT2} = 1.8 V, Auto Mode

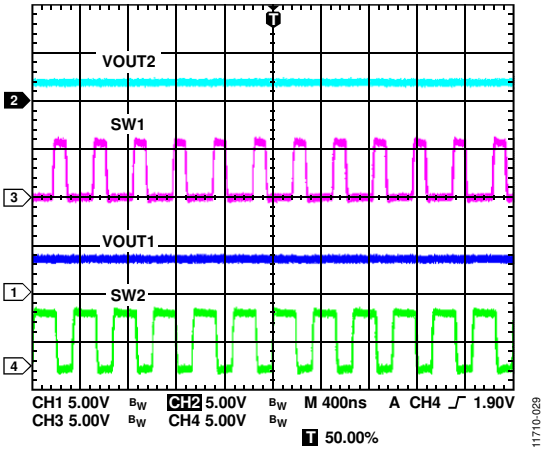

Figure 29. VOUTx and SWx Waveforms for BUCK1 and BUCK2 in PWM Mode Showing Out-of-Phase Operation

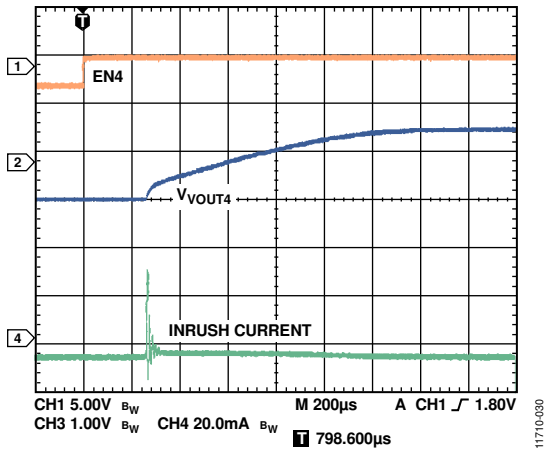

Figure 30. LDO Regulator Startup, V_{VOUT4} = 1.8 V

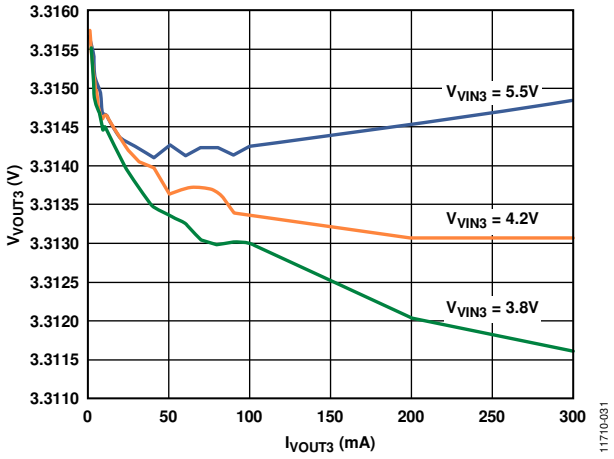

Figure 31. LDO Load Regulation Across Input Voltage, V_{VOUT3} = 3.3 V

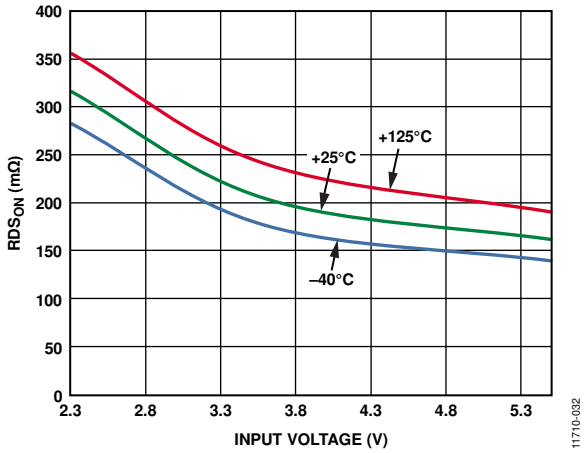

Figure 32. LFCSP NMOS RDS_{ON} vs. Input Voltage Across Temperature

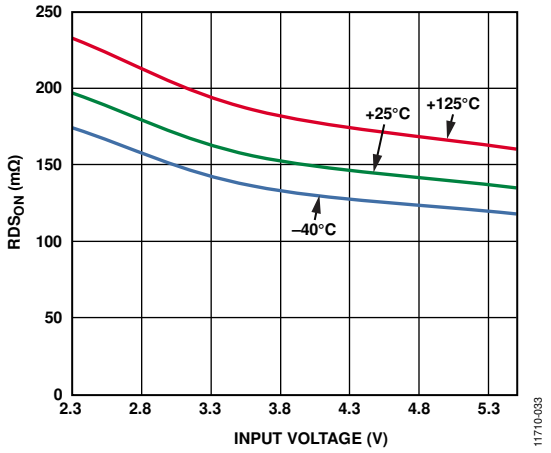

Figure 33. LFCSP PMOS RDS_{ON} vs. Input Voltage Across Temperature

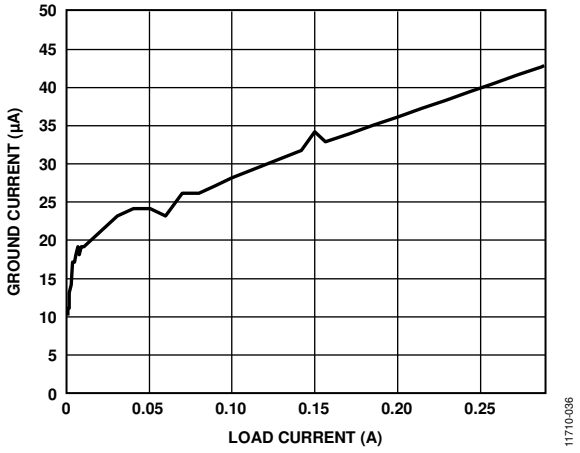

Figure 36. LDO Ground Current vs. Load Current, V_{VIN3} = 3.3 V, V_{VOUT3} = 2.8 V

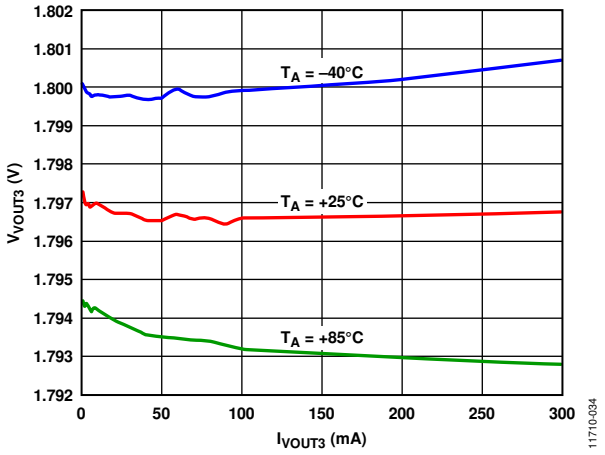

Figure 34. LDO Load Regulation Across Temperature, V_{VIN3} = 3.6 V, V_{VOUT3} = 1.8 V

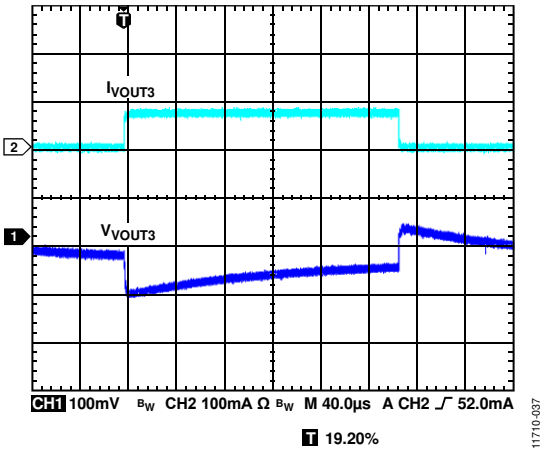

Figure 37. LDO Response to Load Transient, I_{VOUT3} from 1 mA to 80 mA, V_{VOUT3} = 2.8 V

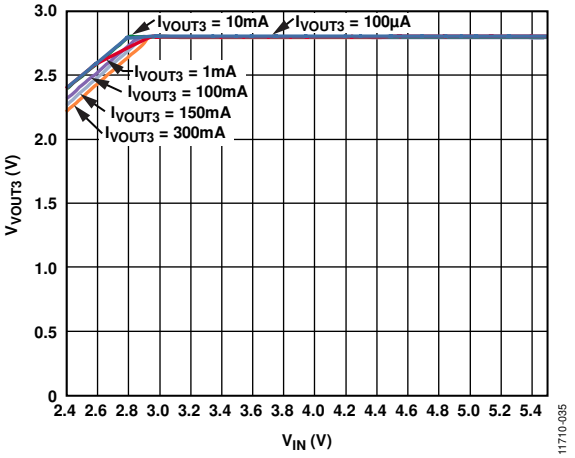

Figure 35. LDO Line Regulation Across Output Load, V_{VOUT3} = 2.8 V

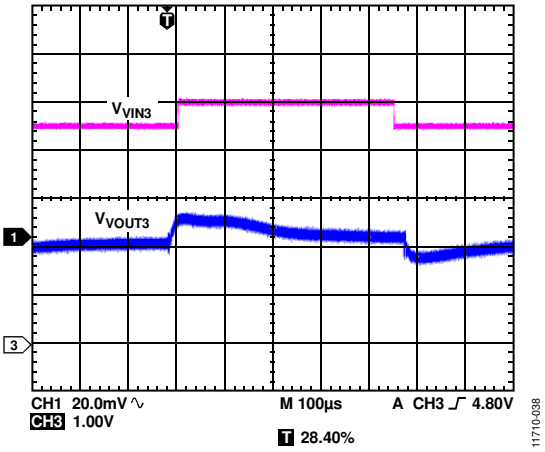

Figure 38. LDO Response to Line Transient, Input Voltage from 4.5 V to 5 V, V_{VOUT3} = 2.8 V

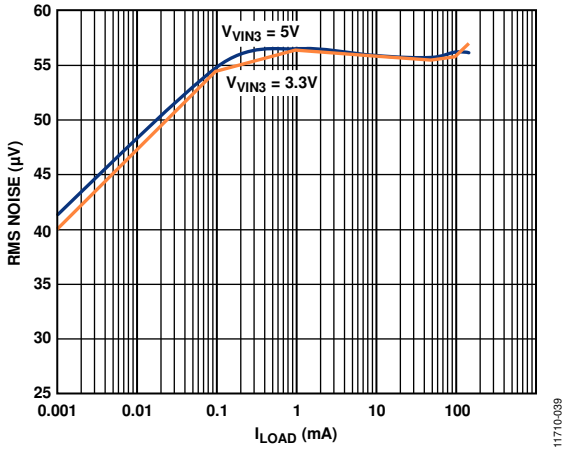

Figure 39. LDO Output Noise vs. Load Current, Across Input Voltage, V_{VOUT3} = 2.8 V

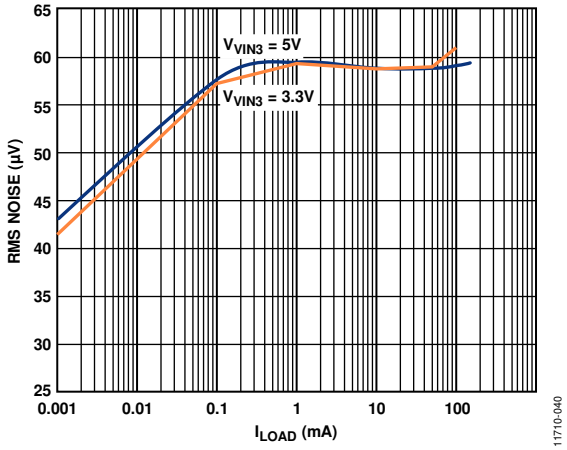

Figure 40. LDO Output Noise vs. Load Current, Across Input Voltage, V_{VOUT3} = 3.0 V

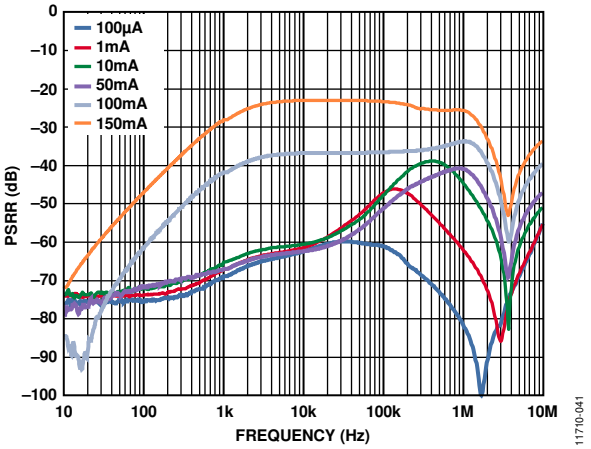

Figure 41. LDO PSRR Across Output Load, V_{VIN3} = 3.3 V, V_{VOUT3} = 2.8 V

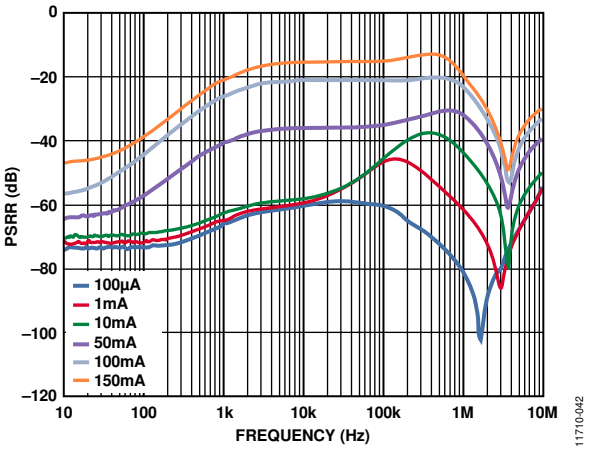

Figure 42. LDO PSRR Across Output Load, V_{VIN3} = 3.3 V, V_{VOUT3} = 3.0 V

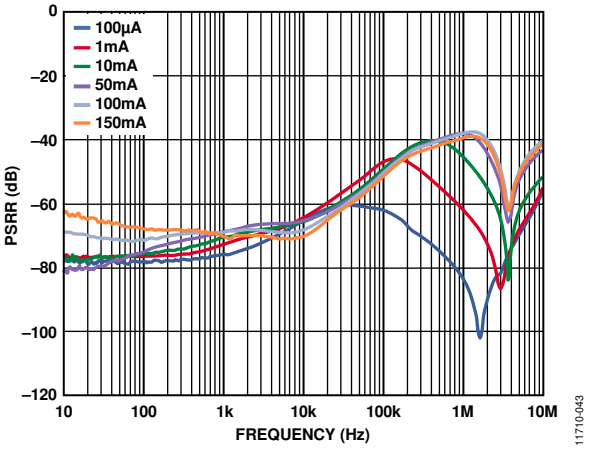

Figure 43. LDO PSRR Across Output Load, V_{VIN3} = 5.0 V, V_{VOUT3} = 2.8 V

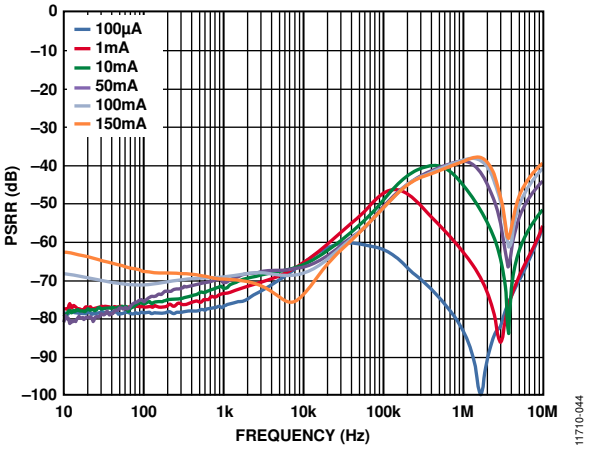

Figure 44. LDO PSRR Across Output Load, V_{VIN3} = 5.0 V, V_{VOUT3} = 3.0 V

THEORY OF OPERATION

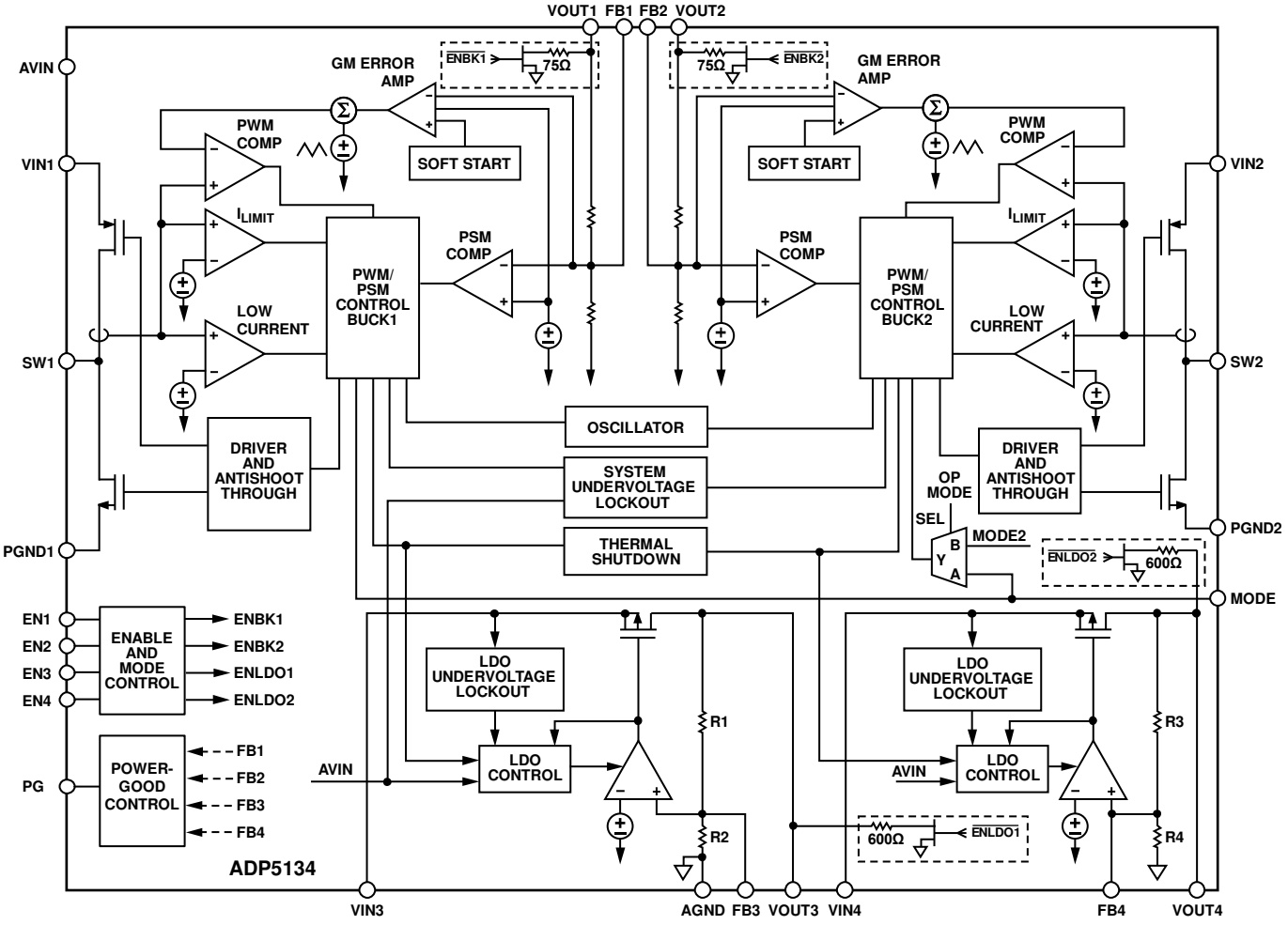

Figure 45. Functional Block Diagram

POWER MANAGEMENT UNIT

The ADP5134 is a micropower management unit (micro PMU) combining two step-down (buck) dc-to-dc converters and two low dropout (LDO) linear regulators. The high switching frequency and tiny 24-lead LFCSP package provide a small power management solution.

To combine these high performance regulators into the micro PMU, there is a system controller allowing them to operate together.

The buck regulators can operate in forced PWM mode if the MODE pin is set to logic high. In forced PWM mode, the buck regulator switching frequency is always constant and does not change with the load current. If the MODE pin is set to logic low, the switching regulators operate in automatic PWM/PSM mode. In this mode, the regulators operate at a fixed PWM frequency when the load current is above the PSM current threshold. When the load current falls below the PSM current threshold, the regulator in question enters PSM mode, where the switching occurs in bursts. The burst repetition rate is a function of the current load and the output capacitor value. This operating mode reduces the switching and quiescent current losses. The automatic PWM/PSM mode transition is controlled independently for each buck regulator. The two buck regulators operate in synchronization with each other.

The ADP5134 has individual enable pins (EN1 to EN4) that control the activation of each regulator. The regulators are activated by a high logic level applied to the respective ENx pin. EN1 controls BUCK1, EN2 controls BUCK2, EN3 controls LDO1, and EN4 controls LDO2.

Regulator output voltages are set through external resistor dividers or can be optionally factory programmed to default values (see the Ordering Guide section).

When a regulator is turned on, the output voltage ramp rate is controlled through a soft start circuit to avoid a large inrush current due to the charging of the output capacitors.

Power-Good Output

A power-good output is available at Pin 6 (PG) to monitor the output voltage of any combination of the four regulators. The PG output can also be factory programmed to monitor a specific regulator channel, such as BUCK1, as shown in Figure 46. The PG pin can connect to a pull-up current to drive external regulators or other circuits. In this configuration, the PG pin goes high when the channels monitored are in regulation and goes low when the output voltage falls below 90% of the nominal V_{VOUTx} level. The PG pin can also drive an LED for fault monitoring. For example, in this configuration, a red LED is biased, and current sinks into the PG pin when the output voltage falls below 90% of the nominal V_{VOUTx} level. This turns the LED on, and, when the output voltage is in regulation, turns it off.

Thermal Protection

In the event that the junction temperature rises above 150°C, the thermal shutdown circuit turns off all the regulators. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 20°C hysteresis is included so that when thermal shutdown occurs, the regulators do not return to operation until the on-chip temperature drops below 130°C. When coming out of thermal shutdown, all regulators restart with soft start control.

Undervoltage Lockout

To protect against battery discharge, undervoltage lockout (UVLO) circuitry is integrated into the system. If the input voltage on AVIN drops below a typical 2.15 V UVLO threshold, all channels shut down. In the buck regulator channels, both the power switch and the synchronous rectifier turn off. When the voltage on AVIN rises above the UVLO threshold, the device is enabled once more.

Alternatively, the user can request a new device model with a UVLO set at a higher level, suitable for 5 V supply applications. For these models, the device reaches the turn-off threshold when the input supply drops to 3.65 V typical. To order a device with options other than the default options listed in the Ordering Guide section, contact your local Analog Devices sales or distribution representative.

In case of a thermal or UVLO event, the active pull-downs (unless factory disabled) are enabled to discharge the output capacitors quickly. The pull-down resistors remain engaged until the thermal fault event is no longer present or the input supply voltage falls below the power-on reset voltage (V_{POR}) level. The typical value of V_{POR} is approximately 1 V.

Precision Enable and Shutdown Control

The ADP5134 has an individual enable control pin for each regulator. A voltage input to the ENx pin above the V_{IH_EN} level takes the device out of shutdown and turns on the housekeeping block of the ADP5134. As the V_{ENx} level continues to rise above the precision enable threshold (V_{ENR}), the regulators activate.

When V_{ENx} goes 80 mV typical below the V_{ENR} level, the regulators deactivate, and as the V_{ENx} level continues to go down below the V_{IL_EN} level, the device enters shutdown mode. In this mode, the current consumption of the device falls to below 1 µA.

Figure 46 shows the activation timings for the ADP5134 when regulators are in sequence, VOUT1 controlling EN2, VOUT2 controlling EN3, and VOUT3 controlling EN4. Also shown is the power-good signal monitoring BUCK1 only.

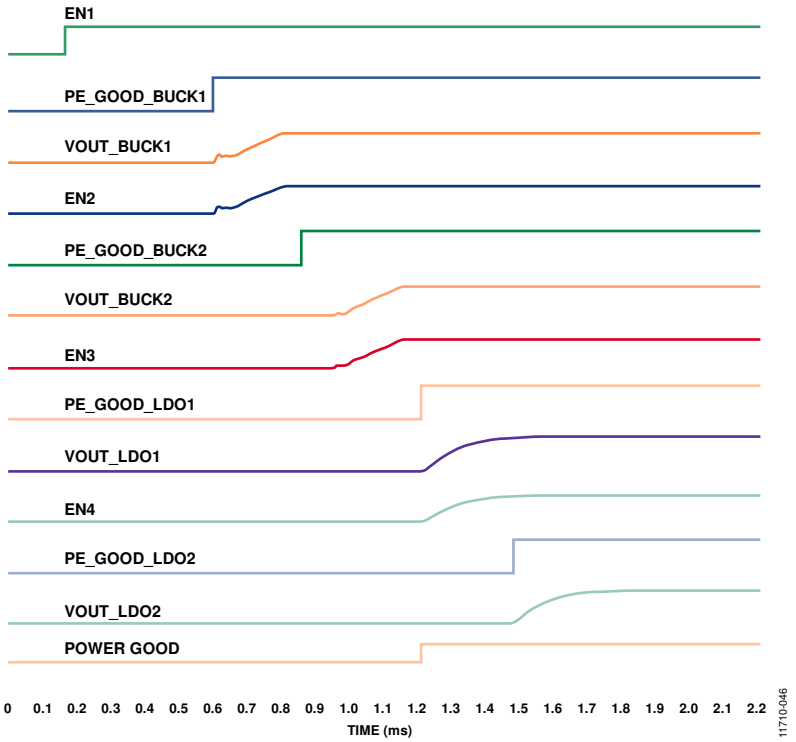

Figure 46. Regulator Sequencing on the ADP5134, Shutdown Control and Precision Enable Thresholds with PG Monitoring BUCK1 Only

BUCK1 AND BUCK2

The buck regulator uses a fixed frequency and high speed current mode architecture. The buck regulator operates with an input voltage of 2.5 V to 5.5 V.

The buck regulator output voltage is resistor programmable from 0.8 V to 3.8 V, shown in Figure 47 for BUCK1. The ratio of R1 and R2 multiplied by the feedback voltage determines the voltage level at output. For example, if R1 and R2 are chosen to have equal resistance values, the output voltage is set to 1.0 V. The output voltage can optionally be factory programmed to default values as indicated in the Ordering Guide section. In this event, R1 and R2 are not needed, and FB1 can be left unconnected. In all cases, VOUT1 must be connected to the output capacitor. FB1 is 0.5 V.

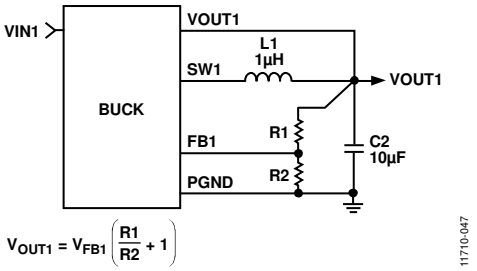

Figure 47. BUCK1 External Output Voltage Setting

Control Scheme

The buck regulators operate with a fixed frequency, current mode PWM control architecture at medium to high loads for high efficiency; however, they shift to a power save mode (PSM) control scheme at light loads to lower the regulation power losses. When operating in fixed frequency PWM mode, the duty cycle of the integrated switches is adjusted and regulates the output voltage. When operating in PSM at light loads, the output voltage is controlled in a hysteretic manner, with higher output voltage ripple. During this time, the converter is able to stop switching and enters an idle mode, which improves conversion efficiency.

PWM Mode

In PWM mode, the buck regulators operate at a fixed frequency of 3 MHz, set by an internal oscillator. At the start of each oscillator cycle, the positive channel field effect transistor (PFET) turns on, sending a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current threshold that turns off the PFET switch and turns on the negative channel field effect transistor (NFET) synchronous rectifier. When the NFET switches on, it sends a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle. The buck regulator regulates the output voltage by adjusting the peak inductor current threshold.

Power Save Mode (PSM)

The buck regulators smoothly transition to PSM operation when the load current decreases below the PSM current threshold. When either of the buck regulators enters PSM, an offset is induced in the PWM regulation level, which makes the output voltage rise. When the output voltage reaches a level approximately 1.5% above the PWM regulation level, PWM operation is turned off. At this point, both power switches are off, and the buck regulator enters an idle mode. The output capacitor discharges until the output voltage falls to the PWM regulation voltage level, at which point the device drives the inductor to make the output voltage rise again to the upper threshold. This process is repeated while the load current is below the PSM current threshold.

The ADP5134 has a dedicated MODE pin that controls the PSM and PWM operation. A logic high level applied to the MODE pin forces both bucks to operate in PWM mode. A low logic level sets the buck regulators to operate in automatic PSM/PWM mode.

PSM Current Threshold

The PSM current threshold is set to 100 mA. The buck regulators employ a scheme that enables this current to remain accurately controlled, independent of input and output voltage levels. This scheme also ensures that there is very little hysteresis between the PSM current threshold for entry to and exit from the PSM. The PSM current threshold is optimized for excellent efficiency over all load currents.

Oscillator and Phasing of Inductor Switching

The ADP5134 ensures that both buck regulators operate at the same switching frequency when both buck regulators are in PWM mode.

Additionally, the ADP5134 ensures that when both buck regulators are in PWM mode, they operate out of phase, whereby the BUCK2 PFET starts conducting exactly half a clock period after the BUCK1 PFET starts conducting.

Short-Circuit Protection

The buck regulators include frequency foldback to prevent output current runaway on a hard short. When the voltage at the feedback pin falls below half the target output voltage, indicating the possibility of a hard short at the output, the switching frequency is reduced to half the internal oscillator frequency. The reduction in the switching frequency allows more time for the inductor to discharge, preventing a runaway of output current.

Buck Regulator Soft Start

The buck regulators have an internal soft start function that ramps up the output voltage in a controlled manner upon startup, thereby limiting the inrush current. Limiting the inrush current prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the converter.

Current Limit

Each buck regulator has protection circuitry to limit the amount of positive current flowing through the PFET switch and the amount of negative current flowing through the synchronous rectifier. The positive current limit on the power switch limits the amount of current that can flow from the input to the output. The negative current limit prevents the inductor current from reversing direction and flowing out of the load.

100% Duty Operation

With a drop in input voltage, or with an increase in load current, the buck regulator may reach a limit where, even with the PFET switch on 100% of the time, the output voltage drops below the desired output voltage. At this limit, the buck regulator transitions to a mode where the PFET switch stays on 100% of the time. When the input conditions change again and the required duty cycle falls, the buck immediately restarts PWM regulation without allowing overshoot on the output voltage.

Active Pull-Down Resistors

All regulators have optional, factory programmable, active pull-down resistors that discharge the respective output capacitors when the regulators are disabled. The pull-down resistors are connected between VOUTx and AGND. Active pull-down resistors are disconnected when the regulators are turned on. The typical value of the pull-down resistors is 600 Ω for the LDO regulators and 75 Ω for the buck regulators.

LDO1 AND LDO2

The ADP5134 contains two LDO regulators with low quiescent current and low dropout linear regulators, and it provides up to 300 mA of output current. Drawing a low 10 µA quiescent current (typical) at no load makes the LDO regulator ideal for battery-operated portable equipment.

Each LDO regulator operates with an input voltage of 1.7 V to 5.5 V. The wide operating range makes these LDO regulators suitable for cascading configurations where the LDO regulator supply voltage is provided from one of the buck regulators.

Each LDO regulator output voltage is set through the external resistor dividers shown in Figure 48 for LDO1. The output voltage can optionally be factory programmed to default values as indicated in the Ordering Guide section. In this event, R5 and R6 are not needed, and FB3 must be connected to the top of the capacitor on VOUT3.

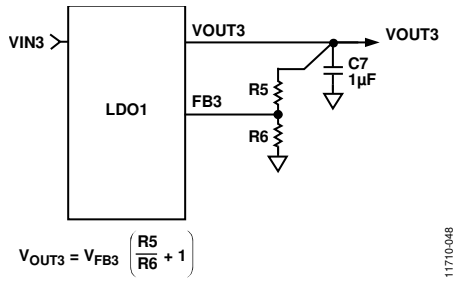

Figure 48. LDO1 External Output Voltage Setting

The LDO regulators also provide high power supply rejection ratio (PSRR), low output noise, and excellent line and load transient response with only a small 1 µF ceramic input and output capacitor.

LDO1 is optimized to supply the analog circuits because it offers better noise performance compared to LDO2. Use LDO1 in applications where noise performance is critical.

LDO Regulator Soft Start

On the ADP5134, the LDO regulators also have an internal soft start function that ramps up the output voltage in a controlled manner upon startup, thereby limiting the inrush current. There are two soft start options, fast and slow, to control how long the output voltage is ramped up. These options are factory programmed.

APPLICATIONS INFORMATION

BUCK REGULATOR EXTERNAL COMPONENT SELECTION

Trade-offs between performance parameters such as efficiency and transient response can be made by varying the choice of external components in the applications circuit, as shown in Figure 1.

Feedback Resistors

For the adjustable model, referring to Figure 47, the total combined resistance for R1 and R2 is not to exceed 400 kΩ.

Inductor

The high switching frequency of the ADP5134 buck regulators allows the selection of small chip inductors. For best performance, use inductor values between 0.7 µH and 3 µH. Suggested inductors are shown in Table 9.

The peak-to-peak inductor current ripple is calculated using the following equation:

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

where:
f_{SW} is the switching frequency.
L is the inductor value.

The minimum dc current rating of the inductor must be greater than the inductor peak current. The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{I_{RIPPLE}}{2}$$

Inductor conduction losses are caused by the flow of current through the inductor, which has an associated internal dc resistance (DCR). Larger sized inductors have smaller DCR, which can decrease inductor conduction losses. Inductor core losses are related to the magnetic permeability of the core material. Because the buck regulators are high switching frequency dc-to-dc converters, shielded ferrite core material is recommended for its low core losses and low electromagnetic interference (EMI).

Output Capacitor

Higher output capacitor values reduce the output voltage ripple and improve load transient response. When choosing this value, it is also important to account for the loss of capacitance due to output voltage dc bias.

Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. However, Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

The worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage is calculated using the following equation:

$$C_{EFF} = C_{OUT} \times (1 - TEMPCO) \times (1 - TOL)$$

where:
C_{EFF} is the effective capacitance at the operating voltage.
$TEMPCO$ is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{OUT} is 9.2 µF at 1.8 V, as shown in Figure 49.

Substituting these values in the equation yields

$$C_{EFF} = 9.2\ \mu F \times (1 - 0.15) \times (1 - 0.1) \approx 7.0\ \mu F$$

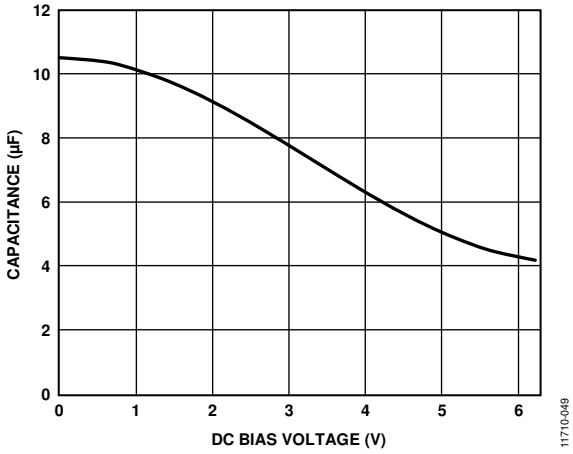

Figure 49. Capacitance vs. Voltage Characteristic

Table 9. Suggested 1.0 µH Inductors

Vendor	Model	Dimensions (mm)	ISAT (mA)	DCR (mΩ)
Murata	LQM2MPN1R0NG0B	2.0 × 1.6 × 0.9	1400	85
Murata	LQM2HPN1R0MJ0L	2.5 × 2.0 × 1.1	1500	90
Murata	LQH32PN1R0NN0	3.2 × 2.5 × 1.6	2300	45
Taiyo Yuden	CBC3225T1R0MR	3.2 × 2.5 × 2.5	2000	71
Coilcraft®	XFL4020-102ME	4.0 × 4.0 × 2.1	5400	11
Coilcraft	XPL2010-102ML	1.9 × 2.0 × 1.0	1800	89
Toko	MDT2520-CN	2.5 × 2.0 × 1.2	1350	85

To guarantee the performance of the buck regulators, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

The peak-to-peak output voltage ripple for the selected output capacitor and inductor values is calculated using the following equation:

$$V_{RIPPLE} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}} \approx \frac{V_{IN}}{(2\pi \times f_{SW})^2 \times L \times C_{OUT}}$$

Capacitors with lower effective series resistance (ESR) are preferred to guarantee low output voltage ripple, as shown in the following equation:

$$ESR_{COUT} \leq \frac{V_{RIPPLE}}{I_{RIPPLE}}$$

The effective capacitance needed for stability, which includes temperature and dc bias effects, is a minimum of 7 µF and a maximum of 40 µF.

The buck regulators require 10 µF output capacitors to guarantee stability and response to rapid load variations and to transition into and out of the PWM/PSM modes. A list of suggested capacitors is shown in Table 10. In certain applications where one or both buck regulators power a processor, the operating state is known because it is controlled by software. In this condition, the processor can drive the MODE pin according to the operating state; consequently, it is possible to reduce the output capacitor from 10 µF to 4.7 µF because the regulator does not expect a large load variation when working in PSM mode (see Figure 50).

Input Capacitor

Higher value input capacitors help to reduce the input voltage ripple and improve transient response. Maximum input capacitor current is calculated using the following equation:

$$I_{CIN} \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

To minimize supply noise, place the input capacitor as close as possible to the VINx pin of the buck regulator. As with the output capacitor, a low ESR capacitor is recommended.

The effective capacitance needed for stability, which includes temperature and dc bias effects, is a minimum of 3 µF and a maximum of 10 µF. The recommended range is from 4.7 µF to 10 µF to compensate for any capacitance losses for the buck regulator input and output capacitors. A list of suggested capacitors is shown in Table 10 and Table 11.

Table 10. Suggested 10 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60J106	0603	6.3
TDK	X5R	C1608JB0J106K	0603	6.3
Taiyo Yuden	X5R	JMK107BJ106MA-T	0603	6.3
Panasonic	X5R	ECJ-1VB0J106M	0603	6.3

Table 11. Suggested 4.7 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60J475ME19D	0603	6.3
Taiyo Yuden	X5R	JMK107BJ475	0603	6.3
Panasonic	X5R	ECJ-0EB0J475M	0402	6.3

LDO REGULATOR EXTERNAL COMPONENT SELECTION

Feedback Resistors

For the adjustable model, the maximum value of R6 is not to exceed 200 kΩ (see Figure 48).

Output Capacitor

The ADP5134 LDO regulators are designed for operation with small, space-saving ceramic capacitors; however, they function with most commonly used capacitors as long as care is taken with the ESR value. The ESR of the output capacitor affects stability of the LDO control loop. A minimum of 0.70 µF capacitance with an ESR of 1 Ω or less is recommended to ensure the stability of the ADP5134. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP5134 to large changes in load current.

Input Bypass Capacitor

Connecting a 1 µF capacitor from VIN3 and VIN4 to ground reduces the circuit sensitivity to printed circuit board (PCB) layout, especially when long input traces or high source impedance is encountered. A list of 1.0 µF output capacitors is shown in Table 12. If greater than 1.0 µF of output capacitance is required, increase the input capacitor to match it.

Table 12. Suggested 1.0 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM155B30J105K	0402	6.3
Murata	X5R	GRM155R61A105KE15D	0402	10.0
TDK	X5R	C1005JB0J105K	0402	6.3
Panasonic	X5R	ECJ0EB0J105K	0402	6.3
Taiyo Yuden	X5R	LMK105BJ105MV-F	0402	10.0

Input and Output Capacitor Properties

Use any good quality ceramic capacitors with the ADP5134 as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. However, Y5V and Z5U dielectrics are not recommended for use with any LDO because of their poor temperature and dc bias characteristics.

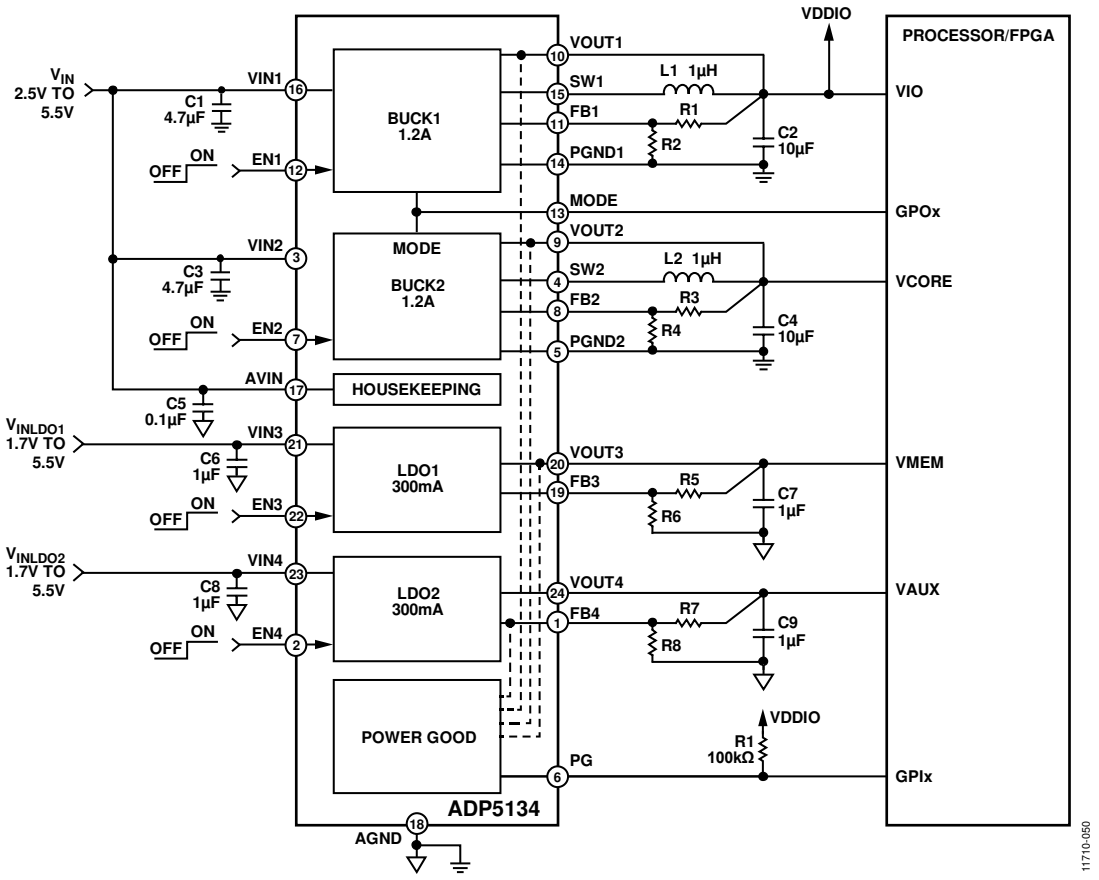

Figure 50. Processor System Power Management with PSM/PWM Control and PG

Figure 51 depicts the capacitance vs. dc bias voltage characteristic of a 0402 size, 1 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or with higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

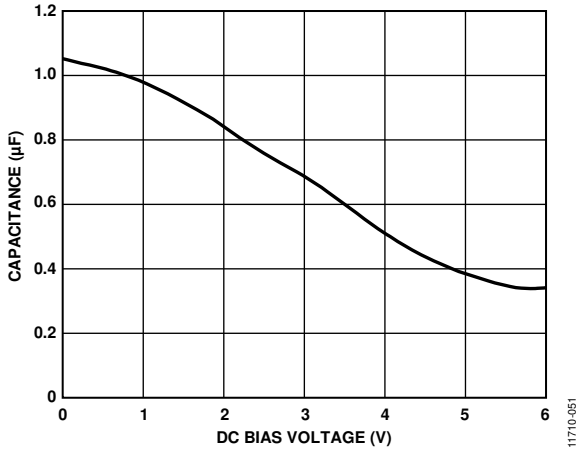

Figure 51. Capacitance vs. DC Bias Voltage Characteristic

Use the following equation to determine the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage:

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL)$$

where:

C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{BIAS} is 0.85 µF at 1.8 V, as shown in Figure 51.

Substituting these values into the following equation,

$$C_{EFF} = 0.85\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.65\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO regulator over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP5134, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors are evaluated for each application.

POWER DISSIPATION AND THERMAL CONSIDERATIONS

The ADP5134 is a highly efficient micro PMU, and, in most cases, the power dissipated in the device is not a concern. However, if the device operates at high ambient temperatures and maximum loading condition, the junction temperature can reach the maximum allowable operating limit (125°C).

When the temperature exceeds 150°C, the ADP5134 turns off all the regulators, allowing the device to cool down. When the die temperature falls below 130°C, the ADP5134 resumes normal operation.

This section provides guidelines to calculate the power dissipated in the device and ensure that the ADP5134 operates below the maximum allowable junction temperature.

The efficiency for each regulator on the ADP5134 is given by

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100\% \quad (1)$$

where:
η is the efficiency.
P_{OUT} is the output power.
P_{IN} is the input power.

Power loss is given by

$$P_{LOSS} = P_{IN} - P_{OUT} \quad (2a)$$

or

$$P_{LOSS} = P_{OUT}(1-\eta)/\eta \quad (2b)$$

Power dissipation can be calculated in several ways. The most intuitive and practical method is to measure the power dissipated at the input and all the outputs. Perform the measurements at the worst-case conditions (voltages, currents, and temperature). The difference between input and output power is dissipated in the device and the inductor. Use Equation 4 to derive the power lost in the inductor and, from this, use Equation 3 to calculate the power dissipation in the ADP5134 buck converter.

A second method to estimate the power dissipation uses the efficiency curves provided for the buck regulator, and the power lost on each LDO regulator can be calculated using Equation 12. When the buck regulator efficiency is known, use Equation 2b to derive the total power lost in the buck regulator and inductor, use Equation 4 to derive the power lost in the inductor, and then calculate the power dissipation in the buck converter using Equation 3. Add the power dissipated in the buck regulator and in the two LDO regulators to find the total dissipated power.

Note that the efficiency curves of the buck regulator are typical values and may not be provided for all possible combinations of V_{VINx}, V_{VOUTx}, and I_{VOUTx}. To account for these variations, it is necessary to include a safety margin when calculating the power dissipated in the buck regulator.

A third way to estimate the power dissipation is analytical and involves modeling the losses in the buck regulator circuit provided by Equation 8 to Equation 11 and the losses in the LDO regulator provided by Equation 12.

BUCK REGULATOR POWER DISSIPATION

The power loss of the buck regulator is approximated by

$$P_{LOSS} = P_{DBUCK} + P_L \quad (3)$$

where:
P_{DBUCK} is the power dissipation on one of the ADP5134 buck regulators.
P_L is the inductor power losses.

The inductor power losses are external to the device, and they do not have any effect on the die temperature.

The inductor power losses are estimated (without core losses) by

$$P_L \approx I_{VOUT1(RMS)}^2 \times DCR_L \quad (4)$$

where:
$I_{VOUT1(RMS)}$ is the rms load current of the buck regulator.
DCR_L is the inductor series resistance.

$$I_{VOUT1(RMS)} = I_{VOUT1} \times \sqrt{1 + \frac{r}{12}} \quad (5)$$

where r is the normalized inductor ripple current.

$$r = V_{VOUT1} \times (1 - D)/(I_{VOUT1} \times L \times f_{SW}) \quad (6)$$

where:
L is the inductance.
f_{SW} is the switching frequency.
D is the duty cycle.

$$D = V_{VOUT1}/V_{VIN1} \quad (7)$$

The buck regulator power dissipation, P_{DBUCK}, of the ADP5134 includes power switch conductive losses, switch losses, and transition losses of each channel. There are other sources of loss; however, these are generally less significant at high output load currents where the thermal limit of the application is. Equation 8 captures the calculation that can estimate the power dissipation in the buck regulator.

$$P_{DBUCK} = P_{COND} + P_{SW} + P_{TRAN} \quad (8)$$

The power switch conductive losses are due to the output current, I_{VOUT1}, flowing through the P-channel MOSFET and the N-channel MOSFET power switches that have internal resistance, RDS_{ON-P} and RDS_{ON-N}, respectively. The amount of conductive power loss is found by

$$P_{COND} = [RDS_{ON-P} \times D + RDS_{ON-N} \times (1 - D)] \times I_{VOUT1}(RMS)^2 \quad (9)$$

where:
RDS_{ON-P} is approximately 0.2 Ω.
RDS_{ON-N} is approximately 0.16 Ω.

The RDS_{ON-P} and RDS_{ON-N} values are correct given that VIN1 = VIN2 = 3.6 V, at a junction temperature of 25°C.

At VIN1 = VIN2 = 2.5 V, these values change to 0.31 Ω and 0.21 Ω, respectively, and at VIN1 = VIN2 = 5.5 V, the values are 0.16 Ω and 0.14 Ω, respectively.

Switching losses are associated with the current drawn by the driver to turn on and turn off the power devices at the switching frequency. The amount of switching power loss is given by

$$P_{SW} = (C_{GATE\text{-}P} + C_{GATE\text{-}N}) \times V_{VIN1}^2 \times f_{SW} \quad (10)$$

where:
$C_{GATE\text{-}P}$ is the P-channel MOSFET gate capacitance.
$C_{GATE\text{-}N}$ is the N-channel MOSFET gate capacitance.

For the ADP5134, the total of ($C_{GATE\text{-}P}$ + $C_{GATE\text{-}N}$) is approximately 150 pF.

The transition losses occur because the P-channel power MOSFET cannot be turned on or off instantaneously, and the SWx node takes some time to slew from near ground to near V_{VOUTx} (and from V_{VOUTx} to ground). The amount of transition loss is calculated by

$$P_{TRAN} = V_{VINx} \times I_{VOUTx} \times (t_{RISE} + t_{FALL}) \times f_{SW} \quad (11)$$

where t_{RISE} and t_{FALL} are the rise time and the fall time of the switching node, SWx. For the ADP5134, the rise and fall times of SWx are approximately 5 ns.

If Equation 1 through Equation 11 and their associated parameters are used for estimating the converter efficiency, note that the equations do not describe all of the converter losses, and the parameter values given are typical numbers. The converter performance also depends on the choice of passive components and board layout; therefore, include a sufficient safety margin in the estimate.

LDO Regulator Power Dissipation

The power loss of an LDO regulator is given by

$$P_{DLDO} = [(V_{VINx} - V_{VOUTx}) \times I_{LOAD}] + (V_{VINx} \times I_{GND}) \quad (12)$$

where:
V_{VINx} and V_{VOUTx} are the input and output voltages of the LDO regulator, respectively.
I_{LOAD} is the load current of the LDO regulator.
I_{GND} is the ground current of the LDO regulator.

Power dissipation due to the ground current is small, and it can be ignored.

The total power dissipation in the ADP5134 simplifies to

$$P_D = P_{DBUCK1} + P_{DBUCK2} + P_{DLDO1} + P_{DLDO2} \quad (13)$$

JUNCTION TEMPERATURE

In cases where the board temperature, T_A, is known, the thermal resistance parameter, θ_{JA}, can be used to estimate the junction temperature rise. T_J is calculated from T_A and P_D using the formula

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (14)$$

Refer to Table 7 for the thermal resistance values. A very important factor to consider is that θ_{JA} is based on a 4-layer, 4 in × 3 in, 2.5 oz copper board, as per JEDEC standard, and real applications can use different sizes and layers. It is important to maximize the copper used to remove the heat from the device. Copper exposed to air dissipates heat better than copper used in the inner layers. Connect the exposed pad to the ground plane with several vias.

If the case temperature is measured, the junction temperature is calculated by

$$T_J = T_C + (P_D \times \theta_{JC}) \quad (15)$$

where:
T_C is the case temperature.
θ_{JC} is the junction-to-case thermal resistance provided in Table 7.

When designing an application for a particular ambient temperature range, calculate the expected ADP5134 power dissipation (P_D) due to the losses of all channels by using Equation 8 to Equation 13. From this power calculation, the junction temperature, T_J, can be estimated using Equation 14.

The reliable operation of the converter and the two LDO regulators can be achieved only if the estimated die junction temperature of the ADP5134 (Equation 14) is less than 125°C. Reliability and mean time between failures (MTBFs) are highly affected by increasing the junction temperature. Additional information about product reliability can be found in the *ADI Reliability Handbook* at www.analog.com/UG-311.

PCB LAYOUT GUIDELINES

Poor layout can affect the performance of the ADP5134, causing EMI and electromagnetic compatibility (EMC) problems, ground bounce, and voltage losses. Poor layout can also affect regulation and stability. A good layout is implemented using the following guidelines. Also, refer to the User Guide UG-591, *Evaluating the ADP5134 Micropower Management Unit (PMU)*.

- Place the inductor, input capacitor, and output capacitor near the IC using short tracks. These components carry high switching frequencies, and large tracks act as antennas.
- Route the output voltage path away from the inductor and SWx node to minimize noise and magnetic interference.
- Maximize the size of ground metal on the component side to help with thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.
- Connect VIN1, VIN2, and AVIN together near the IC using short tracks.