Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# Charge Pump, 7-Channel Smart LED Driver with I²C Interface

Data Sheet **ADP8861**

## FEATURES

- Charge pump with automatic gain selection of 1×, 1.5×, and 2× for maximum efficiency
- 7 independent, programmable LED drivers
  - 7 drivers capable of 30 mA (typical)
  - 1 driver also capable of 60 mA (typical)
- Programmable maximum current limit (128 levels)
- Standby mode for <1 µA current consumption
- 16 programmable fade in and fade out times
  - 0.1 sec to 5.5 sec
  - Choose from linear, square, or cubic rates
- Fading override
- I²C-compatible interface for all programming
- Dedicated reset pin and built-in power-on reset (POR)
- Short-circuit, overvoltage, and overtemperature protection
- Internal soft start to limit inrush currents
- Input-to-output isolation during faults or shutdown
- Operation down to $V_{IN}$ = 2.5 V with undervoltage lockout (UVLO) at $V_{IN}$ = 2.0 V
- Available in a small 20-ball, 2.15 mm × 2.36 mm × 0.6 mm WLCSP or a 20-lead, 4 mm × 4 mm × 0.75 mm LFCSP

## APPLICATIONS

- Mobile display backlighting
- Mobile phone keypad backlighting
- Dual RGB backlighting
- LED indication
- General backlighting of small format displays

## TYPICAL OPERATING CIRCUIT

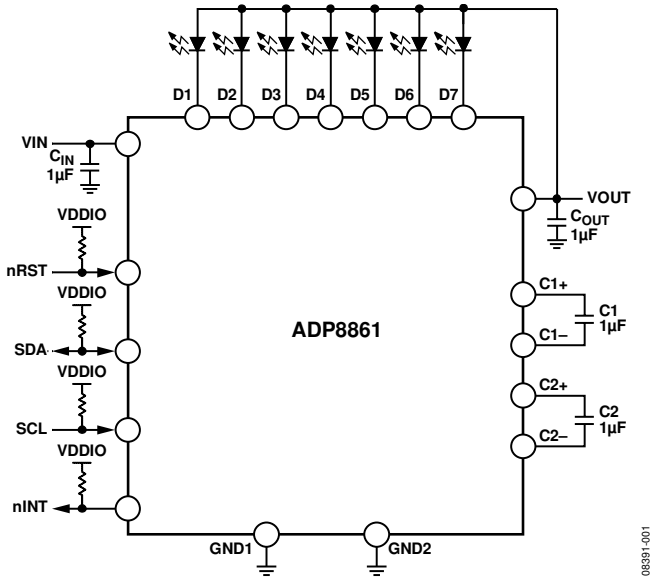


*Figure 1.*

## GENERAL DESCRIPTION

The ADP8861 provides a powerful charge pump driver with independent control of up to seven LEDs. These seven LEDs can be independently driven up to 30 mA (typical). The seventh LED can also be driven to 60 mA (typical). All LEDs are programmable for maximum current and fade in/out times via the I²C interface. These LEDs can also be combined into groups to reduce the processor instructions during fade in/out.

This entire configuration is driven by a two-capacitor charge pump with gains of 1×, 1.5×, and 2×. The charge pump is capable of driving a maximum $I_{OUT}$ of 240 mA from a supply of 2.5 V to 5.5 V. A full suite of safety features, including short-circuit, overvoltage, and overtemperature protection, allows easy implementation of a safe and robust design. Additionally, input inrush currents are limited via an integrated soft start combined with controlled input-to-output isolation.

Rev. C
Document Feedback


One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 
Technical Support www.analog.com

# ADP8861* PRODUCT PAGE QUICK LINKS

**Last Content Update: 03/03/2017**

## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- ADP8861 Evaluation Board

## DOCUMENTATION

**Data Sheet**

- ADP8861: Charge Pump, 7-Channel Smart LED Driver with I2C Interface Data Sheet

**User Guides**

- UG-005: Software User Guide

## SOFTWARE AND SYSTEMS REQUIREMENTS

- ADP8860 Back-light LED Linux Driver

## DESIGN RESOURCES

- ADP8861 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all ADP8861 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

Submit feedback for this data sheet.

# TABLE OF CONTENTS



## REVISION HISTORY

**2/2017—Rev. B to Rev. C**

Updated Outline Dimensions ... 39
Changes to Ordering Guide ... 40

**4/2012—Rev. A to Rev. B**

Changes to Table 1 ... 4
Updated Outline Dimensions ... 40
Changes to Ordering Guide ... 40

**6/2010—Rev. 0 to Rev. A**

Changes to Features Section and General Description Section . 1
Changes to Thermal Resistance Section and Table 3 ... 5
Added Figure 4; Renumbered Sequentially ... 6
Changes to Table 4 ... 6
Changes to Layout Guidelines Section ... 19
Updated Outline Dimensions ... 39
Changes to Ordering Guide ... 40

**4/2010—Revision 0: Initial Version**

# SPECIFICATIONS

VIN = 3.6 V, SCL = 2.7 V, SDA = 2.7 V, nINT = open, nRST = 2.7 V, $V_{D1:D7}$ = 0.4 V, Capacitor C1 = 1 µF, Capacitor C2 = 1 µF, $C_{OUT}$ = 1 µF, typical values are at $T_A$ = 25°C and are not guaranteed, minimum and maximum limits are guaranteed from $T_A$ = −40°C to +85°C, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SUPPLY | | | | | | |
| Input Voltage | | | | | | |
| Operating Range | $V_{IN}$ | | 2.5 | | 5.5 | V |
| Start-Up Level | $V_{IN(START)}$ | $V_{IN}$ increasing | | 2.05 | 2.30 | V |
| Low Level | $V_{IN(STOP)}$ | $V_{IN}$ decreasing | 1.75 | 1.97 | | V |
| $V_{IN(START)}$ Hysteresis | $V_{IN(HYS)}$ | After startup | | 80 | | mV |
| UVLO Noise Filter | $t_{UVLO}$ | | | 10 | | µs |
| Quiescent Current | $I_Q$ | | | | | |
| Prior to $V_{IN(START)}$ | $I_{Q(START)}$ | $V_{IN} = V_{IN(START)} - 100$ mV | | 10 | | µA |
| During Standby | $I_{Q(STBY)}$ | $V_{IN}$ = 3.6 V, Bit nSTBY = 0, SCL = SDA = 0 V | | 0.3 | 1.0 | µA |
| After Startup and Switching | $I_{Q(ACTIVE)}$ | $V_{IN}$ = 3.6 V, Bit nSTBY = 1, $I_{OUT}$ = 0 mA, gain = 2× | | 4.5 | 7.2 | mA |
| OSCILLATOR | | Charge pump gain = 2× | | | | |
| Switching Frequency | $f_{SW}$ | | 0.8 | 1 | 1.32 | MHz |
| Duty Cycle | D | | | 50 | | % |
| OUTPUT CURRENT CONTROL | | | | | | |
| Maximum Drive Current | $I_{D1:D7(MAX)}$ | $V_{D1:D7}$ = 0.4 V | | | | |
| Diode1 to Diode 7 | | Bit SCR = 0 in the ISC7 register | | | | |
| $T_J$ = 25°C | | | 26.2 | 30 | 34.1 | mA |
| $T_J$ = −40°C to +85°C | | | 24.4 | | 34.1 | mA |
| Diode 7 Only (60 mA Setting) | $I_{D7(60\ mA)}$ | $V_{D7}$ = 0.4 V, Bit SCR = 1 in the ISC7 register | | | | |
| $T_J$ = 25°C | | | 52.5 | 60 | 67 | mA |
| $T_J$ = −40°C to +85°C | | | 48.8 | | 67 | mA |
| LED Current Source Matching[1] | $I_{MATCH}$ | | | | | |
| All Current Sinks | $I_{MATCH7}$ | $V_{D1:D7}$ = 0.4 V | | 2.0 | | % |
| Diode 2 to Diode 7 Current Sinks | $I_{MATCH6}$ | $V_{D2:D7}$ = 0.4 V | | 1.5 | | % |
| Leakage Current on LED Pins | $I_{D1:D7(LKG)}$ | $V_{IN}$ = 5.5 V, $V_{D1:D7}$ = 2.5 V, Bit nSTBY = 1 | | | 0.5 | µA |
| Equivalent Output Resistance | $R_{OUT}$ | | | | | |
| Gain = 1× | | $V_{IN}$ = 3.6 V, $I_{OUT}$ = 100 mA | | 0.5 | | Ω |
| Gain = 1.5× | | $V_{IN}$ = 3.1 V, $I_{OUT}$ = 100 mA | | 3.0 | | Ω |
| Gain = 2× | | $V_{IN}$ = 2.5 V, $I_{OUT}$ = 100 mA | | 3.8 | | Ω |
| Regulated Output Voltage | $V_{OUT(REG)}$ | $V_{IN}$ = 3 V, gain = 2×, $I_{OUT}$ = 10 mA | 4.3 | 4.9 | 5.5 | V |
| AUTOMATIC GAIN SELECTION | | | | | | |
| Minimum Voltage | | | | | | |
| Gain Increases | $V_{HR(UP)}$ | Decrease $V_{D1:D7}$ until the gain switches up | 162 | 200 | 276 | mV |
| Minimum Current Sink Headroom Voltage | $V_{HR(MIN)}$ | $I_{DX} = I_{DX(MAX)} \times 95\%$ | | 180 | | mV |
| Gain Delay | $t_{GAIN}$ | The delay after gain has changed and before gain is allowed to change again | | 100 | | µs |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| FAULT PROTECTION | | | | | | |
| Start-Up Charging Current Source | $I_{SS}$ | $V_{IN}$ = 3.6 V, $V_{OUT}$ = 0.8 × $V_{IN}$ | 2.5 | 3.75 | 5.5 | mA |
| Output Voltage Threshold | $V_{OUT}$ | | | | | |
| Exit Soft Start | $V_{OUT(START)}$ | $V_{OUT}$ rising | | 0.92 × $V_{IN}$ | | V |
| Short-Circuit Protection | $V_{OUT(SC)}$ | $V_{OUT}$ falling | | 0.55 × $V_{IN}$ | | V |
| Output Overvoltage Protection | $V_{OVP}$ | | | | | |
| Activation Level | | | | 5.8 | | V |
| OVP Recovery Hysteresis | | | | 500 | | mV |
| Thermal Shutdown | | | | | | |
| Threshold | TSD | | | 150 | | °C |
| Hysteresis | $TSD_{(HYS)}$ | | | 20 | | °C |
| Isolation from Input to Output During Fault | $I_{OUTLKG}$ | $V_{IN}$ = 5.5 V, $V_{OUT}$ = 0 V, Bit nSTBY = 0 | | | 1.5 | µA |
| Time to Validate a Fault | $t_{FAULT}$ | | | 2 | | µs |
| I²C INTERFACE | | | | | | |
| Operating $V_{DDIO}$ Voltage | $V_{DDIO}$ | | | | 5.5 | V |
| Logic Low Input[2] | $V_{IL}$ | $V_{IN}$ = 2.5 V | | | 0.5 | V |
| Logic High Input[3] | $V_{IH}$ | $V_{IN}$ = 5.5 V | 1.55 | | | V |
| I²C TIMING SPECIFICATIONS | | Guaranteed by design | | | | |
| Delay from Reset Deassertion to I²C Access | $t_{RESET}$ | | | | 20 | µs |
| SCL Frequency | $f_{SCL}$ | | | | 400 | kHz |
| SCL High Time | $t_{HIGH}$ | | 0.6 | | | µs |
| SCL Low Time | $t_{LOW}$ | | 1.3 | | | µs |
| Setup Time | | | | | | |
| Data | $t_{SU, DAT}$ | | 100 | | | ns |
| Repeated Start | $t_{SU, STA}$ | | 0.6 | | | µs |
| Stop Condition | $t_{SU, STO}$ | | 0.6 | | | µs |
| Hold Time | | | | | | |
| Data | $t_{HD, DAT}$ | | 0 | | 0.9 | µs |
| Start/Repeated Start | $t_{HD, STA}$ | | 0.6 | | | µs |
| Bus Free Time (Stop and Start Conditions) | $t_{BUF}$ | | 1.3 | | | µs |
| Rise Time (SCL and SDA) | $t_R$ | | 20 + 0.1 $C_B$ | | 300 | ns |
| Fall Time (SCL and SDA) | $t_F$ | | | | 300 | ns |
| Pulse Width of Suppressed Spike | $t_{SP}$ | | 0 | | 50 | ns |
| Capacitive Load per Bus Line | $C_B$ | | | | 400 | pF |

[1] Current source matching is calculated by dividing the difference between the maximum and minimum currents from the sum of the maximum and minimum.
[2] $V_{IL}$ is a function of the input voltage. See Figure 16 in the Typical Performance Characteristics section for typical values over operating ranges.
[3] $V_{IH}$ is a function of the input voltage. See Figure 16 in the Typical Performance Characteristics section for typical values over operating ranges.

## I²C TIMING DIAGRAM

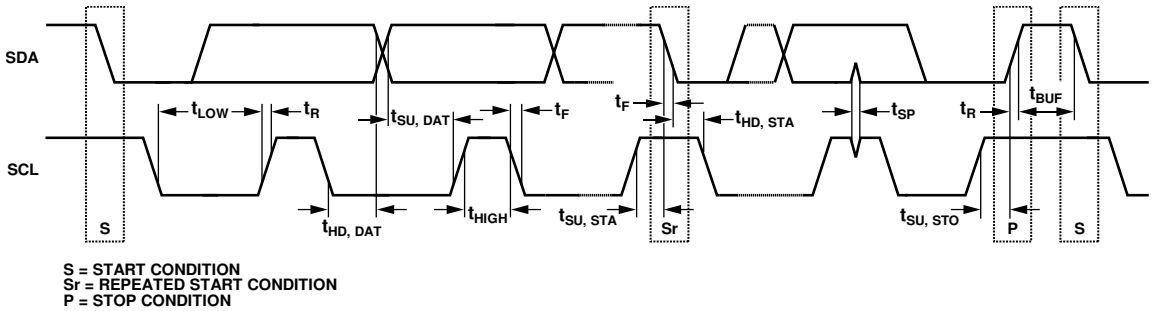


*Figure 2. I²C Interface Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| VIN, VOUT | −0.3 V to +6 V |
| D1, D2, D3, D4, D5, D6, and D7 | −0.3 V to +6 V |
| nINT, nRST, SCL, and SDA | −0.3 V to +6 V |
| Output Short-Circuit Duration | Indefinite |
| Operating Temperature Range | |
| Ambient ($T_A$) | −40°C to +85°C[1] |
| Junction ($T_J$) | −40°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Soldering Conditions | JEDEC J-STD-020 |
| ESD (Electrostatic Discharge) | |
| Human Body Model (HBM) | ±3 kV |
| Charged Device Model (CDM) | ±1.5 kV |

[1] The maximum operating junction temperature ($T_{J(MAX)}$) takes precedence over the maximum operating ambient temperature ($T_{A(MAX)}$). See the Maximum Temperature Ranges section for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all voltages are referenced to ground.

## MAXIMUM TEMPERATURE RANGES

The maximum operating junction temperature ($T_{J(MAX)}$) takes precedence over the maximum operating ambient temperature ($T_{A(MAX)}$). Therefore, in situations where the ADP8861 is exposed to poor thermal resistance and high power dissipation ($P_D$), the maximum ambient temperature may need to be derated. In these cases, the maximum ambient temperature can be calculated with the following equation:

$$T_{A(MAX)} = T_{J(MAX)} - (\theta_{JA} \times P_{D(MAX)})$$

## THERMAL RESISTANCE

$\theta_{JA}$ (junction to air) is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. The $\theta_{JA}$, $\theta_{JB}$ (junction to board), and $\theta_{JC}$ (junction to case) are determined according to JESD51-9 on a 4-layer printed circuit board (PCB) with natural convection cooling. For the LFCSP package, the exposed pad must be soldered to GND.

**Table 3. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JB}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|---|
| WLCSP | 48 | 9 | N/A[1] | °C/W |
| LFCSP | 49.5 | N/A[1] | 5.3 | °C/W |

[1] N/A stands for not applicable.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

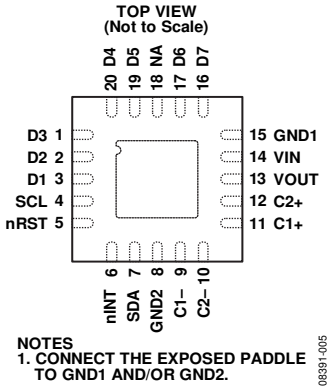


*Figure 3. LFCSP Pin Configuration*

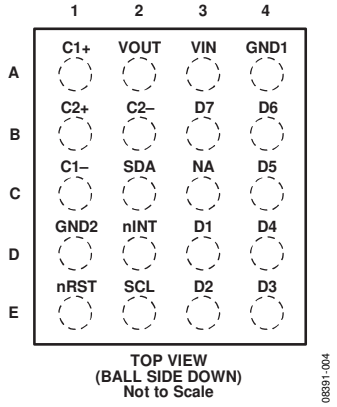


*Figure 4. WLCSP Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin No. | | | |
|---|---|---|---|
| **LFCSP** | **WLCSP** | **Mnemonic** | **Description** |
| 14 | A3 | VIN | Input Voltage, 2.5 V to 5.5 V. |
| 3 | D3 | D1 | LED Sink 1. |
| 2 | E3 | D2 | LED Sink 2. |
| 1 | E4 | D3 | LED Sink 3. |
| 20 | D4 | D4 | LED Sink 4. |
| 19 | C4 | D5 | LED Sink 5. |
| 17 | B4 | D6 | LED Sink 6. |
| 16 | B3 | D7 | LED Sink 7. |
| 18 | C3 | NA | This pin is not used and must be connected to ground. |
| 13 | A2 | VOUT | Charge Pump Output. |
| 11 | A1 | C1+ | Charge Pump C1+. |
| 9 | C1 | C1− | Charge Pump C1−. |
| 12 | B1 | C2+ | Charge Pump C2+. |
| 10 | B2 | C2− | Charge Pump C2−. |
| 15 | A4 | GND1 | Ground. Connect the exposed pad to GND1 and/or GND2. |
| 8 | D1 | GND2 | Ground. Connect the exposed pad to GND1 and/or GND2. |
| 6 | D2 | nINT | Processor Interrupt (Active Low). Requires an external pull-up resistor. If this pin is not used, it can be left floating. |
| 5 | E1 | nRST | Hardware Reset (Active Low). This pin resets the device to the default conditions. If not used, this pin must be tied above $V_{IH(MIN)}$. |
| 7 | C2 | SDA | $I^2C$ Serial Data. Requires an external pull-up resistor. |
| 4 | E2 | SCL | $I^2C$ Clock. Requires an external pull-up resistor. |
| 21 | Not applicable | EPAD | Exposed Paddle. Connect the exposed paddle to GND1 and/or GND2. |

# TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 3.6 V, SCL = 2.7 V, SDA = 2.7 V, nRST = 2.7 V, $V_{D1:D7}$ = 0.4 V, $C_{IN}$ = 1 µF, Capacitor C1 = 1 µF, Capacitor C2 = 1 µF, $C_{OUT}$ = 1 µF, $T_A$= 25°C, unless otherwise noted.

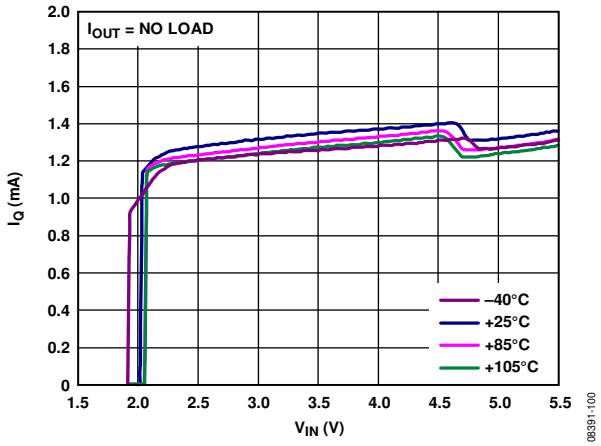


Figure 5. Typical Quiescent Current, G = 1×

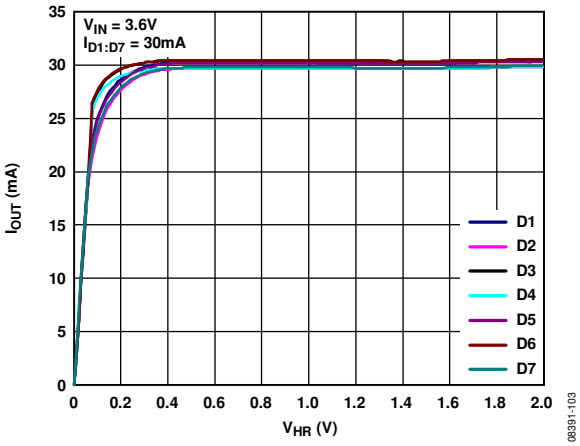


Figure 8. Typical Diode Current vs. Current Sink Headroom Voltage ($V_{HR}$)

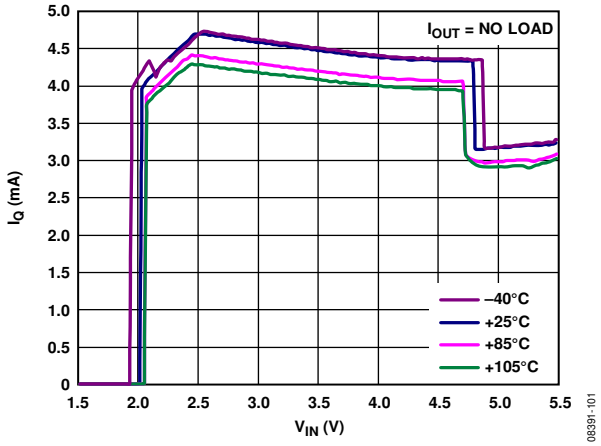


Figure 6. Typical Quiescent Current, G = 2×, $I_{Q(ACTIVE)}$

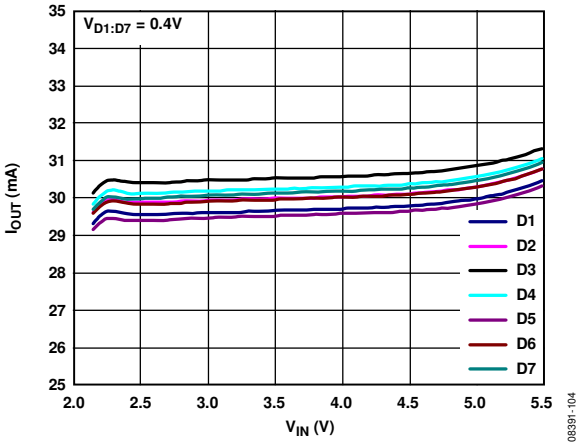


Figure 9. Typical Diode Current vs. $V_{IN}$

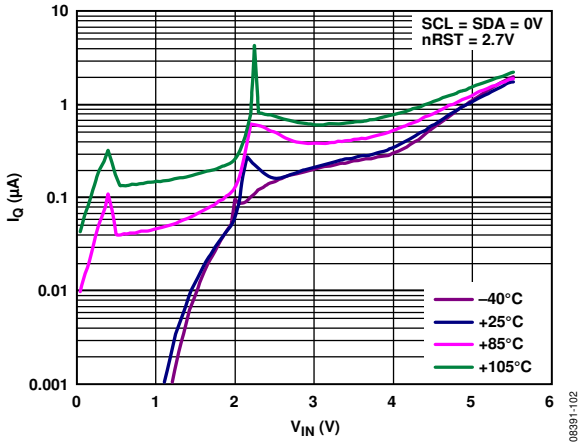


Figure 7. Typical Standby $I_Q$ vs. $V_{IN}$

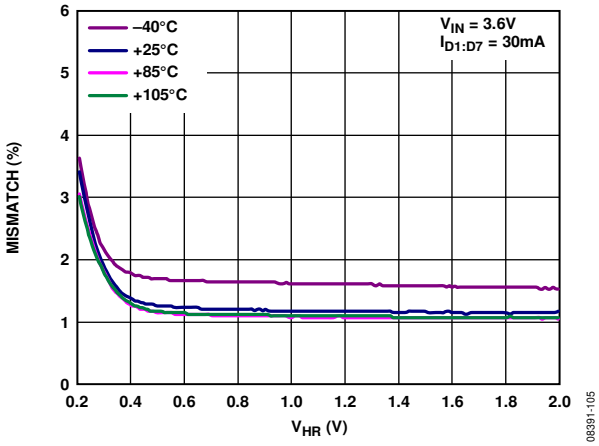


Figure 10. Typical Diode Matching vs. Current Sink Headroom Voltage ($V_{HR}$)

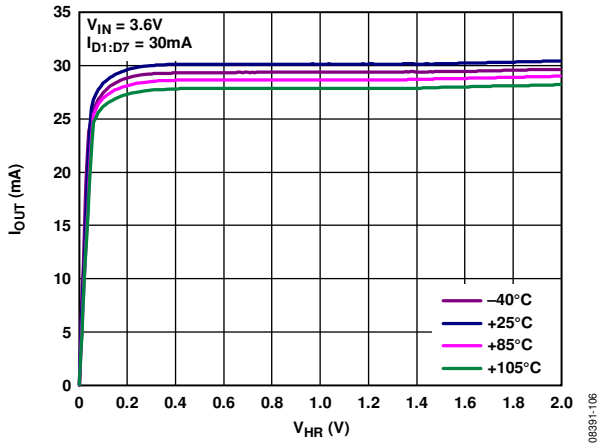


Figure 11. Typical Diode Current vs. Current Sink Headroom Voltage ($V_{HR}$)

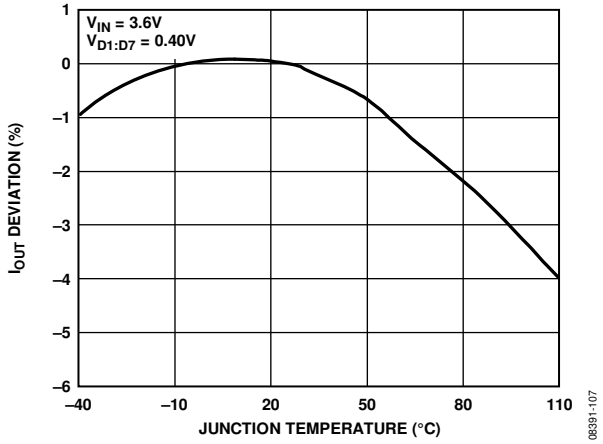


Figure 12. Typical Change In Diode Current vs. Temperature

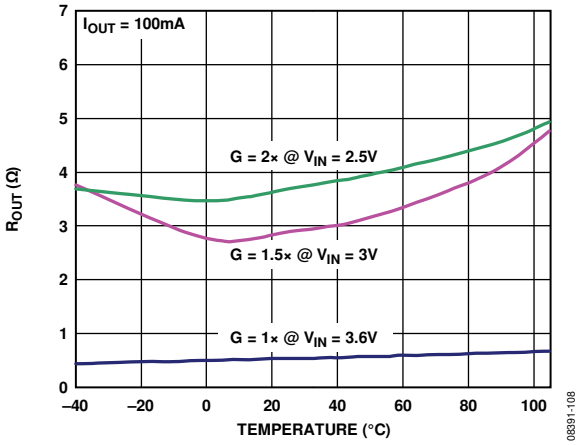


Figure 13. $R_{OUT}$ vs. Temperature

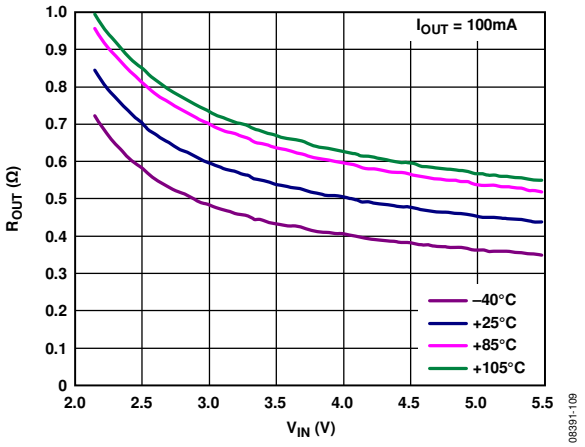


Figure 14. Typical $R_{OUT}$ ($G = 1\times$) vs. $V_{IN}$

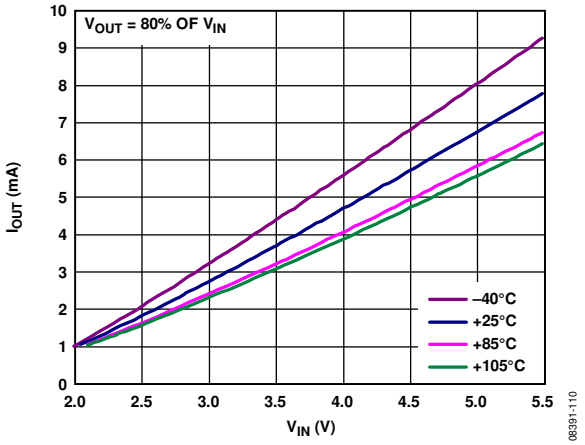


Figure 15. Typical Output Soft Start Current, $I_{SS}$

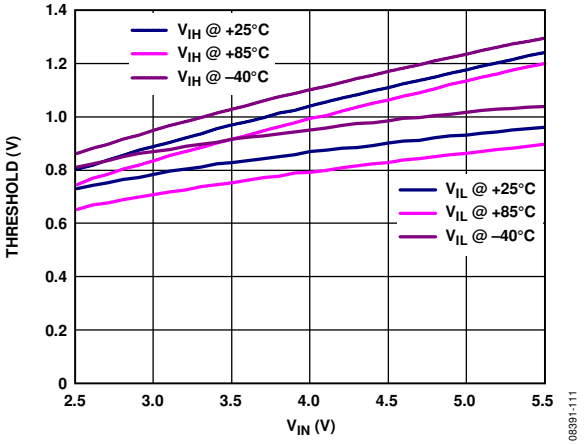


Figure 16. Typical I²C Thresholds, $V_{IH}$ and $V_{IL}$

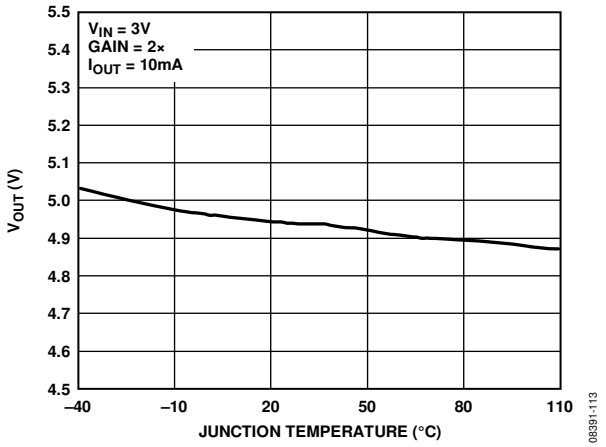


Figure 17. Typical Regulated Output Voltage ($V_{OUT(REG)}$)

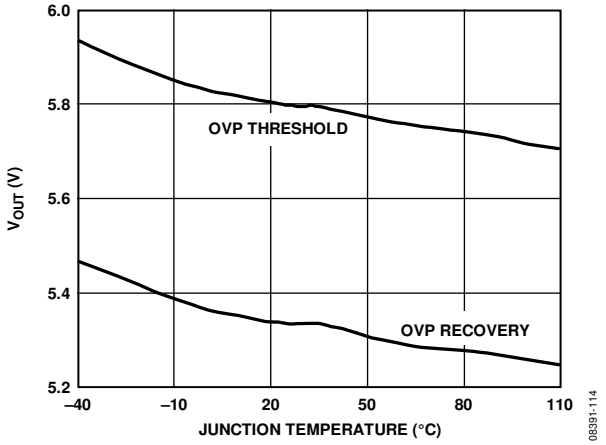


Figure 18. Typical Overvoltage Protection (OVP) Threshold

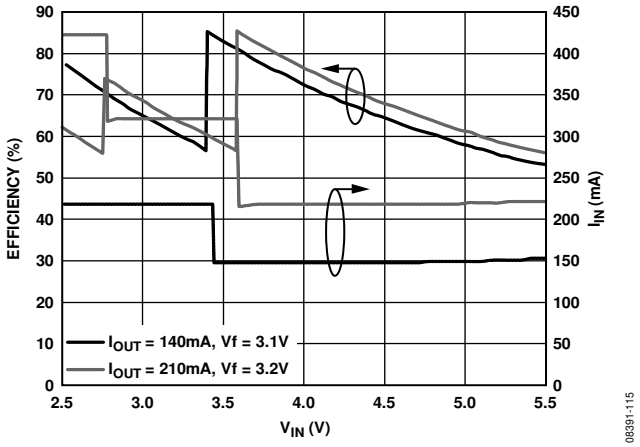


Figure 19. Typical Efficiency (Low Vf Diode)

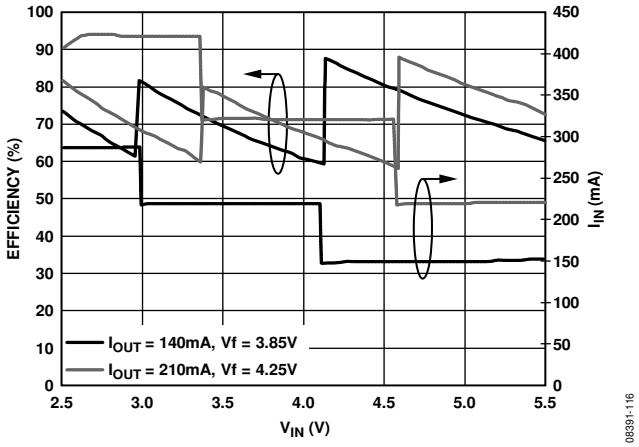


Figure 20. Typical Efficiency (High Vf Diode)

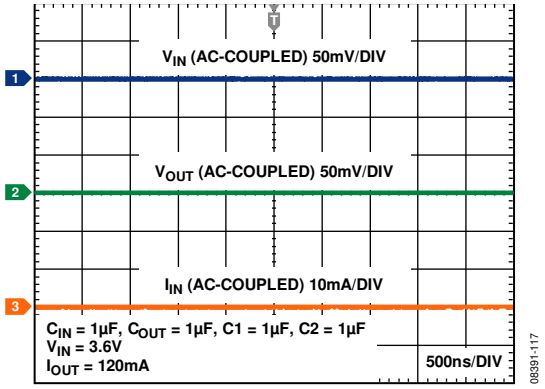


Figure 21. Typical Operating Waveforms, G = 1×

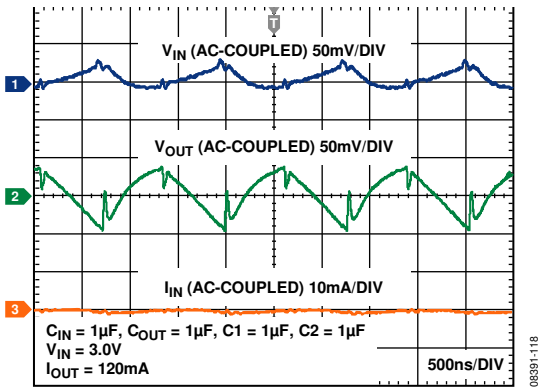


Figure 22. Typical Operating Waveforms, G = 1.5×

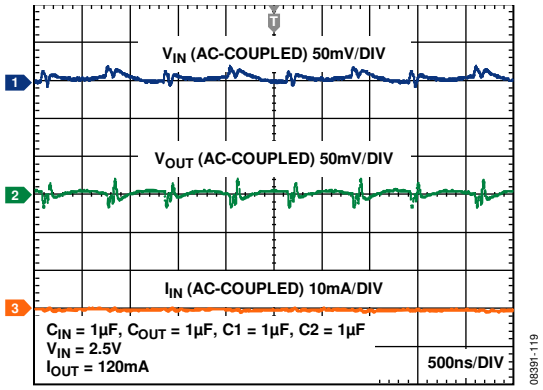


Figure 23. Typical Operating Waveforms, G = 2×

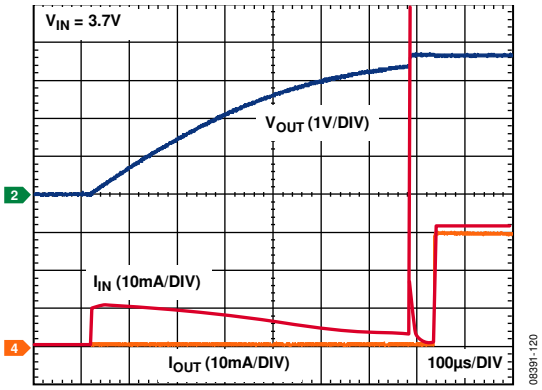


Figure 24. Typical Start-Up Waveform

# THEORY OF OPERATION

The ADP8861 provides a powerful charge pump driver with programmable LED control. Up to seven LEDs can be independently driven up to 30 mA (typical) each. The seventh LED can also be driven to 60 mA (typical). All LEDs can be individually programmed or combined into a group to operate backlight LEDs. A full suite of safety features, including short-circuit, overvoltage, and overtemperature protection with input-to-output isolation, allows for a robust and safe design. The integrated soft start limits inrush currents at startup, restart attempts, and gain transitions.

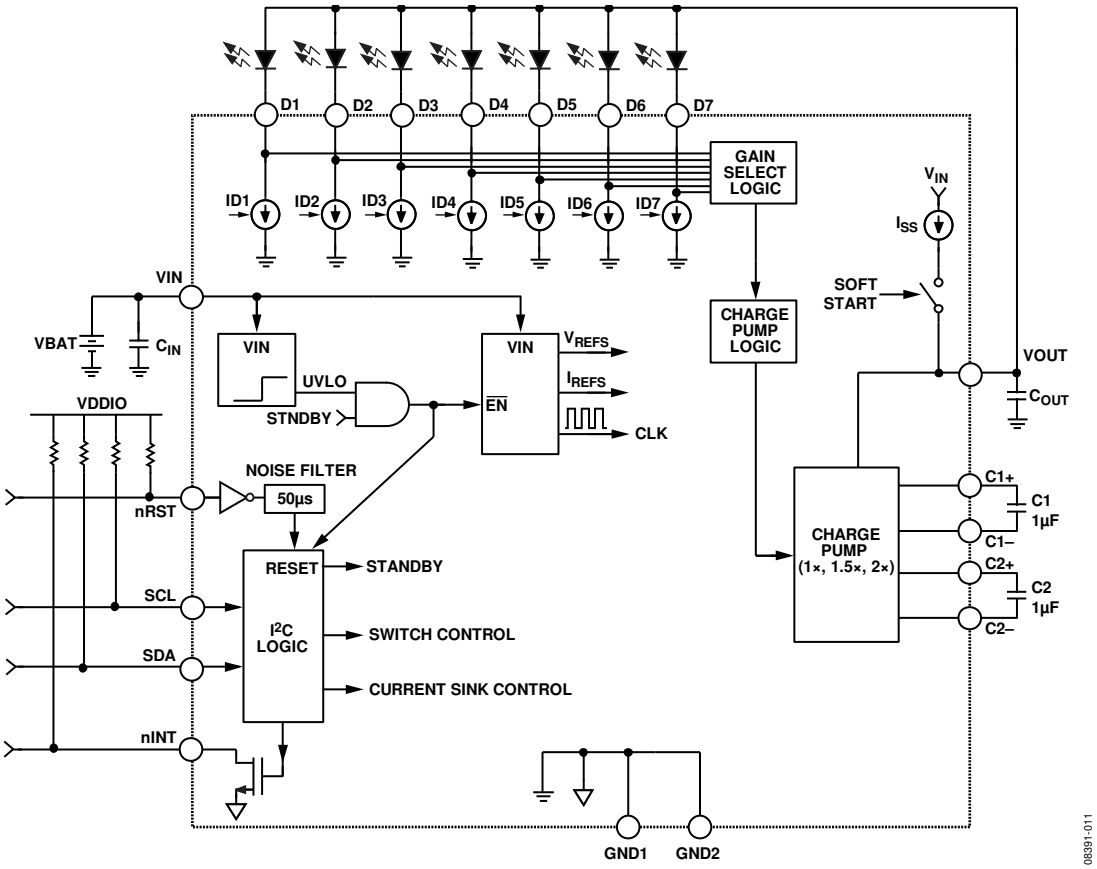


*Figure 25. Detailed Block Diagram*

## POWER STAGE

Because typical white LEDs require up to 4 V to drive them, some form of boosting is required over the typical variation in battery voltage. The ADP8861 accomplishes this with a high efficiency charge pump capable of producing a maximum $I_{OUT}$ of 240 mA over the entire input voltage range (2.5 V to 5.5 V). Charge pumps use the basic principle that a capacitor stores charge based on the voltage applied to it, as shown in the following equation:

$$Q = C \times V \quad (1)$$

By charging the capacitors in different configurations, the charge, and therefore the gain, can be optimized to deliver the voltage required to power the LEDs. Because a fixed charging and discharging combination must be used, only certain multiples of gain are available. The ADP8861 is capable of automatically optimizing the gain (G) from 1×, 1.5×, and 2×. These gains are accomplished with two capacitors (labeled C1 and C2 in Figure 25) and an internal switching network.

In G = 1× mode, the switches are configured to pass VIN directly to VOUT. In this mode, several switches are connected in parallel to minimize the resistive drop from input to output. In G = 1.5× and 2× modes, the switches alternatively charge from the battery and discharge into the output. For G = 1.5×, the capacitors are charged from $V_{IN}$ in series and are discharged to $V_{OUT}$ in parallel. For G = 2×, the capacitors are charged from $V_{IN}$ in parallel and are discharged to $V_{OUT}$ in parallel. In certain fault modes, the switches are opened and the output is physically isolated from the input.

### Automatic Gain Selection

Each LED that is driven requires a current source. The voltage on this current source must be greater than a minimum headroom voltage (180 mV typical) to maintain accurate current regulation. The gain is automatically selected based on the minimum voltage ($V_{DX}$) at all of the current sources. At startup, the device is placed into G = 1× mode and the output charges to $V_{IN}$. If any $V_{D1:D7}$ level is less than the required headroom (180 mV), the gain is increased to the next step (G = 1.5×). A 100 µs delay is allowed for the output to stabilize prior to the next gain switching decision. If there remains insufficient current sink headroom, then the gain is increased again to 2×. Conversely, to optimize efficiency, it is not desirable for the output voltage to be too high. Therefore, the gain reduces when the headroom voltage is great enough. This point (labeled $V_{DMAX}$ in Figure 26) is internally calculated to ensure that the lower gain still results in ample headroom for all the current sinks. The entire cycle is illustrated in Figure 26.

Note that the gain selection criteria apply only to active current sources. If current sources have been deactivated through an $I^2C$ command (for example only five LEDs are used), then the voltages on the deactivated current sources are ignored.

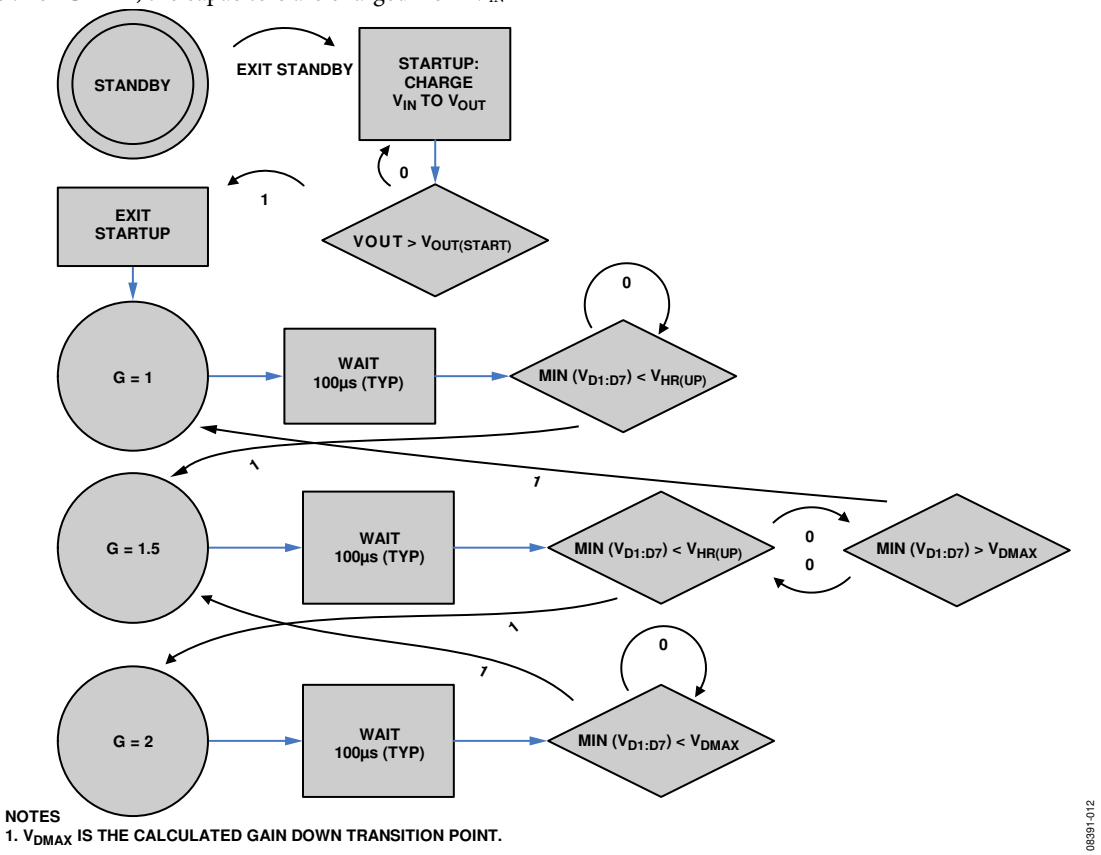


*Figure 26. State Diagram for Automatic Gain Selection*

### Soft Start Feature

At startup (either from UVLO activation or fault/standby recovery), the output is first charged by $I_{SS}$ (3.75 mA typical) until it reaches about 92% of $V_{IN}$. This soft start feature reduces the inrush current that is otherwise present when the output capacitance is initially charged to $V_{IN}$. When this point is reached, the controller enters G = 1× mode. If the output voltage is not sufficient, then the automatic gain selection determines the optimal point as defined in the Automatic Gain Selection section.

## OPERATING MODES

There are four different operating modes: active, standby, shutdown, and reset.

### Active Mode

In active mode, all circuits are powered up and in a fully operational state. This mode is entered when Bit nSTBY (in Register MDCR) is set to 1.

### Standby Mode

Standby mode disables all circuitry except for the I²C receivers. Current consumption is reduced to less than 1 µA. This mode is entered when the nSTBY bit is set to 0 or when the nRST pin is held low for more than 100 µs (maximum). When standby is exited, a soft start sequence is performed.

### Shutdown Mode

Shutdown mode disables all circuitry, including the I²C receivers. Shutdown occurs when $V_{IN}$ is below the undervoltage thresholds. When $V_{IN}$ rises above $V_{IN(START)}$ (2.05 V typical), all registers are reset and the part is placed into standby mode.

### Reset Mode

In reset mode, all registers are set to their default values and the part is placed into standby. There are two ways to reset the part: by power-on reset (POR) or using the nRST pin. POR is activated any time that the part exits shutdown mode. After a POR sequence is complete, the part automatically enters standby mode.

After startup, the part can be reset by pulling the nRST pin low. As long as the nRST pin is low, the part is held in a standby state but no I²C commands are acknowledged (all registers are kept at their default values). After releasing the nRST pin, all registers remain at their default values, and the part remains in standby; however, the part does accept I²C commands.

The nRST pin has a 50 µs (typical) noise filter to prevent inadvertent activation of the reset function. The nRST pin must be held low for this entire time to activate reset.

The operating modes function according to the timing diagram in Figure 27.

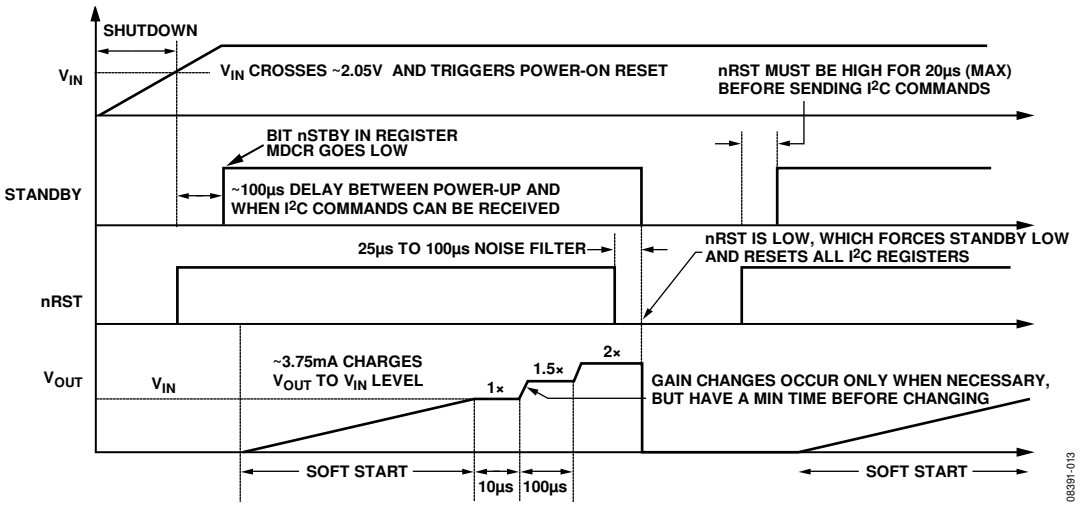


*Figure 27. Typical Timing Diagram*

## BACKLIGHT OPERATING LEVELS

The backlight can be operated at either the maximum level (Register 0x09) or the dim level (Register 0x0A). The backlight maximum and dim current settings are determined by a 7-bit code programmed by the user into these registers. The 7-bit resolution allows the user to set the backlight to one of 128 different levels between 0 mA and 30 mA.

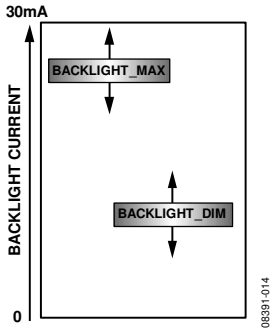


*Figure 28. Backlight Operating Levels*

The maximum and dim settings can be set between 0 mA and 30 mA; therefore, it is possible to program a dim setting that is greater than a maximum setting. For normal expected operation, ensure that the dim setting is programmed to be less than the maximum setting.

## BACKLIGHT MAXIMUM AND DIM SETTINGS

The ADP8861 can implement two distinct algorithms to achieve a linear and a nonlinear relationship between input code and backlight current. The law bits in Register 0x04 are used to change between these algorithms.

By default, the ADP8861 uses a linear algorithm (law = 00), where the backlight current increases linearly for a corresponding increase in input code. Backlight current (in milliamperes) is determined by the following equation:

$$Backlight\ Current\ (\text{mA}) = Code \times (Full\text{-}Scale\ Current/127) \quad (2)$$

where:
*Code* is the input code programmed by the user.
*Full-Scale Current* is the maximum sink current allowed per LED (typically 30 mA).

The ADP8861 can also implement a nonlinear (square approximation) relationship between input code and backlight current level. In this case (law = 01), the backlight current (in milliamperes) is determined by the following equation:

$$Backlight\ Current\ (\text{mA}) = \left( Code \times \frac{\sqrt{Full-Scale\ Current}}{127} \right)^2 \quad (3)$$

Figure 29 shows the backlight current level vs. input code for both the linear and square law algorithms.

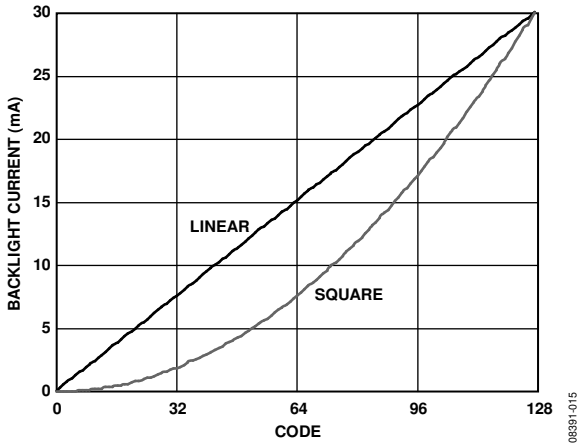


*Figure 29. Backlight Current vs. Input Code*

## AUTOMATED FADE IN AND FADE OUT

The LED drivers are easily configured for automated fade in and fade out. Sixteen fade in and fade out rates can be selected via the I²C interface. Fade in and fade out rates range from 0.1 sec to 5.5 sec (per full-scale current, either 30 mA or 60 mA).

**Table 5. Available Fade In and Fade Out Rates**

| Code | Fade Rate (in sec per Full-Scale Current) |
|---|---|
| 0000 | 0.1 (disabled) |
| 0001 | 0.3 |
| 0010 | 0.6 |
| 0011 | 0.9 |
| 0100 | 1.2 |
| 0101 | 1.5 |
| 0110 | 1.8 |
| 0111 | 2.1 |
| 1000 | 2.4 |
| 1001 | 2.7 |
| 1010 | 3.0 |
| 1011 | 3.5 |
| 1100 | 4.0 |
| 1101 | 4.5 |
| 1110 | 5.0 |
| 1111 | 5.5 |

The fade profile is based on the transfer law selected (linear, square, Cubic 10, or Cubic 11) and the delta between the actual current and the target current. Smaller changes in current reduce the fade time. For linear and square law fades, the fade time is given by

$$Fade\ Time = Fade\ Rate \times (Code/127) \quad (4)$$

where the *Fade Rate* is shown in Table 5.

The Cubic 10 and Cubic 11 laws also use the square law backlight currents derived from Equation 3; however, the time between each step is varied to produce a steeper slope at higher currents and a shallower slope at lower currents (see Figure 30).

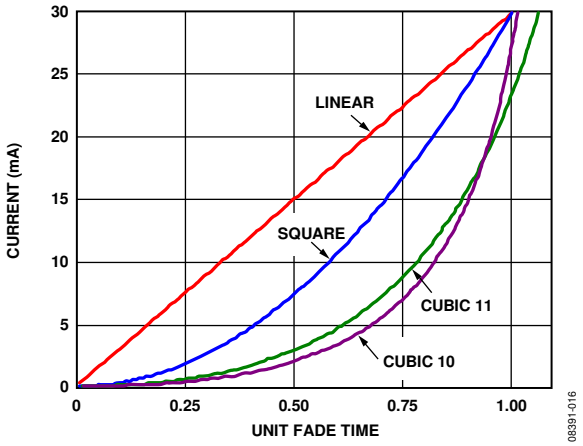


*Figure 30. Comparison of the Dimming Transfers Laws*

## BACKLIGHT TURN ON/TURN OFF/DIM

With the device in active mode (nSTBY = 1), the backlight can be turned on using the BL_EN bit in Register 0x01. Before turning on the backlight, the user should ensure that the maximum and dim settings are programmed. The backlight turns on when BL_EN = 1. The backlight turns off when BL_EN = 0.

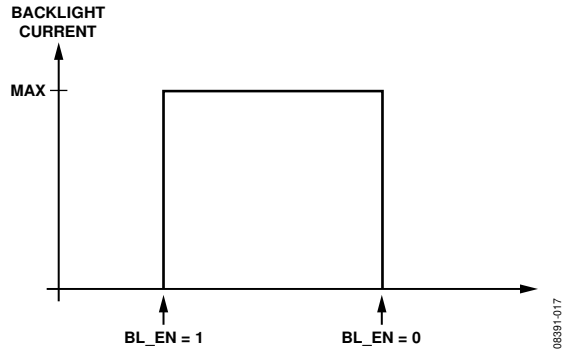


*Figure 31. Backlight Turn On/Turn Off*

While the backlight is on (BL_EN = 1), the user can change to the dim setting by programming DIM_EN = 1 in Register 0x01. If DIM_EN = 0, the backlight reverts to its maximum setting.

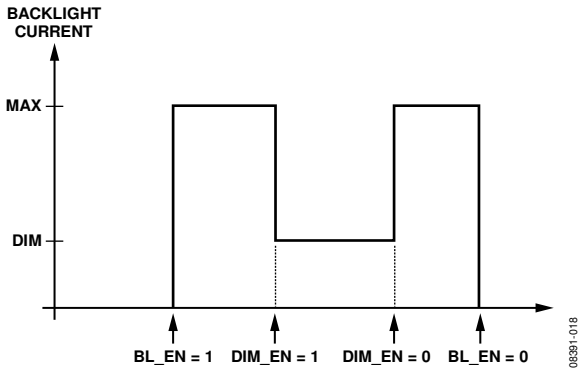


*Figure 32. Backlight Turn On/Dim/Turn Off*

## AUTOMATIC DIM AND TURN OFF TIMERS

The user can program the backlight to dim automatically by using the DIMT bits in Register 0x07. The dim timer has 127 settings ranging from 1 sec to 127 sec. Program the dim timer (DIMT) before turning on the backlight. If BL_EN = 1, the backlight turns on to its maximum setting and the dim timer starts counting. When the dim timer expires, the internal state machine sets DIM_EN = 1, and the backlight enters its dim setting.

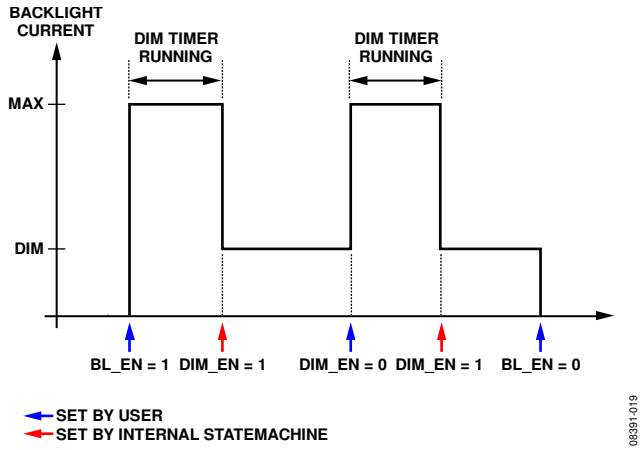


*Figure 33. Dim Timer*

If the user clears the DIM_EN bit, the backlight reverts to its maximum setting and the dim timer begins counting again. When the dim timer expires, the internal state machine again sets DIM_EN = 1, and the backlight enters its dim setting. The backlight can be turned off at any point during the dim timer countdown by clearing BL_EN.

The user can also program the backlight to turn off automatically by using the OFFT bits in Register 0x06. The off timer has 127 settings ranging from 1 sec to 127 sec. Program the off timer (OFFT) before turning on the backlight. If BL_EN = 1, the backlight turns on to its maximum setting and the off timer starts counting. When the off timer expires, the internal state machine clears the BL_EN bit, and the backlight turns off.

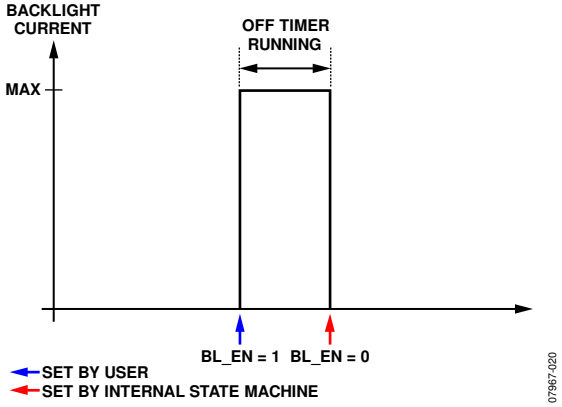


*Figure 34. Off Timer*

The backlight can be turned off at any point during the off timer countdown by clearing BL_EN.

The dim timer and off timer can be used together for sequential maximum-to-dim-to-off functionality. With both the dim and off timers programmed, and BL_EN asserted, the backlight turns on to its maximum setting, and when the dim timer expires, the backlight changes to its dim setting. When the off timer expires, the backlight turns off.

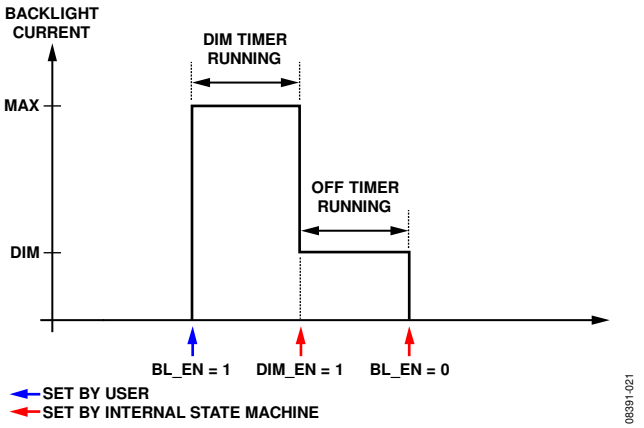


*Figure 35. Dim and Off Timers Used Together*

## FADE OVERRIDE

A fade override feature (FOVR in Register CFGR (0x04)) enables the host to override the preprogrammed fade in or fade out settings. If FOVR is set and the backlight is enabled in the middle of a fade out process, the backlight instantly (within approximately 100 ms) returns to its prefade brightness level. Alternatively, if the backlight is fading in, reasserting BL_EN overrides the programmed fade in time, and the backlight instantly goes to its final fade value. This is useful for situations where a key is pressed during a fade sequence. However, if FOVR is cleared and the backlight is enabled in the middle of a fade process, the backlight gradually brightens from where it was interrupted (it does not go down to 0 and then comes back on).

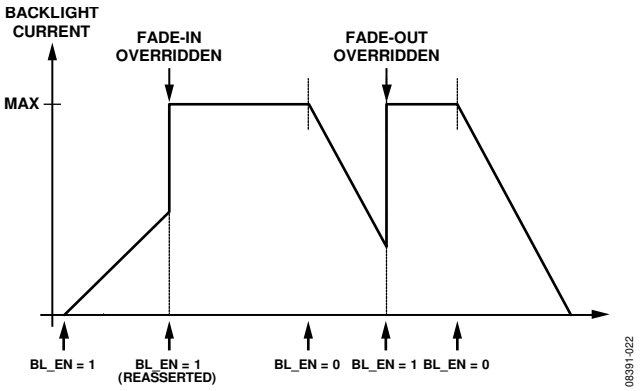


*Figure 36. Fade Override Function (FOVR Is High)*

## INDEPENDENT SINK CONTROL

Each of the seven LEDs can be configured (in Register 0x05) to operate as either part of the backlight or to operate as an independent sink current (ISC). Each ISC can be enabled independently and has its own current level. All ISCs share the same fade in rates, fade out rates, and fade law.

The ISCs have additional timers to facilitate blinking functions. A shared on timer (SCON) used in conjunction with the off timers of each ISC (SC1_OFF, SC2_OFF, SC3_OFF, and SC4_OFF in Register 0x12, and SC5_OFF, SC6_OFF, and SC7_OFF in Register 0x11) allows the LED current sinks to be configured in various blinking modes. The on timer can be set to one of four different settings: 0.2 sec, 0.6 sec, 0.8 sec, or 1.2 sec. The off timers have four different settings: disabled, 0.6 sec, 1.2 sec, and 1.8 sec. Blink mode is activated by setting the off timers to any setting other than disabled.

Program all fade, on, and off timers before enabling any of the LED current sinks. If ISCx is on during a blink cycle and SCx_EN is cleared, the LED turns off (or fades to off if fade out is enabled). If ISCx is off during a blink cycle and SCx_EN is cleared, it stays off.

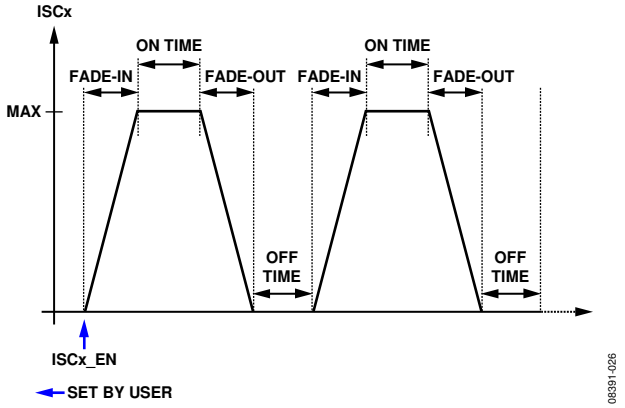


*Figure 37. Independent Sink Blink Mode with Fading*

## SHORT-CIRCUIT PROTECTION MODE

The ADP8861 can protect against short circuits on the output (VOUT). Short-circuit protection (SCP) is activated at the point when VOUT < 55% of $V_{IN}$. Note that SCP sensing is disabled during both startup and restart attempts (fault recovery). SCP sensing is reenabled 4 ms (typical) after activation. During a short-circuit fault, the device enters a low current consumption state and an interrupt flag is set. The device can be restarted at any time after receiving a short-circuit fault by simply rewriting nSTBY = 1. It then repeats another complete soft start sequence. Note that the value of the output capacitance ($C_{OUT}$) should be small enough to allow VOUT to reach approximately 55% (typical) of $V_{IN}$ within the 4 ms (typical) time. If $C_{OUT}$ is too large, the device inadvertently enters short-circuit protection.

## OVERVOLTAGE PROTECTION

Overvoltage protection (OVP) is implemented on the output. There are two types of overvoltage events: normal (no fault) and abnormal (from a fault or sudden load change).

### *Normal Overvoltage*

In a normal (no fault) overvoltage, the output voltage approaches $V_{OUT(REG)}$ (4.9 V typical) during normal operation. This is not caused by a fault or load change, but it is simply a consequence of the input voltage times the gain reaching the same level as the clamped output voltage ($V_{OUT(REG)}$). To prevent this type of overvoltage, the ADP8861 detects when the output voltage rises to $V_{OUT(REG)}$. It then increases the effective $R_{OUT}$ of the gain stage to reduce the voltage that is delivered. This effectively regulates $V_{OUT}$ to $V_{OUT(REG)}$; however, there is a limit to the effect that this system can have on regulating $V_{OUT}$. It is designed only for normal operation and it is not intended to protect against faults or sudden load changes. When the output voltage is regulated to $V_{OUT(REG)}$, no interrupt is set and the operation is transparent to the LEDs and the overall application.

### *Abnormal Overvoltage*

Because of the open-loop behavior of the charge pump as well as how the gain transitions are computed, a sudden load change or fault can abnormally force $V_{OUT}$ beyond 6 V. This causes an abnormal overvoltage situation. If the event happens slowly enough, the system first tries to regulate the output to 4.9 V as in a normal overvoltage scenario. However, if this is not sufficient, or if the event happens too quickly, then the ADP8861 enters OVP mode when $V_{OUT}$ exceeds the OVP threshold (typically 5.8 V). In OVP mode, only the charge pump is disabled to prevent $V_{OUT}$ from rising too high. The current sources and all other device functionality remain intact. When the output voltage falls by about 500 mV (to 5.3 V typical), the charge pump resumes operation. If the fault or load event recurs, the process may repeat. An interrupt flag is set at each OVP instance.

## THERMAL SHUTDOWN/OVERTEMPERATURE PROTECTION

If the die temperature of the ADP8861 rises above a safe limit (150°C typical), the controllers enter thermal shutdown (TSD) protection mode. In this mode, most of the internal functions shut down, the part enters standby, and the TSD_INT interrupt (Register 0x02) is set. When the die temperature decreases below ~130°C, the part can be restarted. To restart the part, simply remove it from standby. No interrupt is generated when the die temperature falls below 130°C. However, if the software clears the pending TSD_INT interrupt and the temperature remains above 130°C, another interrupt is generated.

The complete state machine for these faults (SCP, OVP, and TSD) is shown in Figure 38.

## INTERRUPTS

There are three interrupt sources available on the ADP8861 in Register 0x02.

- Overvoltage protection: The OVP_INT interrupt is generated when the output voltage exceeds 5.8 V (typical).
- Thermal shutdown circuit: An interrupt (TSD_INT) is generated when entering overtemperature protection.
- Short-circuit detection: SHORT_INT is generated when the device enters short-circuit protection mode.

The interrupt (if any) that appears on the nINT pin is determined by the bits mapped in Register INTR_EN (0x03). To clear an interrupt, write a 1 to the interrupt in the MDCR2 register (0x02) or reset the part. Reading the interrupt, or writing a 0, has no effect.

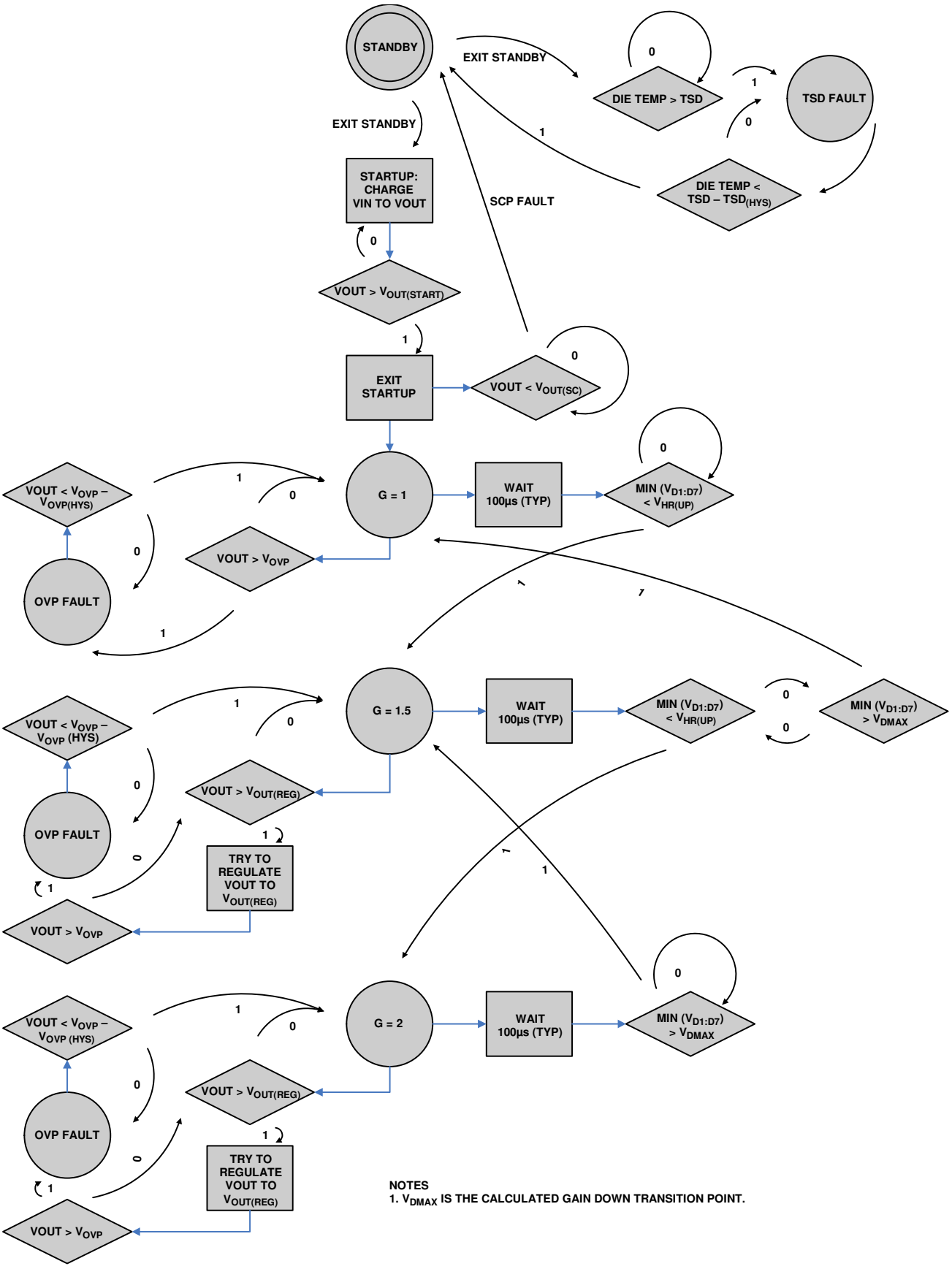


*Figure 38. Fault State Machine*

# APPLICATIONS INFORMATION

The ADP8861 allows the charge pump to operate efficiently with a minimum of external components. Specifically, the user must select an input capacitor ($C_{IN}$), output capacitor ($C_{OUT}$), and two charge pump fly capacitors (C1 and C2). $C_{IN}$ should be 1 µF or greater. The value must be high enough to produce a stable input voltage signal at the minimum input voltage and maximum output load. A 1 µF capacitor for $C_{OUT}$ is recommended. Larger values are permissible, but care must be exercised to ensure that VOUT charges above 55% (typical) of $V_{IN}$ within 4 ms (typical). See the Short-Circuit Protection Mode section for more details.

For best practice, it is recommended that the two charge pump fly capacitors be 1 µF; larger values are not recommended, and smaller values may reduce the ability of the charge pump to deliver maximum current. For optimal efficiency, the charge pump fly capacitors should have low equivalent series resistance (ESR). Low ESR X5R or X7R capacitors are recommended for all four components. The use of fly capacitors sized 0402 and smaller is allowed, but the GDWN_DIS bit in Register 0x01 must be set. Minimum voltage ratings should adhere to the guidelines in Table 6.

**Table 6. Capacitor Stress in Each Charge Pump Gain State**

| Capacitor | Gain = 1× | Gain = 1.5× | Gain = 2× |
|---|---|---|---|
| $C_{IN}$ | $V_{IN}$ | $V_{IN}$ | $V_{IN}$ |
| $C_{OUT}$ | $V_{IN}$ | $V_{IN} \times 1.5$ (max of 5.5 V) | $V_{IN} \times 2.0$ (max of 5.5 V) |
| C1 | None | $V_{IN}/2$ | $V_{IN}$ |
| C2 | None | $V_{IN}/2$ | $V_{IN}$ |

Any color LED can be used if the Vf (forward voltage) is less than 4.1 V. However, using lower Vf LEDs reduces the input power consumption by allowing the charge pump to operate at lower gain states.

The equivalent circuit model for a charge pump is shown in Figure 39.

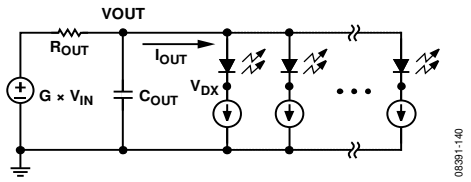


*Figure 39. Charge Pump Equivalent Circuit Model*

The input voltage is multiplied by the gain (G) and delivered to the output through an effective resistance ($R_{OUT}$). The output current flows through $R_{OUT}$ and produces an IR drop to yield:

$$V_{OUT} = G \times V_{IN} - I_{OUT} \times R_{OUT}(G) \quad (5)$$

The $R_{OUT}$ term is a combination of the $R_{DSON}$ resistance for the switches used in the charge pump and a small resistance, which accounts for the effective dynamic charge pump resistance. The $R_{OUT}$ level changes based upon the gain (the configuration of the switches). Typical $R_{OUT}$ values are given in Table 1, Figure 13, and Figure 14.

$V_{OUT}$ is also equal to the largest Vf of the LEDs used plus the voltage drop across the regulating current source. This gives

$$V_{OUT} = Vf_{(MAX)} + V_{DX} \quad (6)$$

Combining Equation 5 and Equation 6 gives

$$V_{IN} = (Vf_{(MAX)} + V_{DX} + I_{OUT} \times R_{OUT}(G))/G \quad (7)$$

Equation 7 is useful for calculating approximate bounds for the charge pump design.

## DETERMINING THE TRANSITION POINT OF THE CHARGE PUMP

Consider the following design example where:

$Vf_{(MAX)}$ = 3.7 V
$I_{OUT}$ = 140 mA (7 LEDs at 20 mA each)
$R_{OUT}$ (G = 1.5×) = 3 Ω (obtained from Figure 13)

At the point of a gain transition, $V_{DX} = V_{HR(UP)}$. Table 1 gives the typical value of $V_{HR(UP)}$ as 0.2 V. Therefore, the input voltage level when the gain transitions from 1.5× to 2× is

$$V_{IN} = (3.7\text{ V} + 0.2\text{ V} + 140\text{ mA} \times 3\ \Omega)/1.5 = 2.88\text{ V}$$

## LAYOUT GUIDELINES

Note the following layout guidelines:

- For optimal noise immunity, place the $C_{IN}$ and $C_{OUT}$ capacitors as close to their respective pins as possible. These capacitors should share a short ground trace. If the LEDs are a significant distance from the VOUT pin, another capacitor on VOUT, placed closer to the LEDs, is advisable.
- For optimal efficiency, place the charge pump fly capacitors (C1 and C2) as close to the part as possible.
- The ADP8861 does not distinguish between power ground and analog ground. Therefore, both ground pins can be connected directly together. It is recommended that these ground pins be connected at the ground for the input and output capacitors.
- The LFCSP package requires the exposed pad to be soldered at the board to the GND1 and/or GND2 pin(s).
- Unused diode pins (Pin D1 to Pin D7) can be connected to ground or to VOUT, or remain floating. However, the unused diode current sinks must be disabled by setting them as independent sinks in Register 0x05 and then disabling them in Register 0x10. If they are not disabled, the charge pump efficiency may suffer.
- If the interrupt pin (nINT) is not used, connect it to ground or leave it floating. Never connect it to a voltage supply, except through a ≥1 kΩ series resistor.
- The ADP8861 has an integrated noise filter on the nRST pin. Under normal conditions, it is not necessary to filter the reset line. However, if the part is exposed to an unusually noisy signal, it is beneficial to add a small RC filter or bypass capacitor on this pin. If the nRST pin is not used, it must be pulled well above the $V_{IH(MIN)}$ level (see Table 1). Do not allow the nRST pin to float.

## EXAMPLE CIRCUITS

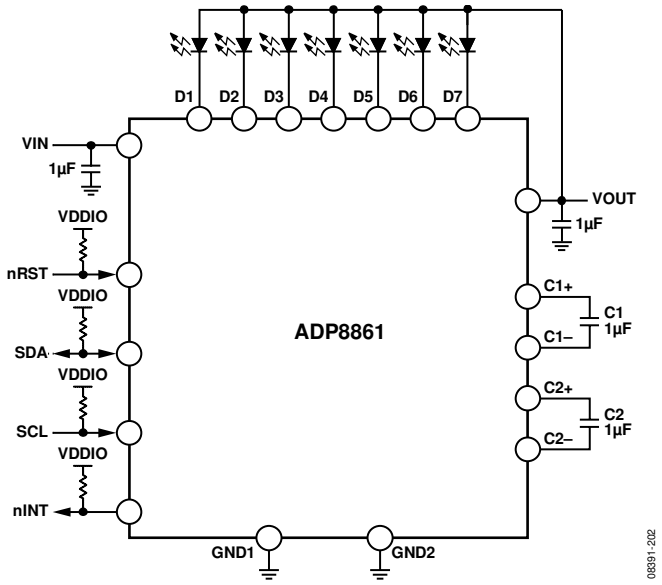


*Figure 40. Generic Application Schematic*

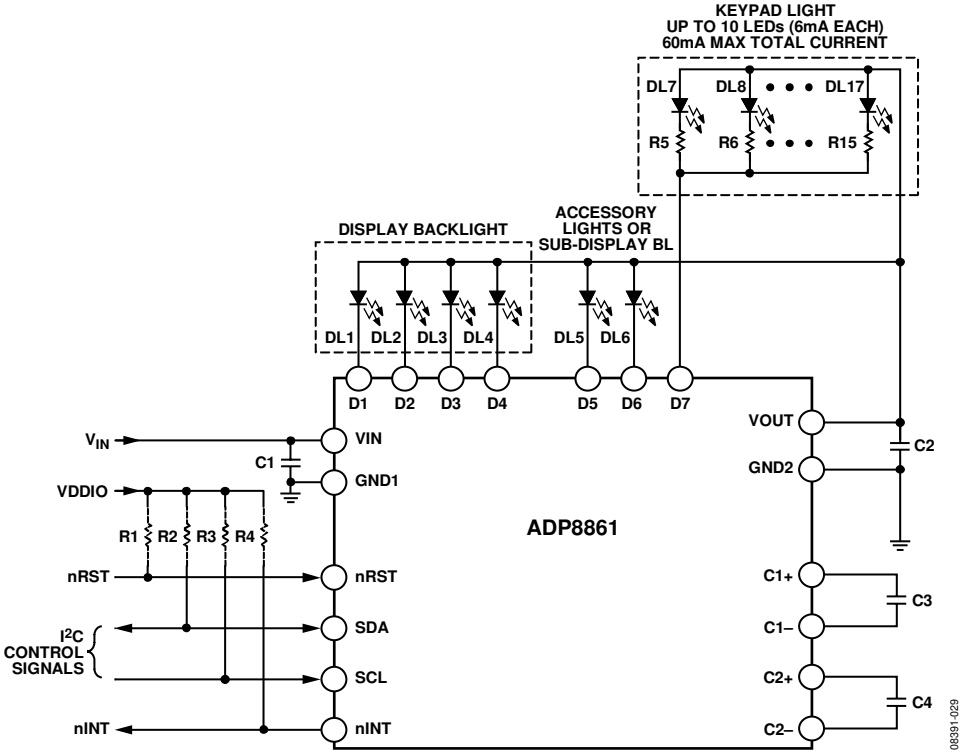


*Figure 41. Application Schematic with Keypad Light Control*

# I²C PROGRAMMING AND DIGITAL CONTROL

The ADP8861 provides full software programmability to facilitate its adoption in various product architectures. The default I²C address is 0101010x (x = 0 during write, x = 1 during read). Therefore, the default write address is 0x54 and the read address is 0x55.

Note the following general behavior of registers:

- All registers are set to their default values during reset or after a UVLO event.
- All registers are read/write unless otherwise specified.
- Unused bits are read as zero.

Table 7 through Table 55 provide register and bit descriptions. The reset value for all bits in the bit map tables is all 0s, except in Table 9 (see Table 9 for its unique reset value). Wherever the acronym N/A appears in the tables, it means not applicable.

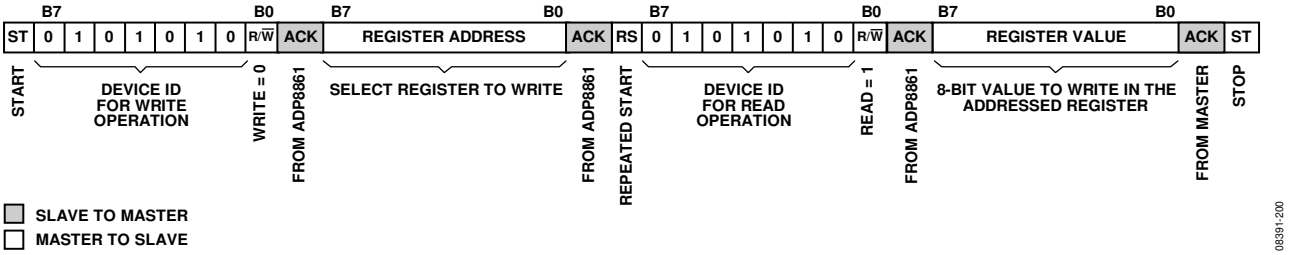


*Figure 42. I²C Read Command Sequence*

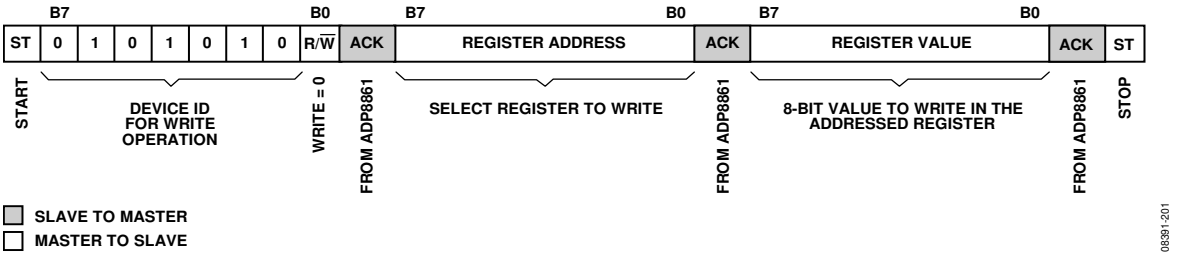


*Figure 43. I²C Write Command Sequence*

**Table 7. Register Set Definitions**

| Address (Hex) | Register Name | Description |
|---|---|---|
| 0x00 | MFDVID | Manufacturer and device ID |
| 0x01 | MDCR | Device mode and status |
| 0x02 | MDCR2 | Device mode and Status Register 2 |
| 0x03 | INTR_EN | Interrupts enable |
| 0x04 | CFGR | Configuration register |
| 0x05 | BLSEN | Sink enable, backlight or independent |
| 0x06 | BLOFF | Backlight off timeout |
| 0x07 | BLDIM | Backlight dim timeout |
| 0x08 | BLFR | Backlight fade in and fade out rates |
| 0x09 | BLMX | Backlight maximum current |
| 0x0A | BLDM | Backlight dim current |
| 0x0B to 0x0E | Reserved | |
| 0x0F | ISCFR | Independent sink current fade control register |
| 0x10 | ISCC | Independent sink current control register |
| 0x11 | ISCT1 | Independent Sink Current Timer Register, LED[7:5] |
| 0x12 | ISCT2 | Independent Sink Current Timer Register, LED[4:1] |
| 0x13 | ISCF | Independent sink current fade register |
| 0x14 | ISC7 | Independent Sink Current, LED7 |
| 0x15 | ISC6 | Independent Sink Current, LED6 |
| 0x16 | ISC5 | Independent Sink Current, LED5 |
| 0x17 | ISC4 | Independent Sink Current, LED4 |
| 0x18 | ISC3 | Independent Sink Current, LED3 |
| 0x19 | ISC2 | Independent Sink Current, LED2 |
| 0x1A | ISC1 | Independent Sink Current, LED1 |

**Table 8. Register Map**

| Address (Hex) | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x00 | MFDVID | Manufacturer ID | | | | Device ID | | | |
| 0x01 | MDCR | Reserved | INT_CFG | nSTBY | DIM_EN | GDWN_DIS | SIS_EN | Reserved | BL_EN |
| 0x02 | MDCR2 | Reserved | | | SHORT_INT | TSD_INT | OVP_INT | Reserved | |
| 0x03 | INTR_EN | Reserved | | | SHORT_IEN | TSD_IEN | OVP_IEN | Reserved | |
| 0x04 | CFGR | Reserved | | | | | Law | | FOVR |
| 0x05 | BLSEN | Reserved | D7EN | D6EN | D5EN | D4EN | D3EN | D2EN | D1EN |
| 0x06 | BLOFF | Reserved | OFFT | | | | | | |
| 0x07 | BLDIM | Reserved | DIMT | | | | | | |
| 0x08 | BLFR | BL_FO | | | | BL_FI | | | |
| 0x09 | BLMX | Reserved | BL_MC | | | | | | |
| 0x0A | BLDM | Reserved | BL_DC | | | | | | |
| 0x0B to 0x0E | N/A | Reserved | | | | | | | |
| 0x0F | ISCFR | Reserved | | | | | | SC_LAW | |
| 0x10 | ISCC | Reserved | SC7_EN | SC6_EN | SC5_EN | SC4_EN | SC3_EN | SC2_EN | SC1_EN |
| 0x11 | ISCT1 | SCON | | SC7_OFF | | SC6_OFF | | SC5_OFF | |
| 0x12 | ISCT2 | SC4_OFF | | SC3_OFF | | SC2_OFF | | SC1_OFF | |
| 0x13 | ISCF | SCFO | | | | SCFI | | | |
| 0x14 | ISC7 | SCR | SCD7 | | | | | | |
| 0x15 | ISC6 | Reserved | SCD6 | | | | | | |
| 0x16 | ISC5 | Reserved | SCD5 | | | | | | |
| 0x17 | ISC4 | Reserved | SCD4 | | | | | | |
| 0x18 | ISC3 | Reserved | SCD3 | | | | | | |
| 0x19 | ISC2 | Reserved | SCD2 | | | | | | |
| 0x1A | ISC1 | Reserved | SCD1 | | | | | | |

### *Manufacturer and Device ID (MFDVID)—Register 0x00*

Multiple device revisions are tracked by the device ID field. This is a read-only register.

**Table 9. MFDVID Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Manufacturer ID | | | | Device ID | | | |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

### *Mode Control Register (MDCR)—Register 0x01*

**Table 10. MDCR Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | INT_CFG | nSTBY | DIM_EN | GDWN_DIS | SIS_EN | Reserved | BL_EN |

**Table 11. Bit Descriptions for the MDCR Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| N/A | 7 | Reserved. |
| INT_CFG | 6 | Interrupt configuration.<br>1 = processor interrupt deasserts for 50 µs and reasserts with pending events.<br>0 = processor interrupt remains asserted if the host tries to clear the interrupt while there is a pending event. |
| nSTBY | 5 | 1 = device is in active mode.<br>0 = device is in standby mode; only the $I^2C$ interface is enabled. |
| DIM_EN | 4 | DIM_EN is set by the hardware after a dim timeout. The user can also force the backlight into dim mode by asserting this bit. Dim mode can only be entered if BL_EN is also enabled.<br>1 = backlight is operating at the dim current level (BL_EN must also be asserted).<br>0 = backlight is not in dim mode. |
| GDWN_DIS | 3 | 1 = the charge pump does not switch down in gain until all LEDs are off. The charge pump switches up in gain as needed. This feature is useful if the ADP8861 charge pump is used to drive an external load. This feature must be used when utilizing small fly capacitors (0402 or smaller).<br>0 = the charge pump automatically switches up and down in gain. This provides optimal efficiency, but is not suitable for driving loads that are not connected through the ADP8861 diode drivers. Additionally, the charge pump fly capacitors should be low ESR and sized 0603 or greater. |
| SIS_EN | 2 | Synchronous independent sinks enable.<br>1 = enables all LED current sinks designated as independent sinks. This bit has no effect if any of the SCx_EN bits in Register 0x10 are set.<br>0 = disables all LED current sinks designated as independent sinks. This bit has no effect if any of the SCx_EN bits in Register 0x10 are set. |
| N/A | 1 | Reserved. |
| BL_EN | 0 | 1 = backlight is enabled (nSTBY must also be asserted).<br>0 = backlight is disabled. |