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Charge-Pump, Parallel Backlight Driver with Image Content PWM Input

Data Sheet

ADP8870

FEATURES

- Charge pump with automatic gain selection of 1×, 1.5×, and 2× for maximum efficiency
- Two high accuracy (±5%) phototransistor inputs for automated ambient light sensing (ALS)
- 5 programmable ambient light-sensing zones for optimal backlight power savings
- Independent ALS control of D7, for automated response of keypad lighting to ambient light levels
- PWM input can be used for content adaptive brightness control (CABC) of any, or all, of the LEDs
- PWM input scales the LED output current
- 7 independent, programmable LED drivers
  - 6 drivers capable of 30 mA (maximum)
  - 1 driver capable of 60 mA (maximum)
- Programmable maximum current limit (128 levels)
- Standby mode for <1 µA current consumption
- 16 programmable fade-in and fade-out times (0.1 sec to 5.5 sec) with choice of square or cubic rates
- Fading override
- I²C-compatible interface for all programming
- Dedicated reset pin and built-in power-on reset (POR)
- Short-circuit, overvoltage, and overtemperature protection
- Internal soft start to limit inrush currents
- Input-to-output isolation during faults or shutdown
- Operates down to V_{IN} = 2.5 V, with undervoltage lockout (UVLO) at 2.0 V.
- Available in a small, 2.15 mm × 2.36 mm × 0.6 mm wafer level chip scale package (WLCSP) or a 4 mm × 4 mm × 0.75 mm lead frame chip scale package (LFCSP)

APPLICATIONS

- Mobile display backlighting
- Mobile phone keypad backlighting
- RGB LED lighting
- LED indication
- General backlighting of small format displays

TYPICAL OPERATING CIRCUIT

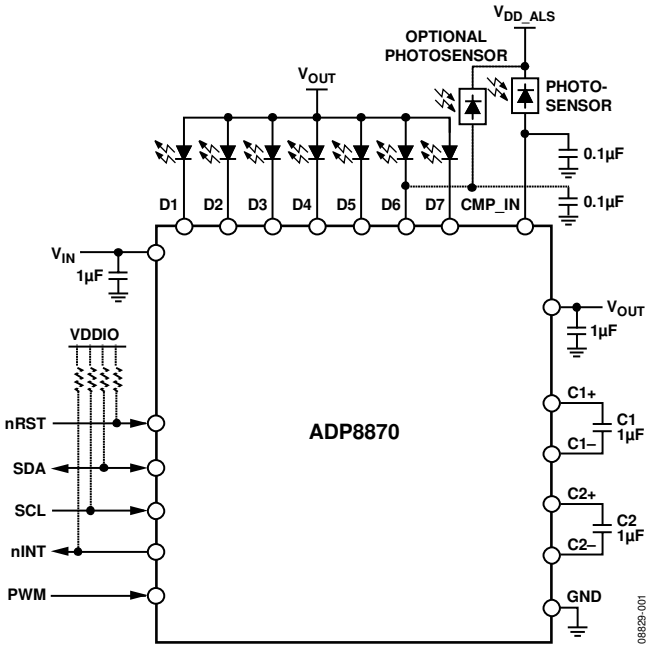

Figure 1.

GENERAL DESCRIPTION

The ADP8870 combines a programmable backlight LED charge-pump driver with automatic phototransistor control of the brightness (LED current) and a PWM input to control the scale of the output current. This combination allows significant power savings because it automatically changes the current intensity based on the sensed ambient lighting levels and the display image content. It performs this function automatically, eliminating the need for a processor to monitor the phototransistor. The light intensity thresholds are fully programmable via the I²C interface.

The ADP8870 allows up to six LEDs to be independently driven up to 30 mA (maximum). An additional seventh LED can be driven to 60 mA (maximum). All LEDs are individually programmable for minimum/maximum current and fade-in/fade-out times through an I²C interface. These LEDs can also be combined into groups to reduce the processor instructions during fade-in and fade-out.

Driving these components is a two-capacitor charge pump with gains of 1×, 1.5×, and 2×. This setup is capable of driving a maximum I_{OUT} of 240 mA from a supply of 2.5 V to 5.5 V. A full suite of safety features, including short-circuit, overvoltage, and overtemperature protection, allows easy implementation of a safe and robust design. Additionally, input inrush currents are limited via an integrated soft start combined with controlled input-to-output isolation.

Rev. B
Document Feedback

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- ADP8870 Evaluation Board

DOCUMENTATION

Data Sheet

- ADP8870: Charge-Pump, Parallel Backlight Driver with Image Content PWM Input Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADP8870 Back-light LED Linux Driver

DESIGN RESOURCES

- ADP8870 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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View all ADP8870 EngineerZone Discussions.

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REVISION HISTORY

1/14—Rev. A to Rev. B

Change to Figure 35 ... 17

8/12—Revision A: Initial Version

SPECIFICATIONS

VIN = 3.6 V, SCL = 2.7 V, SDA = 2.7 V, nINT = open, nRST = 2.7 V, CMP_IN = 0 V, $V_{D1:D7}$ = 0.4 V, C1 = 1 µF, C2 = 1 µF, C_{OUT} = 1 µF, typical values are at T_J = 25°C and are not guaranteed, minimum and maximum limits are guaranteed from T_J = −40°C to +105°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
Input Voltage						
Operating Range	V_{IN}		2.5		5.5	V
Start-Up Level	$V_{IN(START)}$	V_{IN} increasing		2.02	2.3	V
Low Level	$V_{IN(STOP)}$	V_{IN} decreasing	1.6	1.94		V
$V_{IN(START)}$ Hysteresis	$V_{IN(HYS)}$	After startup		80		mV
Quiescent Current	I_Q					
During Standby	$I_{Q(STBY)}$	V_{IN} = 3.6 V, Bit nSTBY = 0, SCL = SDA = 0 V		0.3	1.5	µA
I_Q Active at Gain = 1×	$I_{Q(1×)}$	V_{IN} = 3.6 V, Bit nSTBY = 1, I_{OUT} = 0 mA		1.4	2.0	mA
I_Q Active at Gain = 1.5×	$I_{Q(1.5×)}$	V_{IN} = 3.6 V, Bit nSTBY = 1, I_{OUT} = 0 mA		3.9	5.1	mA
I_Q Active at Gain = 2×	$I_{Q(2×)}$	V_{IN} = 3.6 V, Bit nSTBY = 1, I_{OUT} = 0 mA		4.6	6.2	mA
OSCILLATOR		Charge-pump gain = 2×				
Switching Frequency	f_{SW}		0.90	1.00	1.10	MHz
Duty Cycle	D			50		%
OUPUT CURRENT CONTROL						
Maximum Drive Current	$I_{D1:D7(MAX)}$	$V_{D1:D7}$ = 0.4 V				
D1 to D7		Bit SCR = 0 in the ISC7 register				
T_J = 25°C			28.0	30.0	32.0	mA
T_J = −40°C to +105°C			27.0		33.0	mA
D7 (60 mA Setting)	$I_{D7(60\ mA)}$	V_{D7} = 0.4 V, Bit SCR = 1 in the ISC7 register				
T_J = 25°C			55.0	60.0	65.0	mA
T_J = −40°C to +105°C			52.5		67.0	mA
LED Current Source Matching[1]	I_{MATCH}	$V_{D1:D7}$ = 0.4 V		1	2.5	%
Leakage Current on LED Pins	$I_{D1:D7(LKG)}$	V_{IN} = 5.5 V, $V_{D1:D7}$ = 2.5 V, Bit nSTBY=1			0.5	µA
Equivalent Output Resistance	R_{OUT}					
Gain = 1×		V_{IN} = 3.6 V, I_{OUT} = 100 mA		0.5	1.0	Ω
Gain = 1.5×		V_{IN} = 3.1 V, I_{OUT} = 100 mA		3.0		Ω
Gain = 2×		V_{IN} = 2.5 V, I_{OUT} = 100 mA		3.8		Ω
Regulated Output Voltage	$V_{OUT(REG)}$	V_{IN} = 3 V, gain = 2×, I_{OUT} = 10 mA	4.3	4.7	5.1	V
AUTOMATIC GAIN SELECTION						
Headroom Voltage Threshold for Gain Increase	$V_{HR(UP)}$	Decrease V_{Dx} until the gain switches up	115	180	245	mV
Minimum Current Sink Headroom Voltage	$V_{HR(MIN)}$	I_{Dx} = $I_{Dx(MAX)}$ × 95%		50		mV
Gain Delay	t_{GAIN}	The delay after gain has changed and before gain is allowed to change again		100		µs
AMBIENT LIGHT-SENSING COMPARATORS						
Ambient Light Sensor Current	I_{ALS}					
T_J = 25°C			1.05	1.10	1.15	mA
T_J = −40°C to +105°C			1.00		1.20	mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DAC Bit Step						
Threshold for Level 2	I_{L2BIT}	$I_{L2BIT} = I_{ALS}/250$		4.4		µA
Threshold for Level 3	I_{L3BIT}	$I_{L3BIT} = I_{ALS}/500$		2.2		µA
Threshold for Level 4	I_{L4BIT}	$I_{L4BIT} = I_{ALS}/1000$		1.1		µA
Threshold for Level 5	I_{L5BIT}	$I_{L5BIT} = I_{ALS}/2000$		0.55		µA
Ambient Light Sensor Threshold Voltage	V_{ALS}			0.95	1.12	V
PWM SPECIFICATIONS						
V_{DDIO} Voltage Operating Range	V_{DDIO}				5.5	V
Logic Low Input[2]	V_{PWMIL}	V_{IN} = 2.5 V			0.5	V
Logic High Input[3]	V_{PWMIH}	V_{IN} = 5.5 V	1.45			V
Minimum PWM Clock Frequency	$f_{PWM(MIN)}$				140	Hz
Maximum PWM Clock Frequency	$f_{PWM(MAX)}$		60			kHz
PWM Pulse Width	$t_{PWM(MIN)}$	PWM on time for valid detection of PWM input	2			µs
PWM to Output Current Linearity		Maximum deviation in output current vs. PWM duty cycle from 100% to 25%		1.4		%
Response Time of PWM Controlled Output		f_{PWM} < 2 kHz		$1/f_{PWM}$		sec
Response Time of PWM Controlled Output		f_{PWM} > 2 kHz			1.3	ms
PWM Accuracy		BLMX = 0x7F (30 mA), PWM duty cycle = 50%		1.0		%
FAULT PROTECTION						
Start-Up Charging Current Source	I_{SS}	V_{IN} = 3.6 V, $V_{OUT} = 0.8 \times V_{IN}$	3.5	7.0	11.0	mA
Output Voltage Threshold	V_{OUT}					
Exit Soft Start	$V_{OUT(START)}$	V_{OUT} rising		$0.92 \times V_{IN}$		V
Short-Circuit Protection	$V_{OUT(SC)}$	V_{OUT} falling		$0.55 \times V_{IN}$		V
Output Overvoltage Protection Activation Level	V_{OVP}			5.7		V
Thermal Shutdown						
Threshold	TSD			150		°C
Hysteresis	$TSD_{(HYS)}$			20		°C
Isolation from Input to Output During Fault	I_{OUTLKG}	V_{IN} = 5.5 V, V_{OUT} = 0 V, Bit nSTBY = 0			1	µA
Time to Validate a Fault	t_{FAULT}			2		µs
I²C INTERFACE						
V_{DDIO} Voltage Operating Range	V_{DDIO}				5.5	V
Logic Low Input[2]	V_{IL}	V_{IN} = 2.5 V			0.5	V
Logic High Input[3]	V_{IH}	V_{IN} = 5.5 V	1.45			V
I²C TIMING SPECIFICATIONS		Guaranteed by design				
Delay from Reset Deassertion to I²C Access	t_{RESET}				20	µs
SCL Clock Frequency	f_{SCL}				400	kHz
SCL High Time	t_{HIGH}		0.6			µs
SCL Low Time	t_{LOW}		1.3			µs
Setup Time						
Data	$t_{SU, DAT}$		100			ns
Repeated Start	$t_{SU, STA}$		0.6			µs
Stop Condition	$t_{SU, STO}$		0.6			µs

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Hold Time						
Data	$t_{HD, DAT}$		0		0.9	µs
Start/Repeated Start	$t_{HD, STA}$		0.6			µs
Bus-Free Time (Stop and Start Conditions)	t_{BUF}		1.3			µs
Rise Time (SCL and SDA)	t_R		20 + 0.1 C_B		300	ns
Fall Time (SCL and SDA)	t_F		20 + 0.1 C_B		300	ns
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns
Capacitive Load Per Bus Line	C_B				400	pF

[1] Matching is calculated by dividing the difference between the maximum and minimum current from the sum of the maximum and minimum.
[2] V_{IL} is a function of the V_{IN} voltage. See Figure 19 in the Typical Performance Characteristics section for typical values over operating ranges.
[3] V_{IH} is a function of the V_{IN} voltage. See Figure 19 in the Typical Performance Characteristics section for typical values over operating ranges.

Timing Diagram

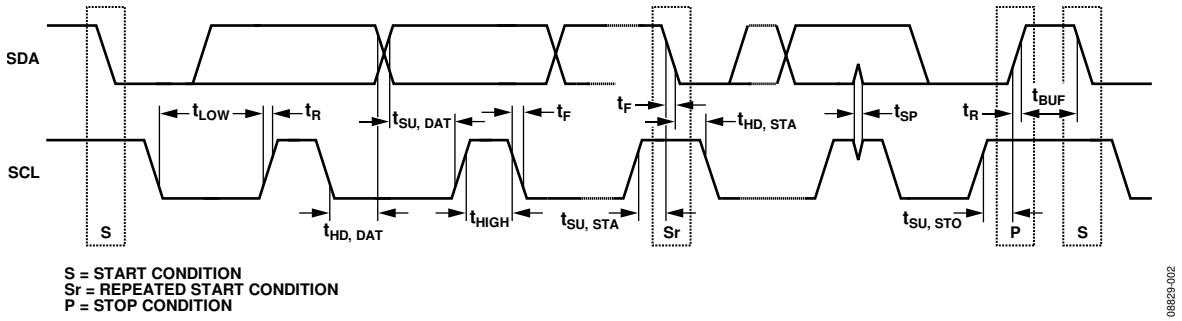

Figure 2. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, VOUT to GND	−0.3 V to +6 V
D1, D2, D3, D4, D5, D6, and D7 to GND	−0.3 V to +6 V
CMP_IN to GND	−0.3 V to +6 V
nINT, nRST, SCL, and SDA to GND	−0.3 V to +6 V
Output Short-Circuit Duration	Indefinite
Operating Ambient Temperature Range[1]	−40°C to +85°C
Operating Junction Temperature Range[1]	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020
ESD (Electrostatic Discharge)	
Human Body Model (HBM)	±2.0 kV
Charged Device Model (CDM)	±1.5 kV

[1] The maximum operating junction temperature ($T_{J(MAX)}$) supersedes the maximum operating ambient temperature ($T_{A(MAX)}$). See the Maximum Temperature Ranges section for more information.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all voltages are referenced to GND.

MAXIMUM TEMPERATURE RANGES

The maximum operating junction temperature ($T_{J(MAX)}$) supersedes the maximum operating ambient temperature ($T_{A(MAX)}$). Therefore, in situations where the ADP8870 is exposed to poor thermal resistance and a high power dissipation (P_D), the maximum ambient temperature may need to be derated. In these cases, the ambient temperature maximum can be calculated with the following equation:

$$T_{A(MAX)} = T_{J(MAX)} - (\theta_{JA} \times P_{D(MAX)}).$$

THERMAL RESISTANCE

θ_{JA} (junction to air) is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. The θ_{JA}, θ_{JB} (junction to board), and θ_{JC} (junction to case) are determined according to JESD51-9 on a 4-layer printed circuit board (PCB) with natural convection cooling. For the LFCSP package, the exposed pad must be soldered to GND.

Table 3. Thermal Resistance[1]

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
WLCSP	48	9	N/A	°C/W
LFCSP	49.5	N/A	5.3	°C/W

[1] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

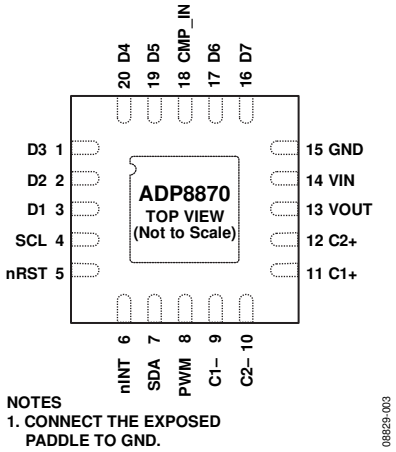

Figure 3. LFCSP Pin Configuration

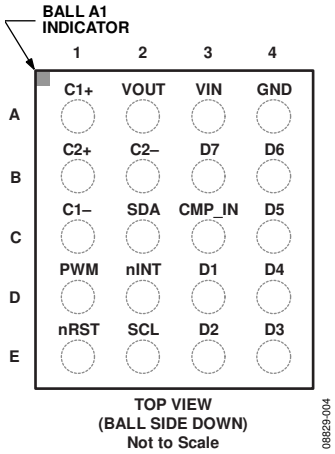

Figure 4. WLCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.			
LFCSP	**WLCSP**	**Mnemonic**	**Description**
14	A3	VIN	Input Voltage (2.5 V to 5.5 V).
3	D3	D1	LED Sink 1.
2	E3	D2	LED Sink 2.
1	E4	D3	LED Sink 3.
20	D4	D4	LED Sink 4.
19	C4	D5	LED Sink 5.
17	B4	D6	LED Sink 6 and optional comparator input for second phototransistor. When this pin is used as a second phototransistor input, a capacitor (0.1 µF recommended) must be connected from this pin to ground.
16	B3	D7	LED Sink 7.
18	C3	CMP_IN	Comparator Input for Phototransistor. When this pin is used, a capacitor (0.1 µF recommended) must be connected from this pin to ground.
13	A2	VOUT	Charge-Pump Output.
11	A1	C1+	Charge-Pump C1+.
9	C1	C1−	Charge-Pump C1−.
12	B1	C2+	Charge-Pump C2+.
10	B2	C2−	Charge-Pump C2−.
15	A4	GND	Ground.
8	D1	PWM	PWM Input for LED Dimming.
6	D2	nINT	Processor Interrupt (Active Low). Requires an external pull-up resistor. If this pin is not used, it can be left floating.
5	E1	nRST	Hardware Reset (Active Low). This bit resets the device to the default conditions. If this pin is not used, it must be tied above $V_{IH(MAX)}$.
7	C2	SDA	I^2C Serial Data. Requires an external pull-up resistor.
4	E2	SCL	I^2C Clock. Requires an external pull-up resistor.
EP		EP	Exposed Paddle. The exposed paddle must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 3.6 V, SCL = 2.7 V, SDA = 2.7 V, nRST = 2.7 V, $V_{D1:D7}$ = 0.4 V, C_{IN} = 1 µF, C1 = 1 µF, C2 = 1 µF, C_{OUT} = 1 µF, T_A= 25°C, unless otherwise noted.

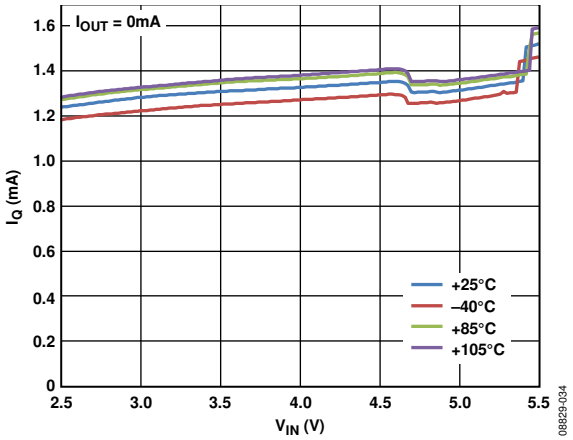

Figure 5. Typical Operating Current, G = 1×

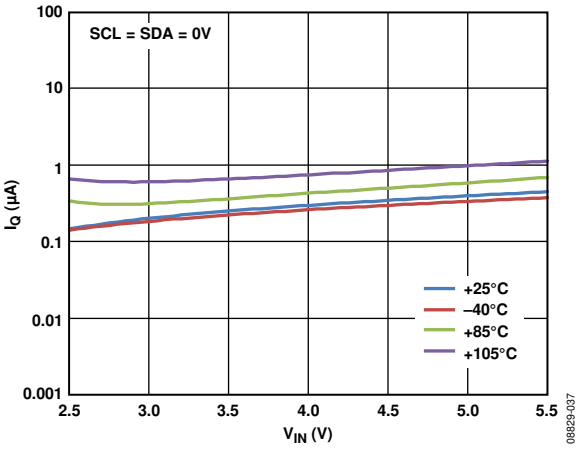

Figure 8. Typical Standby I_Q

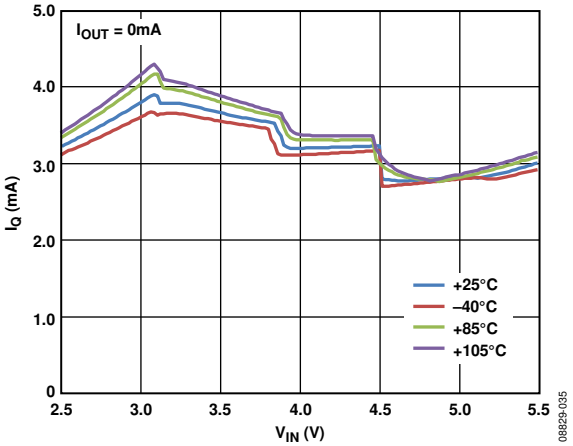

Figure 6. Typical Operating Current, G = 1.5×

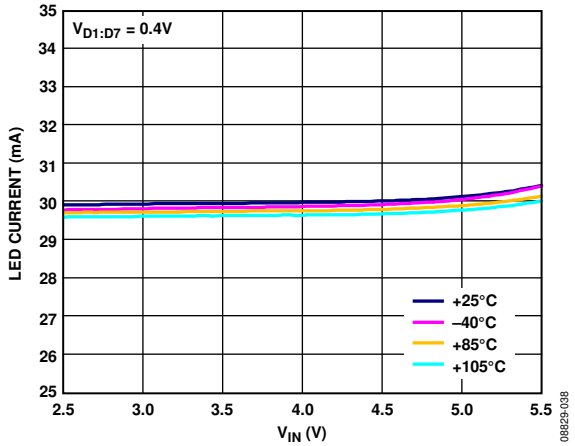

Figure 9. Typical Diode Current vs. V_{IN}

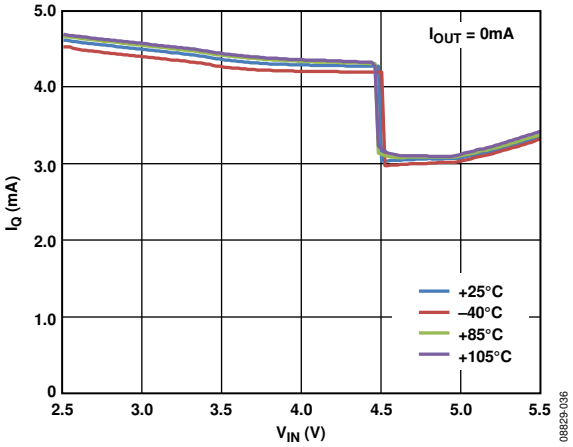

Figure 7. Typical Operating Current, G = 2×

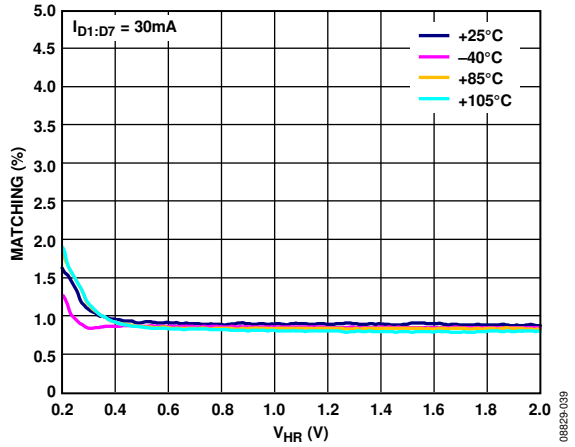

Figure 10. Typical Diode Matching vs. Current Sink Headroom Voltage (V_{HR})

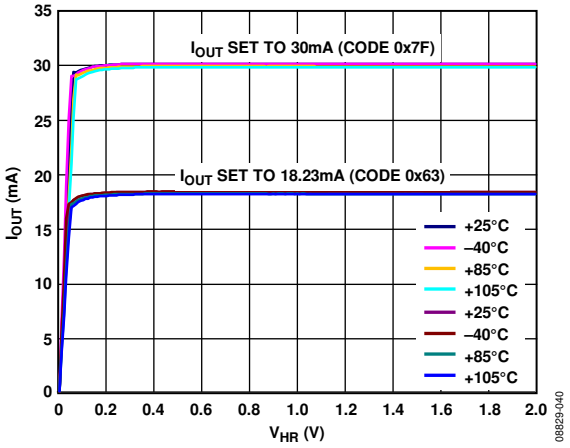

Figure 11. Typical Diode Current vs. Current Sink Headroom Voltage (V_{HR})

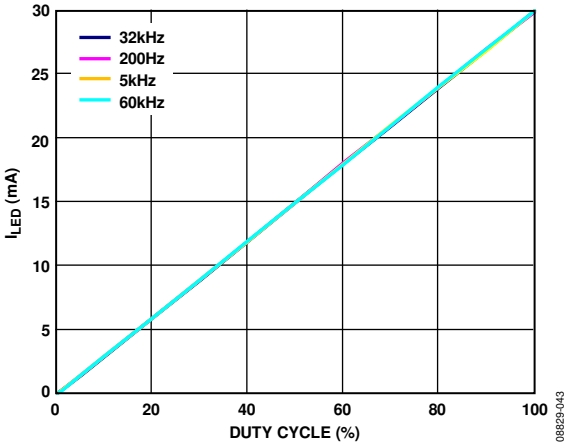

Figure 14. PWM Current Scaling Across PWM Frequency

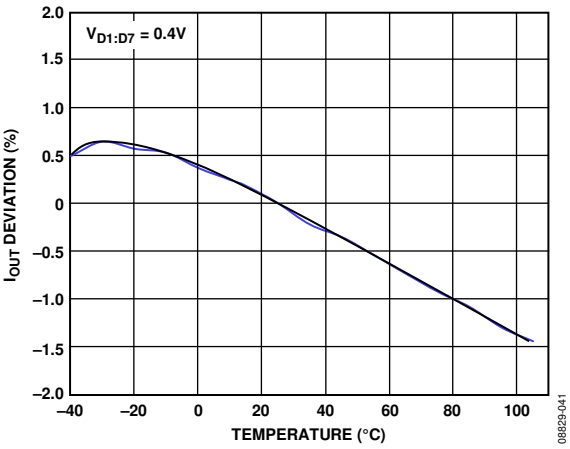

Figure 12. Typical Change In Diode Current vs. Temperature

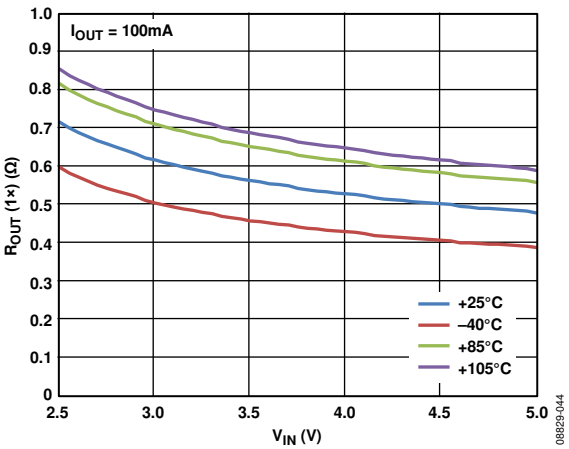

Figure 15. Typical R_{OUT} (G = 1×) vs. V_{IN}

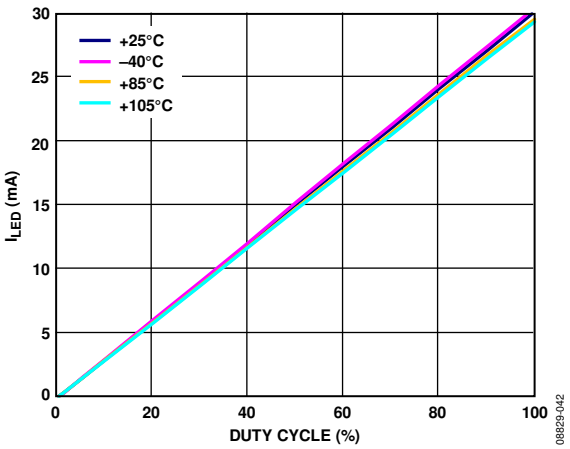

Figure 13. PWM Current Scaling Across Temperature

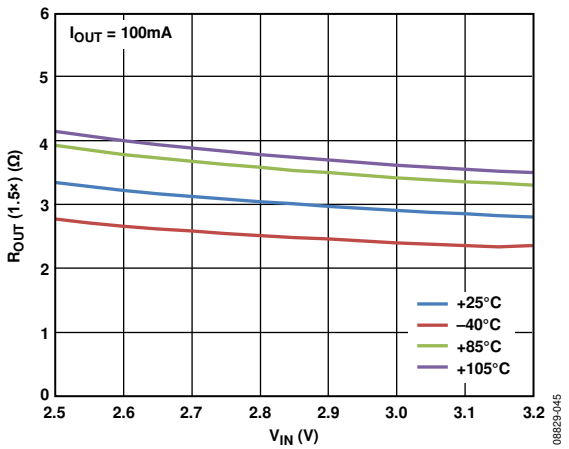

Figure 16. Typical R_{OUT} (G = 1.5×) vs. V_{IN}

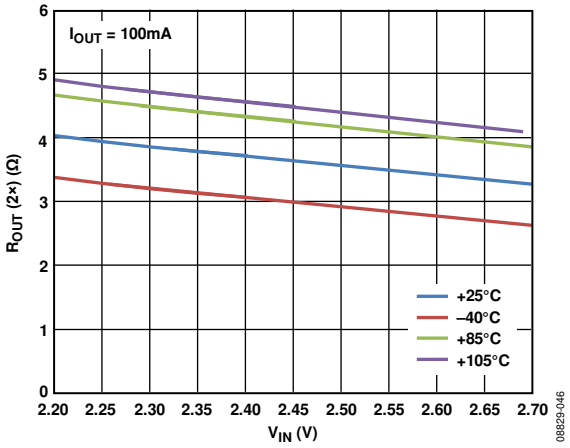

Figure 17. Typical R_{OUT} (G = 2×) vs. V_{IN}

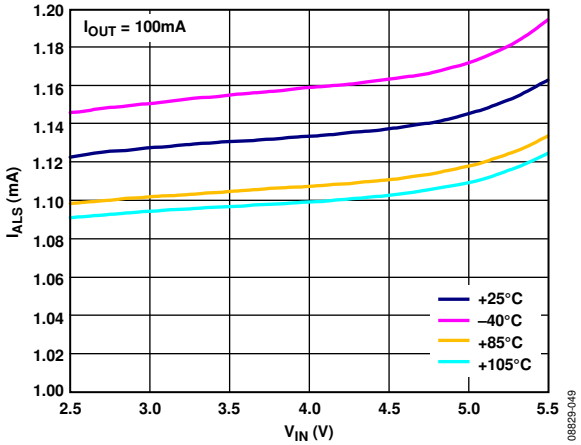

Figure 20. Typical ALS Current (I_{ALS})

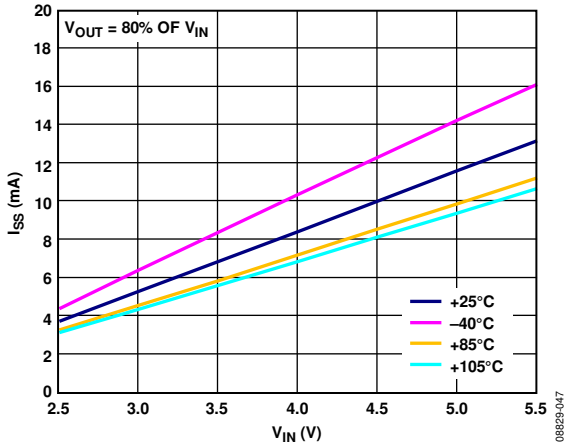

Figure 18. Typical Output Soft Start Current (I_{SS})

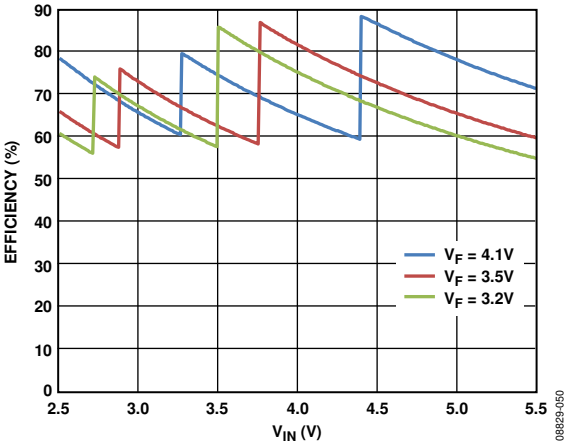

Figure 21. Typical Efficiency (Seven LEDs, 30 mA per LED)

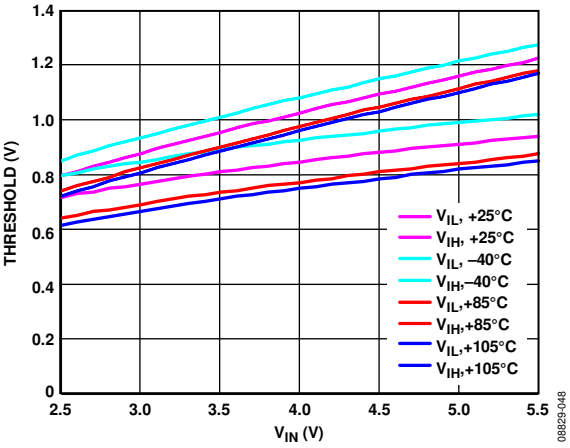

Figure 19. Typical I^2C Thresholds (V_{IH} and V_{IL})

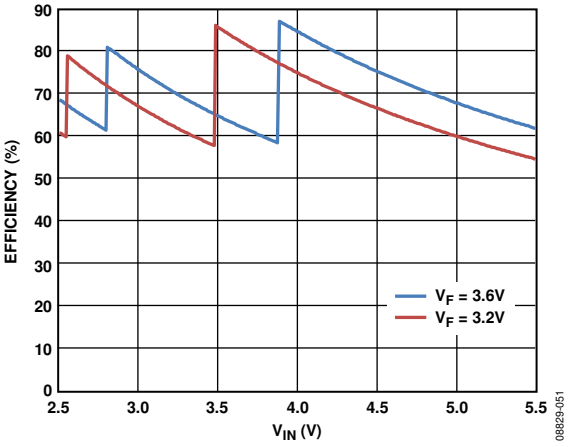

Figure 22. Typical Efficiency (Seven LEDs, 18 mA per LED)

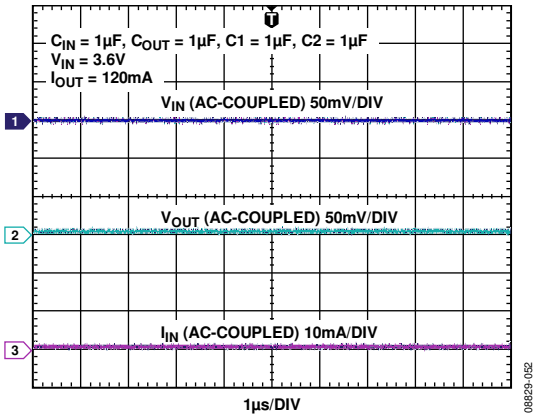

Figure 23. Typical Operating Waveforms, G = 1×

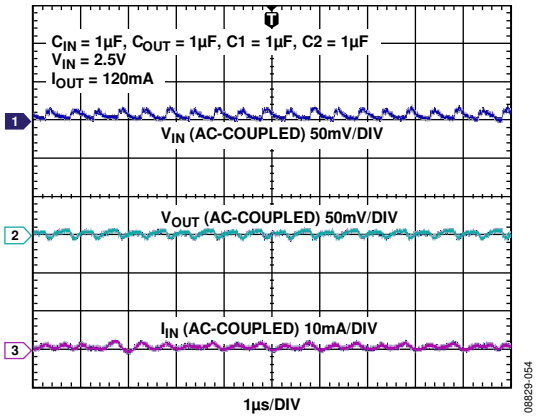

Figure 25. Typical Operating Waveforms, G = 2×

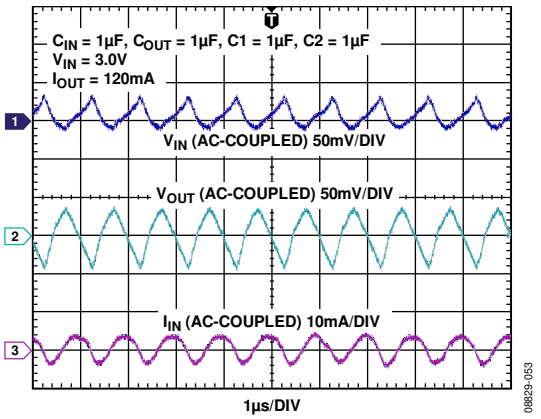

Figure 24. Typical Operating Waveforms, G = 1.5×

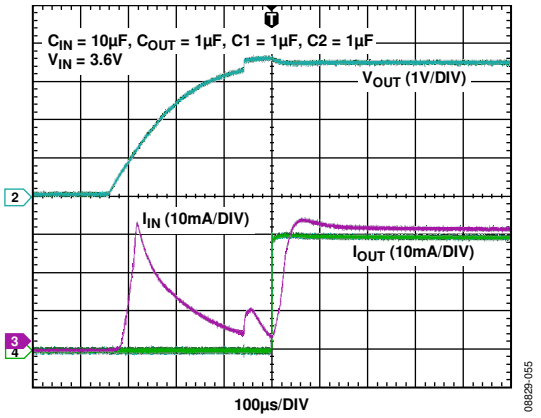

Figure 26. Typical Start-Up Waveforms

THEORY OF OPERATION

The ADP8870 combines a programmable backlight LED charge-pump driver with automatic phototransistor brightness control (LED current) and a PWM input to control the scale of the output current. This combination allows significant power savings because it automatically changes the current intensity based on the sensed ambient lighting levels and the display image content. It performs this function automatically and, therefore, removes the need for a processor to monitor the phototransistor. The light intensity thresholds are fully programmable via the I²C interface. A second phototransistor input, with dedicated comparators, improves the ambient light detection abilities for various operating conditions.

The ADP8870 allows up to seven LEDs to be independently driven up to 30 mA (typical). The seventh LED can be driven an additional 30 mA, for a maximum of up to 60 mA (typical). All LEDs can be individually programmed or combined into a group to operate backlight LEDs. A full suite of safety features, including short-circuit, overvoltage, and overtemperature protection with input-to-output isolation, allow for a robust and safe design. The integrated soft start limits inrush currents at startup, restart attempts, and gain transitions.

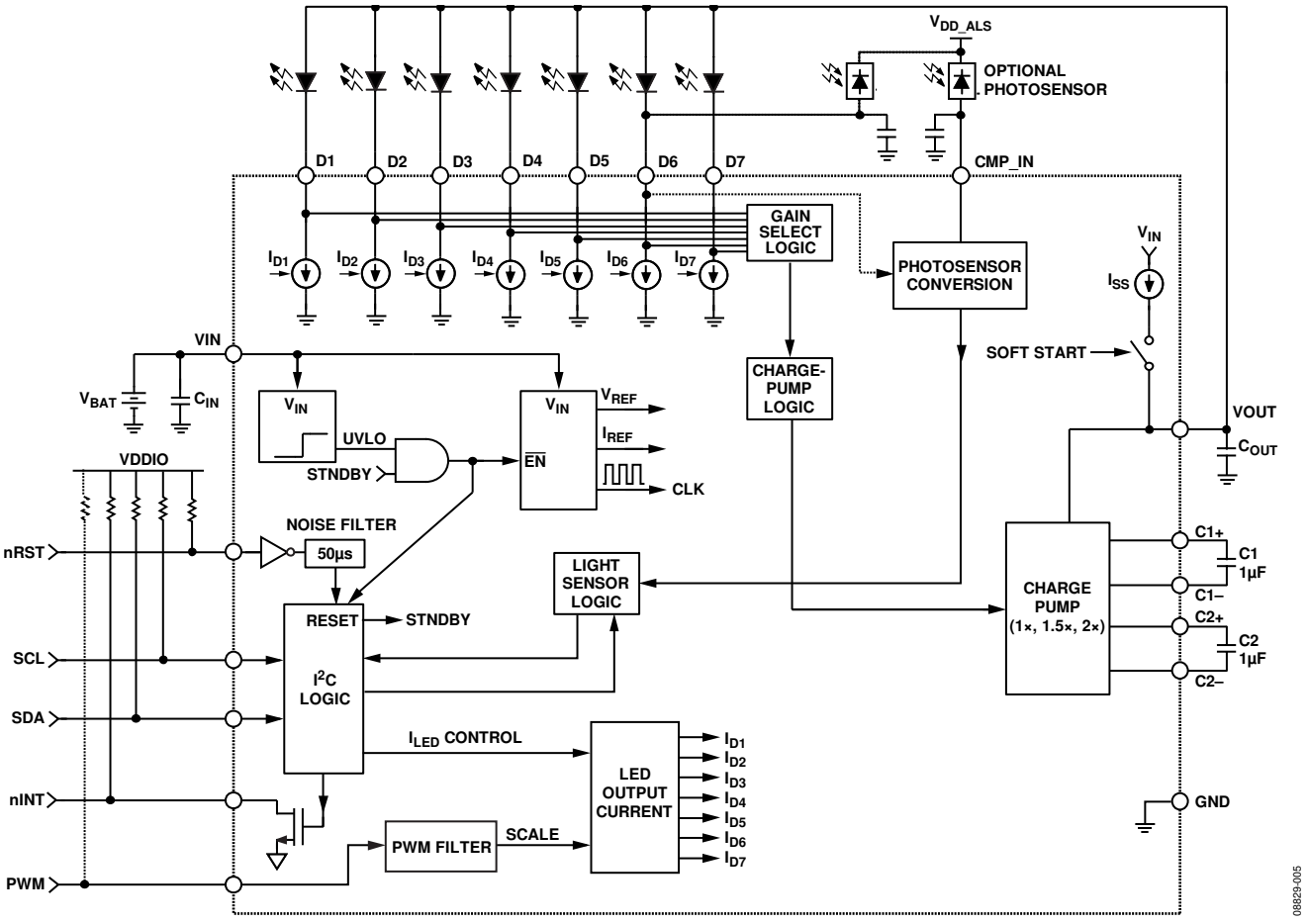

Figure 27. Detailed Block Diagram

POWER STAGE

Because typical white LEDs require up to 4 V to drive them, some form of boosting is required over the typical variation in battery voltage. The ADP8870 accomplishes this with a high efficiency charge pump capable of producing a maximum I_{OUT} of 240 mA over the entire input voltage range (2.5 V to 5.5 V). Charge pumps use the basic principle that a capacitor stores charge based on the voltage applied to it, as shown in the following equation:

$$Q = C \times V \quad (1)$$

By charging the capacitors in different configurations, the charge, and hence the gain, can be optimized to deliver the voltage required to power the LEDs. Because a fixed charging and discharging combination must be used, only certain multiples of gain are available. The ADP8870 is capable of automatically optimizing the gain (G) from 1×, 1.5×, and 2×. These gains are accomplished with two capacitors and an internal switching network.

In G = 1× mode, the switches are configured to pass VIN directly to VOUT. In this mode, several switches are connected in parallel to minimize the resistive drop from input to output. In G = 1.5× and G = 2× modes, the switches alternatively charge from the battery and discharge into the output. For G = 1.5×, the capacitors are charged from VIN in series and are discharged to VOUT in parallel. For G = 2×, the capacitors are charged from VIN in parallel and are discharged to VOUT in parallel. In certain fault modes, the switches are opened and the output is physically isolated from the input.

Automatic Gain Selection

Each LED that is driven requires a current source. The voltage on this current source must be greater than a minimum headroom voltage (225 mV typical) to maintain accurate current regulation. The gain is automatically selected based on the minimum voltage (V_{Dx}) at all of the current sources. At startup, the device is placed into G = 1× mode and the output charges to V_{IN}. If any V_{Dx} level is less than the required headroom (200 mV), then the gain is increased to the next step (G = 1.5 ×). A 100 µs delay is allowed for the output to stabilize prior to the next gain switching decision. If there remains insufficient current sink headroom, then the gain is increased again to 2×. Conversely, to optimize efficiency, it is not desirable for the output voltage to be too high. Therefore, the gain reduces when the headroom voltage is great enough. This point (labeled $V_{D(MAX)}$ in Figure 28) is internally calculated to ensure that the lower gain still results in ample headroom for all the current sinks. The entire cycle is illustrated in Figure 28.

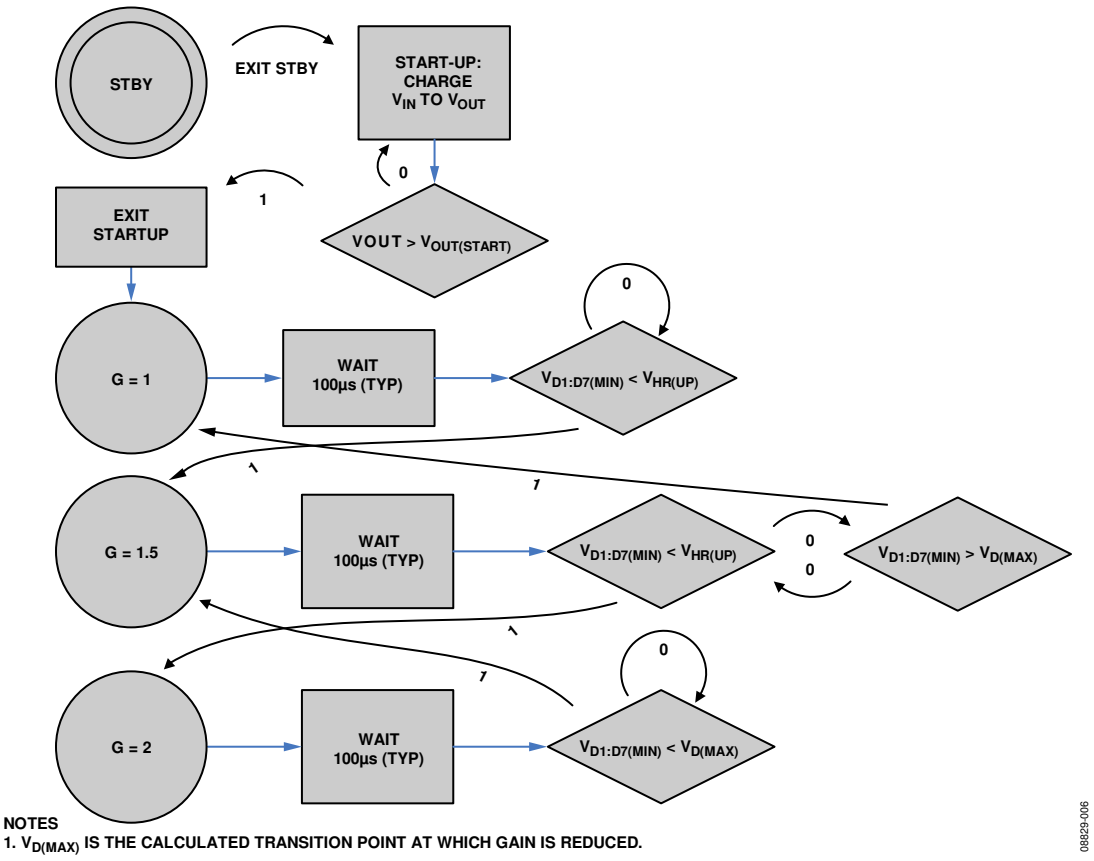

Figure 28. State Diagram for Automatic Gain Selection

Note that the gain selection criteria apply only to active current sources. If a current source has been deactivated through an I²C command (that is, if only five LEDs are used for an application), the voltages on these current sources are ignored.

Soft Start Feature

At startup (either from UVLO activation or fault/standby recovery), the output is first charged by I_{SS} (7.0 mA typical) until it reaches about 92% of V_{IN}. This soft start feature reduces the inrush current that is otherwise present when the output capacitance is initially charged to V_{IN}. When this point is reached, the controller enters 1× mode. If the output voltage is not sufficient, then the automatic gain selection determines the optimal point as described in the Automatic Gain Selection section.

OPERATING MODES

There are four different operating modes: active, standby, shutdown, and reset.

Active Mode

In active mode, all circuits are powered up and in a fully operational state. This mode is entered when nSTBY (in Register MDCR) is set to 1.

Standby Mode

Standby mode disables all circuitry except the I²C receivers. Current consumption is reduced to less than 1 μA. This mode is entered when nSTBY is set to 0 or when the nRST pin is held low for more than 100 μs (maximum). When standby is exited, a soft start sequence is performed.

Shutdown Mode

Shutdown mode disables all circuitry, including the I²C receivers. Shutdown occurs when V_{IN} is below the undervoltage thresholds. When V_{IN} rises above $V_{IN(START)}$ (2.02 V typical), all registers are reset and the part is placed into standby mode.

Reset Mode

In reset mode, all registers are set to their default values and the part is placed into standby. There are two ways to reset the part: power-on reset (POR) and the nRST pin. POR is activated anytime that the part exits shutdown mode. After a POR sequence is complete, the part automatically enters standby mode.

After startup, the part can be reset by pulling the nRST pin low. As long as the nRST pin is low, the part is held in a standby state but no I²C commands are acknowledged (all registers are kept at their default values). After releasing the nRST pin, all registers remain at their default values, and the part remains in standby; however, the part does accept I²C commands.

The nRST pin has a 50 μs (typical) noise filter to prevent inadvertent activation of the reset function. The nRST pin must be held low for this entire time to activate a reset.

The operating modes function according to the timing shown in Figure 29.

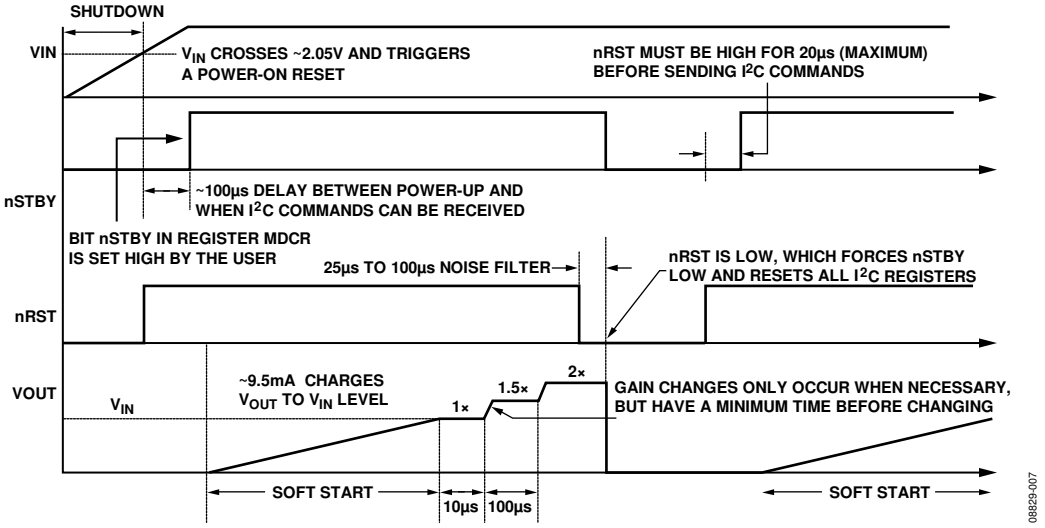

Figure 29. Typical Timing Diagram

IMAGE CONTENT CONTROL

Modern LCD display drivers often output the white intensity of the displayed image in the form of a PWM signal. When the white content of the displayed image is very small, the LCD driver generates a PWM duty cycle that is large. The ADP8870 takes advantage of this feature by incorporating a PWM input pin that scales the backlight intensity. When the PWM signal is at 100% duty cycle, the backlight current functions at its programmed value. However, when the PWM duty cycle drops, the ADP8870 automatically scales the output LED current down.

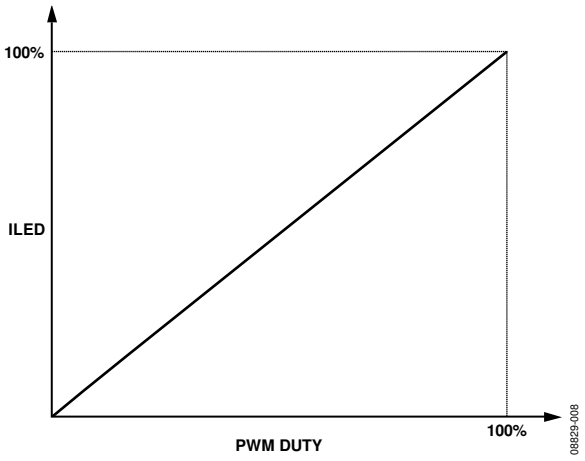

Figure 30. Output Current Response to PWM Input Duty Cycle

The LEDs that respond to the PWM input can be selected in the PWMLED register (Register 0x06). This image content works naturally with the automatic ambient light sensing and the three gains of the charge pump (see Figure 31).

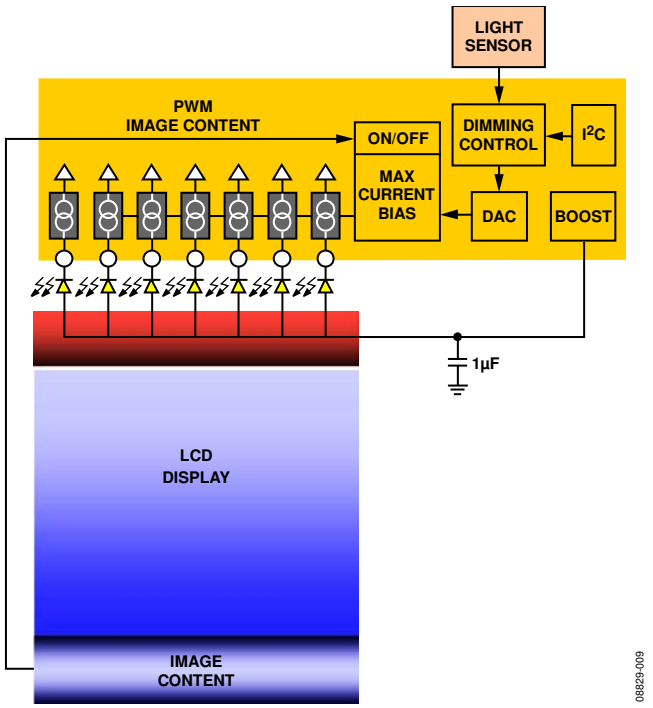

Figure 31. Functional Overview of the PWM Image Content Control, Ambient Light Sensor, and Charge Pump

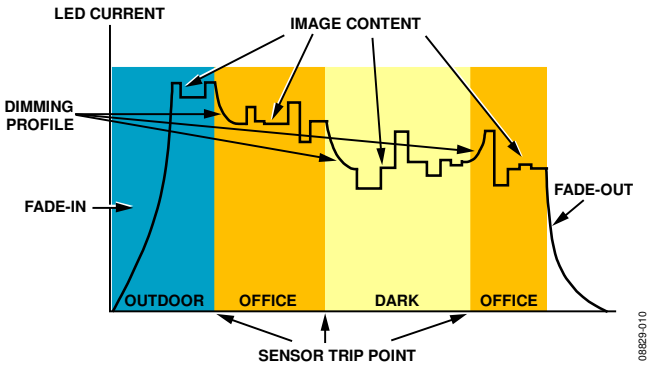

Figure 32. Example LED Output Current with the Effects of the Image Content PWM and Ambient Light Sensing

BACKLIGHT OPERATING LEVELS

Backlight brightness control can operate in five distinct levels: daylight (Level 1), bright (Level 2), office (Level 3), indoor (Level 4), and dark (Level 5). The BLV bits in Register 0x04 control the specific level in which the backlight operates. These bits can be changed manually, or if in automatic mode (that is, when CMP_AUTOEN is set high in Register 0x01), by the ambient light sensor (see the D7 Ambient Light-Sensing Control section).

By default, the backlight operates at daylight level (BLV = 000), where the maximum brightness is set using Register 0x0A (BLMX1). A daylight dim setting can also be set using Register 0x0B (BLDM1). Similarly, when operating at the bright, office, indoor, or dark level, the corresponding register is used (Register 0x0C to Register 0x13).

BACKLIGHT MAXIMUM AND DIM SETTINGS

The backlight maximum and dim current settings are determined by a 7-bit code programmed by the user into the registers previously listed in the Image Content Control section.

The 7-bit resolution allows the user to set the backlight to one of 128 different levels between 0 mA and 30 mA. The ADP8870 implements a square law algorithm to achieve a nonlinear relationship between input code and backlight current. The backlight current (in milliamperes) is determined by the following equation:

$$Backlight\ Current\ (\text{mA}) = \left(Code \times \frac{\sqrt{Full-Scale\ Current}}{127} \right)^2 \quad (2)$$

where:
Code is the input code programmed by the user.
Full-Scale Current is the maximum sink current allowed per LED (typically 30 mA).

Figure 34 shows the backlight current level vs. input code.

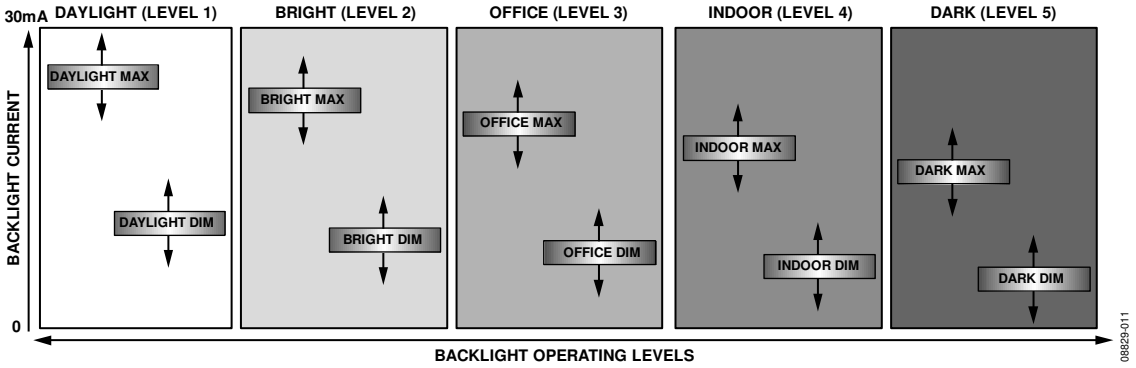

Figure 33. Backlight Operating Level

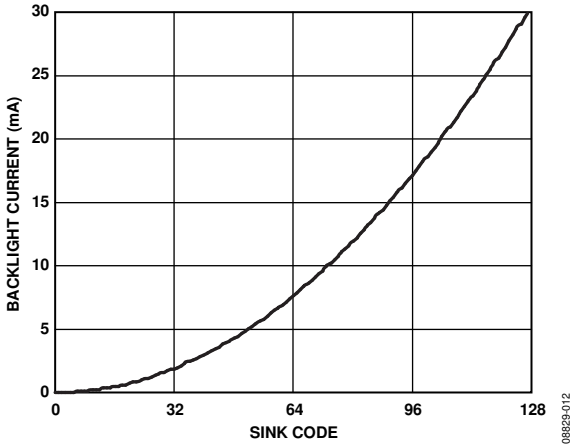

Figure 34. Backlight Current vs. Sink Code

AUTOMATED FADE-IN AND FADE-OUT

The LED drivers are easily configured for automated fade-in and fade-out. Sixteen fade-in and fade-out rates can be selected via the I²C interface. Fade-in and fade-out rates range from 0.1 sec to 5.5 sec (per full-scale current, either 30 mA or 60 mA). The BLOFF_INT bit (Register 0x02) can be used to flag the interrupt pin when an automated backlight fade-out occurs (see the Interrupts section).

Table 5. Available Fade-In and Fade-Out Times

Code	Fade Rate (sec)
0000	0.1 (disabled)
0001	0.3
0010	0.6
0011	0.9
0100	1.2
0101	1.5
0110	1.8
0111	2.1
1000	2.4
1001	2.7
1010	3.0
1011	3.5
1100	4.0
1101	4.5
1110	5.0
1111	5.5

The fade profile is based on the transfer law selected (square, Cubic 10, or Cubic 11) and the delta between the actual current and the target current. Smaller changes in current reduce the fade time. For square law fades, the fade time is given by

$$Fade\ Time = Fade\ Rate \times (Code/127) \quad (3)$$

where the *Fade Rate* is as shown in Table 5.

The Cubic 10 and Cubic 11 laws also use the square backlight currents in Equation 3; however, the time between each step is varied to produce a steeper slope at higher currents and a shallower slope at lighter currents (see Figure 35).

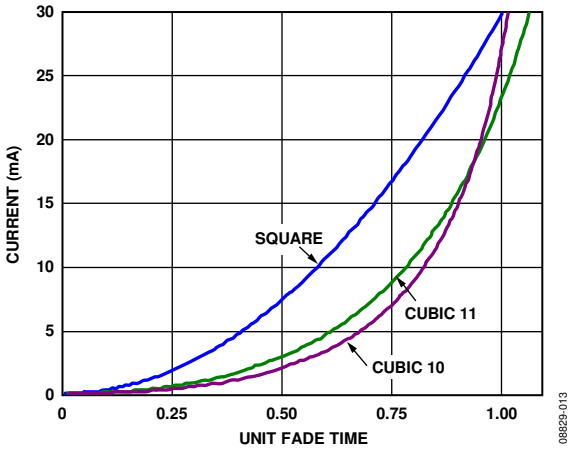

Figure 35. Comparison of the Dimming Transfers Laws

BACKLIGHT TURN ON/TURN OFF/DIM

With the device in active mode (nSTBY = 1), the backlight can be turned on using the BL_EN bit in Register 0x01. Before turning on the backlight, the user chooses which level (daylight, bright, office, indoor, or dark) in which to operate and ensures that maximum and dim settings are programmed for that level. The backlight turns on when BL_EN = 1. The backlight turns off when BL_EN = 0.

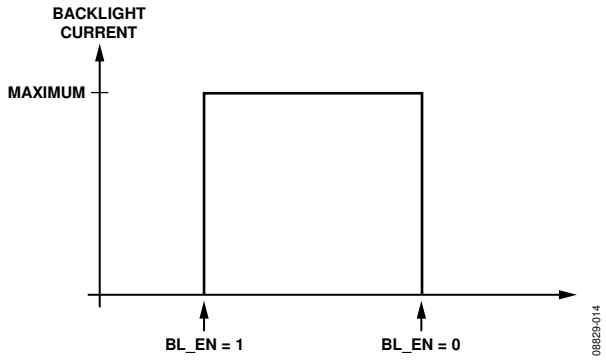

Figure 36. Backlight Turn On/Turn Off

While the backlight is on (BL_EN = 1), the user can make it change to a dim setting by programming DIM_EN = 1 in Register 0x01. If DIM_EN = 0, then the backlight reverts to its maximum setting.

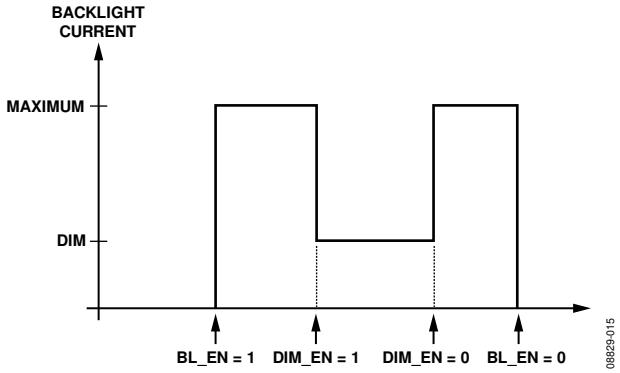

Figure 37. Backlight Turn On/Dim/Turn Off

The maximum and dim settings can be set between 0 mA and 30 mA; therefore, it is possible to program a dim setting that is greater than a maximum setting. For normal expected operation, ensure that the dim setting is programmed to be less than the maximum setting.

AUTOMATIC DIM AND TURN OFF TIMERS

The user can program the backlight to dim automatically by using the DIMT timer in Register 0x08. The dim timer has 127 settings, ranging from 1 sec to 127 sec. Program the dim timer before turning on the backlight. If BL_EN = 1, the backlight turns on to its maximum setting and the dim timer starts counting. When the dim timer expires, the internal state machine sets DIM_EN = 1, and the backlight enters its dim setting.

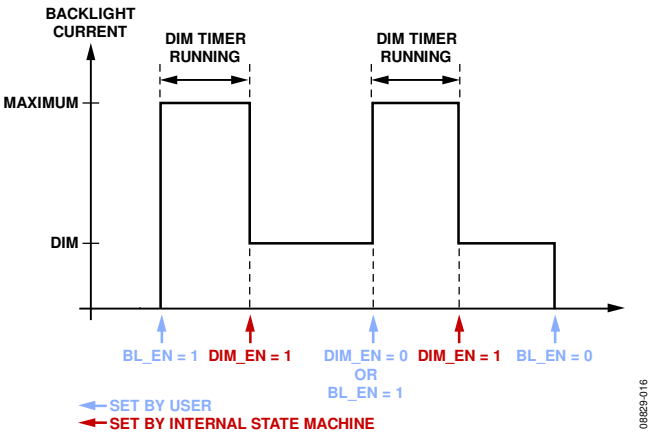

Figure 38. Dim Timer

If the user clears the DIM_EN bit (or reasserts the BL_EN bit), the backlight reverts to its maximum setting and the dim timer begins counting again. When the dim timer expires, the internal state machine again sets DIM_EN = 1, and the backlight enters its dim setting. Reasserting BL_EN at any point during the dim timer countdown causes the timer to reset and resume counting. The backlight can be turned off at any point during the dim timer countdown by clearing BL_EN.

The user can also program the backlight to turn off automatically by using the OFFT timer in Register 0x07. The off timer has 127 settings, ranging from 1 sec to 127 sec. Program the off timer before turning on the backlight. If BL_EN = 1, the backlight turns on to its maximum setting and the off timer starts counting. When the off timer expires, the internal state machine clears the BL_EN bit, and the backlight turns off.

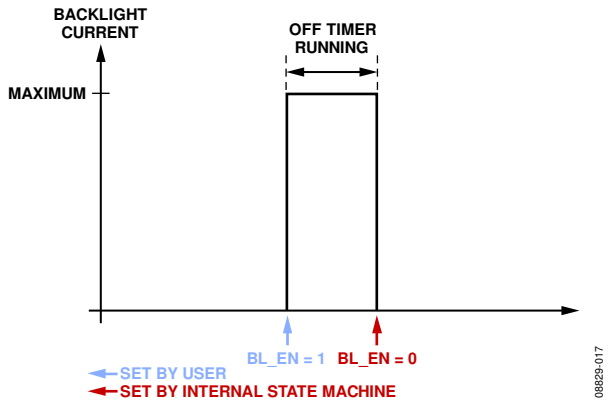

Figure 39. Off Timer

Reasserting BL_EN at any point during the off timer countdown causes the timer to reset and resume counting. The backlight can be turned off at any point during the off timer countdown by clearing BL_EN.

The dim timer and off timer can be used together for sequential maximum-to-dim-to-off functionality. With both the dim and off timers programmed, if BL_EN is asserted, the backlight turns on to its maximum setting. When the dim timer expires, the backlight changes to its dim setting. When the off timer expires, the backlight turns off.

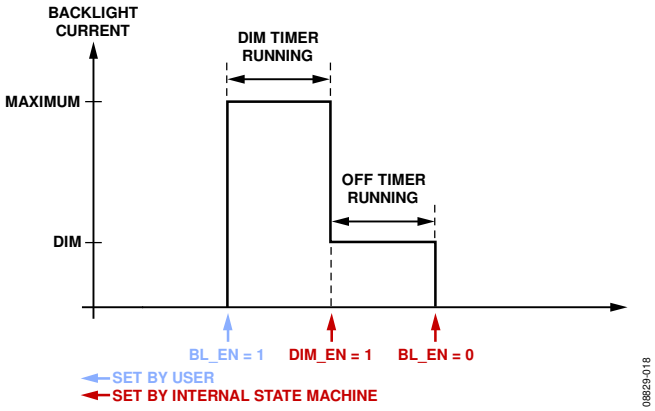

Figure 40. Dim Timer and Off Timer Used Together

FADE OVERRIDE

A fade override feature (FOVR in Register CFGR (Address 0x04)) enables the host to override the preprogrammed fade-in or fade-out settings. If FOVR is set and the backlight is enabled in the middle of a fade-out process, the backlight instantly (within approximately 100 ms) returns to its prefade brightness level. Alternatively, if the backlight is fading in, reasserting BL_EN overrides the programmed fade-in time and the backlight instantly goes to its final fade value. This is useful for situations where a key is pressed during a fade sequence. Alternatively, if FOVR is cleared and the backlight is enabled in the middle of a fade process, the backlight fades in from where it was interrupted (that is, it does not go down to 0 and then come back on).

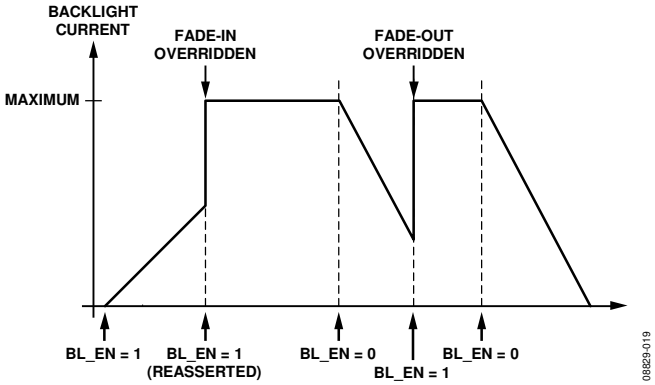

Figure 41. Fade Override Function (FOVR is High)

BACKLIGHT AMBIENT LIGHT SENSING

The ADP8870 integrates two ambient light-sensing comparators. One of the ambient light sensing comparators (CMP_IN) is always available. The second one (CMP_IN2) can be activated instead of having an LED connected to D6. Activating CMP_IN2 is accomplished through Bit CMP2_SEL in Register CFGR. Therefore, when Bit CMP2_SEL is set to 0, Pin D6 is programmed as a current sink. When Bit CMP2_SEL is set to 1, Pin D6 becomes the input for a second phototransistor.

These comparators have four programmable trip points (Level 2, Level 3, Level 4, and Level 5) that can be used to select between the five backlight operating modes (daylight, bright, office, indoor, and dark) based on the ambient lighting conditions.

The Level 5 comparator controls the dark-to-indoor mode transition. The Level 4 comparator controls the indoor-to-office transition. The Level 3 comparator controls the office-to-bright transition. The Level 2 comparator controls the bright-to-outdoor transition (see Figure 42). The currents for the different lighting modes are defined in the BLMXx and BLDMx registers (see the Backlight Operating Levels section).

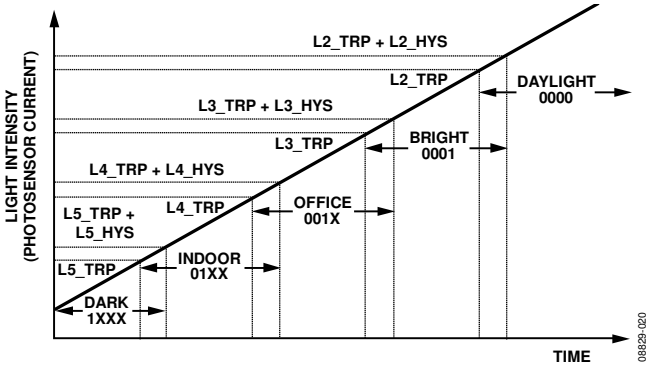

Figure 42. Light Sensor Modes are Based on the Ambient Light Level Detected

Each light sensor comparator uses an external capacitor together with an internal reference current source to form an analog-to-digital converter (ADC) that samples the output of the external photosensor. The ADC result is fed into four programmable trip comparators. The ADC has an input range of 0 µA to 1100 µA (typical).

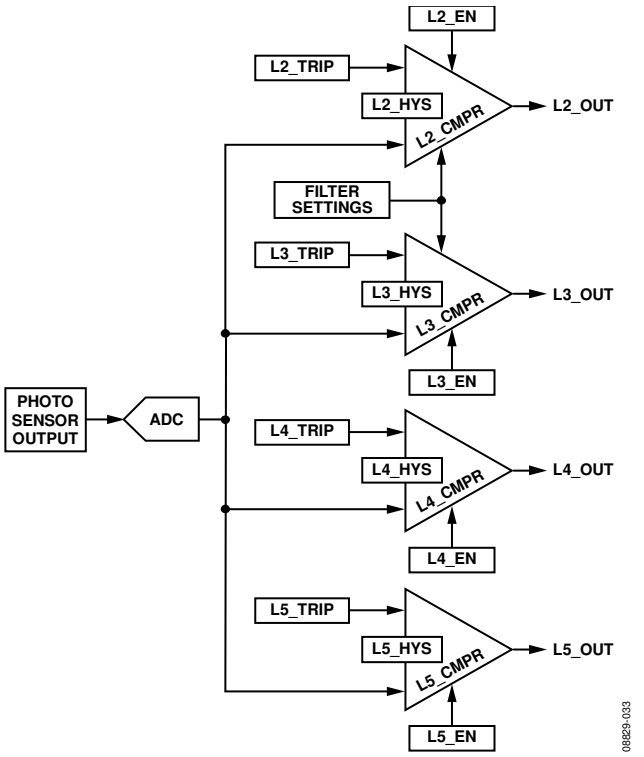

Figure 43. Ambient Light-Sensing and Trip Comparators

Each level comparator detects when the photosensor output has dropped below the programmable trip point (defined in Register 0x32, Register 0x34, Register 0x36, and Register 0x38). If this event occurs, then the corresponding level output status signal is set in Register 0x30 and Register 0x31. Each level comparator contains programmable hysteresis, meaning that the photosensor output must rise above the trip threshold plus the hysteresis value before the level output clears. Each level is enabled via a corresponding bit in the ALS1_EN (Address 0x2E) and ALS2_EN (Address 0x2F) registers.

The L2_TRP and L2_HYS values of Level 2 comparator can be set between 0 µA and 1100 µA (typical) in steps of 4.4 µA (typical).

The L3_TRP and L3_HYS values of Level 3 comparator can be set between 0 µA and 550 µA (typical) in steps of 2.2 µA (typical).

The L4_TRP and L4_HYS values of Level 4 comparator can be set between 0 µA and 275 µA (typical) in steps of 1.1 µA (typical).

The L5_TRP and L5_HYS values of Level 5 comparator can be set between 0 µA and 137 µA (typical) in steps of 0.55 µA (typical).

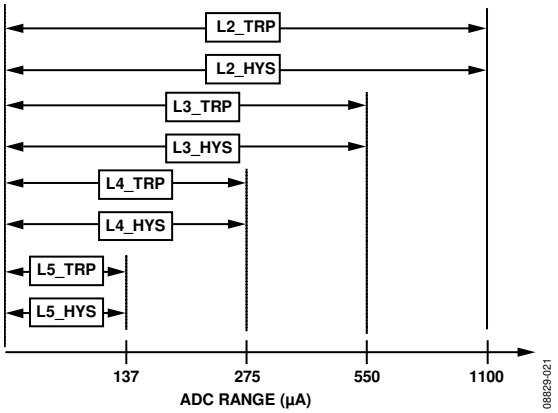

Figure 44. Comparator Ranges

It is important to note that the full-scale value of the L2_TRP and L2_HYS registers is 250 d. Therefore, if the value of L2_TRP + L2_HYS exceeds 250 d, the comparator output cannot deassert. For example, if L2_TRP is set at 204 d (80% of the full-scale value, or approximately 0.80 × 1122 µA = 898 µA), then L2_HYS must be set at less than 46 d (250 − 204 = 46). If it is not, then L2_HYS + L2_TRP exceeds 250 d and the Level 2 comparator is not allowed to go low.

When both phototransistors are enabled and programmed in automatic mode, the user application needs to determine which of the comparator outputs to use, selecting via Bit SEL_AB in Register 0x04 for automatic light sensing transitions. For example, the user's software might select the comparator of the phototransistor exposed to higher light intensity to control the transition between the programmed backlight intensity levels.

The level comparators can be enabled independent of each other or can operate simultaneously. A single conversion from each ADC takes 80 ms (typical). When set for automatic backlight adjustment (see the Automatic Backlight Adjustment section), the ADC and comparators run continuously. If the backlight is disabled, it is possible to use the light sensor comparators in a single-shot mode. A single-shot read of the photocomparators is performed by setting the FORCE_RD bit (Register 0x2D). After the single shot measurement is completed, the internal state machine clears the FORCE_RD bit.

Interrupt Flag CMP_INT (Register 0x02) is set if any of the level output status bits change state for the main photosensor input. This means that interrupts can be generated if ambient light conditions transition between any of the programmed trip points. CMP_INT can cause the nINT pin to be asserted if the CMP_IEN bit (Register 0x03) is set. The CMP_INT flag can only be cleared by writing a 1 to it or resetting the part.

The operation of CMP2_INT (Register 0x02) and CMP2_IEN (Register 0x03) is similar except that the second phototransistor (that is, CMP_IN2) is used.

D7 AMBIENT LIGHT-SENSING CONTROL

LED D7 can be programmed to operate independent from the backlight reset when under ALS control. This is useful when D7 is used to control peripheral lighting (for example, the keypad) that needs to respond differently than the backlight lighting. This feature uses the same ALS controls and thresholds as the backlight.

To engage D7 ALS control, first program the five ALS levels of D7 found in Register 0x25 to Register 0x29. Then set Bit D7ALS_EN in Register 0x01 and Bit D7SEL in Register 0x05.

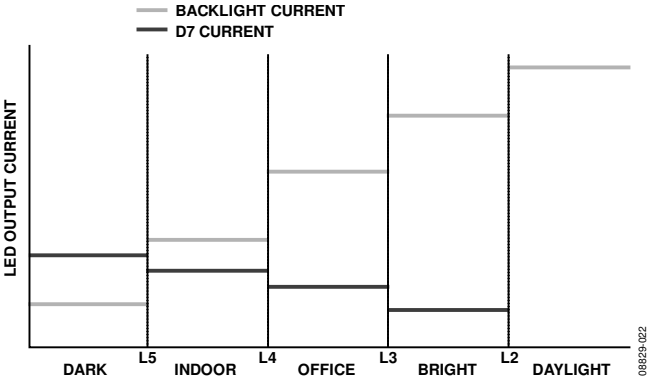

Figure 45. A Possible Example of the Separate ALS Control of D7

AUTOMATIC BACKLIGHT ADJUSTMENT

The ambient light sensor comparators can be used to automatically transition the backlight between one of its three operating levels. To enable this mode, set the CMP_AUTOEN bit in Register 0x01.

When enabled, the internal state machine takes control of the BLV bits and changes them based on the level output status bits. Table 6 shows the relationship between backlight operation and the ambient light sensor comparator outputs. The higher numbered level output status bit have greater priority over the lower numbered levels.

Filter times between 80 ms and 10 sec can be programmed for the comparators (Register 0x2D) before they change state.

Table 6. Comparator Output Truth Table[1]

L5_OUT	L4_OUT	L3_OUT	L2_OUT	ALS Level	BLV Code
1	X	X	X	Dark	100
0	1	X	X	Indoor	011
0	0	1	X	Office	010
0	0	0	1	Bright	001
0	0	0	0	Outdoor	000

[1]X is the don't care bit.

INDEPENDENT SINK CONTROL (ISC)

Each of the 7 LEDs can be configured (in Register 0x05) to operate as either part of the backlight or to operate as an independent sink current (ISC). Each ISC can be enabled independently and has its own current level. All ISCs share the same fade-in times, fade-out times, and fade law.

The ISCs have additional timers to facilitate blinking functions. A shared on timer (SCON), used in conjunction with the off timers of each ISC (SC1OFF, SC2OFF, SC3OFF, SC4OFF, SC5OFF, SC6OFF, and SC7OFF), allow the LED current sinks to be configured in various blinking modes. The on timer can be set to four settings: 0.2 sec, 0.6 sec, 0.8 sec, and 1.2 sec. The off timers also have four settings: disabled, 0.6 sec, 0.8 sec, and 1.2 sec. Blink mode is activated by setting the off timers to any setting other than disabled.

Program all fade, on, and off timers before enabling any of the LED current sinks. If ISCx is on during a blink cycle and SCx_EN is cleared, it turns off (or fades to off if fade-out is enabled). If ISCx is off during a blink cycle and SCx_EN is cleared, it stays off.

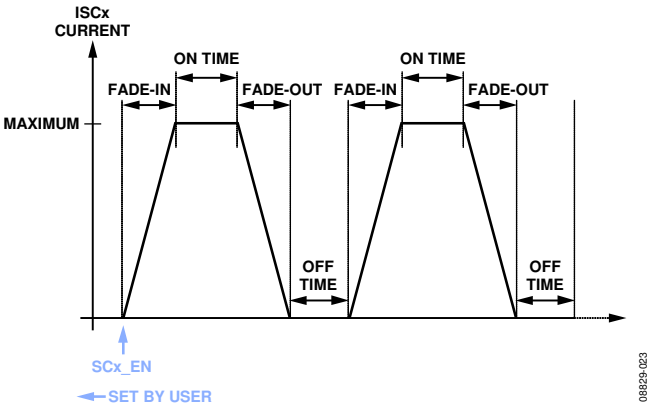

Figure 46. LEDx Blink Mode with Fading

SHORT-CIRCUIT PROTECTION (SCP) MODE

The ADP8870 can protect against short circuits on the output (V_{OUT}). Short-circuit protection (SCP) is activated at the point when V_{OUT} < 55% of V_{IN}. Note that this SCP sensing is disabled during startup and restart attempts (fault recovery). SCP sensing is reenabled 4 ms (typical) after activation. During a short-circuit fault, the device enters a low current consumption state and an interrupt flag is set. The device can be restart at any time after receiving a short-circuit fault by simply rewriting nSTBY = 1. It then repeats another complete soft start sequence. Note that the value of the output capacitance (C_{OUT}) should be small enough to allow V_{OUT} to reach approximately 55% (typical) of V_{IN} within the 4 ms (typical) time. If C_{OUT} is too large, the device inadvertently enters short-circuit protection.

OVERVOLTAGE PROTECTION (OVP)

Overvoltage protection is implemented on the output. There are two types of overvoltage events: normal (no fault) and abnormal.

Normal (No Fault) Overvoltage

The output voltage approaches $V_{OUT(REG)}$ (4.7 V typical) during normal operation. This is not caused by a fault or load change, but simply a consequence of the input voltage times the gain reaching the clamped output voltage $V_{OUT(REG)}$. To prevent this, the ADP8870 detects when the output voltage rises to $V_{OUT(REG)}$. It then increases the effective R_{OUT} of the gain stage to reduce the voltage that is delivered. This effectively regulates V_{OUT} to $V_{OUT(REG)}$; however, there is a limit to the effect that this system can have on regulating V_{OUT}. It is designed only for normal operation and is not intended to protect against faults or sudden load changes. During this mode, no interrupt is set and the operation is transparent to the LEDs and overall application. The automatic gain selection equations take into account the additional drop within R_{OUT} to maintain optimum efficiency.

Abnormal (Fault/Sudden Load Change) Overvoltage

Due to the open loop behavior of the charge pump as well as how the gain transitions are computed, a sudden load change or fault can abnormally force V_{OUT} beyond 6 V. If the event happens slowly enough, the system first tries to regulate the output to 4.7 V (typical) as in a normal overvoltage scenario. However, if this is not sufficient, or if the event happens too quickly, then the ADP8870 enters overvoltage protection mode when V_{OUT} exceeds the OVP threshold (typically 5.7 V). In this mode, the charge pump is disabled to prevent V_{OUT} from rising too high. The current sources and all other device functionality remain intact. When the output voltage falls below the OVP threshold, the charge pump resumes operation. If the fault or load step recurs, the process may repeat. An interrupt flag is set at each OVP instance.

THERMAL SHUTDOWN (TSD)/ OVERTEMPERATURE PROTECTION

If the die temperature of the ADP8870 rises above a safety limit (150°C typical), the controllers enter TSD protection mode. In this mode, most of the internal functions are shut down, the part enters standby, and the TSD_INT interrupt (Register 0x02) is set. When the die temperature decreases below ~130°C, the part is allowed to be restarted. To restart the part, simply remove it from standby. No interrupt is generated when the die temperature falls below 130°C. However, if the software clears the pending TSD_INT interrupt and the temperature remains above 130°C, another interrupt is generated.

The complete state machine for these faults (SCP, OVP, and TSD) is shown in Figure 47.

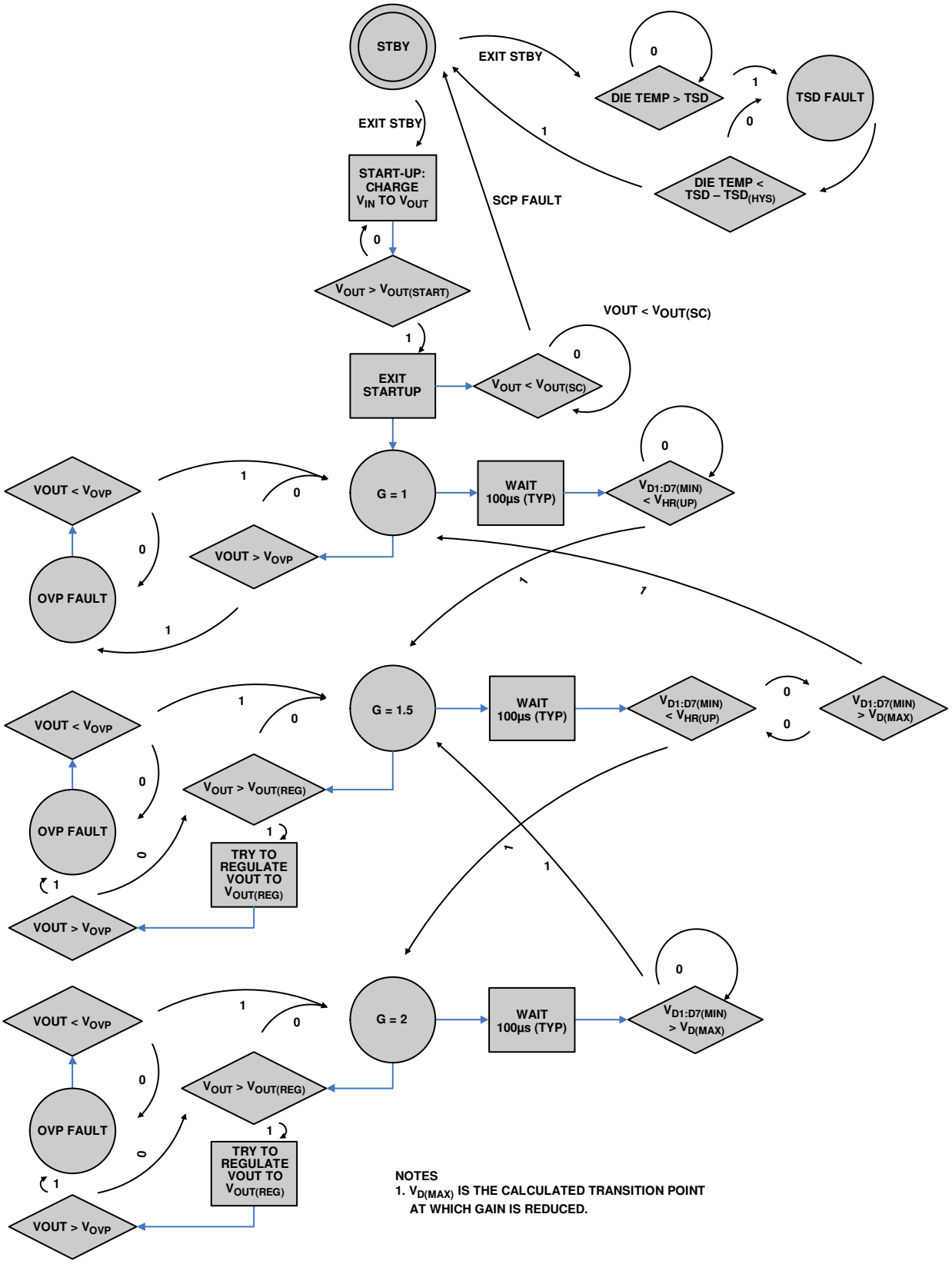

Figure 47. Fault State Machine

INTERRUPTS

There are six interrupt sources available on the ADP8870 (in Register 0x02).

- Backlight off: at the end of each automated backlight fade-out, this interrupt (BLOFF_INT) is set.
- Main light sensor comparator: CMP_INT sets every time the main light sensor comparator detects a threshold (Level 2, Level 3, Level 4, or Level 5) transition (rising or falling conditions).
- Sensor Comparator 2: CMP2_INT interrupt works the same way as CMP_INT, except that the sensing input is coming from the second light sensor. The programmable threshold is the same as the main light sensor comparator.
- Overvoltage protection: OVP_INT is generated when the output voltage exceeds 5.7 V (typical).
- Thermal shutdown circuit: an interrupt (TSD_INT) is generated when entering overtemperature protection.
- Short-circuit detection: SHORT_INT is generated when the device enters short-circuit protection mode.

The interrupt (if any) that appears on the nINT pin is determined by the bits mapped in Register INT_EN. To clear an interrupt, write a 1 to the interrupt in the INT_STAT register or reset the part.

BACKLIGHT OFF INTERRUPT

The backlight off interrupt (BLOFF_INT) is set when the backlight completes an automated fade sequence. This could be a simple fade-out command or a complete dimming profile. This feature is useful to synchronize the backlight turn off with the LCD display driver.

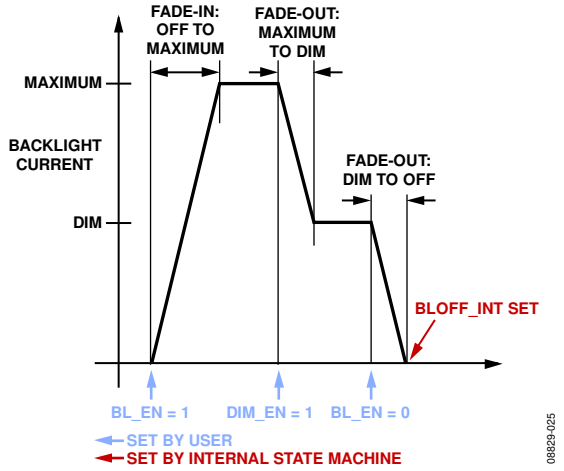

Figure 48. End of Fade-Out (EOF) Interrupt as Used for a Backlight Fade-Out (Set by User)

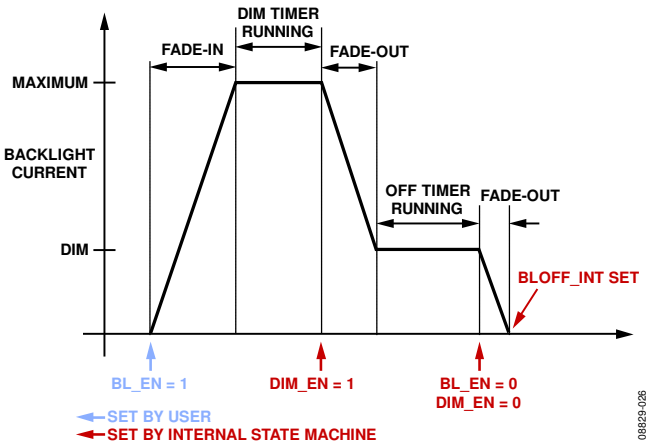

Figure 49. End of Fade-Out (EOF) Interrupt as Used for an Automated Dim Profile (Set by Internal State Machine)

APPLICATIONS INFORMATION

The ADP8870 allows the charge pump to operate efficiently with a minimum of external components, requiring only an input capacitor (C_{IN}), an output capacitor (C_{OUT}), and two charge-pump fly capacitors (C1 and C2). C_{IN} should be 1 µF or greater, and C_{OUT}, C1, and C2 should each be 1 µF. Although in some cases other values can be used, keep in mind the following:

- The value of C_{IN} must be high enough to produce a stable input voltage signal at the minimum input voltage and maximum output load.
- Values larger than 1 µF are permissible for C_{OUT}, but care must be exercised to ensure that V_{OUT} charges above 55% (typ) of V_{IN} within 4 ms (typ). See the Short-Circuit Protection (SCP) Mode section for more details.
- Values larger than 1 µF for C1 and C2 are not recommended, and smaller values may reduce the ability of the charge pump to deliver maximum current.

Furthermore, for optimal efficiency, the charge-pump fly capacitors should have low equivalent series resistance (ESR). Low ESR X5R or X7R capacitors are recommended for all four components. The use of fly capacitors sized 0402 and smaller is allowed, but the GDWN_DIS bit in Register 0x01 must be set. Minimum voltage ratings should adhere to the guidelines in Table 7.

Table 7. Capacitor Stress in Each Charge Pump Gain State

Capacitor	Gain = 1×	Gain = 1.5×	Gain = 2×
C_{IN}	V_{IN}	V_{IN}	V_{IN}
C_{OUT}	V_{IN}	V_{IN} × 1.5 (max of 5.5 V)	V_{IN} × 2.0 (max of 5.5 V)
C1	None	$V_{IN}/2$	V_{IN}
C2	None	$V_{IN}/2$	V_{IN}

If one or both ambient light sensor comparator inputs (CMP_IN and/or D6) are used, a small capacitor (0.1 µF is recommended) must be connected from the comparator input pins to ground. When a light sensor conversion reading takes place, the voltage on these pins is V_{ALS} (0.95 V typical, see Table 1). Therefore, the minimum supply voltage for the ALS sensor should be greater than $V_{ALS(MAX)}$ plus the biasing voltage required for the photosensor.

Any color of LED can be used if the V_F (forward voltage) is less than 4.1 V. However, using lower V_F LEDs reduces the input power consumption by allowing the charge pump to operate at lower gain states.

The equivalent model for a charge pump is shown in Figure 50.

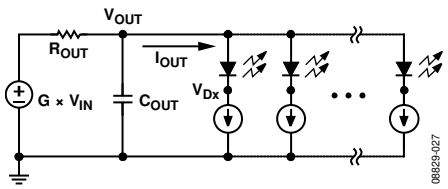

Figure 50. Charge-Pump Equivalent Circuit Model

The input voltage is multiplied by the gain (G) and delivered to the output through an effective resistance (R_{OUT}). The output current flows through R_{OUT} and produces an IR drop that yields

$$V_{OUT} = G \times V_{IN} - I_{OUT} \times R_{OUT}(G) \quad (6)$$

The R_{OUT} term is a combination of the $R_{DS(ON)}$ resistance for the switches used in the charge pump and a small resistance that accounts for the effective dynamic charge-pump resistance. The R_{OUT} level changes based on the gain, which is dependent on the configuration of the switches. Typical R_{OUT} values are given in Table 1 and Figure 15 to Figure 17. V_{OUT} is also equal to the largest V_F of the LEDs used plus the voltage drop across the regulating current source. This gives

$$V_{OUT} = V_{F(MAX)} + V_{Dx} \quad (7)$$

Combining Equation 6 and Equation 7 gives

$$V_{IN} = (V_{F(MAX)} + V_{Dx} + I_{OUT} \times R_{OUT}(G))/G \quad (8)$$

This equation is useful for calculating approximate bounds for the charge pump design.

Determining the Transition Point of the Charge Pump

Consider the following design example where:

$V_{F(MAX)}$ = 3.7 V
I_{OUT} = 140 mA (7 LEDs at 20 mA each)
$R_{OUT}(G = 1.5\times)$ = 3 Ω (obtained from Figure 12)

At the point of a gain transition, $V_{Dx} = V_{HR(UP)}$. Table 1 gives the typical value of $V_{HR(UP)}$ as 0.225 V. Therefore, the input voltage level when the gain transitions from 1.5× to 2× is

$$V_{IN} = (3.7\text{ V} + 0.225\text{ V} + 140\text{ mA} \times 3\ \Omega)/1.5 = 2.90\text{ V}$$

LAYOUT GUIDELINES

Use the following layout guidelines:

- For optimal noise immunity, place the C_{IN} and C_{OUT} capacitors as close to their respective pins as possible. These capacitors should share a short ground trace. If the LEDs are a significant distance from the VOUT pin, another capacitor on VOUT, placed closer to the LEDs, is advisable.
- For optimal efficiency, place the charge-pump fly capacitors as close to the part as possible.
- The ground pin should be connected at the ground for the input and output capacitors. If the LFCSP package is used, the exposed pad must be soldered at the board to the GND pin.
- Unused Diode Pins[D1:D7] can be connected to ground or VOUT, or can remain floating. However, the unused diode current sinks must be disabled by setting them as independent sinks in Register 0x05 and then disabling them in Register 0x1B. If they are not disabled, the charge-pump efficiency may suffer.
- If the CMP_IN phototransistor input is not used, it can be connected to ground or can remain floating.