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ANALOG DEVICES

Photometric Front End

Data Sheet **ADPD103**

FEATURES

- **Multifunction photometric front end**
- **Fully integrated AFE, ADC, LED drivers, and timing core**
- **Usable in a broad range of optical measurement applications, including photoplethysmography**
- **Enables best-in-class ambient light rejection capability without the need for photodiode optical filters**
- **Three 8 mA to 250 mA LED drivers**
- **Separate data registers for each LED/photodiode combination**
- **1 to 8 optical inputs**
- **Flexible, multiple, short LED pulses per optical sample**
- **20-bit burst accumulator enabling 20 bits per sample period**
- **On-board sample to sample accumulator, enabling up to 27 bits per data read**
- **Low power operation**
- **I^2C interface and 1.8 V analog/digital core**
- **Flexible sampling frequency ranging from 0.122 Hz to 3.820 kHz**
- **FIFO data operation**

APPLICATIONS

- **Body worn health and fitness monitors, for example, heart rate monitoring**
- **Clinical measurements, for example, SpO_2**
- **Industrial monitoring**
- **Background light measurements**

GENERAL DESCRIPTION

The ADPD103 is a highly efficient photometric front end with an integrated 14-bit analog-to-digital converter (ADC) and a 20-bit burst accumulator that works in concert with flexible light emitting diode (LED) drivers. It is designed to stimulate an LED and measure the corresponding optical return signal. The data output and functional configuration occur over a 1.8 V I^2C interface. The control circuitry includes flexible LED signaling and synchronous detection.

The analog front end (AFE) features best-in-class rejection of signal offset and corruption due to modulated interference commonly caused by ambient light.

Couple the ADPD103 with a low capacitance photodiode of <100 pF for optimal performance. The ADPD103 can be used with any LED.

Rev. B Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
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REVISION HISTORY

2/16—Revision B: Initial Version

FUNCTIONAL BLOCK DIAGRAM

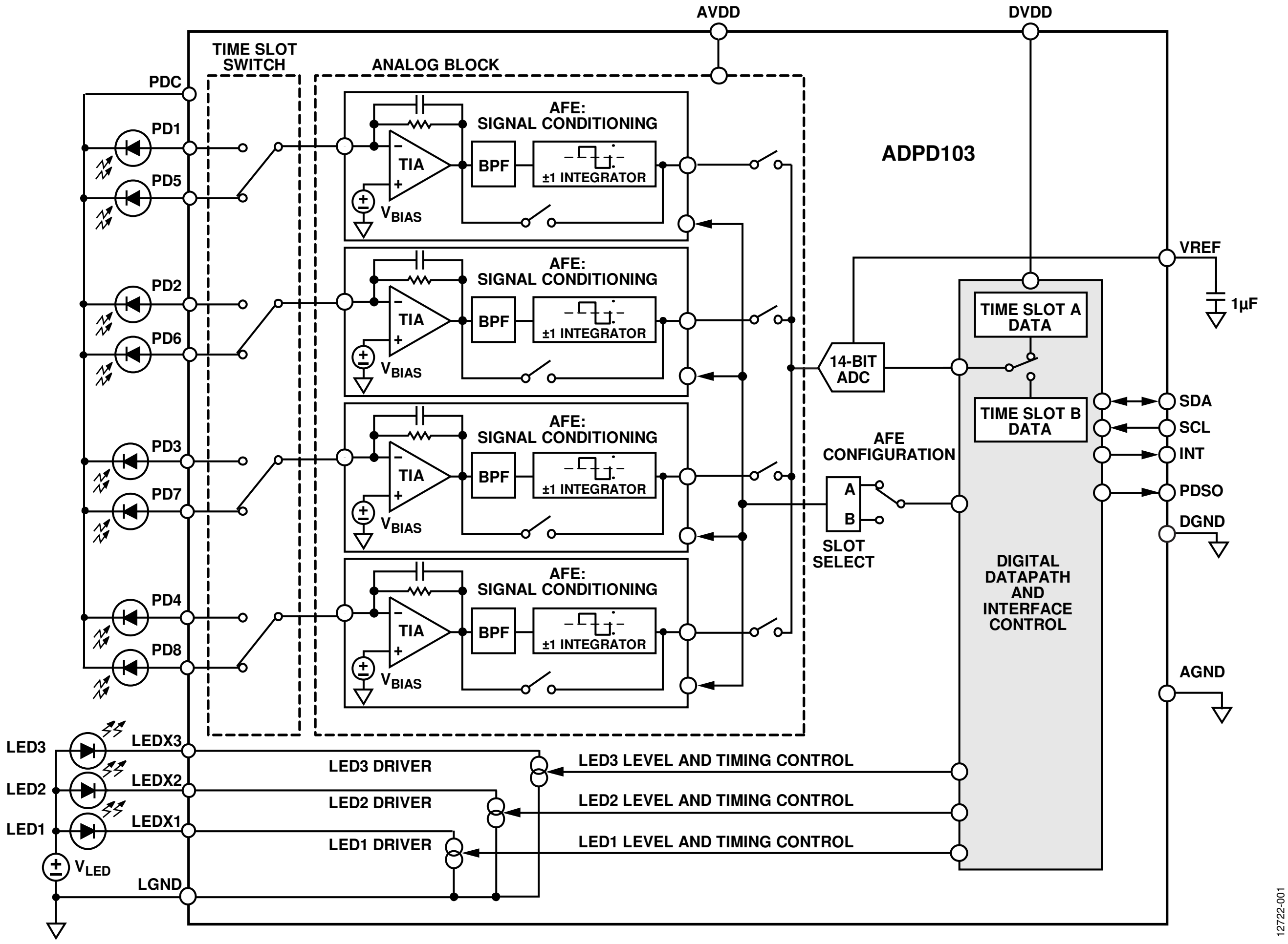


Figure 1. Typical Functional Block Diagram

SPECIFICATIONS

TEMPERATURE AND POWER SPECIFICATIONS

Table 1. Operating Conditions

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE RANGE					
Operating Range		−40		+85	°C
Storage Range		−65		+150	°C
POWER SUPPLY VOLTAGES					
V_{DD}	Applied at the AVDD and DVDD pins	1.7	1.8	1.9	V

AVDD = DVDD = 1.8 V, ambient temperature, unless otherwise noted.

Table 2. Current Consumption[1, 2]

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY (V_{DD}) CURRENT						
V_{DD} Supply Current		LED_OFFSET = 25 µs; LED_PERIOD =19 µs; LED peak current = 25 mA, 4 channels active				
1 Pulse		100 Hz data rate; Time Slot A only		106		µA
		100 Hz data rate; Time Slot B only		94		µA
		100 Hz data rate; both Time Slot A and Time Slot B		151		µA
10 Pulses		100 Hz data rate; Time Slot A only		258		µA
		100 Hz data rate; Time Slot B only		246		µA
		100 Hz data rate; both Time Slot A and Time Slot B		455		µA
Peak V_{DD} Supply Current (1.8 V)	IV_{DD_PEAK}					
4-Channel Operation				9.3		mA
1-Channel Operation				2.3		mA
Standby Mode Current	$IV_{DD\_STANDBY}$			3.5		µA
V_{LEDA} AND V_{LEDB} SUPPLY CURRENT						
Average Supply Current						
V_{LEDA} or V_{LEDB}		Peak LED current = 100 mA; LED_PULSE width = 3 µs				
1 Pulse		50 Hz data rate		15		µA
		100 Hz data rate		30		µA
		200 Hz data rate		60		µA
10 Pulses		50 Hz data rate		150		µA
		100 Hz data rate		300		µA
		200 Hz data rate		600		µA

[1] LEDA or LEDB is one of LED1, LED2, or LED3. V_{LEDA} or V_{LEDB} is one of V_{LED1}, V_{LED2}, or V_{LED3}.
[2] V_{DD} is the voltage applied at the AVDD and DVDD pins.

PERFORMANCE SPECIFICATIONS

AVDD = DVDD = 1.8 V, T_A = full operating temperature range, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DATA AQUISITION					
Resolution	Single pulse		14		Bits
Resolution/Sample	64 to 255 pulses		20		Bits
Resolution/Data Read	64 to 255 pulses and sample average = 128		27		Bits
LED DRIVER					
LED Current Slew Rate[1]					
Rise	Slew rate control setting = 0; T_A = 25°C; I_{LED} = 70 mA		240		mA/µs
	Slew rate control setting = 7; T_A = 25°C; I_{LED} = 70 mA		1400		mA/µs
Fall	Slew rate control setting = 0, 1, 2; T_A = 25°C; I_{LED} = 70 mA		3200		mA/µs
	Slew rate control setting = 6, 7; T_A = 25°C; I_{LED} = 70 mA		4500		mA/µs
LED Peak Current	LED pulse enabled	8		250	mA
Driver Compliance Voltage	Voltage above ground required for LED driver operation	0.2			V
LED PERIOD	AFE width = 4 µs	19			µs
	AFE width = 3 µs	17			µs
Sampling Frequency[2]	Time Slot A only; normal mode; 1 pulse; OFFSET_LEDA = 23 µs; PERIOD_LEDA = 19 µs	0.122		3230	Hz
	Time Slot B only; normal mode; 1 pulse; OFFSET_LEDA = 23 µs; PERIOD_LEDA = 19 µs	0.122		3820	Hz
	Both time slots; normal mode; 1 pulse; OFFSET_LEDA = 23 µs; PERIOD_LEDA = 19 µs	0.122		1750	Hz
	Time Slot A only; normal mode; 8 pulses; OFFSET_LEDA = 23 µs; PERIOD_LEDA = 19 µs	0.122		2257	Hz
	Time Slot B only; normal mode; 8 pulses; OFFSET_LEDA = 23 µs; PERIOD_LEDA = 19 µs	0.122		2531	Hz
	Both time slots; normal mode; 8 pulses; OFFSET_LEDA = 23 µs; PERIOD_LEDA = 19 µs	0.122		1193	Hz
CATHODE PIN (PDC) VOLTAGE					
During All Sampling Periods	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 1[3]		1.8		V
	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 0		1.3		V
During Slot A Sampling	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x0[3]		1.8		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x1		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x2		1.55		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x3[4]		0		V
During Slot B Sampling	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x0[3]		1.8		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x1		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x2		1.55		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x3[4]		0		V
During Sleep Periods	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 1		1.8		V
	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 0		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[13:12] = 0x0		1.8		V
	Register 0x54, Bit 7 = 0x1; Register 0x54[13:12] = 0x1		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54[13:12] = 0x2		1.55		V
	Register 0x54, Bit 7 = 0x1; Register 0x54[13:12] = 0x3		0		V
PHOTODIODE INPUT PINS/ ANODE VOLTAGE					
During All Sampling Periods			1.3		V
During Sleep Periods			Cathode voltage		V

[1] LED inductance is negligible for these values. The effective slew rate slows with increased inductance.
[2] The maximum values in this specification are the internal ADC sampling rates in normal mode. The I^2C read rates in some configurations may limit the actual output data rate of the device
[3] This mode may induce additional noise and is not recommended unless absolutely necessary. The 1.8 V setting uses V_{DD}, which contains greater amounts of differential voltage noise with respect to the anode voltage. A differential voltage between the anode and cathode injects a differential current across the capacitance of the photodiode of the magnitude C × dV/dt.
[4] This setting is not recommended for photodiodes because it causes a 1.3 V forward bias of the photodiode.

ANALOG SPECIFICATIONS

AVDD = DVDD = 1.8 V, T_A = full operating temperature range, unless otherwise noted. Compensation of the AFE offset is explained in the AFE Operation section.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CAPACITANCE				100	pF
PULSED SIGNAL CONVERSIONS, 3 µs WIDE LED PULSE[1]	4 µs wide AFE integration; normal operation, Register 0x43 (Time Slot A) and Register 0x45 (Time Slot B) = 0xADA5				
ADC Resolution[2]	Transimpedance amplifier (TIA) feedback resistor				
	25 kΩ		1.64		nA/LSB
	50 kΩ		0.82		nA/LSB
	100 kΩ		0.41		nA/LSB
	200 kΩ		0.2		nA/LSB
ADC Saturation Level	TIA feedback resistor				
	25 kΩ		13.4		µA
	50 kΩ		6.7		µA
	100 kΩ		3.35		µA
	200 kΩ		1.67		µA
Ambient Signal Headroom on Pulsed Signal	TIA feedback resistor				
	25 kΩ		37		µA
	50 kΩ		18.5		µA
	100 kΩ		9.25		µA
	200 kΩ		4.63		µA
PULSED SIGNAL CONVERSIONS, 2 µs WIDE LED PULSE[1]	3 µs wide AFE integration; normal operation, Register 0x43 (Time Slot A) and Register 0x45 (Time Slot B) = 0xADA5				
ADC Resolution[2]	TIA feedback resistor				
	25 kΩ		2.31		nA/LSB
	50 kΩ		1.15		nA/LSB
	100 kΩ		0.58		nA/LSB
	200 kΩ		0.29		nA/LSB
ADC Saturation Level	TIA feedback resistor				
	25 kΩ		18.9		µA
	50 kΩ		9.46		µA
	100 kΩ		4.73		µA
	200 kΩ		2.37		µA
Ambient Signal Headroom on Pulsed Signal	TIA feedback resistor				
	25 kΩ		31.5		µA
	50 kΩ		15.7		µA
	100 kΩ		7.87		µA
	200 kΩ		3.93		µA
FULL SIGNAL CONVERSIONS[3]					
TIA Saturation Level of Pulsed Signal and Ambient Level	TIA feedback resistor				
	25 kΩ		50.4		µA
	50 kΩ		25.2		µA
	100 kΩ		12.6		µA
	200 kΩ		6.3		µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYSTEM PERFORMANCE					
Total Output Noise Floor	Normal mode; per pulse; per channel; no LED; C_{PD} = 70 pF				
	25 kΩ; referred to ADC input		2.0		LSB rms
	25 kΩ; referred to peak input signal for 2 µs LED pulse		4.6		nA rms
	25 kΩ; referred to peak input signal for 3 µs LED pulse		3.3		nA rms
	25 kΩ; saturation signal-to-noise ratio (SNR) per pulse per channel[4]		72.3		dB
	50 kΩ; referred to ADC input		2.4		LSB rms
	50 kΩ; referred to peak input signal for 2 µs LED pulse		2.8		nA rms
	50 kΩ; referred to peak input signal for 3 µs LED pulse		2.0		nA rms
	50 kΩ; saturation SNR per pulse per channel[4]		70.6		dB
	100 kΩ; referred to ADC input		3.4		LSB rms
	100 kΩ; referred to peak input signal for 2 µs LED pulse		1.9		nA rms
	100 kΩ; referred to peak input signal for 3 µs LED pulse		1.4		nA rms
	100 kΩ; saturation SNR per pulse per channel[4]		67.6		dB
	200 kΩ; referred to ADC input		5.5		LSB rms
	200 kΩ; referred to peak input signal for 2 µs LED pulse		1.6		nA rms
	200 kΩ; referred to peak input signal for 3 µs LED pulse		1.1		nA rms
	200 kΩ; saturation SNR per pulse per channel[4]		63.5		dB
DC Power Supply Rejection Ratio (DC PSRR)			−37		dB

[1] This saturation level applies to the ADC only and, therefore, includes only the pulsed signal. Any nonpulsatile signal is removed prior to the ADC stage.
[2] ADC resolution is listed per pulse when the AFE offset is correctly compensated per the AFE Operation section. If using multiple pulses, divide by the number of pulses.
[3] This saturation level applies to the full signal path and, therefore, includes both the ambient signal and the pulsed signal.
[4] The noise term of the saturation SNR value refers to the receive noise only and does not include photon shot noise or any noise on the LED signal itself.

DIGITAL SPECIFICATIONS

DVDD = 1.7 V to 1.9 V, unless otherwise noted.

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS (SCL, SDA)						
Input Voltage Level						
High	V_{IH}		0.7 × DVDD		3.6	V
Low	V_{IL}				0.3 × DVDD	V
Input Current Level						
High	I_{IH}		−10		+10	µA
Low	I_{IL}		−10		+10	µA
Input Capacitance	C_{IN}			10		pF
LOGIC OUTPUTS						
INT Output Voltage Level						
High	V_{OH}	2 mA high level output current	DVDD − 0.5			V
Low	V_{OL}	2 mA low level output current			0.5	V
PDSO Output Voltage Level						
High	V_{OH}	2 mA high level output current	DVDD − 0.5			V
Low	V_{OL}	2 mA low level output current			0.5	V
SDA Output Voltage Level						
Low	V_{OL1}	2 mA low level output current			0.2 × DVDD	V
SDA Output Current Level						
Low	I_{OL}	V_{OL1} = 0.6 V	6			mA

TIMING SPECIFICATIONS

Table 6. I²C Timing Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
I²C PORT[1]		See Figure 2				
SCL						
Frequency				400		kHz
Minimum Pulse Width						
High	t_1		600			ns
Low	t_2		1300			ns
Start Condition						
Hold Time	t_3		600			ns
Setup Time	t_4		600			ns
SDA Setup Time	t_5		100			ns
SCL and SDA						
Rise Time	t_6				1000	ns
Fall Time	t_7				300	ns
Stop Condition						
Setup Time	t_8		600			ns

[1] Guaranteed by design.

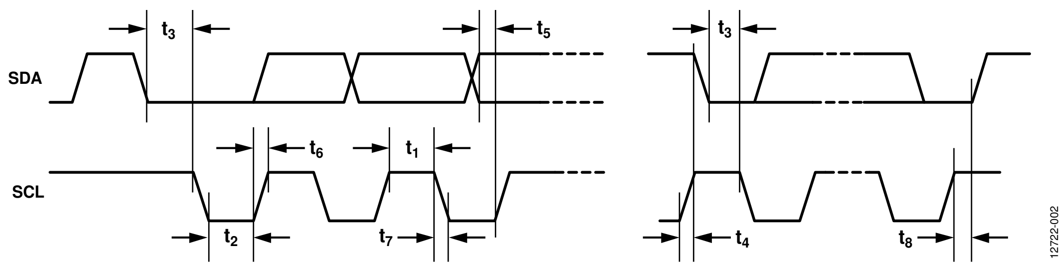


Figure 2. I²C Timing

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
AVDD to AGND	−0.3 V to +2.2 V
DVDD to DGND	−0.3 V to +2.2 V
INT to DGND	−0.3 V to +2.2 V
PDSO to DGND	−0.3 V to +2.2 V
LEDXx to LGND	−0.3 V to +3.6 V
SCL to DGND	−0.3 V to +3.9 V
SDA to DGND	−0.3 V to +3.9 V
Junction Temperature	150°C
ESD	
28-Lead LFCSP	
Human Body Model (HBM)	1500 V
Charge Device Model (CDM)	1250 V
Machine Model (MM)	100 V
16-Ball WLCSP	
Human Body Model (HBM)	1500 V
Charge Device Model (CDM)	500 V
Machine Model (MM)	100 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 8. Thermal Resistance

Package Type	θ_{JA}	Unit
28-Lead LFCSP_WQ	54.9	°C/W
16-Ball WLCSP	60	°C/W

RECOMMENDED SOLDERING PROFILE

Figure 3 and Table 9 provide details about the recommended soldering profile.

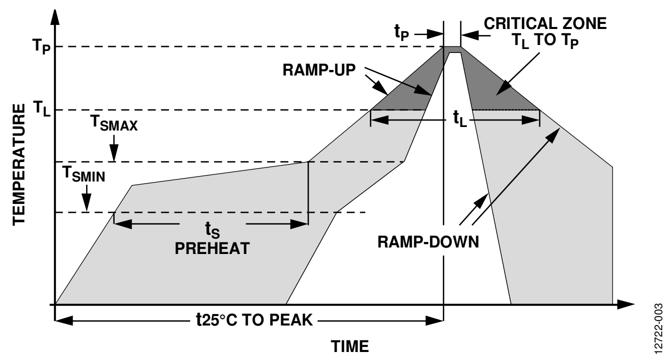
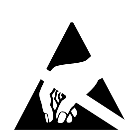


Figure 3. Recommended Soldering Profile

Table 9. Recommended Soldering Profile

Profile Feature	Condition (Pb-Free)
Average Ramp Rate (T_L to T_P)	3°C/sec max
Preheat	
Minimum Temperature (T_{SMIN})	150°C
Maximum Temperature (T_{SMAX})	200°C
Time (T_{SMIN} to T_{SMAX}) (t_S)	60 sec to 180 sec
T_{SMAX} to T_L Ramp-Up Rate	3°C/sec maximum
Time Maintained Above Liquidous Temperature	
Liquidous Temperature (T_L)	217°C
Time (t_L)	60 sec to 150 sec
Peak Temperature (T_P)	+260 (+0/−5)°C
Time Within 5°C of Actual Peak Temperature (t_P)	<30 sec
Ramp-Down Rate	6°C/sec maximum
Time from 25°C to Peak Temperature	8 minutes maximum

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

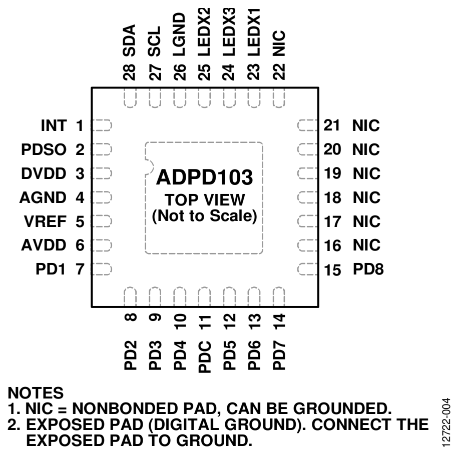


Figure 4. 28-Lead LFCSP Pin Configuration

Table 10. 28-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	INT	DO	Interrupt Output.
2	PDSO	DO	Power-Down Status Output.
3	DVDD	S	1.8 V Digital Supply.
4	AGND	S	Analog Ground.
5	VREF	REF	Internally Generated ADC Voltage Reference. Buffer this pin with a 1 μF capacitor to AGND.
6	AVDD	S	1.8 V Analog Supply.
7	PD1	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
8	PD2	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
9	PD3	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
10	PD4	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
11	PDC	AO	Photodiode Common Cathode Bias.
12	PD5	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
13	PD6	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
14	PD7	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
15	PD8	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
16 to 22	NIC	R	Not Internally Connected (Nonbonded Pad). This pin can be grounded.
23	LEDX1	AO	LED Driver 1 Current Sink. If not in use, leave this pin floating.
24	LEDX3	AO	LED Driver 3 Current Sink. If not in use, leave this pin floating.
25	LEDX2	AO	LED Driver 2 Current Sink. If not in use, leave this pin floating.
26	LGND	S	LED Driver Ground.
27	SCL	DI	I^2C Clock Input.
28	SDA	DIO	I^2C Data Input/Output.
	EPAD (DGND)	S	Exposed Pad (Digital Ground). Connect the exposed pad to ground.

[1] DO means digital output, S means supply, REF means voltage reference, AI means analog input, AO means analog output, R means reserved, DI means digital input, and DIO means digital input/output.

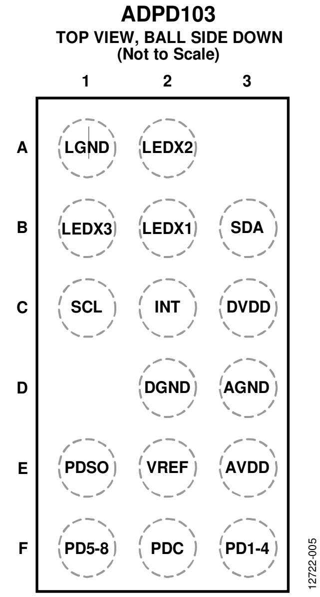


Figure 5. 16-Ball WLCSP Pin Configuration

Table 11. 16-Ball WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1	LGND	S	LED Driver Ground.
A2	LEDX2	AO	LED Driver 2 Current Sink. If not in use, leave this pin floating.
B1	LEDX3	AO	LED Driver 3 Current Sink. If not in use, leave this pin floating.
B2	LEDX1	AO	LED Driver 1 Current Sink. If not in use, leave this pin floating.
B3	SDA	DIO	I^2C Data Input/Output.
C1	SCL	S	I^2C Clock Input.
C2	INT	DO	Interrupt Output.
C3	DVDD	S	1.8 V Digital Supply.
D2	DGND	S	Digital Ground.
D3	AGND	S	Analog Ground.
E1	PDSO	DO	Power-Down Status Output.
E2	VREF	REF	Internally Generated ADC Voltage Reference. Buffer this pin with a 1 µF capacitor to AGND.
E3	AVDD	S	1.8 V Analog Supply.
F1	PD5-8	AI	Photodiode Combined Current Input of PD5 to PD8. If not in use, leave this pin floating.
F2	PDC	AO	Photodiode Common Cathode Bias.
F3	PD1-4	AI	Photodiode Combined Current Input of PD1 to PD4. If not in use, leave this pin floating.

[1] S means supply, AO means analog output, DIO means digital input/output, DO means digital output, REF means voltage reference, and AI means analog input.

TYPICAL PERFORMANCE CHARACTERISTICS

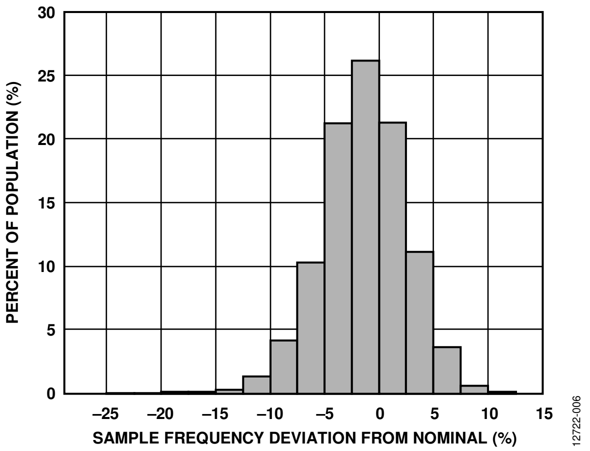


Figure 6. 32 kHz Clock Frequency Distribution (Default Settings, Before User Calibration: Register 0x4B = 0x2612)

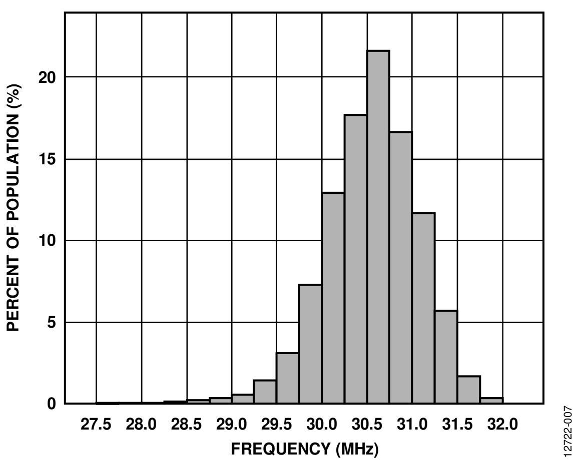


Figure 7. 32 MHz Clock Frequency Distribution (Default Settings, Before User Calibration: Register 0x4D = 0x425E)

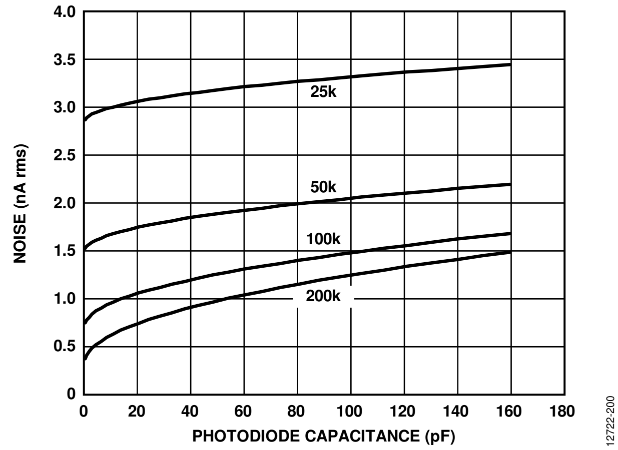


Figure 8. Input Referred Noise vs. Photodiode Capacitance, LED Pulse Width = 3 μs

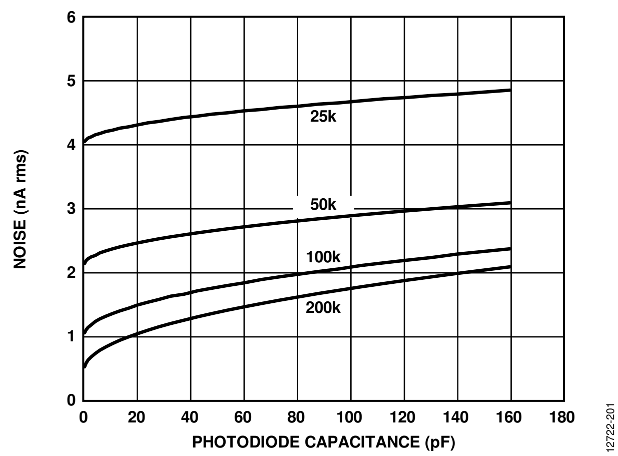


Figure 9. Input Referred Noise vs. Photodiode Capacitance, LED Pulse Width = 2 μs

THEORY OF OPERATION

INTRODUCTION

The ADPD103 operates as a complete optical transceiver stimulating up to three LEDs and measuring the return signal on up to eight separate current inputs. The core consists of a photometric front end coupled with an ADC, digital block, and three independent LED drivers. The core circuitry stimulates the LEDs and measures the return in the analog block through one to eight photodiode inputs, storing the results in discrete data locations. The eight inputs are broken into two blocks of four simultaneous input channels. Data can be read directly by a register, or through a FIFO. This highly integrated system includes an analog signal processing block, digital signal processing block, I²C communication interface, and programmable pulsed LED current sources.

The LED driver is a current sink and is agnostic to LED supply voltage and LED type. The photodiode (PDx) inputs can accommodate any photodiode with an input capacitance of less than 100 pF. The ADPD103 is purposefully designed to produce a high SNR for relatively low LED power while greatly reducing the effect of ambient light on the measured signal.

DUAL TIME SLOT OPERATION

The ADPD103 operates in two independent time slots, Time Slot A and Time Slot B, which are carried out sequentially. The entire signal path from LED stimulation to data capture and processing is executed during each time slot. Each time slot has a separate datapath that uses independent settings for the LED driver, AFE setup, and the resulting data. Time Slot A and Time Slot B operate in sequence for every sampling period, as shown in Figure 10.

The timing parameters are defined as follows:

$$t_A\ (\mu s) = SLOTA\_LED\_OFFSET + n_A \times SLOTA\_LED\_PERIOD$$

where n_A is the number of pulses for Time Slot A (Register 0x31, Bits[15:8]).

$$t_B\ (\mu s) = SLOTB\_LED\_OFFSET + n_B \times SLOTB\_LED\_PERIOD$$

where n_B is the number of pulses for Time Slot B (Register 0x36, Bits[15:8]).

Calculate the LED period using the following equation:

$$LED\_PERIOD,\ minimum = 2 \times AFE\_WIDTH + 11$$

t_1 and t_2 are fixed and based on the computation time for each slot. If a slot is not in use, these times do not add to the total active time. Table 12 defines the values for these LED and sampling time parameters.

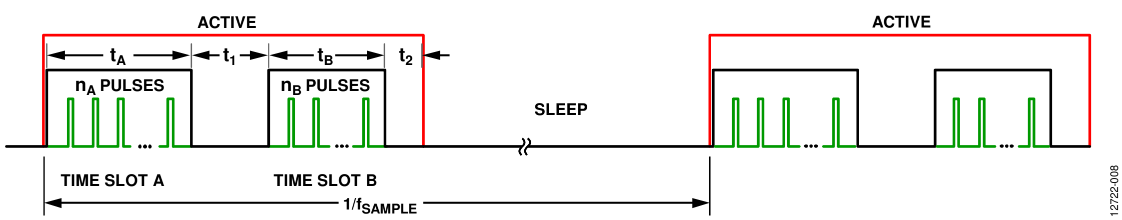


Figure 10. Time Slot Timing Diagram

Table 12. LED Timing and Sample Timing Parameters

Parameter	Register	Bits	Test Conditions/Comments	Min	Typ	Max	Unit
SLOTA_LED_OFFSET[1]	0x30	[7:0]	Delay from power-up to LEDA rising edge	23		63	µs
SLOTB_LED_OFFSET[1]	0x35	[7:0]	Delay from power-up to LEDB rising edge	23		63	µs
SLOTA_LED_PERIOD[2]	0x31	[7:0]	Time between LED pulses in Time Slot A; SLOTx_AFE_WIDTH = 4 µs	19		63	µs
SLOTB_LED_PERIOD[2]	0x36	[7:0]	Time between LED pulses in Time Slot B; SLOTx_AFE_WIDTH = 4 µs	19		63	µs
t_1			Compute time for Time Slot A		68		µs
t_2			Compute time for Time Slot B		20		µs
t_{SLEEP}			Sleep time between sample periods	222			µs

[1] Setting the SLOTx_LED_OFFSET below the specified minimum value may cause failure of ambient light rejection for large photodiodes.
[2] Setting the SLOTx_LED_PERIOD below the specified minimum value can cause invalid data captures.

TIME SLOT SWITCH

Up to eight photodiodes (PD1 to PD8) can be connected to the ADPD103. The photodiode anodes are connected to the PD1 to PD8 input pins; the photodiode cathodes are connected to the cathode pin, PDC. The anodes are assigned in three different configurations depending on the settings of Register 0x14 (see Figure 11, Figure 12, and Figure 13).

A switch sets which photodiode group is connected during Time Slot A and Time Slot B. See Table 13 for the time slot switch registers. When using less than eight photodiodes, it is important to leave the unused inputs floating for proper operation of the device. The photodiode inputs are current inputs and as such, these pins are also considered to be voltage outputs. Tying these inputs to a voltage may saturate the analog block.

Register 0x14, PD1 to PD8 Input Configurations

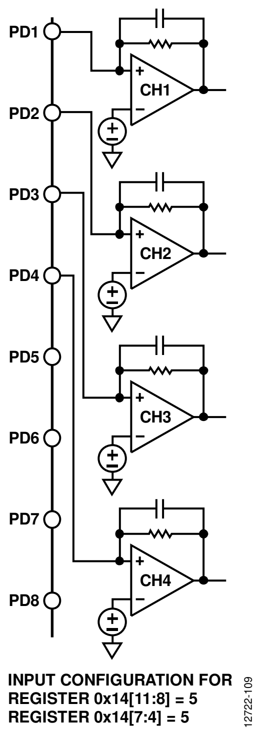


Figure 11. PD1 to PD4 Connection

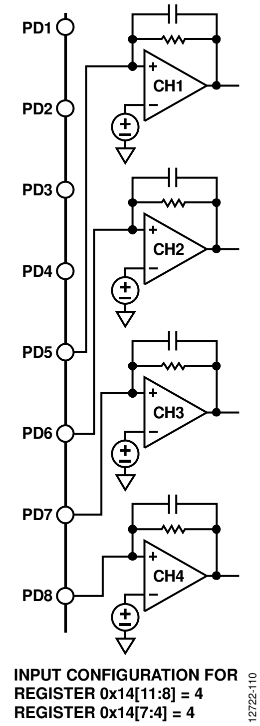


Figure 12. PD5 to PD8 Connection

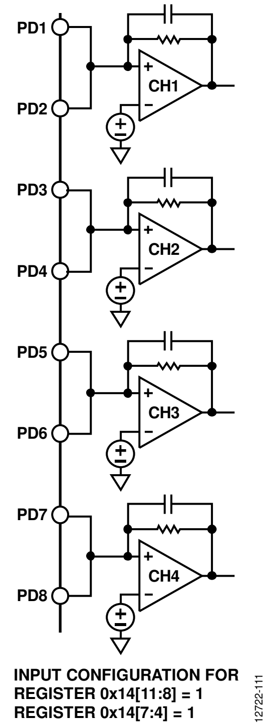


Figure 13. 2-to-1 PD Current Summation

Table 13. Time Slot Switch (Register 0x14)

Address	Bits	Name	Description
0x14	[11:8]	SLOTB_PD_SEL	Selects connection of photodiode for Time Slot B as shown in Figure 11, Figure 12, and Figure 13. 0x0: inputs are floating in Time Slot B. 0x1: all PDx pins (PD1 to PD8) are connected during Time Slot B. 0x4: PD5 to PD8 are connected during Time Slot B. 0x5: PD1 to PD4 are connected during Time Slot B. Other: reserved.
	[7:4]	SLOTA_PD_SEL	Selects connection of photodiode for Time Slot A as shown in Figure 11, Figure 12, and Figure 13. 0x0: inputs are floating in Time Slot A. 0x1: All PDx pins (PD1 to PD8) are connected during Time Slot A. 0x4: PD5 to PD8 are connected during Time Slot A. 0x5: PD1 to PD4 are connected during Time Slot A. Other: reserved.

ADJUSTABLE SAMPLING FREQUENCY

Register 0x12 controls the sampling frequency setting of the ADPD103 and Register 0x4B, Bits[5:0] further tunes this clock for greater accuracy. The sampling frequency is governed by an internal 32 kHz sample rate clock that also drives the transition of the internal state machine. The maximum sampling frequencies for some sample conditions are listed in Table 3. The maximum sample frequency for all conditions is determined by the following equation:

$$f_{SAMPLE,\ MAX} = 1/(t_A + t_1 + t_B + t_2 + t_{SLEEP,\ MIN})$$

If a given time slot is not in use, elements from that time slot do not factor into the calculation. For example, if Time Slot A is not in use, t_A and t_1 do not add to the sampling period and the new maximum sampling frequency is calculated as follows:

$$f_{SAMPLE,\ MAX} = 1/(t_B + t_2 + t_{SLEEP,\ MIN})$$

where $t_{SLEEP,\ MIN}$ is the minimum sleep time required between samples. See the Dual Time Slot Operation section for the definitions of t_A, t_1, t_B, and t_2.

External Sync for Sampling

The ADPD103 provides an option to use an external sync signal to trigger the sampling periods. This external sample sync signal can be provided either on the INT pin or the PDSO pin. This functionality is controlled by Register 0x4F, Bits[3:2]. When enabled, a rising edge on the selected input specifies when the next sample cycle occurs. When triggered, there is a delay of one to two internal sampling clock (32 kHz) cycles, and then the normal start-up sequence occurs. This sequence is the same as if the normal sample timer provided the trigger. To enable the external sync signal feature, use the following procedure:

1. Write 0x1 to Register 0x10 to enter program mode.
2. Write the appropriate value to Register 0x4F, Bits[3:2] to select whether the INT pin or the PDSO pin specifies when the next sample cycle occurs. Also, enable the appropriate input buffer using Register 0x4F, Bit 1, for the INT pin, or Register 0x4F, Bit 5, for the PDSO pin.
3. Write b1 to EXT_SYNC_ENA, Register 0x38, Bit 14 to enable the external sampling trigger.
4. Write 0x2 to Register 0x10 to start the sampling operations.
5. Apply the external sync signal on the selected pin at the desired rate; sampling occurs at that rate. As with normal sampling operations, read the data using the FIFO or the data registers.

The maximum frequency constraints also apply in this case.

Providing an External 32kHz Clock

The ADPD103 has an option for the user to provide an external 32 kHz clock to the device for system synchronization or for situations where a clock with better accuracy than the internal 32 kHz clock is required. The external 32 kHz clock is provided on the PDSO pin. To enable the 32 kHz external clock, use the following procedure at startup:

1. Drive the PDSO pin to a valid logic level or with the desired 32 kHz clock prior to enabling the PDSO pin as an input. Do not leave the pin floating prior to enabling it.
2. Write b1 to Register 0x4F, Bit 5 to enable the PDSO pin as an input.
3. Write b11 to register 0x4B, Bit 7 and Bit 8 (CLK32K_EN and CLK32K_BYP, respectively) to configure the device to use an external 32 kHz clock.
4. Write 0x1 to Register 0x10 to enter program mode.
5. Write additional control registers in any order while the device is in program mode to configure the device as required.
6. Write 0x2 to Register 0x10 to start the normal sampling operation.

STATE MACHINE OPERATION

During each time slot, the ADPD103 operates according to a state machine. The state machine operates in the following sequence, shown in Figure 14.

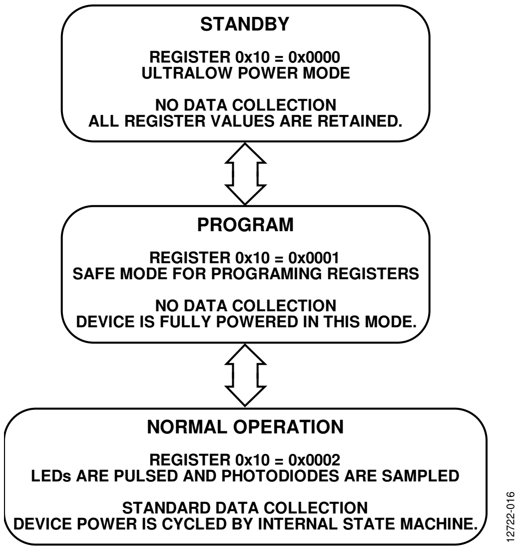


Figure 14. State Machine Operation Flowchart

The ADPD103 operates in one of three modes: standby, program, and normal sampling mode.

Standby mode is a power saving mode in which no data collection occurs. All register values are retained in this mode. To place the device in standby mode, write 0x0 to Register 0x10, Bits[1:0]. The device powers up in standby mode.

Program mode is used for programming registers. Always cycle the ADPD103 through program mode when writing registers or changing modes. Because no power cycling occurs in this mode, the device may consume higher current in program mode than in normal operation. To place the device in program mode, write 0x1 to Register 0x10, Bits[1:0].

In normal operation, the ADPD103 pulses light and collects data. Power consumption in this mode depends on the pulse count and data rate. To place the device in normal sampling mode, write 0x2 to Register 0x10, Bits[1:0].

NORMAL MODE OPERATION AND DATA FLOW

In normal mode, the ADPD103 follows a specific pattern set up by the state machine. This pattern is shown in the corresponding data flow in Figure 15. The pattern is as follows:

1. LED pulse and sample.The ADPD103 pulses external LEDs. The response of a photodiode or photodiodes to the reflected light is measured by the ADPD103. Each data sample is constructed from the sum of n individual pulses, where n is user configurable between 1 and 255.
2. Intersample averaging. If desired, the logic can average n samples, from 2 to 128 in powers of 2, to produce output data. New output data is saved to the output registers every N samples.
3. Data read. The host processor reads the converted results from the data register or the FIFO.
4. Repeat. The sequence has a few different loops that enable different types of averaging while keeping both time slots close in time relative to each other.

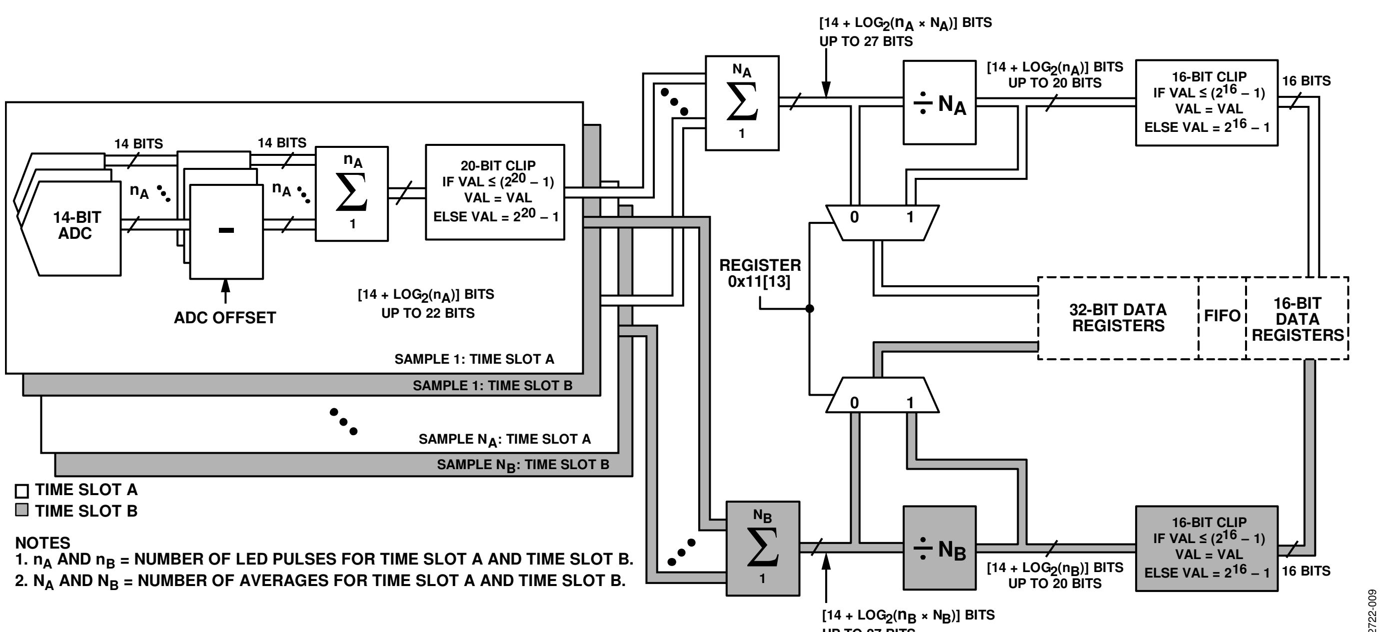


Figure 15. ADPD103 Datapath

LED Pulse and Sample

At each sampling period, the selected LED driver drives a series of LED pulses, as shown in Figure 16. The magnitude, duration, and number of pulses are programmable over the I²C interface. Each LED pulse coincides with a sensing period so that the sensed value represents the total charge acquired on the photodiode in response to only the corresponding LED pulse. Charge, such as ambient light, that does not correspond to the LED pulse is rejected.

After each LED pulse, the photodiode output relating the pulsed LED signal is sampled and converted to a digital value by the 14-bit ADC. Each subsequent conversion within a sampling period is summed with the previous result. Up to 255 pulse values from the ADC can be summed in an individual sampling period. There is a 20-bit maximum range for each sampling period.

Averaging

The ADPD103 offers sample accumulation and averaging functionality to increase signal resolution.

Within a sampling period, the AFE can sum up to 256 sequential pulses. As shown in Figure 15, samples acquired by the AFE are clipped to 20 bits at the output of the AFE. Additional resolution, up to 27 bits, can be achieved by averaging between sampling periods. This accumulated data of N samples is stored as 27-bit values and can be read out directly by using the 32-bit output registers or the 32-bit FIFO configuration.

When using the averaging feature set up by the register, subsequent pulses can be averaged by powers of 2. The user can select from 2, 4, 8 … up to 128 samples to be averaged. Pulse data is still acquired by the AFE at the sampling frequency, f_{SAMPLE} (Register 0x12), but new data is written to the registers at the rate of f_{SAMPLE}/N every N^{th} sample. This new data consists of the sum of the previous N samples. The full 32-bit sum is stored in the 32-bit registers. However, before sending this data to the FIFO, a divide by N operation occurs. This divide operation maintains bit depth to prevent clipping on the FIFO.

Use this between sample averaging to lower the noise while maintaining 16-bit resolution. If the pulse count registers are kept to 8 or less, the 16-bit width is never exceeded. Therefore, when using Register 0x15 to average subsequent pulses, many pulses can be accumulated without exceeding the 16-bit word width. This can reduce the number of FIFO reads required by the host processor.

Data Read

The host processor reads output data from the ADPD103, via the I²C protocol, from the data registers or from the FIFO. New output data is made available every N samples, where N is the user configured averaging factor. The averaging factors for Time Slot A and Time Slot B are configurable independently of each other. If they are the same, both time slots can be configured to save data to the FIFO. If the two averaging factors are different, only one time slot can save data to the FIFO; data from the other time slot can be read from the output registers.

The data read operations are described in more detail in the Reading Data section.

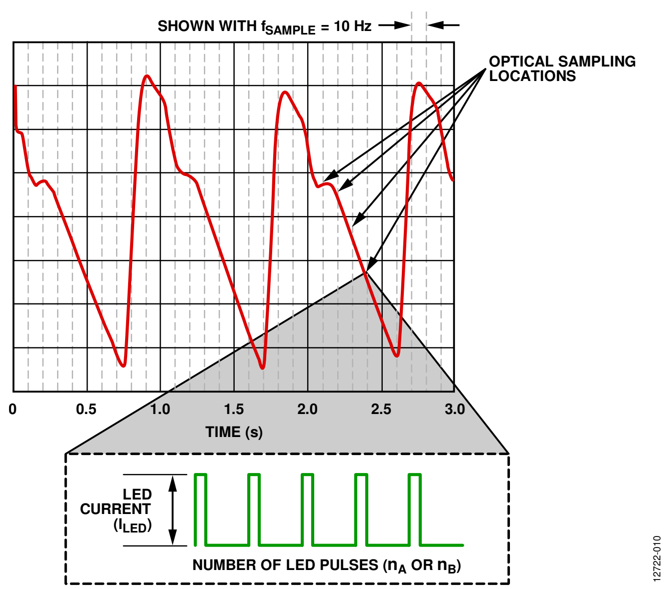


Figure 16. Example of a Photoplethysmography (PPG) Signal Sampled at a Data Rate of 10 Hz Using Five Pulses per Sample

AFE OPERATION

The timing within each pulse burst is important for optimizing the operation of the ADPD103. Figure 17 shows the timing waveforms for a single time slot as an LED pulse response propagates through the analog block of the AFE. The first graph, shown in green, shows the ideal LED pulsed output. The filtered LED response, shown in blue, shows the output of the analog integrator. The third graph, shown in orange, illustrates an optimally placed integration window. When programmed to the optimized value, the full signal of the filtered LED response can be integrated. The AFE integration window is then applied to the output of the bandpass filter (BPF) and the result is sent to the ADC and summed for N pulses. If the AFE window is not correctly sized or located, all of the receive signal is not properly reported and system performance is not optimal; therefore, it is important to verify proper AFE position for every new hardware design or the LED width.

AFE INTEGRATION OFFSET ADJUSTMENT

The AFE integration width must be equal or larger than the LED width. As AFE width increases, the output noise increases and the ability to suppress high frequency content from the environment decreases. It is therefore desirable to keep the AFE integration width small. However, if the AFE width is too small, the LED signal is attenuated. With most hardware selections, the AFE width produces the optimal SNR at 1 µs more than the LED width. After setting LED width, LED offset, and AFE width, the ADC offset can then be optimized. The AFE offset must be manually set such that the falling edge of the first segment of the integration window matches the zero crossing of the filtered LED response.

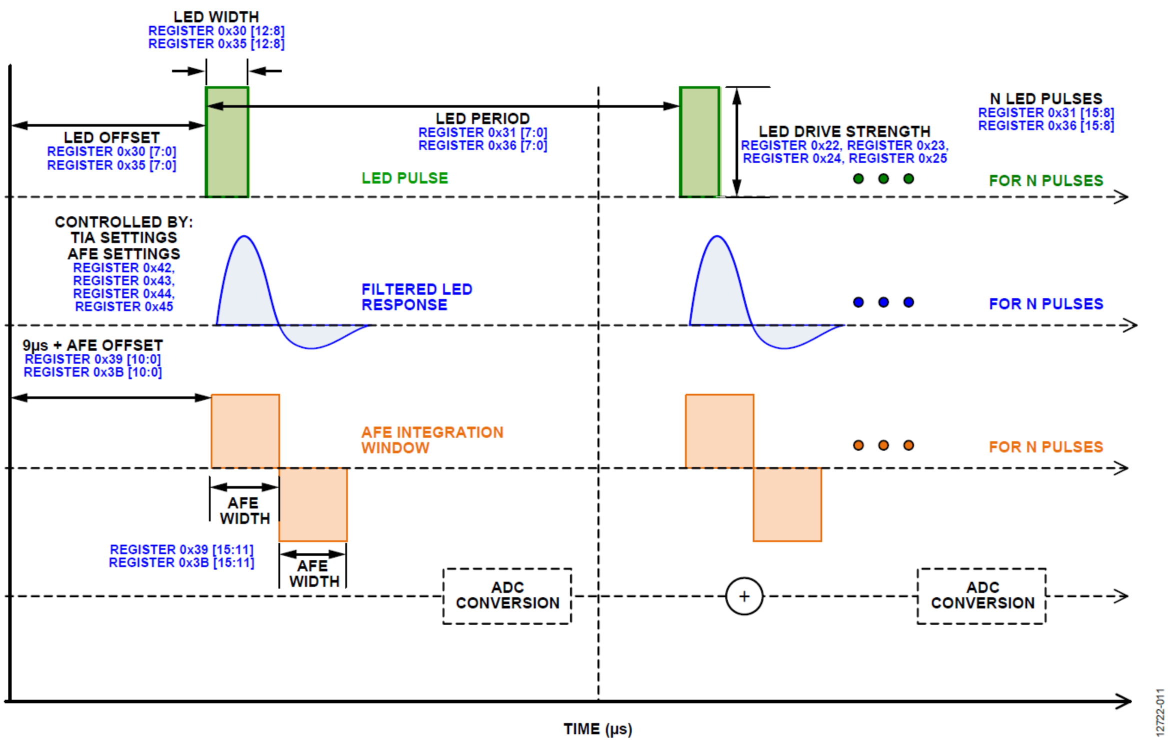


Figure 17. AFE Operation Diagram

AFE Integration Offset Starting Point

The starting point of this offset, as expressed in microseconds, is set such that the falling edge of the integration window aligns with the falling edge of the LED.

LED_FALLING_EDGE = LED_OFFSET + LED_WIDTH

and,

AFE_INTEGRATION_FALLING_EDGE = 9 + AFE_OFFSET + AFE_WIDTH

If both falling edges are set equal to each other, solve for AFE_OFFSET to obtain the following equation:

AFE_OFFSET_STARTING_POINT = LED_OFFSET + LED_WIDTH − 9 − AFE_WIDTH

Setting the AFE offset to any point in time earlier than the starting point is equivalent to setting the integration in the future; the AFE cannot integrate the result from an LED pulse that has not yet occurred. As a result, an AFE_OFFSET value less than the AFE_OFFSET_STARTING_POINT is an erroneous setting. Such a result may indicate that current in the TIA is operating in the reverse direction from the intended schematic, where the LED pulse is causing the current to leave the TIA rather than enter it.

Because, for most setups, the AFE_WIDTH is 1 μs wider than the LED_WIDTH, the AFE_OFFSET_STARTING_POINT value is typically 10 μs less than the LED_OFFSET value. Any value less than LED_OFFSET − 10 is erroneous. The optimal AFE offset is some time after the AFE_OFFSET_STARTING_POINT. The band-pass filter response, LED response, and photodiode response each add some delay. In general, the component choice, board layout, LED_OFFSET, and LED_WIDTH are the variables that can change the AFE_OFFSET. After a specific design is set, the AFE_OFFSET can be locked down and does not need to be optimized further.

Sweeping the AFE Position

The AFE offsets for Time Slot A and Time Slot B are controlled by Bits[10:0] of Register 0x39 and Register 0x3B, respectively. Each LSB represents one cycle of the 32 MHz clock, or 31.25 ns. The register can be thought of as 2^{11-1} of these 31.25 ns steps, or it can be broken into an AFE_COARSE setting using Bits[10:5] to represent 1 μs steps and Bits[4:0] to represent 31.25 ns steps. Sweeping the AFE position from the starting point to find a local maximum is the recommended way to optimize the AFE offset. The setup for this test is to allow the LED light to fall on the photodiode in a static way. This is typically done with a reflecting surface at a fixed distance. The AFE position can then be swept to look for changes in the output level. When adjusting the AFE position, it is important to sweep the position using the 31.25 ns steps. Typically, a local maximum is found within 2 μs of the starting point for most systems. Figure 18 shows an example of an AFE sweep, where 0 on the x-axis represents the AFE starting point defined previously. Each data point in the plot corresponds to one 31.25 ns step of the AFE_OFFSET. The optimal location for AFE_OFFSET in this example is 0.687 μs from the AFE starting point.

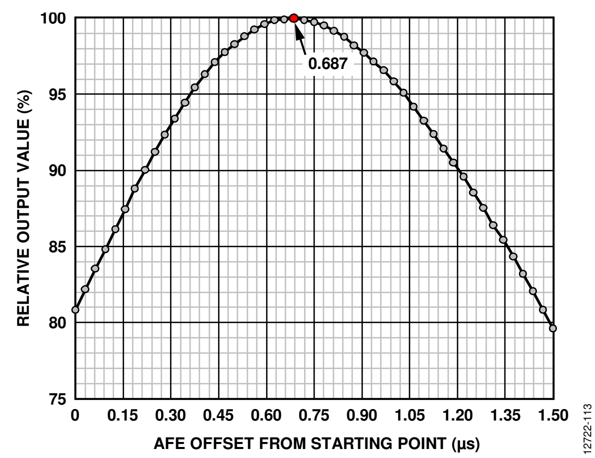


Figure 18. AFE Sweep Example

Table 14 lists some typical LED and AFE values after optimization. In general, it is not recommended to use the AFE_OFFSET numbers in Table 14 without first verifying them against the AFE sweep method. Repeat this method for every new LED width and with every new set of hardware made with the ADPD103. For maximum accuracy, it is recommended that the 32 MHz clock be calibrated prior to sweeping the AFE.

Table 14. AFE Window Settings

LED Register 0x30 or Register 0x35	AFE Register 0x39 or Register 0x3B	Comment
0x0219	0x19FB	2 μs LED pulse, 3 μs AFE width, 25 μs LED delay
0x0319	0x21F4	3 μs LED pulse, 4 μs AFE width, 25 μs LED delay

I²C SERIAL INTERFACE

The ADPD103 supports an I²C serial interface via the SDA (data) and SCL (clock) pins. All internal registers are accessed through the I²C interface.

The ADPD103 conforms to the *UM10204 I²C-Bus Specification and User Manual*, Rev. 05—9 October 2012, available from NXP Semiconductors. It supports a fast mode (400 kbps) data transfer. Register read and write are supported, as shown in Figure 19. Figure 2 shows the timing diagram for the I²C interface.

Slave Address

The default 7-bit I²C slave address for the device is 0x64, followed by the R/$\overline{W}$ bit. For a write, the default I²C slave address is 0xC8; for a read, the default I²C address is 0xC9. The slave address is configurable by writing to Register 0x09, Bits[7:1]. When multiple ADPD103 devices are on the same bus lines, the INT and PDSO pins can be used to select specific devices for the address change. Register 0x0D can be used to select a key to enable address changes in specific devices. Use the following procedure to change the slave address when multiple ADPD103 devices are connected to the same I²C bus lines:

1. Using Register 0x4F, enable the input buffer of the PDSO pin, the INT pin, or both, depending on the key being used.
2. For the device identified as requiring an address change, set the INT and/or PDSO pins high or low to match the key being used.
3. Write the SLAVE_ADDRESS_KEY using Register 0x0D, Bits[15:0] to match the desired function. The allowed keys are shown in Table 24.
4. Write the desired SLAVE_ADDRESS using Register 0x09, Bits[7:1]. While writing to Register 0x09, Bits[7:1], write 0xAD to Register 0x09, Bit[15:8]. Register 0x09 must be written to immediately after writing to Register 0x0D.
5. Repeat Step 1 to Step 4 for all the devices that need the SLAVE_ADDRESS changed.
6. Set the INT and PDSO pins as desired for normal operation using the new SLAVE_ADDRESS for each device.

I²C Write and Read Operations

Figure 19 illustrates the ADPD103 I²C write and read operations. Single word and multiword read operations are supported. For a single register read, the host sends a no acknowledge after the second data byte is read and a new register address is needed for each access.

For multiword operations, each pair of data bytes is followed by an acknowledge from the host until the last byte of the last word is read. The host indicates the last read word by sending a no acknowledge. When reading from the FIFO (Register 0x60), the data is automatically advanced to the next word in the FIFO and the space is freed. When reading from other registers, the register address is automatically advanced to the next register, except at Register 0x5F or Register 0x7F, where the address does not increment. This allows lower overhead reading of sequential registers.

All register writes are single word only and require 16 bits (one word) of data.

The software reset (Register 0x0F, Bit 0) is the only command that does not return an acknowledge because the command is instantaneous.

Table 15. Definition of I²C Terminology

Term	Description
SCL	Serial clock.
SDA	Serial address and data.
Master	The master is the device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The slave is the device addressed by a master. The ADPD103 operates as a slave device.
Start (S)	A high to low transition on the SDA line while SCL is high; all transactions begin with a start condition.
Start (Sr)	Repeated start condition.
Stop (P)	A low to high transition on the SDA line while SCL is high. A stop condition terminates all transactions.
ACK	During the acknowledge or no acknowledge clock pulse, the SDA line is pulled low and remains low.
NACK	During the acknowledge or no acknowledge clock pulse, the SDA line remains high.
Slave Address	After a start (S), a 7-bit slave address is sent, which is followed by a data direction bit (read or write).
Read (R)	A 1 indicates a request for data.
Write (W)	A 0 indicates a transmission.

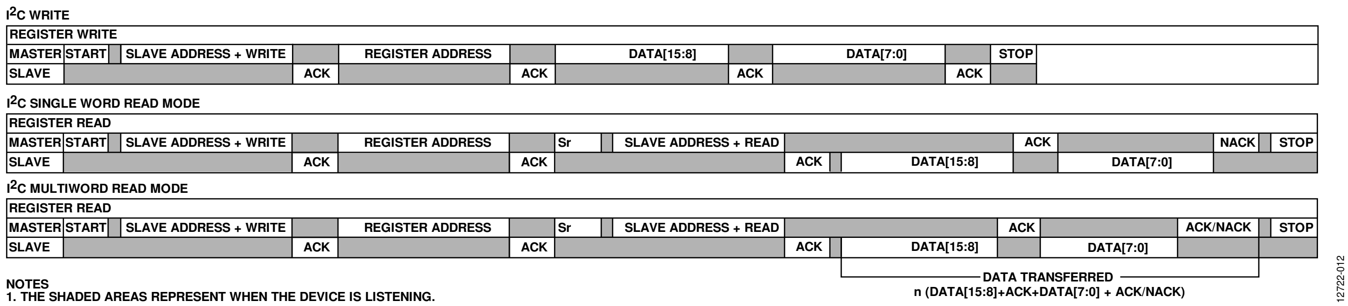


Figure 19. I²C Write and Read Operations

TYPICAL CONNECTION DIAGRAM

Figure 21 and Figure 22 show two possible photodiode input connections for the ADPD103. The 1.8 V I²C communication lines, SCL and SDA, along with the INT line, connect to a system microprocessor or sensor hub. The I²C signals can have pull-up resistors connected to a 1.8 V or a 3.3 V power supply. The INT and PDSO signals are only compatible with a 1.8 V supply and may need a level translator.

Provide the 1.8 V supply, V_{DD}, to AVDD and DVDD. Use single (V_{LED}) or multiple (V_{LED1}, V_{LED2}, and V_{LED3}) sources for the LED supply using standard regulator circuits according to the peak current requirements specified in Table 3 and calculated in the Calculating Current Consumption section.

For best noise performance, connect AGND, DGND (exposed pad), and LGND together at a large conductive surface such as a ground plane, a ground pour, or a large ground trace.

The number of photodiodes or LEDs used varies. There are multiple ways to connect photodiodes to the input channels, as shown in Table 16 and Figure 23. The photodiode anodes are connected to the PD1 to PD8 input pins, and the photodiode cathodes are connected to the cathode pin.

With large photodiodes, the dynamic range can be increased by splitting the current between multiple inputs. As a result, if only one large photodiode is used and the receive signal is expected to be large, the diode can be branched across all four inputs in a given time slot. This type of configuration is shown in Figure 21. For situations where the photodiode is small or the signal is greatly attenuated, the photodiode can be connected directly to a single channel such as PD1 or PD5. This connection, shown in Figure 22, maximizes SNR for low signals. Do not connect the same photodiode to all eight input channels. It is important to leave the unused input channels floating for proper device operation. The WLCSP package is internally wired for high dynamic range mode.

Figure 20 shows the recommended connection diagram and printed circuit board (PCB) layout for the ADPD103 WLCSP package. See Figure 21 or Figure 22 for connection details.

The current input pins (PD1 to PD8) have a typical voltage of 1.3 V during the sampling period. During the sleep period, these pins are connected to the cathode pin. The cathode and anode voltages are listed in Table 3.

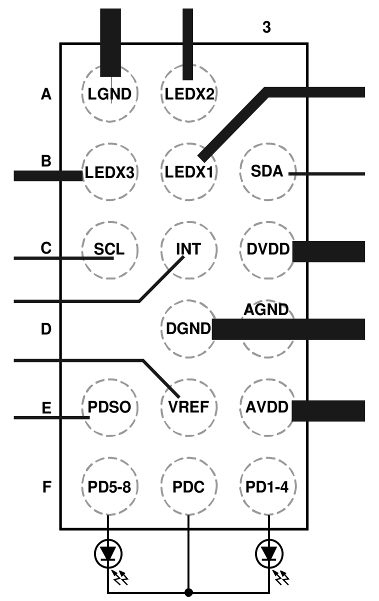


Figure 20. WLCSP Package Connection and PCB Layout Diagram (Top View)

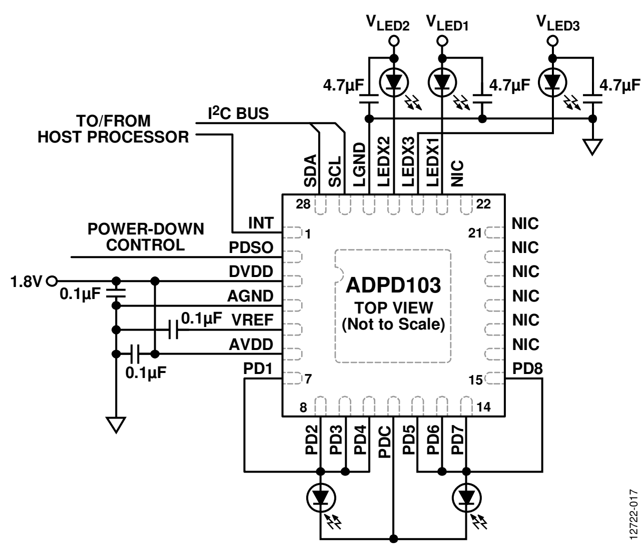


Figure 21. Connection Diagram for Increased Dynamic Range

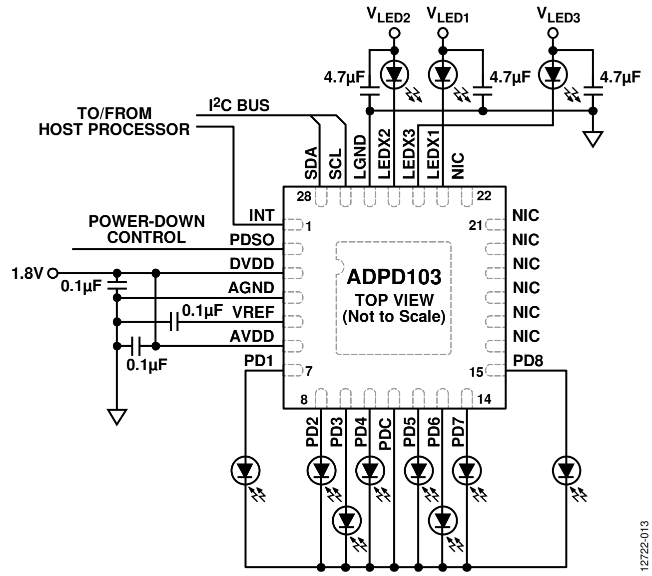


Figure 22. Connection Options for Individual Single Channel Diodes

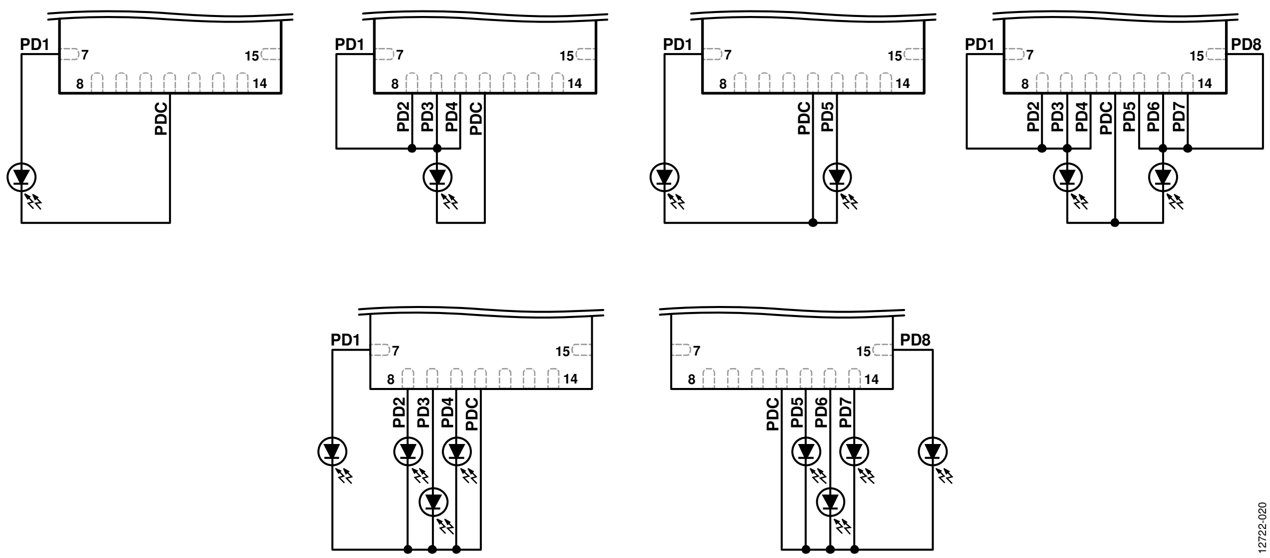


Figure 23. Typical Photodiode Connection Diagram

Table 16. Typical Photodiode Anode to Input Channel Connections

	Input Channel							
Photodiode Anode Configuration	**PD1**	**PD2**	**PD3**	**PD4**	**PD5**	**PD6**	**PD7**	**PD8**
Single Photodiode (D1)	D1	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]
	NC[1]	NC[1]	NC[1]	NC[1]	D1	NC[1]	NC[1]	NC[1]
	D1	D1	D1	D1	NC[1]	NC[1]	NC[1]	NC[1]
	NC[1]	NC[1]	NC[1]	NC[1]	D1	D1	D1	D1
Two Photodiodes (D1, D2)	D1	NC[1]	NC[1]	NC[1]	D2	NC[1]	NC[1]	NC[1]
	D1	D1	D1	D1	D2	D2	D2	D2
Four Photodiodes (D1 to D4)	D1	D2	D3	D4	NC[1]	NC[1]	NC[1]	NC[1]
	NC[1]	NC[1]	NC[1]	NC[1]	D1	D2	D3	D4
Eight Photodiodes (D1 to D8)	D1	D2	D3	D4	D5	D6	D7	D8

[1] NC means do not connect under the conditions provided in Table 16. Leave all unused inputs floating.

LED DRIVER PINS AND LED SUPPLY VOLTAGE

The LEDx1, LEDx2, and LEDx3 pins have an absolute maximum voltage rating of 3.6 V. Any voltage exposure over this rating affects the reliability of the device operation and, in certain circumstances, causes the device to cease proper operation. The voltage of the LEDx pins must not be confused with the supply voltages for the LED themselves (V_{LEDx}). V_{LEDx} is the voltage applied to the anode of the external LED, whereas the LEDx pin is the input of the internal current driver, and the pins are connected to the cathode of the external LED.

LED DRIVER OPERATION

The LED driver for the ADPD103 is a current sink requiring 0.2 V of compliance above ground to maintain the programmed current level. Figure 24 shows the basic schematic of how the ADPD103 connects to an LED through the LED driver. The Determining the Average Current and the Determining CVLED sections define the requirements for the bypass capacitor (C_{VLED}) and the supply voltages of the LEDs (V_{LEDx}).

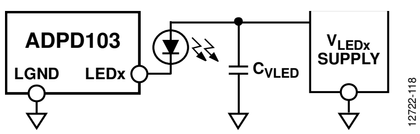


Figure 24. V_{LEDx} Supply Schematic

DETERMINING THE AVERAGE CURRENT

The ADPD103 drives an LED in a series of short pulses. Figure 25 shows the typical ADPD103 configuration of a pulse burst sequence.

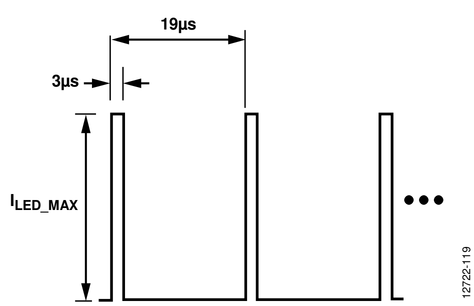


Figure 25. Typical LED Pulse Burst Sequence Configuration

In this example, the LED pulse width, t_{LED_PULSE}, is 3 µs, and the LED pulse period, t_{LED_PERIOD}, is 19 µs. The LED being driven is a pair of green LEDs driven to a 250 mA peak. The goal of C_{VLED} is to buffer the LED between individual pulses. In the worst case scenario, where the pulse train shown in Figure 25 is a continuous sequence of short pulses, the V_{LEDx} supply must supply the average current. Therefore, calculate $I_{LED\_AVERAGE}$ as follows:

$$I_{LED\_AVERAGE} = (t_{LED\_PULSE}/t_{LED\_PERIOD}) \times I_{LED\_PEAK} \quad (1)$$

where:

$I_{LED\_AVERAGE}$ is the average current needed from the V_{LEDx} supply during the pulse period, and it is also the V_{LEDx} supply current rating.

I_{LED_PEAK} is peak current setting of the LED.

For the numbers shown in Equation 1, $I_{LED\_AVERAGE}$ = 3/19 × I_{LED_PEAK}. For typical LED timing, the average V_{LEDx} supply current is 3/19 × 250 mA = 39.4 mA, indicating that the V_{LEDx} supply must support a dc current of 40 mA.

DETERMINING C_{VLED}

To determine the C_{VLED} capacitor value, determine the maximum forward-biased voltage, $V_{FB\_LED\_MAX}$, of the LED in operation. The LED current, $I_{FB\_LED\_MAX}$, converts to $V_{FB\_LED\_MAX}$ as shown in Figure 26. In this example, 250 mA of current through two green LEDs in parallel yields $V_{FB\_LED\_MAX}$ = 3.95 V. Any series resistance in the LED path must also be included in this voltage. When designing the LED path, keep in mind that small resistances can add up to large voltage drops due to the LED peak current being very large. In addition, these resistances can be unnecessary constraints on the V_{LEDx} supply.

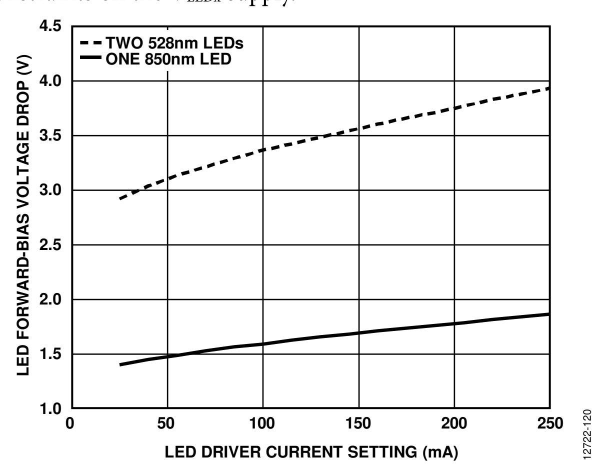


Figure 26. Example of the Average LED Forward-Biased Voltage Drop as a Function of the Driver Current

To correctly size the C_{VLED} capacitor, do not deplete it during the pulse of the LED to the point where the voltage on the capacitor is less than the forward bias on the LED.

To calculate the minimum value for the V_{LEDx} bypass capacitor, use the following equation:

$$C_{VLED} = \frac{t_{LED\_PULSE} \times I_{FB\_LED\_MAX}}{V_{LED\_MIN} - (V_{FB\_LED\_MAX} + 0.2)} \quad (2)$$

where:

t_{LED_PULSE} is the LED pulse width.

$I_{FB\_LED\_MAX}$ is the maximum forward-biased current on the LED used in operating the device.

V_{LED_MIN} is the lowest voltage from the VLEDx supply with no load.

$V_{FB\_LED\_MAX}$ is the maximum forward-biased voltage required on the LED to achieve I_{LED_PEAK}.

The numerator of the C_{VLED} equation sets up the total discharge amount in coulombs from the bypass capacitor to satisfy a single programmed LED pulse of the maximum current. The denominator represents the difference between the lowest voltage from the V_{LEDx} supply and the LED required voltage. The LED required voltage is the voltage of the anode of the LED such that the 0.2 V compliance of the LED driver and the forward-biased voltage of the LED operating at the maximum current is satisfied. For a typical ADPD103 example, assume that the lowest value for the V_{LEDx} supply is 4.4 V, and that the peak current is 250 mA for two 528 nm LEDs in parallel. The minimum value for C_{VLED} is then equal to 3 µF.

$$C_{VLED} = (3 \times 10^{-6} \times 0.250)/(4.4 - (3.95 + 0.2)) = 3\ \mu F \qquad (3)$$

As shown in the Equation 3, as the minimum supply voltage drops close to the maximum anode voltage, the demands on C_{VLED} become more stringent, forcing the capacitor value higher. It is important to insert the correct values into these equations. For example, using an average value for V_{LED_MIN} instead of the worst case value for V_{LED_MIN} can cause a serious design deficiency, resulting in a C_{VLED} value that is too small and that causes insufficient optical power in the application. Therefore, adding a sufficient margin on C_{VLED} is strongly recommended. Add additional margin to C_{VLED} to account for derating of the capacitor value over voltage, bias, temperature and other factors over the life of the component.

LED INDUCTANCE CONSIDERATIONS

The LED drivers (LEDXx) on the ADPD103 have configurable slew rate settings (Register 0x22, Bits[6:4], Register 0x23, Bits[6:4], and Register 0x24, Bits[6:4]). These slew rates are defined in Table 3. Even at the lowest setting, careful consideration must be taken in board design and layout. If a large series inductor, such as a long PCB trace, is placed between the LED cathode and one of the LEDXx pins, voltage spikes from the switched inductor can cause violations of absolute maximum and minimum voltages on the LEDXx pins during the slew portion of the LED pulse.

To verify that there are no voltage spikes on the LEDXx pins due to parasitic inductance, use an oscilloscope on the LEDXx pins to monitor the voltage during normal operation. Any positive spike >3.6 V may damage the device.

In addition, a negative spike <−0.3 V may also damage the device.

RECOMMENDED START-UP SEQUENCE

At power-up, the device is in standby mode (Register 0x10 = 0x0), as shown in Figure 14. The ADPD103 does not require a particular power-up sequence.

From standby mode, to begin measurement, initiate the ADPD103 as follows:

1. Set the CLK32K_EN bit (Register 0x4B, Bit 7) to start the sample clock (32 kHz clock). This clock controls the state machine. If this clock is off, the state machine is not able to transition as defined by Register 0x10.
2. Write 0x1 to Register 0x10 to force the device into program mode. Step 1 and Step 2 can be swapped, but the actual state transition does not occur until both steps occur.
3. Write additional control registers in any order while the device is in program mode to configure the device as required.
4. Write 0x2 to Register 0x10 to start normal sampling operation.

To terminate normal operation, follow this sequence to place the ADPD103 in standby mode:

1. Write 0x1 to Register 0x10 to force the device into program mode.
2. Write to the registers in any order while the device is in program mode.
3. Write 0x00FF to Register 0x00 to clear all interrupts. If desired, clear the FIFO as well by setting the DIGITAL_CLOCK_ENA bit (Register 0x5F, Bit 0) and writing 0x80FF to Register 0x00.
4. Write 0x0 to Register 0x10 to force the device into standby mode.
5. Optionally, stop the 32 kHz clock by resetting the CLK32K_EN bit (Register 0x4B, Bit 7). Register 0x4B, Bit 7 = 0 is the only write that must be written when the device is in standby mode (Register 0x10 = 0x0). If 0 is written to this bit while in program mode or normal mode, the device becomes unable to transition into any other mode, including standby mode, even if it is subsequently written to do so. As a result, the power consumption in what appears to be standby mode is greatly elevated. For this reason, and due to the very low current draw of the 32 kHz clock while in operation, it is recommended from an ease of use perspective to keep the 32 kHz clock running after it is turned on.

READING DATA

The ADPD103 provides multiple methods for accessing the sample data. Each time slot can be independently configured to provide data access using the FIFO or the data registers. Interrupt signaling is also available to simplify timely data access. The FIFO is available to loosen the system timing requirements for data accesses.

Reading Data Using the FIFO

The ADPD103 includes a 128-byte FIFO memory buffer that can be configured to store data from either or both time slots. Register 0x11 selects the kind of data from each time slot to be